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The Future of Semiconductor Packaging

Volume 30, Number 3

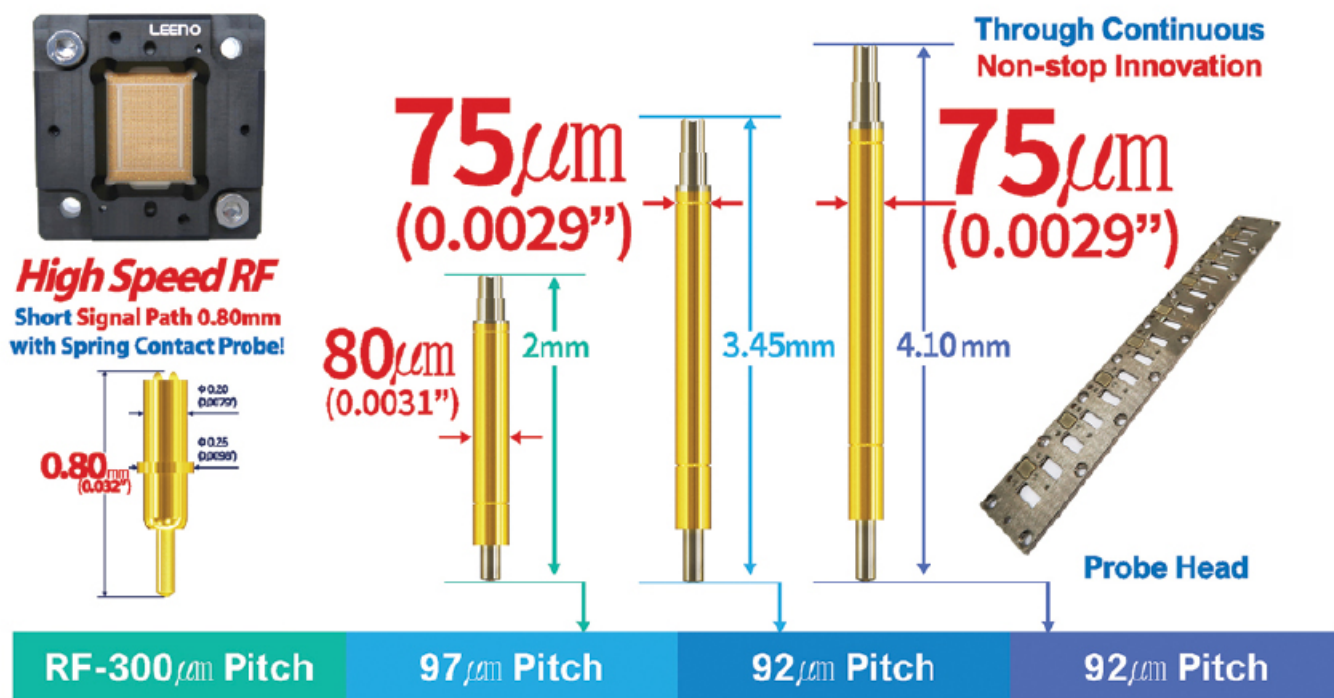
Summer 2026

Hybrid bonding: A critical enabler of next-gen 3D device architectures

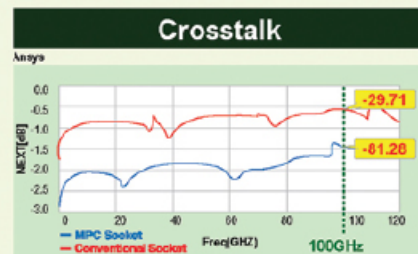
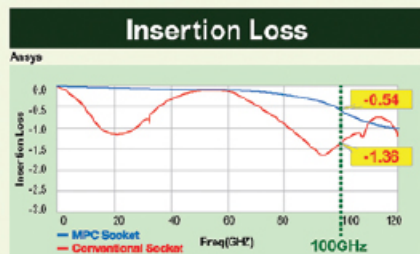
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- Enabling high-performance 3D integration through advanced microbump technology
- Potential applications of Cu-Cu hybrid bonding to heterogeneous integration of chiplets
- Achieving faster ramps and lower costs with yield prediction technology in FOPLP lithography

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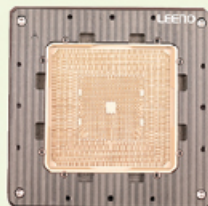


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*In hybrid bonding, tight alignment and overlay accuracy between the wafers is required to achieve good electrical contact between the interconnected devices on the bonded wafers. Constant reduction in pitches is fueling tighter bonding specifications. Shown here is the SmartView® NT3 Aligner, which achieves sub-50nm alignment accuracy on 300 mm wafers, supporting advanced 3D applications such as memory and logic stacking, AI accelerators, and heterogeneous integration.
Cover image courtesy of EV Group*

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Enabling high-performance 3D integration through advanced microbump technology

By Calvin Lee [ASE US]

As front-end transistor scaling approaches fundamental physical and economic limits, the semiconductor industry is increasingly relying on advanced packaging—particularly fine-pitch interconnection technologies—to overcome system-level performance bottlenecks. Leading applications in artificial intelligence (AI), high-performance computing (HPC), and high-bandwidth memory (HBM)-enabled architectures demand levels of bandwidth, latency, and power efficiency that can no longer be delivered through monolithic scaling or conventional 2D packaging alone (Figure 1).

Fine-pitch interconnection technologies—most notably advanced microbumps and hybrid bonding—play a critical role in enabling this transition.

By dramatically reducing interconnect pitch and vertical signal length, these technologies lower parasitic resistance and capacitance while enabling dense die-to-die connections across logic, memory, and accelerator chiplets. This capability allows large monolithic system-on-chips (SoCs) to be disaggregated beyond reticle limits into heterogeneous, function-optimized dies, paving the way for scalable 2.5D and true 3D integration without compromising latency, signal integrity, or energy efficiency (Figure 2).

In light of the discussion above, fine-pitch interconnects have emerged as a foundational enabler of advanced packaging, marking a fundamental shift in the industry's primary scaling vector: From transistor density to high-density, system-level and vertical integration.

Microbump interconnect technology in 2.5D and 3D architectures

Microbumps are a cornerstone technology for chiplet-based systems, HBM, AI accelerators, and heterogeneous integration because they provide ultra-dense, short-range interconnects capable of moving massive amounts of data with high efficiency. Their fine pitch enables thousands of parallel connections between closely-coupled dies, allowing multi-die systems to behave increasingly like monolithic designs while operating at far greater scale.

In HBM stacks and 2.5D interposer-based designs, microbumps enable extremely wide memory interfaces by minimizing microbump pitch and interposer line/spacing between logic and memory. This scheme delivers the high bandwidth and high-power

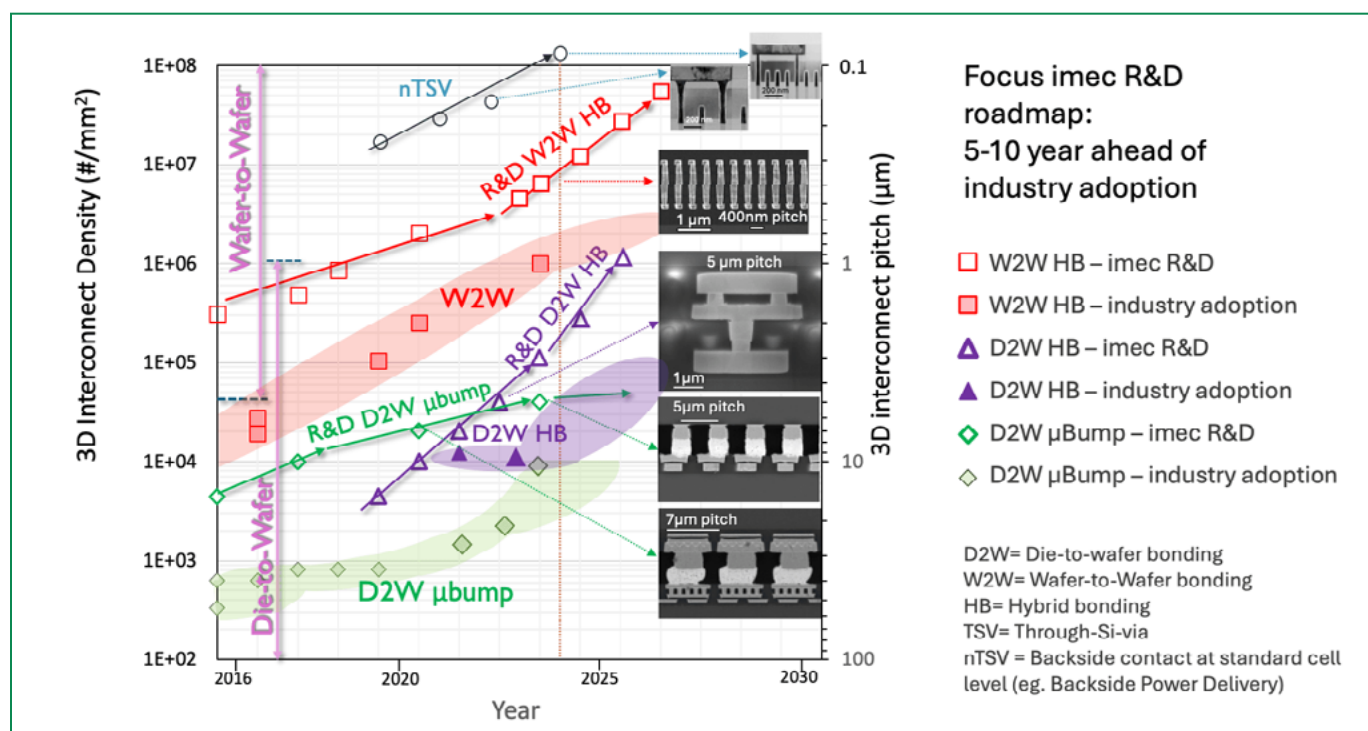


Figure 1: Fine-pitch interconnect roadmap. SOURCE: imec [1]

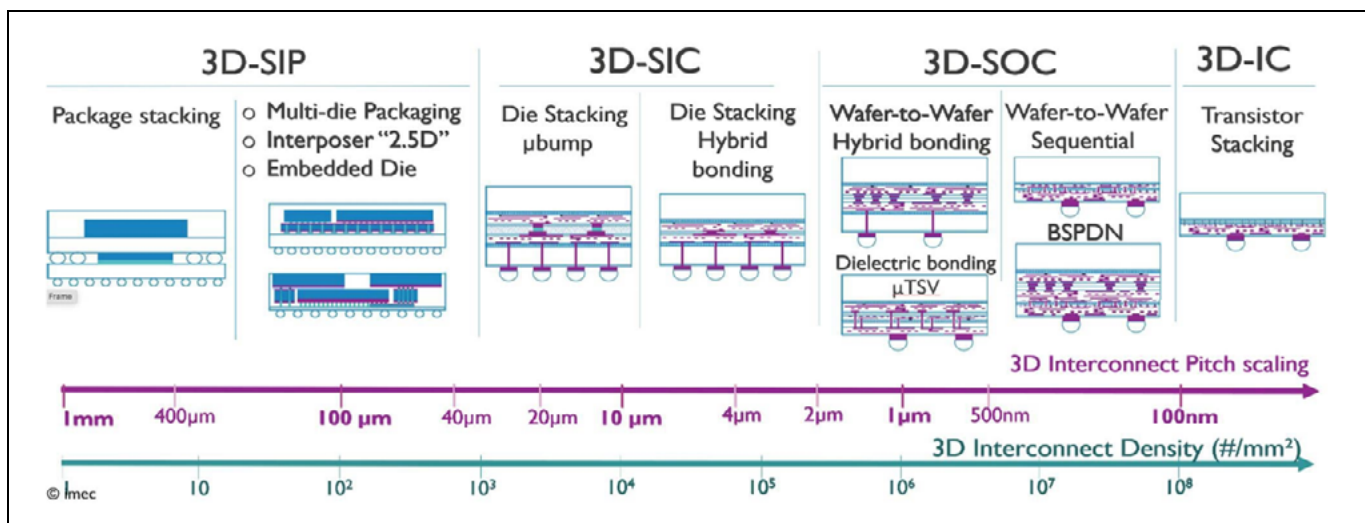


Figure 2: 3D interconnect landscape. SOURCE: imec [2]

efficiency required by data-intensive AI and HPC workloads. In emerging 3D IC architectures, microbumps form the physical backbone of vertical integration, enabling die stacking with manageable thermal, mechanical, and yield trade-offs (Figure 3).

For AI accelerators, where overall performance is increasingly limited by data movement rather than raw computation, microbump-enabled interconnects support fast, energy-efficient memory access and scalable compute tiling. More broadly, microbumps make heterogeneous 3D

integration commercially viable by allowing dies fabricated on different process nodes—or optimized for logic, memory, analog, or I/O—to be tightly integrated into a single high-performance system without incurring the power, latency, and bandwidth penalties of traditional packaging approaches (Figures 4-5).

Microbump bonding vs. hybrid bonding in 3D integration

Table 1 summarizes the key technical and manufacturing tradeoffs between microbump interconnects

and hybrid bonding, illustrating why both technologies coexist and serve different roles across the 2.5D and 3D integration roadmap.

In advanced packaging, both microbump interconnects and hybrid bonding enable high-density die-to-die or die-to-wafer integration, but they differ materially in manufacturing requirements. Microbump processing leverages mature wafer-level facilities already common in outsourced semiconductor assembly and test (OSAT) and foundry environments, including electroplating, resist patterning, and

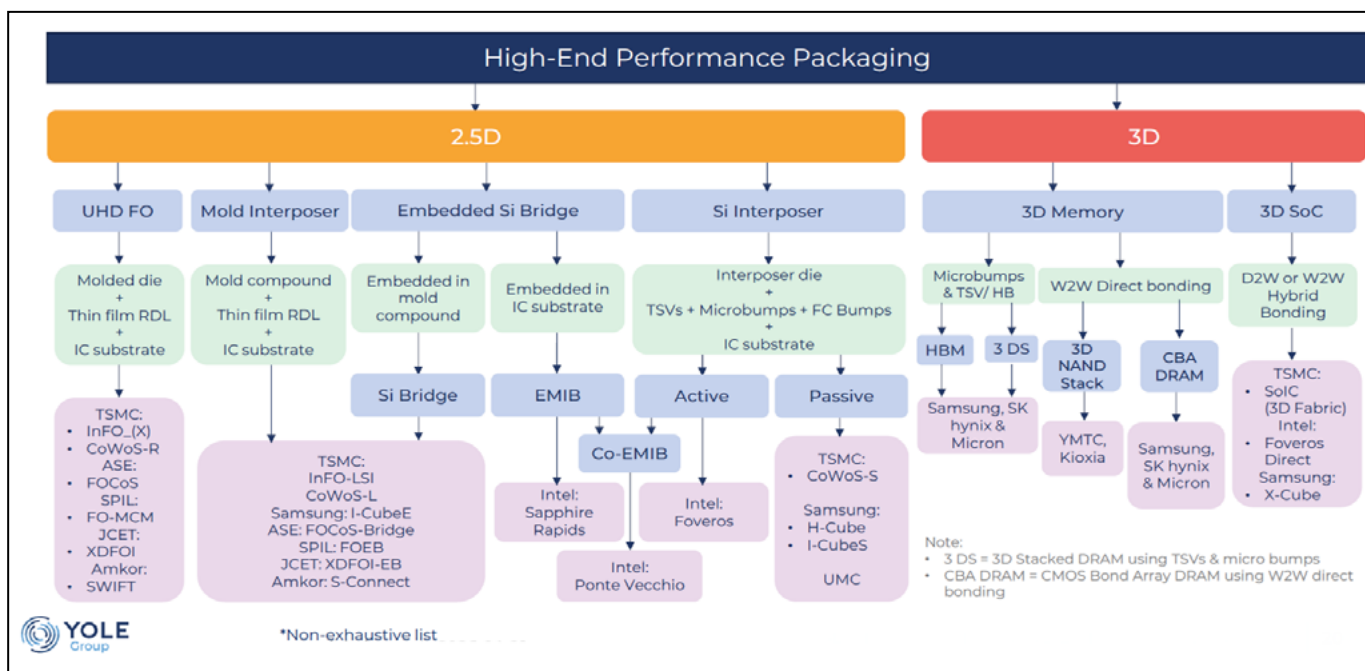


Figure 3: 2.5D and 3D IC packaging categories. SOURCE: Yole

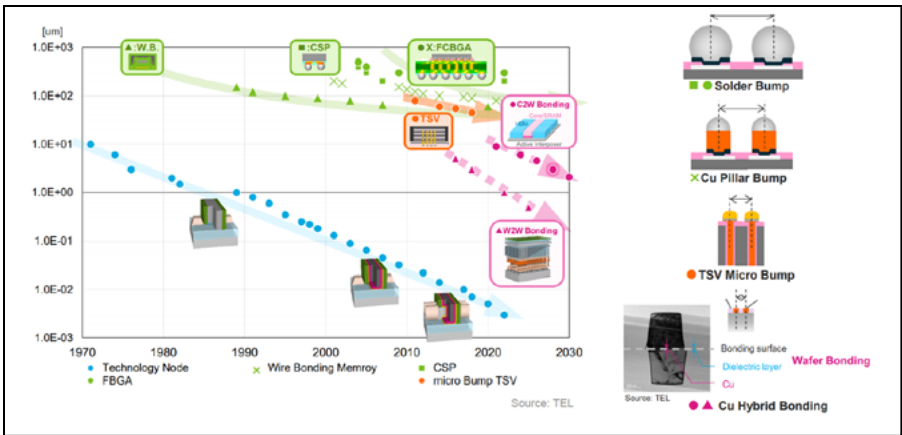


Figure 4: Interconnect distance roadmap. SOURCE: TEL [3]

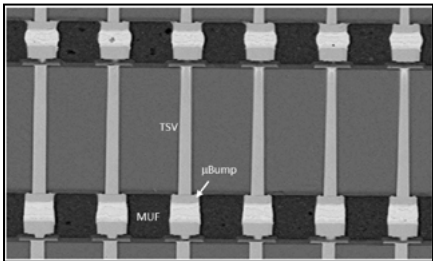


Figure 5: Advanced microbumps with a 20μm bump pitch. SOURCE: ASE

standard reflow equipment. While lithography capability must support fine pitches (typically 40–100μm, trending smaller), these requirements are evolutionary rather than disruptive. In contrast, hybrid bonding demands tightly controlled frontend-like environments, including ultra-clean surfaces, precision chemical-mechanical polishing (CMP), plasma activation, and sub-micron alignment tools often derived from leading-edge wafer fabrication. The capital intensity and process integration complexity of hybrid bonding limit its deployment to a small number of highly advanced manufacturers, whereas microbumps can be implemented across a much broader base of existing facilities.

Supply chain considerations further favor microbump technology, particularly for high-volume manufacturing. Microbump materials, such as copper, nickel, solder alloys, and under-bump metallization (UBM) stacks, are well qualified, widely available, and supported by a deep ecosystem of equipment and materials suppliers. Process flows are tolerant of reasonable variation across vendors, which simplifies sourcing and multi-site production. Hybrid bonding, by

comparison, is highly sensitive to surface preparation, wafer flatness, and material compatibility across oxide and copper interfaces. This sensitivity increases dependence on tightly-coupled tool sets and proprietary process recipes, thereby constraining second-source options and introducing risk in scaling across geographies or partners. As a result,

microbumps offer a more resilient and flexible supply chain for complex, multi-die products.

Bonding alignment requirements represent another key differentiator. Microbump-based assembly benefits from the mechanical compliance of solder joints that can accommodate modest misalignment, wafer bow, and thermal expansion differences during bonding and reflow (Figure 6). This compliance translates into higher assembly yields and a wider process window, especially as die sizes increase or heterogeneous materials are integrated. Hybrid bonding, while offering superior interconnect density and electrical performance, requires near-perfect alignment—often well below one micron—because there is no self-alignment mechanism once surfaces make contact (Figure 6). Any particulate contamination or alignment error can lead to open circuits or voids across large bonded areas, making yield learning and process control significantly more challenging.

Aspect	Microbump Interconnects	Hybrid Bonding
Basic concept	Metal solder bumps used to electrically and mechanically connect stacked dies or dies to interposers	Direct bonding of metal pads (typically Cu-Cu) and dielectric surfaces simultaneously
Interconnect structure	Discrete solder bumps (Sn-based alloys or Cu pillars with solder caps)	Planar copper pads bonded directly, no solder
Typical pitch	~20–40 μm (with advanced processes pushing toward ~10 μm)	~1–10 μm (sub-10 μm widely demonstrated in production)
Interconnect density	Moderate	Very high
Electrical performance	Higher resistance and inductance due to solder and bump height	Lower resistance and parasitics due to direct Cu-Cu contact
Thermal performance	Good, but limited by solder and underfill materials	Better thermal conductivity via direct copper paths
Bonding temperature	Relatively high (≈230–300 °C for reflow)	Lower (≈250 °C or lower, depending on process)
Mechanical compliance	Good stress relief from solder deformation	Less compliant; relies on tight planarity and CTE matching
Surface planarity requirement	Moderate	Extremely high (stringent CMP and alignment requirements)
Process maturity	Very mature, widely used in HBM, interposers, and 3D stacking	Newer, rapidly maturing; adopted in leading-edge logic and memory
Cost	Lower equipment and process cost	Higher upfront cost (CMP, alignment, bonding tools)
Reliability concerns	Solder fatigue, electromigration at small pitches	Interface defects, voids, alignment sensitivity
Scalability	Limited by solder bump size and collapse	Highly scalable to future technology nodes
Common use cases	HBM stacks, die-to-interposer connections, TSV-based 3D ICs	Logic-to-logic stacking, logic-to-memory at ultra-fine pitch (e.g., advanced CPUs, AI accelerators)

Table 1: Comparison of microbump interconnects and hybrid bonding.

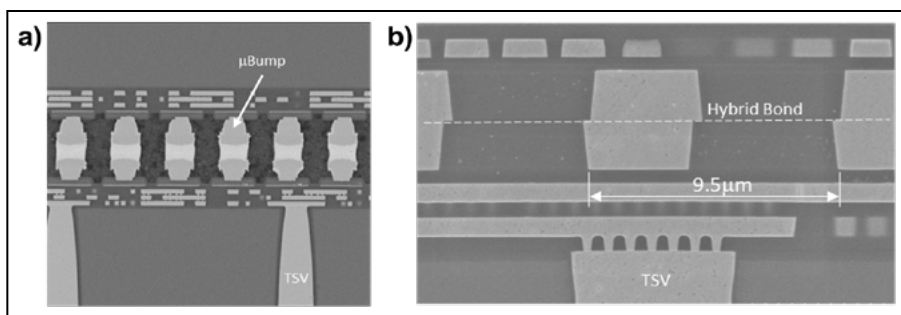


Figure 6: Differences in the impact of alignment challenges for: a) (left) Microbumps @15μm bump pitch; and b) (right) A hybrid bond. SOURCE: ASE

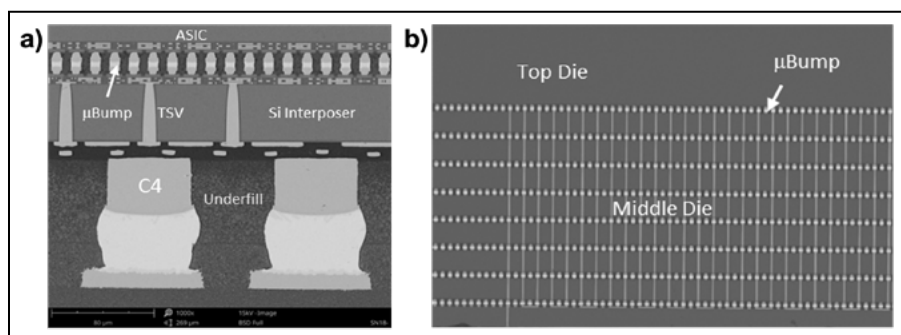


Figure 7: Microbumps: a) (left) On a Si interposer; and b) (right) In 3D die stacking. SOURCE: ASE

Taken together, the factors noted above underscore why microbumps remain a highly attractive interconnect solution for advanced packaging today. While hybrid bonding is a powerful enabler for extreme bandwidth and logic-on-logic integration, microbumps provide a pragmatic balance of performance, manufacturability, and scalability. Their compatibility with existing facilities, robust global supply chain, and forgiving alignment characteristics allow manufacturers to ramp complex architectures with lower risk and capital exposure—benefits that continue to make microbumps a cornerstone of high-volume heterogeneous integration.

OSAT perspective

From our perspective as an OSAT, advanced microbump technology

is a core and durable enabler of leadership in high-density packaging for chiplets, HBM, and AI accelerators. We view microbumps as the optimal balance between performance and manufacturability, delivering the interconnect density, bandwidth, and power efficiency required for CoWoS® class 2.5D architectures and vertically-integrated HBM stacks, while remaining compatible with proven backend assembly flows such as, redistribution layer (RDL) formation, known good die (KGD) assembly, and the high-volume chip-on-wafer (CoW) bonding process.

Within our VIPack™ platform, we continue to advance our interconnect roadmap by scaling microbump pitch from 40μm toward 20μm through innovations in metallurgical stack engineering. These advances directly address critical power delivery, latency,

and signal integrity challenges across 2D, 2.5D, and 3D IC designs. Compared with hybrid bonding, microbumps provide greater process tolerance, yield resilience, and flexibility for multivendor chiplet sourcing—capabilities essential for the complex, high-mix AI systems demanded by our customers.

Summary

Supported by collaborative design enablement through our Integrated Design Ecosystem™ (IDE), microbumps remain a foundational technology that enable the capture of significant value in advanced 3D packaging without relinquishing system integration control to wafer foundries (Figure 7). This reinforces our conviction that backend-driven innovation in 3D integration will be a decisive contributor to system-level performance gains in the AI era.

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Biography

Calvin Lee is Director of Corporate R&D of ASE US, Kaohsiung City, Taiwan, and is leading 3D IC packaging development. He has more than 20 years of experience in package characterization, 2.5D and 3D IC package development. Calvin has 70 patents and more than 20 technical publications. He has a BS and MS degrees in Mechanical Engineering from Taiwan Cheng Kung University and Sun Yat-sen University, respectively. Email: calvin_lee@aseglobal.com

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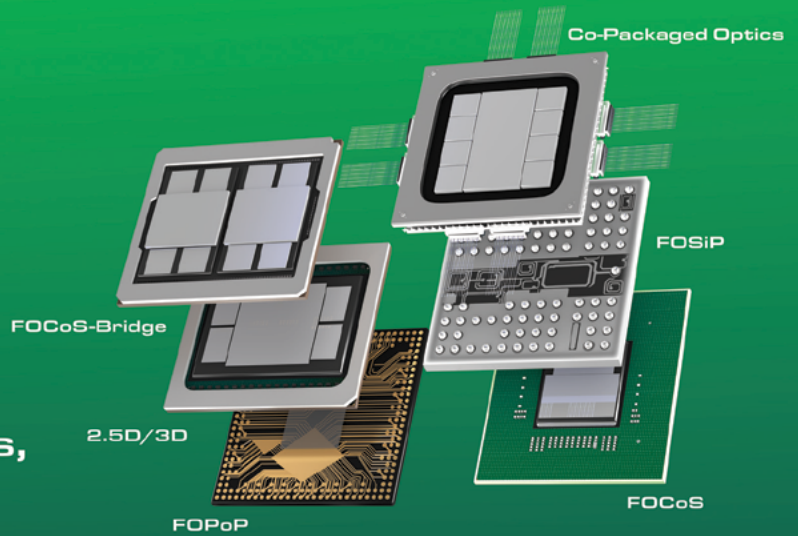
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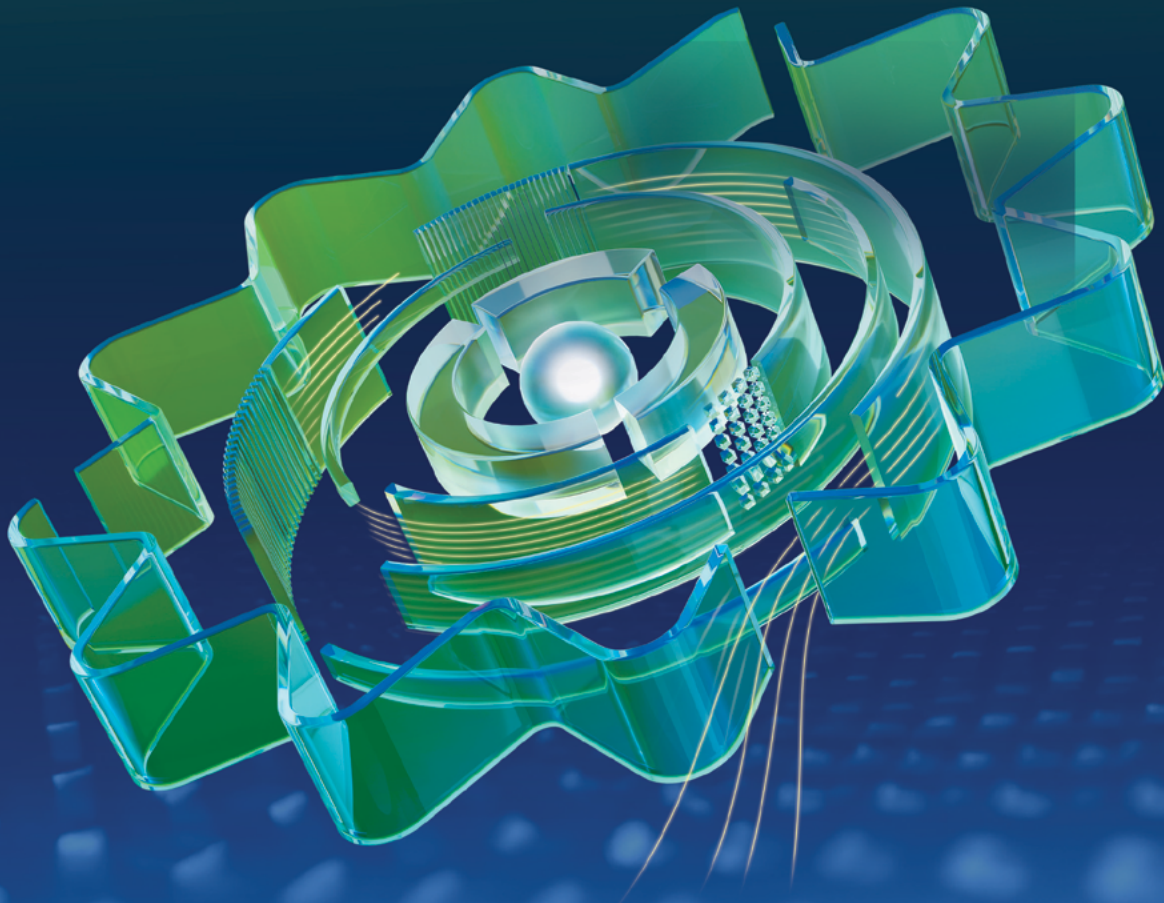


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Bumpless flip-chip (BFC) as a next-generation interconnect technology for the AI era

By Rabindra N. Das, Dan Oates, Alexander Wynn, David Kim, Steven Weber, Mollie Schwartz
[Advanced Technology Division MIT Lincoln Laboratory]

The scaling of AI, HPC, and data-center systems is increasingly constrained by interconnect density, bandwidth, power efficiency, and reliability rather than transistor performance. Solder-based flip-chip interconnects face fundamental pitch-scaling and reliability limits, whereas Cu–Cu hybrid bonding introduces significant manufacturability challenges. This paper presents a bumpless flip-chip (BFC) interconnect technology based on direct under-bump metal (UBM) to UBM thermocompression diffusion bonding. The BFC targets a manufacturable multi-micron pitch regime optimized for yield and robustness. Fine-pitch 8 μ m interconnects were demonstrated on a 200mm silicon multi-chip module platform and electrically characterized down to 4.2K, confirming stable cryogenic performance.

Introduction

The continued scaling of artificial intelligence (AI), high-performance computing (HPC), and data center systems has fundamentally altered the performance balance of advanced electronic systems. While transistor density and device performance continue to improve, interconnects increasingly dominate the system-level power consumption, latency, bandwidth density, and reliability. As heterogeneous integration and chiplet-based architectures become dominant paradigms, packaging technologies are required to support extremely high I/O densities, reduced interconnect lengths, and robust operations across a wide range of environments [1-3].

Traditional solder-based flip-chip interconnect approaches—including controlled collapse chip connection (C4) bumps and microbumps—have fundamental scaling limits (Figure 1). As the interconnect pitch decreases, solder joints suffer from increased parasitic

resistance and capacitance, current density limitations, electromigration, and fatigue-driven failure under thermal cycling. These effects constrain the achievable I/O density and limit the scalability of large multichip modules (MCMs) and 3D integrated systems.

Cu–Cu hybrid bonding has emerged as a promising alternative, enabling solder-free metal-to-metal interconnects at ultra-fine pitches. Hybrid bonding, however, requires extreme surface roughness control (typically <0.4nm root mean square [RMS]), strict oxidation management, tight pre-bond process coupling, and extended post-bond annealing. These requirements complicate the integration of dissimilar dies, increase the sensitivity to surface nonplanarity, and pose yield and cost challenges for large-area heterogeneous assemblies.

Although hybrid bonding is a critical enabler for chiplet integration at ultra-fine pitches approaching and below 1 μ m [4-6], a wide range of heterogeneous

integration applications operate in a pitch regime where manufacturability, yield, and system-level robustness are more important than achieving the minimum possible interconnect pitch. In this regime, UBM-to-UBM bumpless bonding offers a compelling alternative without the stringent surface preparation and process sensitivity associated with hybrid bonding.

In this paper, we present a BFC interconnect technology based on direct UBM-to-UBM thermocompression diffusion bonding. Rather than attempting to replace hybrid bonding, BFC targets the practical design space between solder microbumps and sub-micron hybrid bonding. The BFC approach reduces interconnect parasitics (resistance, inductance, and capacitance), eliminates solder-related reliability concerns, and enables fine-pitch bonding with relaxed surface requirements that are compatible with a mature packaging infrastructure. We demonstrate BFC integration on a silicon MCM platform and evaluate its

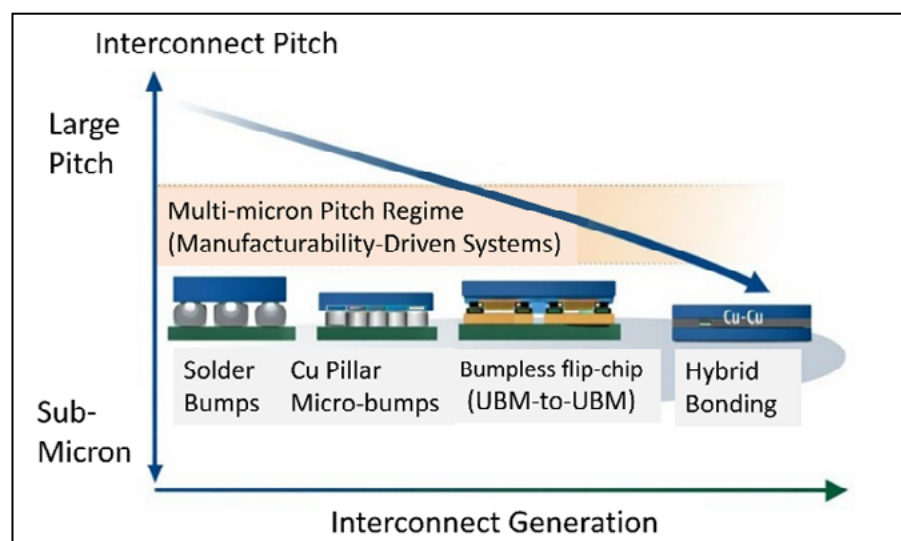


Figure 1: Conceptual illustration of flip-chip interconnect pitch scaling and emerging solder-free integration approaches. BFC using UBM-to-UBM bonding occupies a multi-micron pitch regime that bridges conventional solder-based microbumps and sub-micron Cu–Cu hybrid bonding, targeting applications where manufacturability, yield, and system-level robustness dominate over minimum pitch scaling.

electrical performance at cryogenic temperatures, highlighting its relevance to dense and temperature-stressed packaging platforms used to build AI, HPC, and emerging quantum and cryogenic systems.

Bumpless flip-chip

In subsequent sections, we focus on chip-to-chip bumpless integration using UBM-to-UBM thermocompression bonding. The chip-to-chip integrated stacks described in this work consist of a base chip and a top chip, each implemented as a multilayer module. The module circuits were fabricated on 200mm silicon wafers using a niobium-based integrated-circuit fabrication process. Each module typically incorporates six niobium (Nb) wiring layers separated by plasma-enhanced chemical vapor deposition (PECVD) silicon oxide dielectric layers, with superconducting vias providing vertical interconnects between metal layers. The wiring layers were patterned using i-line (365nm) or EX4 (248nm) photolithography, supporting minimum wiring dimensions down to 0.35 μ m, consistent with fine-pitch heterogeneous integration requirements.

UBM pads were fabricated on both the base and top chips to enable bumpless bonding. The UBM stack consisted of 20nm Ti as the adhesion layer, 50nm Pt as the diffusion barrier, and 50–400nm Au as the bonding layer. This UBM configuration provides robust adhesion, oxidation protection, and a suitable surface for thermocompression diffusion bonding, while maintaining compatibility with circuit fabrication.

Figure 2 summarizes the end-to-end BFC integration flow from wafer-level UBM formation through the final package assembly, and highlights the manufacturability-driven design philosophy of the approach. As shown in **Figure 2a**, UBM pads were fabricated at the wafer level using mature i-line and EX4 lithography, enabling high-throughput and tight dimensional control prior to singulation. Performing UBM formation before dicing ensures uniformity across the wafer and decouples the fine-pitch interconnect definition from later assembly steps, which is particularly advantageous for heterogeneous and MCM integration.

After dicing and removing the dicing resist, the individual chips retained well-defined UBM pads, as illustrated in the scanning electron microscope (SEM) image in **Figure 2b**. The preserved UBM topography above the passivation layer is a key attribute of BFC architecture. Unlike Cu–Cu hybrid bonding, which relies on recessed copper pads and extreme surface planarization, the BFC approach leverages engineered UBM stacks that provide intrinsic oxidation protection and diffusion-bonding capabilities. Mild plasma cleaning is sufficient to prepare a UBM surface for bonding, avoiding the stringent surface roughness and timing constraints typically associated with hybrid bonding.

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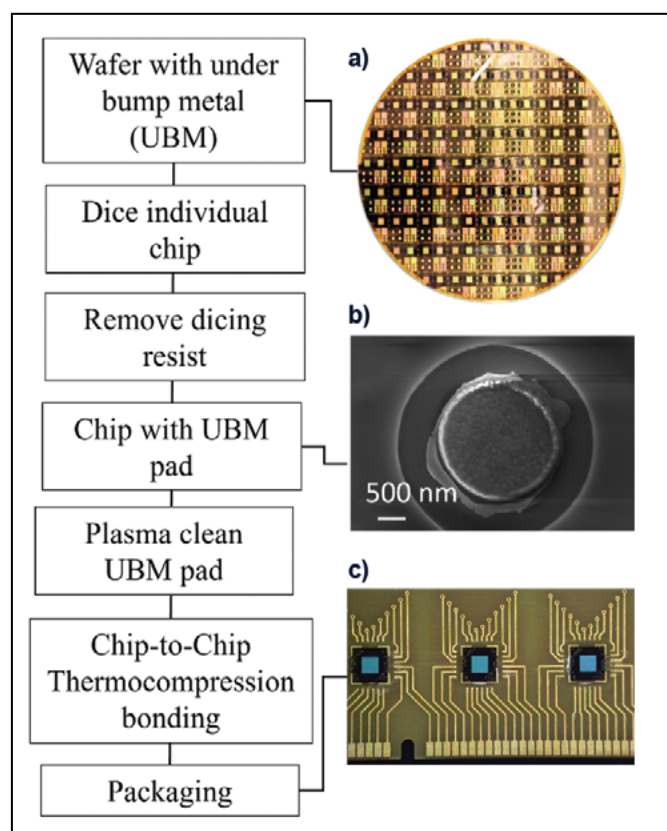


Figure 2: BFC heterogeneous integration process and representative structures: a) Optical image of a wafer patterned with UBM pads prior to dicing, illustrating wafer-level scalability of the BFC approach; b) High-magnification SEM of an individual UBM pad (2 μ m diameter) within the passivation opening, highlighting the pad topography and metal surface prior to bonding; c) Optical image of multiple chips assembled onto a package substrate using BFC bonding for chip-to-chip interconnection, followed by wire bonding to an evaluation PCB, demonstrating fine-pitch, solder-free interconnects compatible with conventional packaging flows.

Figure 2c shows the chip-to-chip or chip-to-substrate assembly using BFC bonding, which resulted in fine-pitch, solder-free interconnects. The elimination of solder removes common failure mechanisms such as solder fatigue and electromigration, whereas the reduced interconnect height lowers the parasitic resistance and capacitance. Importantly, the BFC process flow remains compatible with the established packaging and test infrastructure, enabling integration into the existing MCM and system-in-package manufacturing lines.

Overall, the structures shown in **Figure 2** illustrate how the bumpless flip-chip technology targets a multi-micron pitch regime optimized for manufacturability and system-level robustness. By relaxing the surface preparation requirements and avoiding extended post-bond annealing, BFC interconnects provide a scalable alternative that complements hybrid bonding rather than competing with it. This makes BFC particularly attractive for heterogeneous multi-chip packaging used in AI, HPC, and cryogenic systems, where yield, reliability, and integration flexibility are as critical as interconnect density.

Fabrication process and fine-pitch UBM patterning

Figure 3 illustrates the multilayered superconducting multi-chip module (S-MCM) used as the base platform for chip-to-chip bumpless integration. The wiring stack consists of multiple Nb

metal layers separated by PECVD silicon oxide dielectrics, enabling dense routing while maintaining the superconducting signal integrity. Individual wiring layers are designed with controlled impedance geometries to support high-speed data and clock distributions, which are critical for cryogenic and superconducting computing systems.

Figure 4 illustrates the vertical interconnection between the Nb layers that

is realized through superconducting vias, allowing low-loss signal propagation across the stack. The placement of the UBM pads on the top metal layer (M6) provides a direct electrical and mechanical interface for bumpless bonding while preserving the underlying superconducting wiring architecture. Of particular significance, the UBM pads remain above the passivation surface, improving the tolerance to surface nonplanarity and simplifying

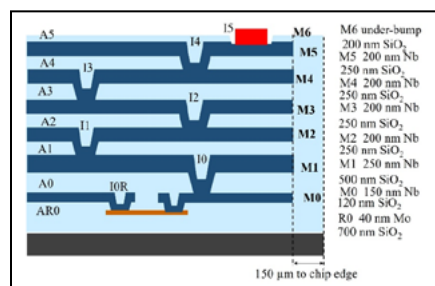


Figure 3: Cross-sectional illustration of the proposed S-MCM illustrating the Nb wiring stack and dielectric architecture used for chip-to-chip bumpless integration. The module incorporates six Nb wiring layers (M0–M6) separated by PECVD silicon oxide dielectric layers with impedance-controlled transmission lines for data and clock distribution. UBM pads are formed on the top metal layer to enable bumpless chip-to-chip thermocompression bonding. The dashed region indicates setback from the chip edge.

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integration compared with the recessed pad architectures used in hybrid bonding.

This S-MCM architecture is inherently compatible with wafer-scale fabrication on 200mm silicon substrates and leverages mature photolithography and deposition processes. By integrating the UBM pads directly into the superconducting wiring stack, the design enables chip-to-chip stacking without introducing solder, minimizes interconnect parasitics, and avoids solder-related reliability issues at cryogenic temperatures.

Figure 4 also presents the experimental validation of the fabricated superconducting Nb wiring stack and the UBM integration, demonstrating the manufacturability of the proposed S-MCM architecture. The layout artwork and corresponding optical images in **Figures 4a** and **b** show the Nb wiring patterns and UBM pad placement and the fabricated chip after patterning using i-line photolithography. The dense routing and consistent feature definition highlight compatibility with fine-pitch heterogeneous integration.

The SEM focused ion beam (FIB)

cross section in **Figure 4c** reveals the as-designed Nb metal and dielectric layer thicknesses across the stack, with well-aligned vias connecting successive wiring layers. This structural integrity is essential for maintaining the superconducting performance and minimizing variability across large-area modules. **Figure 4d** shows an enlarged cross section focusing on the UBM integration region and also shows the UBM pad formed above the Nb wiring layers and dielectric stack. The FIB SEM cross section shows that the UBM pad configuration enables direct UBM-to-UBM thermocompression bonding for chip-to-chip integration (BFC), while preserving the superconducting interconnect performance.

Together, **Figures 3-4** demonstrate that the BFC integration can be seamlessly incorporated into complex superconducting Nb MCM architectures using standard fabrication processes. The results confirm that the proposed approach supports fine-pitch, solder-free, chip-to-chip integration with high structural fidelity, making it well suited for scalable cryogenic and quantum computing systems.

Electrical and cryogenic characterization

A range of UBM pad geometries with pad pitches spanning 5–35 μm was fabricated on a S-MCM to evaluate the scalability of the BFC interconnect architecture. Following UBM formation, superconducting chips were bonded to the superconducting MCM using UBM-to-UBM thermocompression diffusion bonding, completing the electrical daisy-chain structures between the chip and module. Electrical measurements confirm that when paired with an optimized bonding process, the UBM interface maintains a low interconnect resistance while preserving a high Nb critical current (above 15mA), indicating that the bumpless integration process does not degrade the superconducting performance.

Figure 5 demonstrates the practical realization of fine-pitch BFC integration at an 8 μm pitch, combining dense physical assembly with stable electrical behavior. The optical image in **Figure 5a** shows multiple BFCs uniformly wire-bonded to the package substrate. The dense interconnect layout highlights a key advantage of the bumpless approach: by eliminating solder bumps, the interconnect height is minimized, enabling shorter electrical paths and improved routing efficiency compared to conventional solder-based flip-chip assemblies. This reduction in the interconnect length directly lowers parasitic resistance and capacitance, which is particularly critical for high-speed digital systems and superconducting or cryogenic circuits, where parasitics strongly influence signal integrity and timing margins.

The electrical characteristics shown in **Figure 5b** further validate the integrity of bumpless interconnects. The measured current-voltage (I-V) response exhibited a high critical current and stable conduction, confirming the formation of a robust metal-to-metal electrical interface through UBM-to-UBM diffusion bonding. Together, the physical assembly and electrical results confirm that 8 μm -pitch BFC integration can be achieved using manufacturable processes without stringent surface preparation and yield sensitivity typically associated with Cu-Cu hybrid bonding. These results reinforce the positioning of BFC as a scalable interconnect solution for heterogeneous integration in AI, HPC, and cryogenic systems, where

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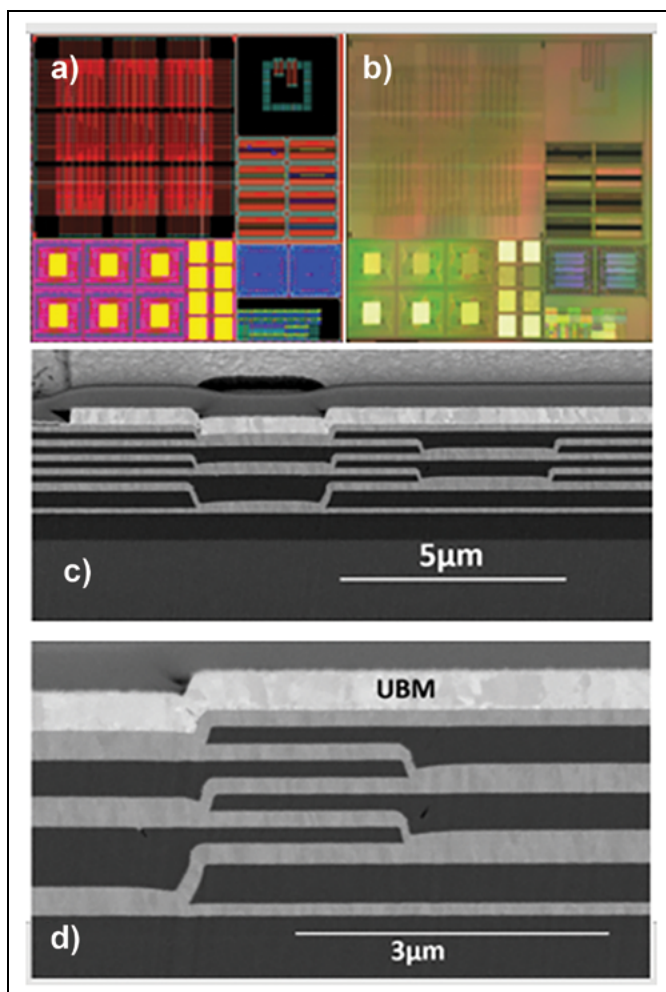


Figure 4: Fabricated structures of superconducting Nb wiring stacks and UBM integration: a) Layout artwork of Nb wiring layers showing dense routing and test structures for the module; b) Optical micrograph of the fabricated module highlighting the UBM pad locations integrated within the Nb wire layout; c) Cross-sectional SEM image of the multilayer Nb wiring stack illustrating the designed layer thickness and alignment; and d) High-magnification SEM image of the UBM region showing the UBM pad integrated above the Nb wiring layers and the dielectric stack.

fine pitch, electrical robustness, and manufacturability must be simultaneously satisfied. Importantly, BFC interconnections are not intended to replace hybrid bonding in submicron regimes, but rather to complement it by addressing a broader and practically significant application space, particularly for large MCMs, chiplet-based architectures, and emerging cryogenic platforms.

Advantages of BFC integration

UBM serves as an enabling interface in BFC integration by consolidating adhesion, diffusion control, oxidation protection, and electrical conduction into a single engineered stack. The UBM stack provides robust adhesion to the underlying Al/Cu pads while acting as a diffusion barrier and an oxidation-resistant surface, eliminating the need for solder-based interconnects. During assembly, the UBM interface supports thermocompression diffusion bonding, forming a direct metal-to-metal interconnect with a reduced parasitic resistance and capacitance.

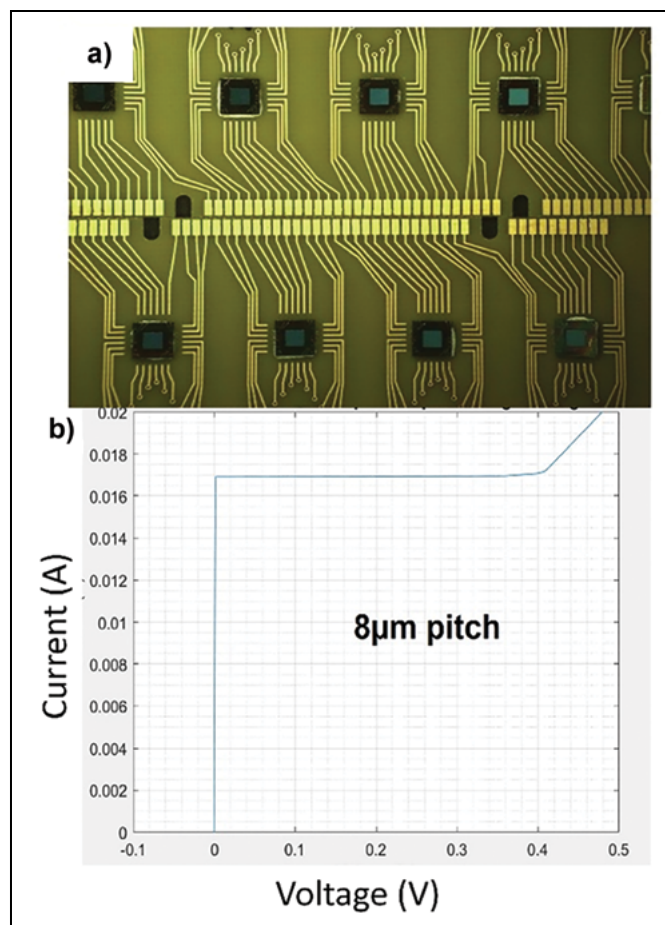


Figure 5: Demonstration of fine-pitch bumpless flip-chip (BFC) integration and electrical performance: a) (top) Optical image of multiple chips assembled onto a package substrate using UBM-to-UBM thermocompression bonding at 8μm pitch, showing dense routing from the chip pads into the substrate wiring; b) (bottom) Representative current–voltage (I–V) characteristics measured across the 8μm pitch BFC interconnect structure, confirming a stable, low-resistance electrical behavior.

By eliminating solder, BFC interconnect schemes remove dominant failure mechanisms such as solder fatigue, creep, and electromigration, which increasingly limit the reliability at fine pitch and under thermal cycling. The metallic bonding interface further enables a high current-carrying capability, making this approach suitable for high-performance digital, superconducting, and cryogenic systems. Importantly, the UBM pads were intentionally maintained above the passivation surface, improving the tolerance to local surface nonplanarity and topographic variation. This architectural feature relaxes the surface roughness requirements and improves the yield relative to recessed-pad bonding schemes. Critical to cryogenic and superconductor systems with low thermal-processing budgets, the elimination of post-bond annealing makes fine-pitch bonding possible, where Cu-Cu hybrid bonding may be damaging.

Collectively, the attributes noted above allow BFC to achieve fine-pitch scalability below 10μm using mature lithography and deposition processes, while remaining compatible with die-to-die, die-to-wafer, and MCM integration flows. As a result, BFC integration occupies a practical design space between solder microbumps and sub-micron bonding approaches, optimized for manufacturability-driven heterogeneous systems.

BFC integration does not compete with hybrid bonding at submicron pitch—rather, it complements it by providing a manufacturable, fine-pitch interconnect solution optimized for multi-micron pitch heterogeneous systems, large MCMs, and cryogenic environments. **Table 1** presents a comparison between bumpless and hybrid bonding.

Attribute	Cu–Cu Hybrid Bonding	Bumpless Flip-Chip (This Work)
Bonding Interface	Cu–Cu Pad Bonding	UBM–UBM Diffusion Bonding
Surface Roughness Requirement	< 0.4 nm RMS	Relaxed
Oxidation Sensitivity	High	Low (UBM-Protected)
Pad Topology	Recessed in Passivation	Raised Above Passivation
Post-Bond Anneal	Required	Eliminated
Minimum Pitch Demonstrated	< 1 μm (W2W)** < 10 μm (D2D)*	5 μm development

*D2D: Die-to-Die **W2W: Wafer-to-Wafer

Table 1: Direct comparison: BFC vs. hybrid bonding.

Summary

This study presents a bumpless flip-chip (BFC) interconnect technology based on UBM-to-UBM thermocompression diffusion bonding as a scalable and manufacturable solution for fine-pitch heterogeneous integration. By eliminating solder and avoiding the stringent surface requirements of hybrid bonding, BFC interconnect technology enables low-parasitic interconnects with improved tolerance to non-planarity and process variation.

The demonstration of 8 μm pitch interconnect arrays on a 200mm silicon MCM platform, combined with stable electrical performance down to 4.2K, confirms the robustness and versatility of this approach. BFC technology occupies a critical design space between solder microbumps and sub-micron hybrid bonding, offering a practical path forward for AI, HPC, and cryogenic systems, where manufacturability and system-level performance are paramount.

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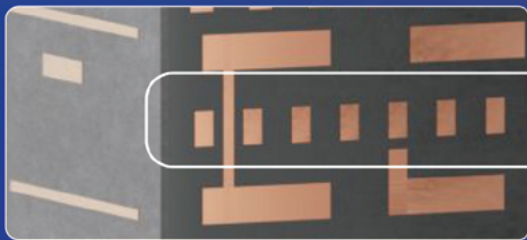
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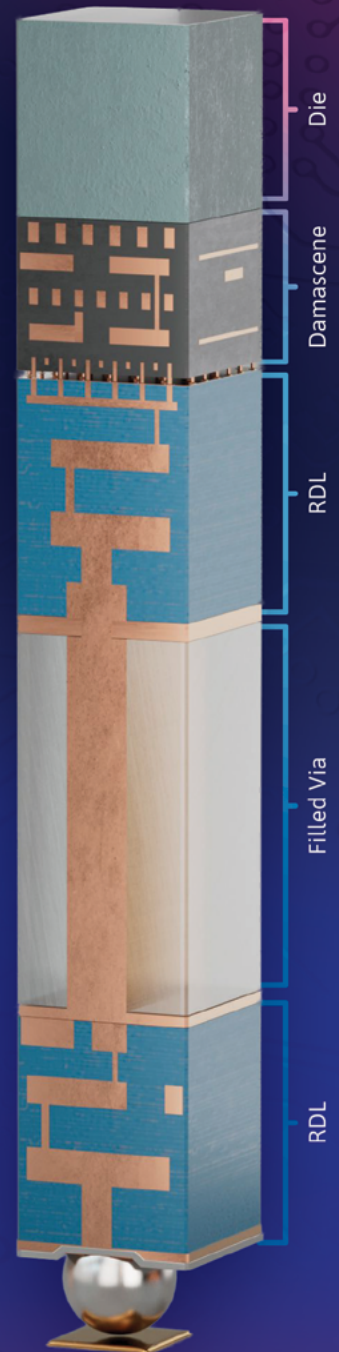


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Hybrid bonding: A critical enabler of next-gen 3D device architectures

By Tobias Wernicke, Bernd Dielacher [EV Group]

The rapid advancement of microelectronics is placing increasing pressure on conventional device architectures to deliver higher performance while maintaining efficiency and scalability. Traditional monolithic scaling is no longer sufficient. As a result, the industry is moving towards new integration schemes combining individually optimized components via advanced 3D stacking and heterogeneous integration approaches.

The technological shift towards new integration schemes is driven in large part by the rapid rise of artificial intelligence (AI), cloud computing, and other data-intensive applications. These workloads place unprecedented demands on compute performance, memory bandwidth, and energy efficiency. Modern data centers are scaling aggressively, and applications such as large language models and real-time analytics require tightly-coupled compute and memory architectures. At the same time, the need to balance performance with power consumption and thermal constraints is becoming more critical than ever. Consequently, system architectures must evolve to support higher data movement efficiency and reduced latency, enabling sustained performance improvements in an era defined by exponential data growth.

In this context, hybrid bonding is emerging as a key technology to meet these escalating system requirements. It provides ultra-fine-pitch connectivity well beyond the capabilities of traditional micro-bump solutions and has become a key enabler of advanced 3D and heterogeneous integration. But what is hybrid bonding? Unlike conventional bonding techniques, hybrid bonding uniquely combines dielectric-to-dielectric fusion bonding with metal-to-metal thermocompression bonding (TCB), usually copper to copper, within a single process step.

Plasma-activated fusion bonding allows the joining of two dielectrics at room temperature through surface-to-surface interactions, primarily driven by capillary forces and secondarily by Van der Waals forces. The initial state, called “pre-bond,” is strong enough to allow wafer handling but requires a subsequent annealing step to form a permanent bond. During this temperature treatment, the pre-bond is transformed into a covalent bond via a hydrolysis reaction between surface oxides and hydroxyl (OH) groups. This bonding mechanism is well described by the Gösele model [1]. To reduce the annealing temperature to a complementary metal-oxide-semiconductor (CMOS)-compatible range (<400°C), the substrates are plasma activated before the pre-bonding. This activation modifies surface hydrophilicity, which ultimately increases the density of reactants for the hydrolysis reactions, most notably hydroxyl (OH) groups [2].

The electrical connection during a hybrid bond is established via a very local metal-to-metal TCB. The driving mechanism during TCB is solid-state interdiffusion. Because there is no liquid metal phase involved, no related wafer-to-wafer alignment shift occurs.

The process of record to create hybrid-bondable structures is the damascene process (Figure 1). While the patterning process can vary significantly across different damascene integration schemes (e.g., dual-damascene, single-damascene), the preparation of the bonding interface

surface always involves an over-polishing step, resulting in a recessed metal surface relative to the bonding dielectric. Because both parts of the hybrid bonding—the plasma-activated fusion bonding and the TCB—require a temperature step, this over-polish is required to compensate for the mismatch in thermal expansion between the metal and the dielectric materials. In addition, to ensure reliable mechanical contact between both materials, the degree of metal recess is a critical parameter. Typically ranging from 2-4nm, the metal recess must be controlled across the entire substrate with sub-nanometer precision.

When looking at roadmaps (Figure 2), particularly in terms of pitch scaling and associated wafer-to-wafer overlay requirements, the primary challenge in current hybrid bonding processes becomes very obvious: How can wafer-to-wafer overlay be controlled and further improved? Considering the latest reference data [5], the success of a hybrid bond in terms of wafer-to-wafer overlay is typically evaluated based on the maximum misalignment vector measured across the wafer. However, to optimize wafer overlay performance, it is essential to understand the individual contributors to misalignment and their respective origins.

The EVG overlay model analyzes an overlay measurement, which represents the vector-based misalignment between top-to-bottom alignment marks at multiple locations across the wafer

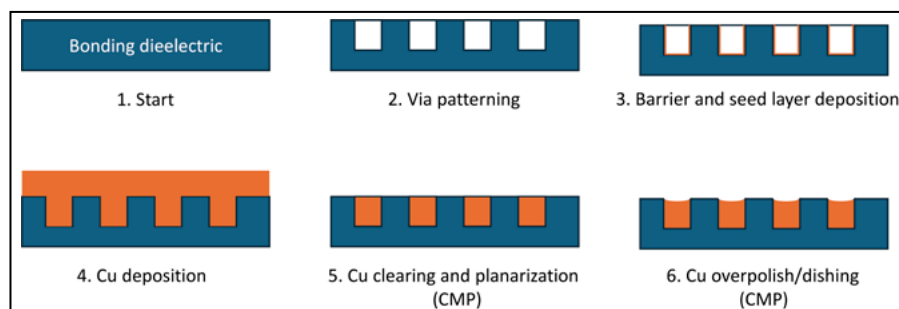


Figure 1: Simplified damascene process flow. SOURCE: EVG

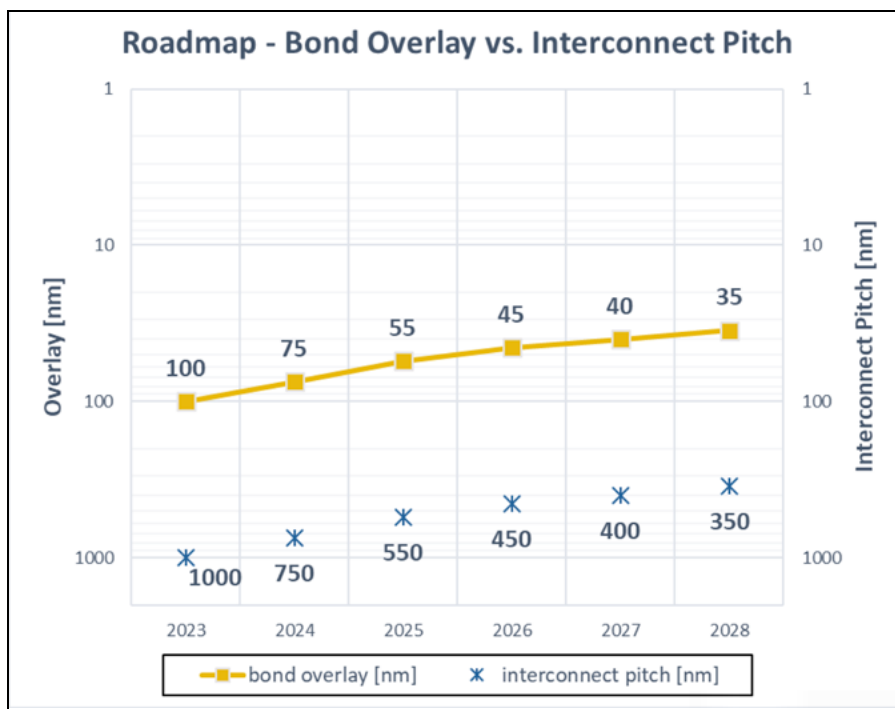


Figure 2: Roadmap bond overlay vs. interconnect pitch [3]. SOURCE: EVG

(“Overlay”), and separates them into overall linear (“Alignment”) and nonlinear (“Distortion”) components (Figure 3).

The alignment component describes the global wafer-to-wafer shift and comprises four sub-components: Translation in the x-direction, translation in the y-direction, rotation, and wafer-to-wafer scaling. By subtracting these linear components from the measured overlay, the remaining residuals—referred to as distortion—can be isolated and analyzed.

Origin of alignment errors

Global shifts between wafers in x- and y-directions are straightforward to understand and can be directly corrected using standard wafer-to-wafer optical alignment systems. The scaling component, however, can originate from various sources, such as environmental differences during top- and bottom-production, respectively, and different stress-induced wafer shapes.

It is important to mention that the bonding process itself also introduces a scaling component. This is primarily attributed to the point-contact initiation of the bonding process via a bond pin, which triggers the fusion bond process (Figure 4). During the bonding process, the bond pin locally pushes the center of the top wafer towards the bottom

wafer while the outer regions are still being held by vacuum. This results in a radial stretching of the top wafer, which is transferred to the bottom wafer as the bond wave propagates. Various techniques are available in

industry to compensate for this inherent scaling effect, as illustrated in Figure 5. Because the scaling induced by the bonding process exhibits a strong linear dependence on the curvature of the top wafer, a highly effective compensation method is to intentionally induce a matching curvature on the counter-wafer, thereby canceling the inherent scaling effect.

Origin of distortion errors

When analyzing distortion behavior and its origins in hybrid bonding, a distinction must be made between blank and patterned wafers. As shown in Figure 6, the bond wave propagation of a patterned wafer differs significantly compared to a blank wafer, adopting a more square-shaped profile. This behavior arises because the bond wave of the dielectric regions must propagate around the embedded metal features, which are typically arranged in orthogonal (horizontal-vertical) layouts. As a result, the bond wave front is constrained by the metal pattern geometry, which translates into different bond wave shapes. Ultimately, this behavior has a direct impact on the overlay.

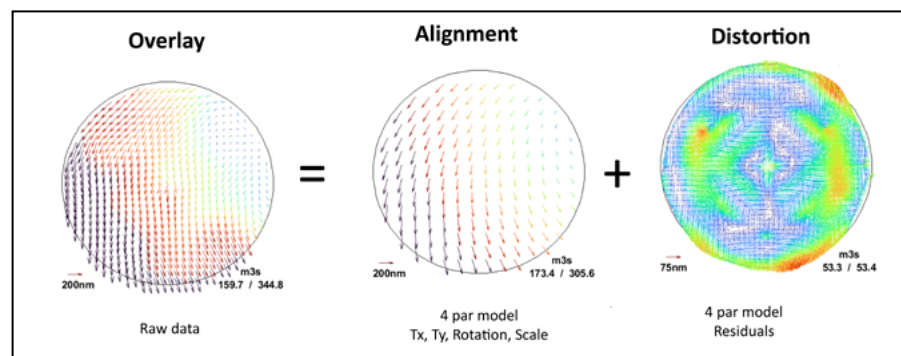


Figure 3: Example of overlay breakdown. SOURCE: EVG

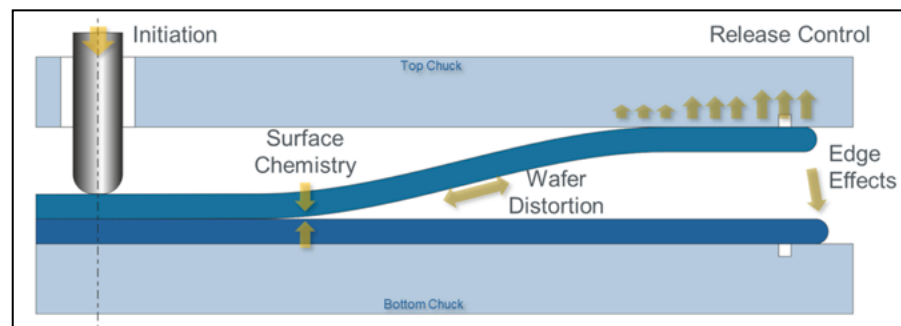
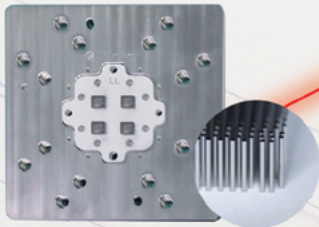


Figure 4: Scaling and distortion dynamics during the fusion bonding process. SOURCE: EVG



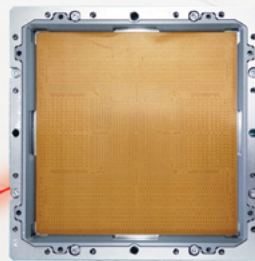
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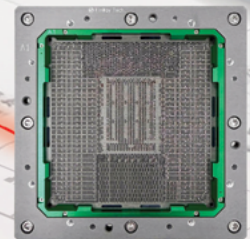
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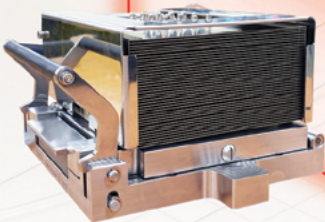
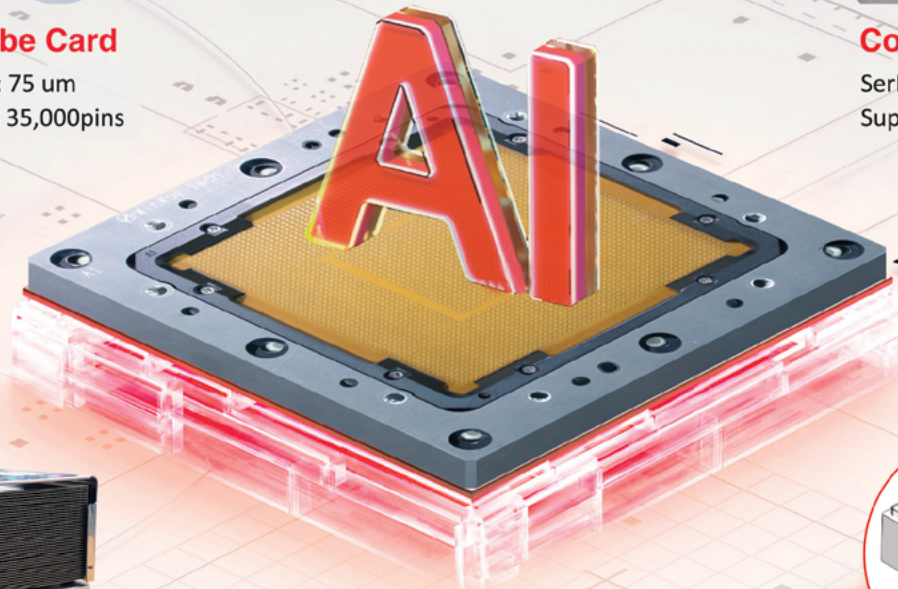
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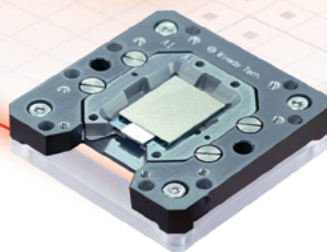
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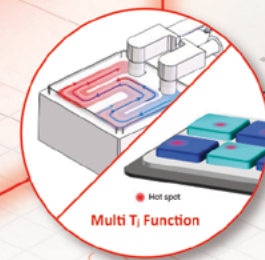
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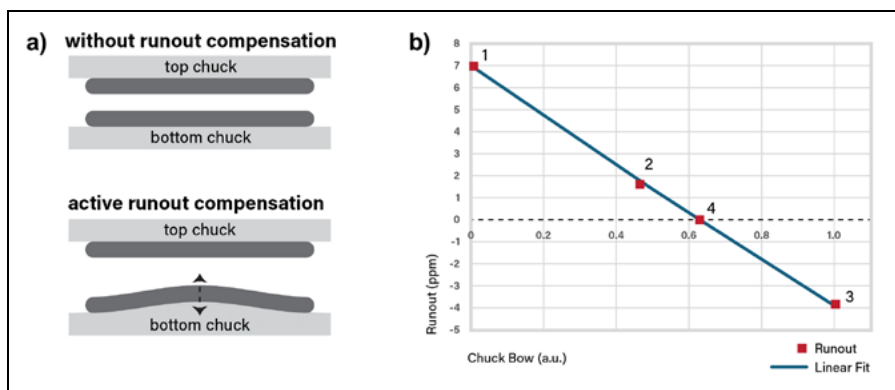


Figure 5: a) Schematic illustration of scaling (runout) compensation in wafer bonding; and b) Linear relationship between chuck bow and runout [4]. SOURCE: EVG

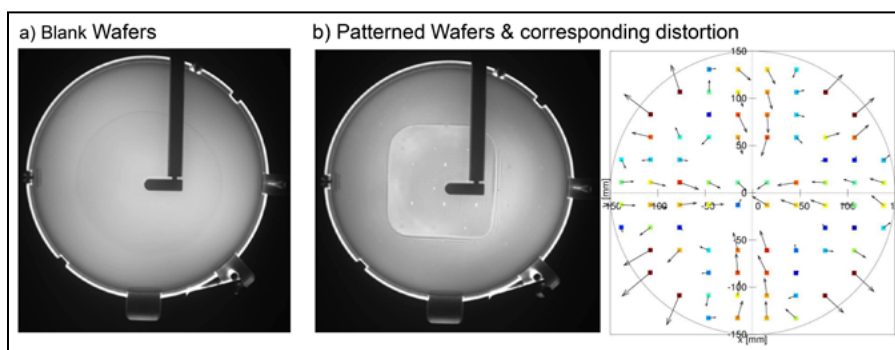


Figure 6: Bond wave propagation behavior of: a) Blank vs. b) Patterned wafers. SOURCE: EVG

Benefits of hybrid bonding

Hybrid bonding offers a scalable pathway to extend system-level performance beyond the limits of traditional device scaling. It enables each functional chip to be independently optimized, leveraging the most suitable process node or material while maintaining tight system-level coupling. As a result, designers can move beyond monolithic scaling and adopt more flexible, performance-driven integration strategies. These approaches are already being deployed in applications such as AI accelerators and high-performance computing (HPC), where memory bandwidth and latency represent critical bottlenecks. In this context, hybrid bonding enables the close integration of logic and memory, supporting advanced architectures such as high-bandwidth memory (HBM) stacks and emerging logic-on-memory concepts.

The developments noted above align closely with imec's CMOS 2.0 vision, which extends 3D integration towards system-level partitioning into distinct tiers, reconnected through dense vertical interconnects. These architectures require extremely fine pitches for logic-to-logic and memory-to-logic stacking. Recent

results from imec and EV Group highlight the state of the art in hybrid bonding [5], demonstrating wafer-to-wafer hybrid bonding at a 200nm interconnect pitch with sub-40nm alignment accuracy across full 300mm wafers, representing a record level of precision (Figure 7). This breakthrough, enabled by optimized materials, chemical-mechanical polishing (CMP) processing, and advanced bonding equipment, marks a key milestone toward the interconnect densities required for CMOS 2.0 and future 3D system architectures. Looking further ahead, hybrid bonding is also expected to support future device architectures such

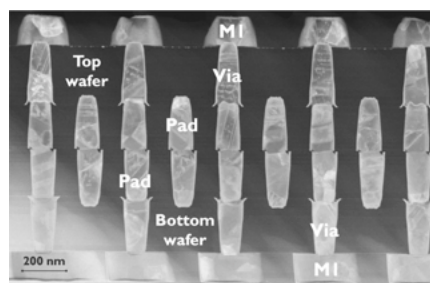


Figure 7: Transverse electromagnetic mode (TEM) image of daisy chain structures on a 200nm hexagonal pad grid with equal hybrid pad size and 25% designed Cu density [5]. SOURCES: imec/EVG

as complementary field-effect transistor (CFET), where vertical stacking at the transistor level will impose even more stringent requirements on nanoscale interconnect definition and alignment.

New hybrid bonding challenges

The challenges of these scaling and integration strategies extend beyond wafer-to-wafer overlay requirements and include material-related issues, such as thermal and electrical properties, discussed below.

In terms of thermal properties, particularly in the context of logic-memory integration, increasingly stringent temperature budget must be maintained to avoid issues such as unwanted diffusion or excessive thermomechanical stress. This temperature budget can be below 200°C, which is significantly below the commonly used annealing temperatures for hybrid bonding (around 300°C). One promising approach to achieve bonding at reduced temperatures is copper grain-engineering, specifically, fine-grain copper, often referred to in literature as nano-crystalline copper [6]. The modification of the grain structure is typically achieved during the copper electroplating by introducing different additives during deposition that impact the grain-growth behavior. Because the metal bonding mechanism in hybrid bonding is based on diffusion, the use of fine-grain copper is motivated by the increased density of grain boundaries, which act as fast diffusion pathways. Diffusion along grain boundaries occurs at significantly higher rates than bulk (volume) diffusion. This allows interconnect formation similar to “conventional copper,” but at significantly reduced temperatures. During annealing, fine-grain copper recrystallizes resulting in low electrical resistivity.

Regarding the electrical properties of hybrid bond interconnects, significant research efforts are focused on sub-10nm via dimensions, as required for advanced logic applications, such as the hybrid-bonded CFET architecture. While copper-based hybrid bonding is well established, scaling copper to these dimensions becomes increasingly challenging for two main reasons. First, copper can easily diffuse into silicon, necessitating the use of a robust diffusion barrier within the interconnect structure. As dimensions shrink, this barrier must scale accordingly. Second, the electrical resistivity of thin-film copper increases exponentially for

film thicknesses approaching the mean free path of copper (~40nm), primarily due to enhanced surface and grain boundary electron scattering. Therefore, alternative materials are being investigated—the most promising being ruthenium—particularly when grown epitaxially, as it is well suited for front-end integration.

As shown in **Figure 8**, ruthenium, especially epitaxial ruthenium, exhibits favorable resistivity for thin films below 10nm. In addition, ruthenium interconnects do not require diffusion barriers, like for copper interconnects. This enables a significantly higher fraction of the interconnect cross section to be occupied by the conducting material, rather than by auxiliary layers such as barriers [7]. Consequently, ruthenium is considered one of the most promising candidates for advanced interconnect scaling in hybrid bonding applications.

An equally important aspect of

advanced hybrid bonding integration schemes is the need to enable the extreme wafer thinning of these architectures. As interconnect pitch scales into the sub-micron regime, the entire stack must become thinner, flatter, and more precisely controlled. This shifts temporary bonding from a supporting process step to a critical technology driver on its own. An enabler in this domain is EVG's LayerRelease™ technology, an infrared (IR) laser debonding technology based on silicon carriers and inorganic release layers that allows fusion bonding to the carrier—providing superior rigidity during device thinning. In addition, its inorganic nature is front-end compatible and supports high-temperature processing steps directly on the carrier. IR laser debonding has emerged as a particularly effective solution for next-generation integration schemes that require extreme thinning in advanced process flows.

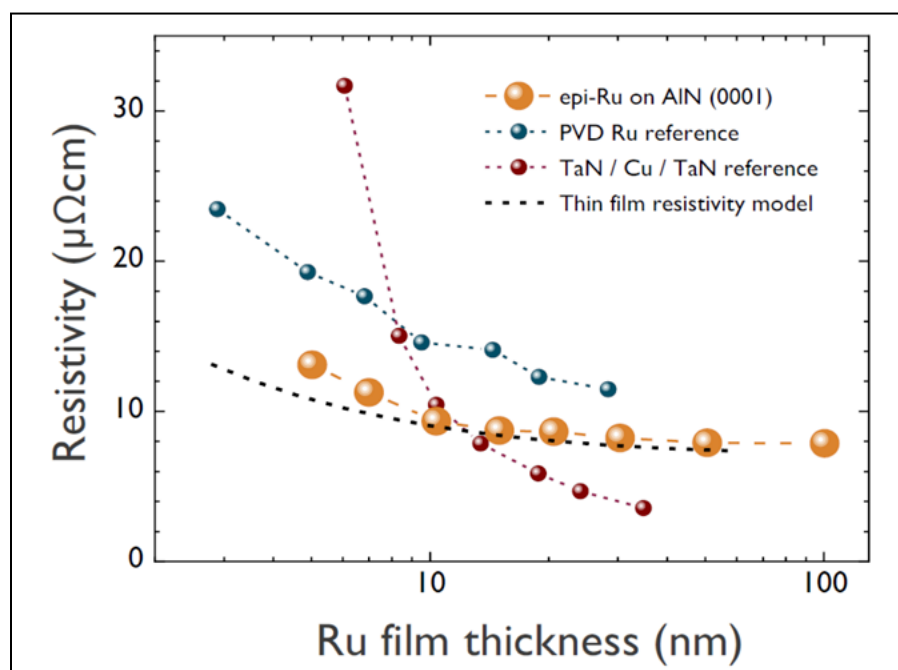


Figure 8: Resistivity of ruthenium and other metals related to film thickness [7]. SOURCE: Used with permission of IEEE

Summary

As the semiconductor industry continues to push beyond the limits of conventional scaling, hybrid bonding is rapidly evolving into the dominant interconnect technology for advanced integration. While wafer-to-wafer overlay is constantly optimized, new materials and processes are being introduced to enable new technology nodes and integration schemes.

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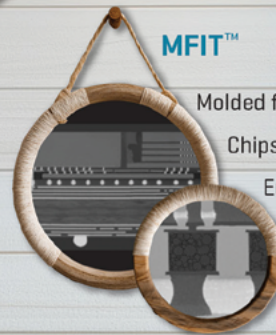
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Achieving faster ramps/lower costs with yield prediction technology in FOPLP lithography

By John Chang, Jian Lu, Timothy Chang [Onto Innovation]

Artificial intelligence (AI) packages combine multiple advanced logic and high-bandwidth memory (HBM) devices into a single architecture supporting higher I/O density, increased bandwidth, and improved power efficiency. But as AI packages grow in complexity and volume, manufacturers are under pressure to ramp quickly while maintaining high yield. For those looking to scale production of these complex packages, the economics favor approaches that improve substrate utilization and deliver more output per cycle. To accomplish this, manufacturers increasingly are adopting fan-out panel-level packaging (FOPLP) to maintain cost efficiency at scale.

Traditional wafer-based processing typically achieves approximately 55% substrate utilization with limited output per wafer. Panel-based approaches, however, can reach approximately 74% to

81% utilization according to internal Onto Innovation estimates—while significantly increasing the number of packages produced per substrate. These panel-based approaches reinforce the economic advantage of FOPLP at scale while improving material utilization across the substrate (**Figure 1**).

FOPLP places new demands on lithography in the form of nonlinear distortion, die shift, and overlay variation across the panel. These issues directly constrain yield and limit the ability of manufacturers to operate efficiently and at scale. Further complicating matters, traditional correction approaches offer ill-fitting lithography solutions for AI packaging, with most manufacturing strategies hampered by a fundamental tradeoff between yield and throughput. These challenges directly impact manufacturing cost, capacity utilization, and time to production.

Addressing the problems noted above by conventional means can require extensive iteration to identify acceptable operating conditions. This approach, however, is unacceptable for accelerated ramps to high-volume manufacturing (HVM). As a result, lithography itself has become a limiting factor in achieving consistent yield, controlling cost, and accelerating ramp time. These pressures are not incremental, however—they are structural consequences of the transition from wafer-based to panel-based manufacturing at larger formats and higher levels of integration. These challenges must be addressed for successful HVM.

In this article, we will examine how nonlinear distortion and lithography correction tradeoffs hamper yield and throughput in FOPLP manufacturing and why conventional approaches impede ramp time to HVM. We will also explore how yield prediction technology enables earlier process visibility, reduces iteration, accelerates ramp, and lowers the cost of yield loss in advanced AI packaging.

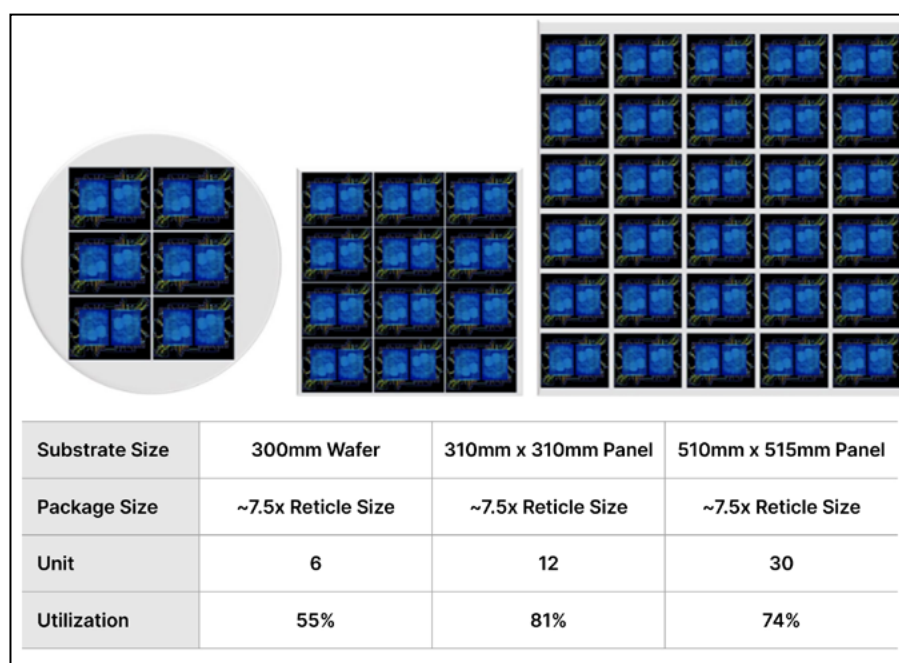


Figure 1: Substrate utilization efficiency improves from 55% for a 300mm wafer (supporting 6 units per substrate) to 81% for a 310×310mm panel (12 units per substrate), and reaches 74% for a 510×515mm panel (30 units per substrate).

Conventional correction strategies

As noted earlier, in FOPLP lithography, pattern errors and die shift contribute to yield loss. These errors originate during reconstitution and redistribution layer (RDL) processing and do not follow uniform distributions (**Figure 2**). Instead, they exhibit region-specific, nonlinear spatial variation across the panel, often transitioning between positive and negative error regions. Because the distortion is nonlinear and spatially nonuniform, traditional linear correction approaches cannot maintain overlay accuracy across the entire substrate. This distortion results in localized misalignment, which directly reduces yield and introduces panel-level variability that is difficult to

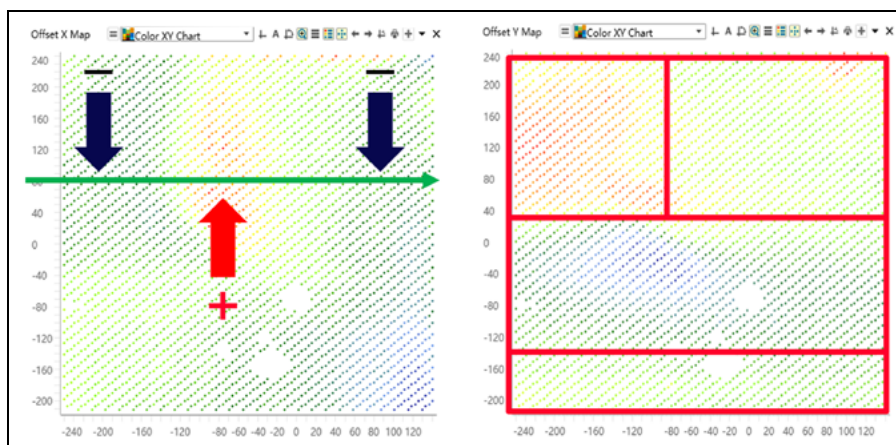


Figure 2: Heat maps of error distribution in regular FOPLP substrates. Blue regions indicate negative errors, while red regions represent positive errors. The heat maps reveal nonlinear pattern errors across the substrate.

manufacturers to control in HVM. To address this challenge, multiple correction strategies are required to compensate for spatial variations at the exposure tool level. Unfortunately, each one introduces yield and throughput tradeoffs, discussed below and shown in **Figure 3**.

- Global correction applies a single adjustment across the panel (**Figure 3a**). While this strategy maintains high throughput, it fails to compensate for localized errors, resulting in poor yield.
- Zone-based correction improves performance by applying localized corrections, but its effectiveness is limited, with observed yields typically ranging from 40% to 90% (**Figure 3b**).
- Die-by-die correction provides the highest overlay accuracy by aligning each die individually, but this strategy is time-intensive and, as a result, reduces throughput (**Figure 3c**).
- Site-by-site correction offers a partial compromise that improves yield while maintaining more practical processing times (**Figure 3d**). This strategy, however, requires careful tuning. As a result, manufacturers must operate within a constrained optimization space.

In practice, selecting among the strategies listed above requires manufacturers to balance yield targets against throughput requirements while maintaining production schedules and tool availability. Once a minimum yield threshold is defined by engineers, multiple operating points can emerge. The preferred solution is typically one that achieves acceptable yield while maximizing throughput—this is the

sweet spot (**Figure 4**). Identifying the sweet spot requires extensive production constraints, repeated trials, and data re-analysis, resulting in increased engineering cost, extended development timelines, and delayed production ramp.

Even when engineers are able to optimize this tradeoff, existing correction strategies remain fundamentally constrained. Because these strategies rely on predefined models and localized adjustments, they cannot completely compensate for complex, panel-scale distortion patterns. As a result, residual overlay errors persist, limiting achievable yield and forcing continued process optimization.

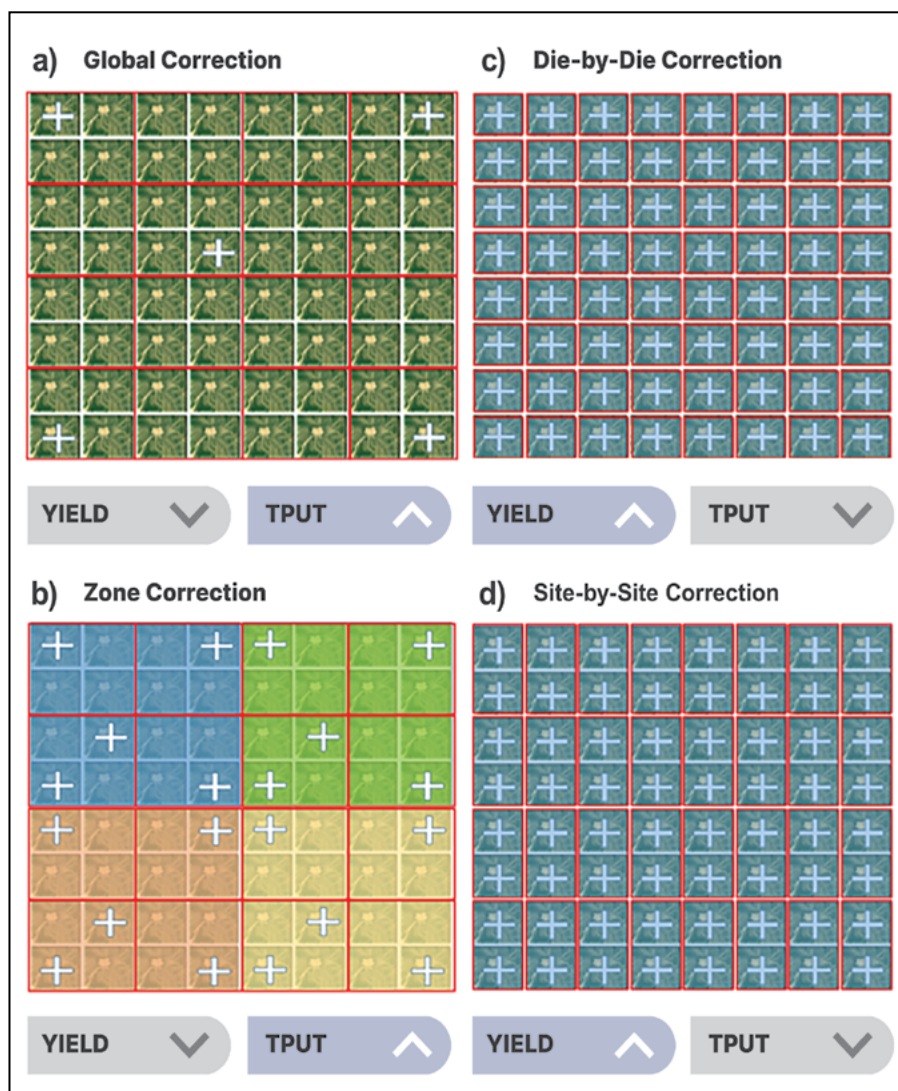


Figure 3: Lithography correction strategies to address the nonlinear errors in FOPLP substrate: a) Global correction: A single correction is applied uniformly across the entire substrate; b) Zone correction: The substrate is divided into zones, and corrections are applied to each zone individually; c) Die-by-die correction: Each die on the substrate is aligned and corrected individually; d) Site-by-site correction: Corrections are applied to multiple dies within a larger exposure field at once.

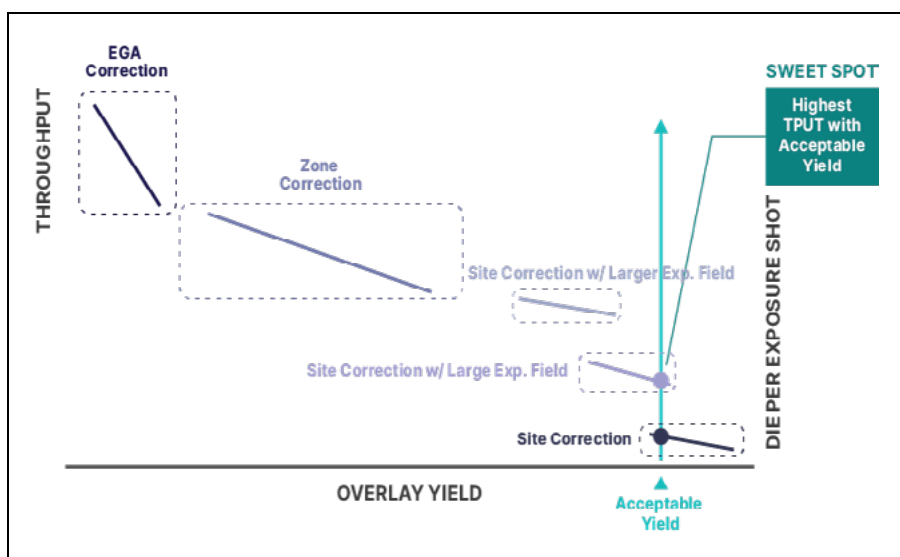


Figure 4: Determining the sweet spot in a regular lithography process requires significant time and effort because adjustments often necessitate repeated trials and data re-analysis.

Determining optimal lithography conditions requires repeated experiments across multiple variables, including exposure settings, field configurations, and alignment strategies. Each iteration involves exposure, measurement, and analysis, thereby increasing engineering workload, material usage, and development cycle time while extending development timelines.

Improving yield often requires adopting more granular correction strategies that inherently reduce throughput. Such correction strategies create structural inefficiency: Higher accuracy comes at the expense of productivity, limiting overall manufacturing output and reducing effective tool utilization in HVM environments.

Conventional workflows also rely heavily on post-lithography inspection to evaluate yield. Because defects are detected after processing is complete, corrective actions are inherently reactive, preventing manufacturers from addressing yield issues before additional process value has been added to the substrate. This results in avoidable rework, scrap, additional cycle time, and higher labor cost when excursions are detected late.

A new strategy

To overcome the limitations noted above, manufacturers need a new strategy that reduces reliance on iterative experimentation and

enables earlier visibility into yield performance. This brings us to yield prediction technology (**Figure 5**). This technology addresses FOPLP lithography limitations by introducing a predictive approach to process control. Instead of relying solely on post-process inspection, this method enables manufacturers to forecast yield outcomes before lithography is completed—a clear time saver.

By combining offline metrology data with predictive analytics and machine learning algorithms, manufacturers can evaluate process performance in advance and select optimal process conditions prior to exposure and identify optimal operating conditions without extensive physical experimentation. This reduces iteration cycles, accelerates ramp, and

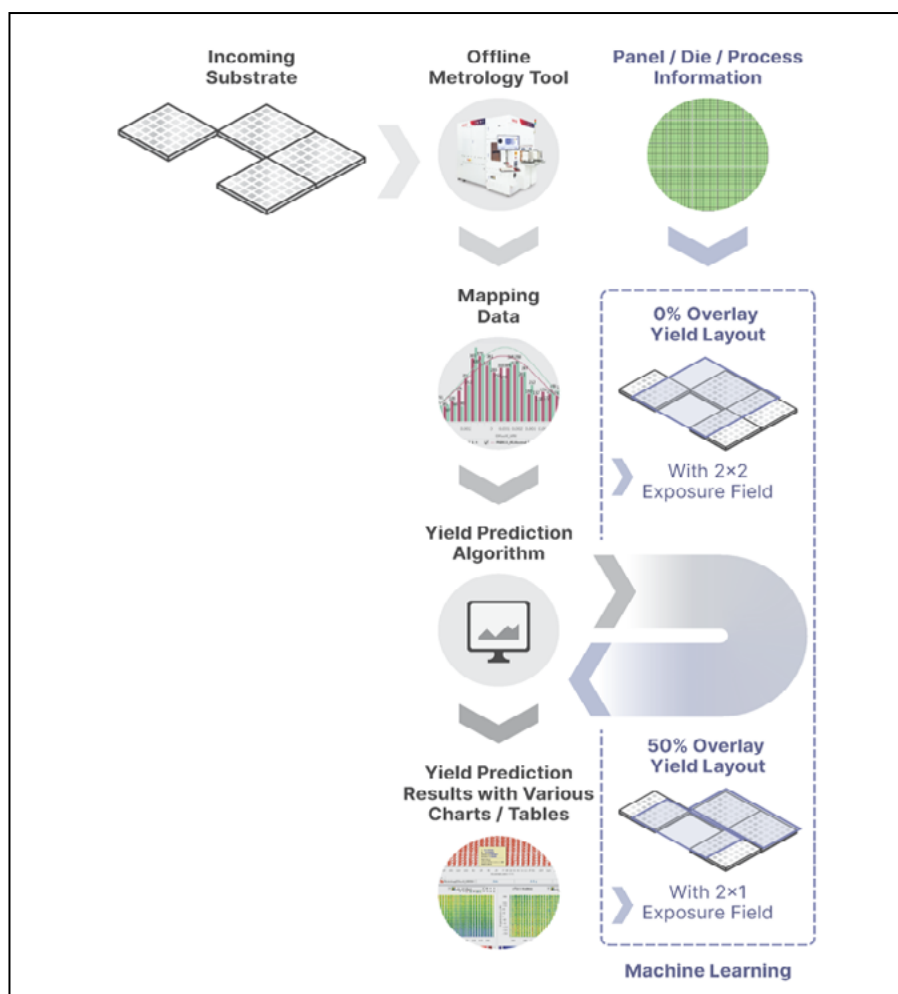


Figure 5: Graphic depicting a yield prediction technology working scenario. An offline metrology tool captures data from a substrate, creating a comprehensive mapping dataset. The algorithms analyze the mapping data to predict overlay yield. The results are presented through a variety of visual formats, including detailed tables and graphical charts, enabling intuitive analysis, and facilitating root cause identification.

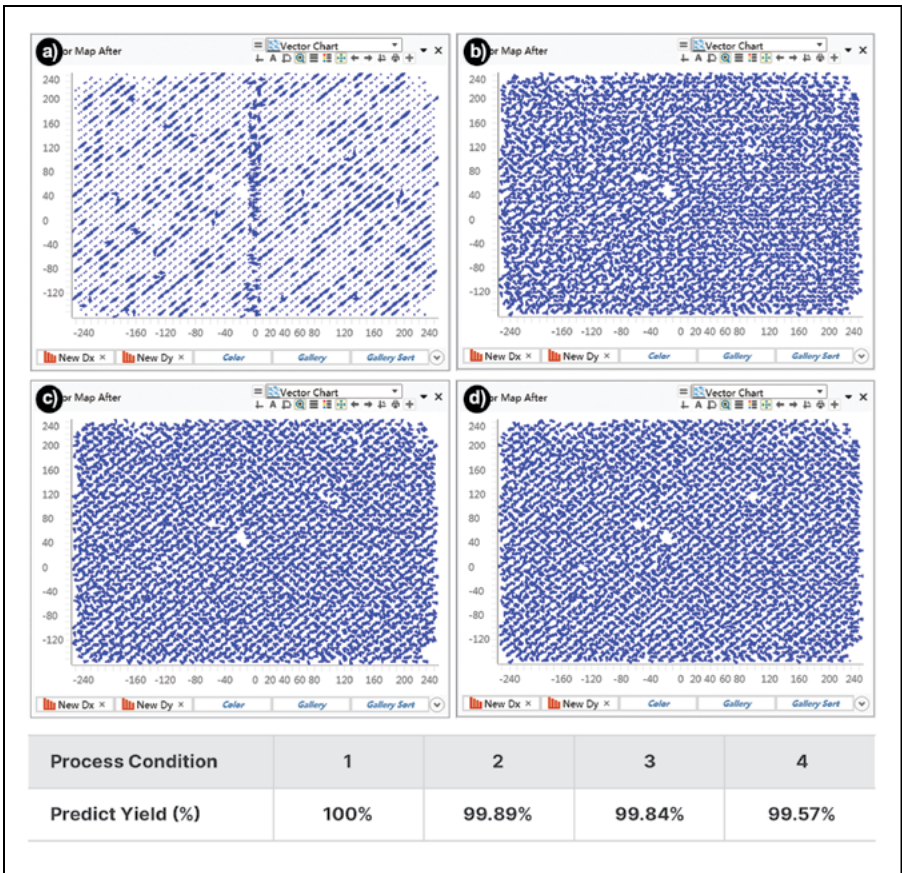


Figure 8: Vector maps of residual overlay errors are generated using yield prediction based on various process conditions. The maps are organized by shot size: a) 1x1, b) 3x3, c) 4x4, and d) 6x6. By leveraging this data-driven approach, users can accelerate process refinement, reduce trial-and-error iterations, and achieve more efficient improvements during the R&D stage, ultimately enhancing production efficiency and yield outcomes.



Figure 9: Visual charts and analytical tools of yield prediction technology showing: a) Various parameters for in-depth analysis; b) X-axis overlay error heat map; c) Y-axis overlay error heat map. A comparison of these maps reveals that the Y-axis exhibits the most significant overlay errors, which directly contribute to yield loss. This insight enables users to pinpoint the root cause of the issue and take corrective actions effectively, thereby improving overall process performance.

By standardizing inspection criteria and implementing training, the variability was reduced and prediction accuracy improved to within 0.2% to 0.8%. These results confirm predictive modeling can achieve the precision required for both development and production decision making. Beyond validation, this capability provides practical value across both development and manufacturing environments.

Accelerating development

In development environments, yield prediction technology enables simulation-based process optimization. Engineers can evaluate multiple parameter sets, analyze overlay error behavior, and identify yield-limiting mechanisms without conducting repeated physical experiments. By reducing the number of required experiments, this approach shortens development cycles, lowers material consumption, and accelerates process qualification. It also improves the ability to understand process sensitivities and enables more targeted optimization strategies.

Practically, the new approach offers manufacturers a simulation-first workflow: Teams can identify optimal parameters through simulation and then validate the predicted operating conditions using qualification substrates. This approach reduces both the time and cost associated with trial-and-error lithography learning (Figure 8). While these benefits are most evident during development, the impact extends further into production.

In production, yield prediction enables the earlier detection of defects within the lithography process flow, including in the coating, exposure, development, and post-treatment steps. Because early process defects can propagate through subsequent steps, the late discovery of defects can drive rework or, in some cases, permanent yield loss after additional value has already been added.

By enabling earlier visibility and decision making, predictive analysis allows manufacturers to intervene before issues escalate (Figure 9). This analysis reduces rework, limits scrap, and prevents additional value from being added to defective substrates. Equally as important, predictive

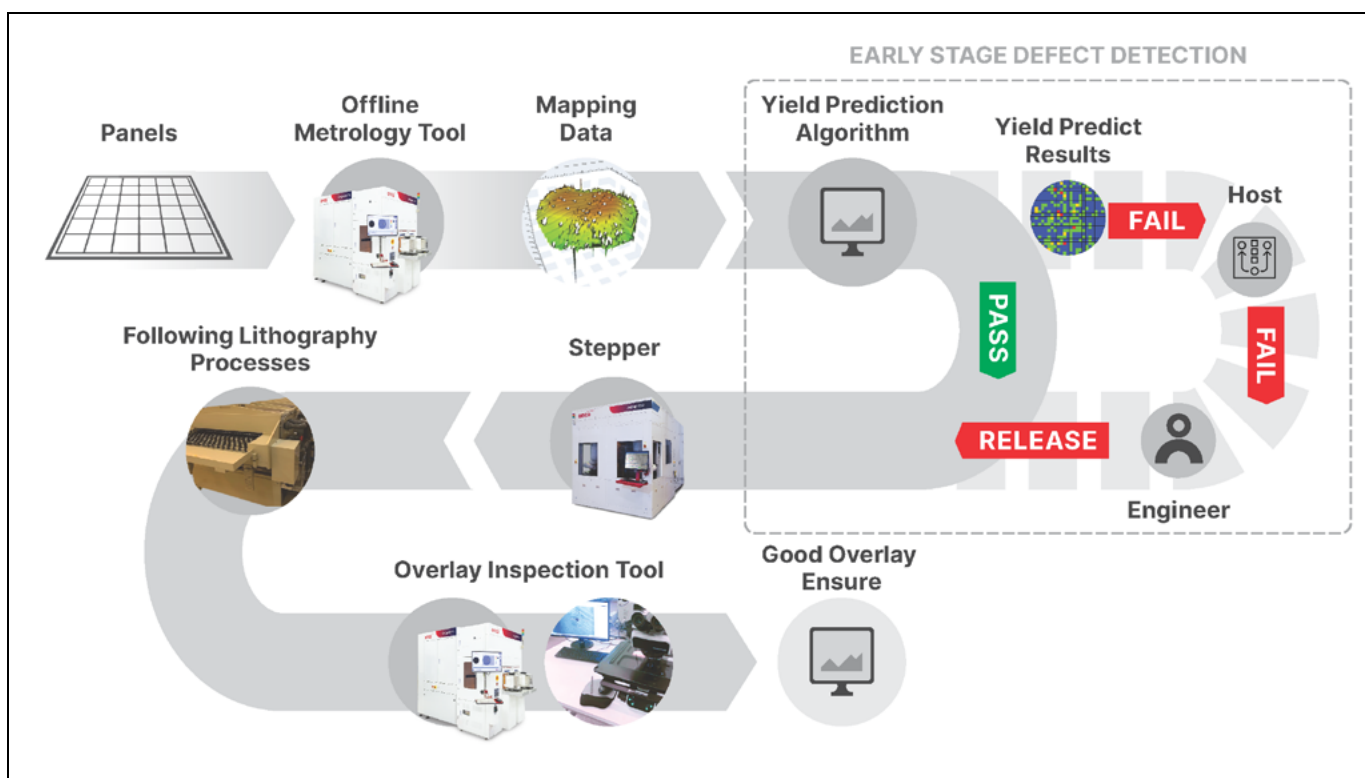


Figure 10: The workflow of yield prediction technology for real-time, in-line process monitoring. By leveraging predictive insights, users can proactively address issues before they escalate, ensuring higher yield outcomes while minimizing rework, downtime, and associated costs.

analysis reduces the manpower, time, and costs associated with late-stage troubleshooting in FOPLP lithography, enabling engineering teams to respond earlier in the process and freeing them to focus on process optimization rather than reactive issue resolution.

As described above, yield prediction can be implemented as a form of preemptive quality control in mass production lines, supporting early stage screening and more reliable containment of excursions before they impact large substrate volumes (**Figure 10**). More importantly, yield prediction shifts defect management upstream, allowing engineers to correct for potential yield loss rather than reacting to it after completion. Taken together, these capabilities address the core constraints of FOPLP lithography.

Summary

FOPLP lithography is fundamentally constrained by nonlinear distortion, yield-throughput tradeoffs, and the rising costs of AI packages. These challenges are compounded by conventional process control approaches that rely on iterative experimentation and post-process inspection, both of which limit ramp speed and efficiency and delay the transition to HVM. Yield prediction technology addresses these limitations by enabling early visibility into the production process and reduces engineering reliance on trial-and-error optimization. This approach provides a practical and scalable method for improving both yield and throughput in FOPLP lithography.

By shifting process control from a reactive to predictive strategy,

manufacturers can reduce yield loss, accelerate ramp to HVM, and improve overall manufacturing performance, thereby enabling more stable, cost-efficient production at scale.

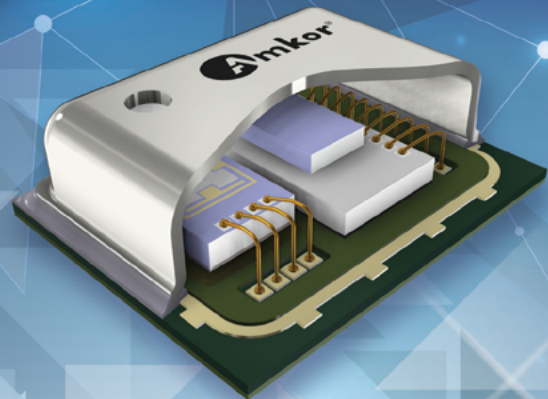


Biography

John Chang is a Senior Principal Product Marketing Manager at Onto Innovation, Hsinchu, Taiwan. He holds a Master's degree in Nanoelectronics and Photonics from National Chung Hsing University and has over 22 years of experience in semiconductor advanced packaging. Throughout his career, he has authored over 20 publications and holds numerous U.S. and Taiwan patents in metrology, lithography, advanced packaging, and AICS. Email john.chang@ontoinnovation.com

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Potential applications of Cu-Cu hybrid bonding to heterogeneous integration of chiplets

By John H. Lau [Unimicron Technology Corporation]

In the past, the performance of semiconductor products has been driven by Moore's Law—smaller feature size leads to more transistors. However, in the future, the performance will not only be driven by purely smaller process nodes, but also by the following: 1) How the chips are stacked; 2) How the chips are interconnected; 3) How the chips are cooled; and 4) How the chips are packaged. The methods, among others, are: 1) Chiplets heterogeneous integration (HI) [1]; 2) Bridges connecting chiplets [2]; 3) Cu-Cu hybrid bonding (HB) [3]; 4) Panel-level packaging (PLP) [4]; 5) Glass packaging [5]; 6) Co-packaged optics (CPO) with Si/Glass photonics [6]; and 7) Superior thermal management [5]. Cu-Cu HB is the focus of this brief article.

Cu-Cu HB is one of the flip-chip bumpless assembly technologies. As shown in Figure 1, Cu-Cu HB yields the finest pad and pitch of flip-chip interconnects. It can be applied to very high-density and high-performance applications. Additionally, HB leads to a low-profile, low-thermal resistance, and low-insertion loss 3D package. It is mostly suitable for silicon-to-silicon and silicon-to-glass assemblies. The assembly methods can be chip-on-chip (CoC), chip-on-wafer (CoW), wafer-on-wafer (WoW), chip-on-wafer-on-wafer (CoWoW), wafer-on-wafer-on-wafer (WoWoW), reconstructed wafer, direct transfer bonding, etc. [7-12].

Cu-Cu HB is an old packaging technology. It has been in high-volume manufacturing (HVM) for more than 10 years. In this article, 13 different potential applications of Cu-Cu HB to

chiplets HI will be briefly mentioned. Some recommendations will be provided. A brief history and fundamentals of HB will be presented first.

The origin and brief fundamentals of HB

HB that combines a dielectric bond with a metal bond to form an interconnection is known industry wide as a low-temperature direct bond interconnect (DBI[®]) that operates at room temperature and then anneals at, e.g., 150°C–300°C. DBI[®] was invented by the Research Triangle Institute (RTI) and patented as ZiBond[™] (a direct oxide-to-oxide bonding that involves wafer-to-wafer processing at room or low temperatures to initiate high bond strengths). Between 2000 and 2001, Fountain, Engquist, Tong, and several other colleagues, along with their ZiBond[™] [13-14], founded Ziptronix as a spin-out of RTI.

Between 2003 and 2005, based on its ZiBond[™] technology, Ziptronix combined the dielectric bond with embedded metal to simultaneously bond wafers and form the interconnects at low temperature (so-called DBI[®]) [15-16]. The breakthrough for the DBI[®] technology came in the

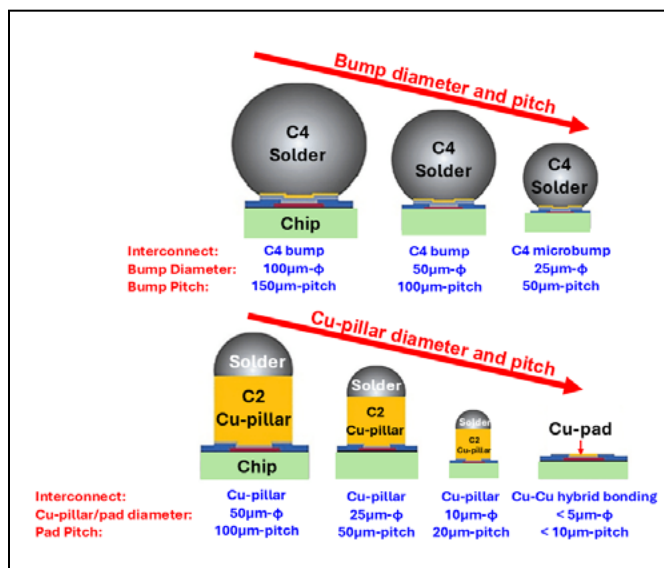


Figure 1: Trends in flip-chip interconnects.

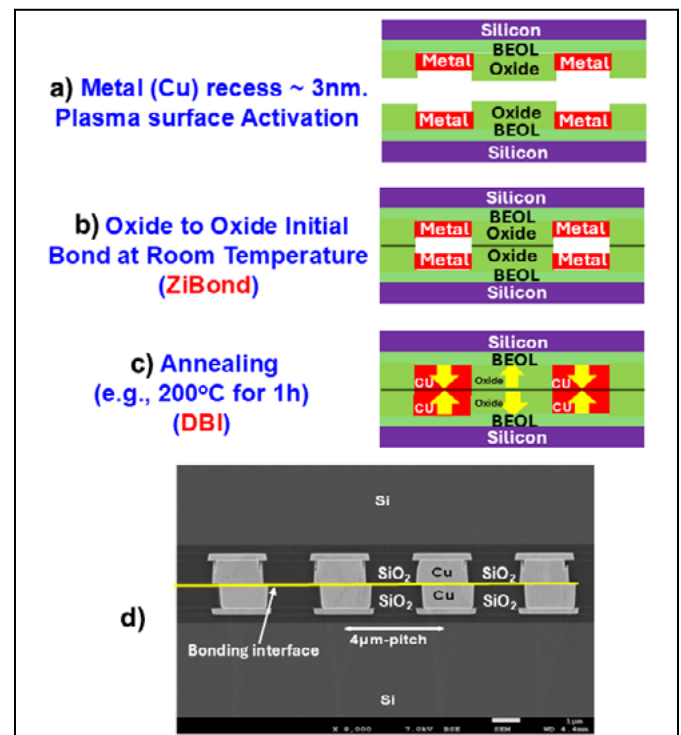


Figure 2: Brief fundamental (key process steps) of hybrid bonding.

spring of 2015 when Sony, already using the “ZiBond™” oxide-to-oxide bonding technology for its complementary metal-oxide-semiconductor (CMOS) image sensor (CIS), extended its license to include DBI®. Today, the industry calls DBI®, “hybrid bonding.”

Figure 2 shows the key process steps for the HB. First, controlling nanoscale topography is very important. The dielectric surface should be extremely flat and smooth before activation and bonding. Chemical–mechanical polishing (CMP) should achieve a very low dielectric roughness (<0.5nm rms) and a certain recess (e.g., 3nm) of metal areas below the dielectric surface, as shown in **Figure 2a**. Upon contact, the dry plasma-activated dielectric surfaces bond together instantaneously, as shown in **Figure 2b**, at room temperature. Metal-to-metal bonding occurs during batch annealing. The coefficient of thermal expansion of metals is typically far larger than for dielectrics. The metal expands to fill the gap and then builds up the internal pressure, as shown in **Figure 2c**. It is under this internal pressure and annealing temperature that metal atoms diffuse across the interface, making a good metal-to-metal bond and, therefore, electrical connection. In this case, the copper oxidation during bonding is minimized because the bonded oxide layer surrounding the copper interconnect protects the interconnect from oxidation in the annealing oven, thereby minimizing Cu oxidation during the anneal. The bonded oxide surface also hermetically seals the Cu interconnect during operation. **Figure 2d** shows an optimal Cu-Cu HB with 4μm-pitch and 2μm-diameter pads.

Potential application of Cu-Cu HB to HI of chiplets

The following sections discuss a number of potential applications of Cu-Cu HB to the HI of chiplets.

HB bridge for HI of chiplets. Unimicron proposed the use of Cu–Cu hybrid bonding for the bridge between chiplets in chiplet design and HI packaging (**Figure 3**). The advantages of this structure are: 1) Higher density, 2) Finer pitch, 3) Better performance, and 4) Ordinary package substrate. The patent has been granted [17].

3D chiplets embedded in build-up substrate with HB. Embedding chips in build-up package substrates for high-density and high-performance applications is the trend for high-performance computing (HPC). In order to embed more chips in the substrate, stacking up the chips in the build-up package substrate is one of the methods and HB can keep the thickness of the stacking to a minimum. **Figure 4** shows an example of embedded 3D chiplets with HB in a build-up package substrate.

Package-on-package: Chiplets embedded in fan-out (RDL-First) EMC with HB. Package-on-package (PoP) is a common packaging format for housing the application processor (bottom package) and the mobile memory (upper package). In order to save semiconductor manufacturing cost, the large application processor is split into small chiplets (to have a higher semiconductor manufacturing yield). Silicon bridges are used to connect the chiplets and Cu-Cu HB is used between the bridges and processor chiplets (**Figure 5**).

2.5D IC integration of SoC and HBMs with bridge by HB. Today, the package of choice for HPC and data centers driven by AI is the chip-on-wafer-on-substrate (CoWoS®). In order to

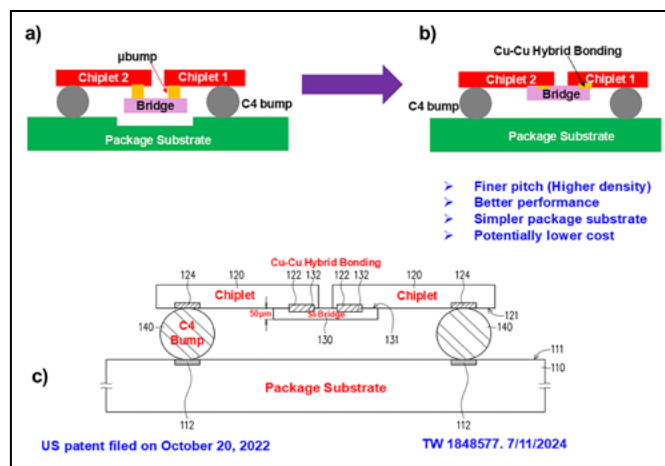


Figure 3: Hybrid bonding bridge for the heterogeneous integration of chiplets.

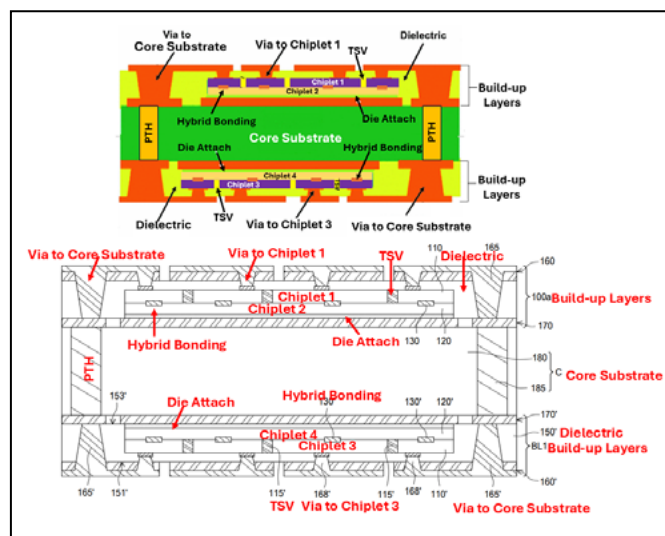


Figure 4: 3D chiplets embedded in build-up substrate with hybrid bonding.

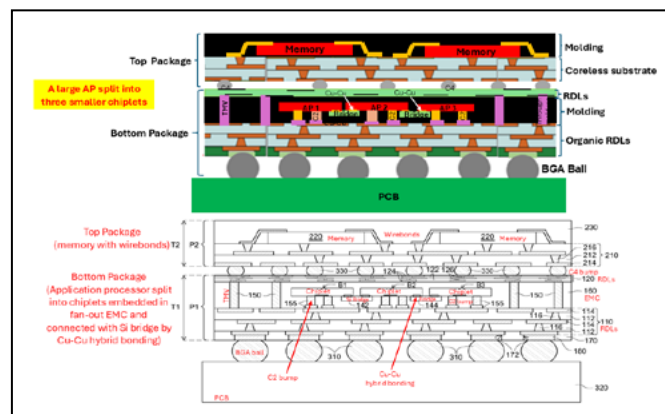


Figure 5: Package-on-package: Chiplets embedded in fan-out (RDL-first) EMC with hybrid bonding.

enhance the performance, silicon bridges are used to connect the high-bandwidth memory (HBM) and the system-on-chip (SoC)—such as the graphic processor unit (GPU)—by HB as shown in **Figure 6**.

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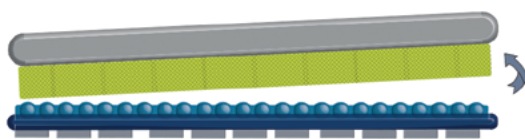
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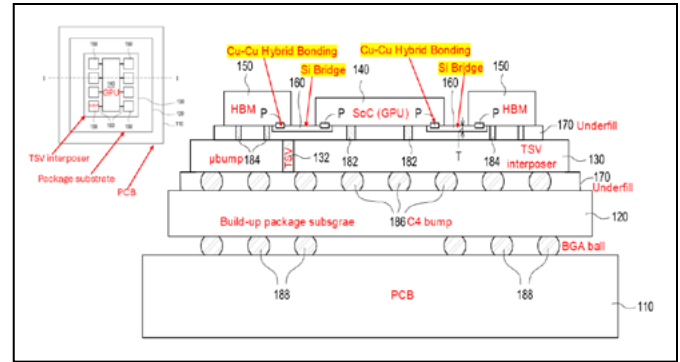


Figure 6: 2.5D IC integration of SoC and HBM with a bridge using hybrid bonding.

3.3D IC integration of cHBMs on top of a SoC on a glass substrate. Figure 7 shows a new 3.3 IC integration structure. It can be seen that the interconnects between the dynamic random access memories (DRAMs) and logic base of the customized HBMs (cHBMs) are Cu-Cu hybrid bonded. The cHBMs are then (Cu-Cu HB) directly attached to the top surface of the SoC. Finally, the SoC with cHBMs are Cu-Cu hybrid bonded directly to the top surface of a glass substrate.

3D HI of PIC and EIC with HB on fan-out RDLs and polymer waveguides. Figure 8 shows a co-packaged optics (CPO) system. It can be seen that the photonic

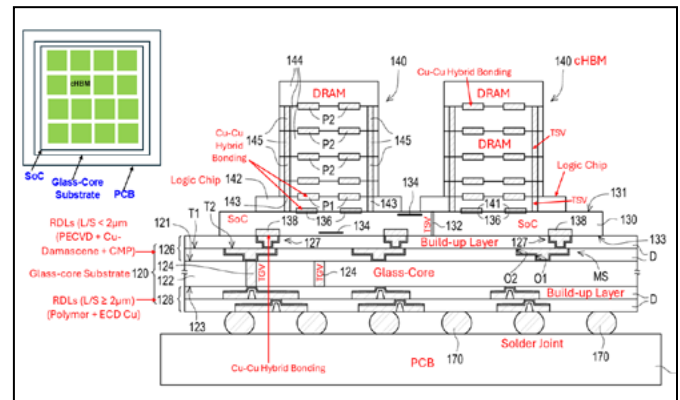


Figure 7: 3.3D IC integration of cHBMs on top of a SoC on a glass substrate.

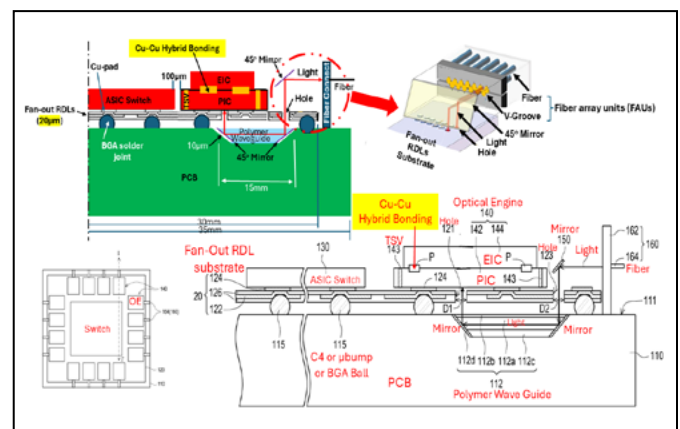


Figure 8: 3D heterogeneous integration of PIC and EIC using hybrid bonding on fan-out RDLs and polymer waveguides.

integrated circuits (PICs) and electronic integrated circuits (EICs) are 3D stacked with HB, and then they are side-by-side with a switch attached to a fan-out RDL CPO substrate with holes. The holes are used for lights to pass through. There are polymer waveguides with 45° mirrors at both of their ends that are semi-embedded in the printed circuit board (PCB). The light from the external fiber through the V-groove hits the 45° physical mirror and then reflects and passes through the hole and hits one end of the 45° mirror of the polymer waveguide. The light travels along the polymer waveguide, hits the other end of the 45° mirror, and then reflects off the PIC. Finally, the photodiode (PD) in the PIC receives the light.

3.5D HI of PIC and EIC with HB on an organic interposer with polymer waveguides. Figure 9 shows another CPO system. It can be seen that the PIC and EIC are stacked using HB, and then they are side-by-side with the switch attached to an organic interposer with an embedded polymer waveguide with 45° mirrors at both ends. There are holes in the organic interposer. The CPO interposer is attached to a build-up package substrate, and then onto a PCB.

3.5D HI of PIC/EIC/switch with Si bridge using HB. Figure 10 shows another CPO system. It can be seen that the optical engines (PIC and EIC) are stacked using HB. In order to enhance the performance, the switch is connected to the PIC with HB. The switch and the optical engines are side-by-side microbumped on a CPO interposer and then onto a package substrate.

3D HI of PIC and EIC with a glass interposer and HB. Figure 11 shows another CPO system with a through-glass via (TGV) interposer. The PIC and EIC are 3D-stacked through a TGV interposer with Cu-Cu HB. The PIC and EIC are side-by-side with the switch microbumped attached to a build-up package substrate. The package substrate is then attached to the PCB. The glass waveguide on the glass interposer receives the light from the external fiber and sends the light to the PD of the PIC. The patent has been granted [18].

3D HI of EIC and PIC using HB with the PIC embedded in a co-

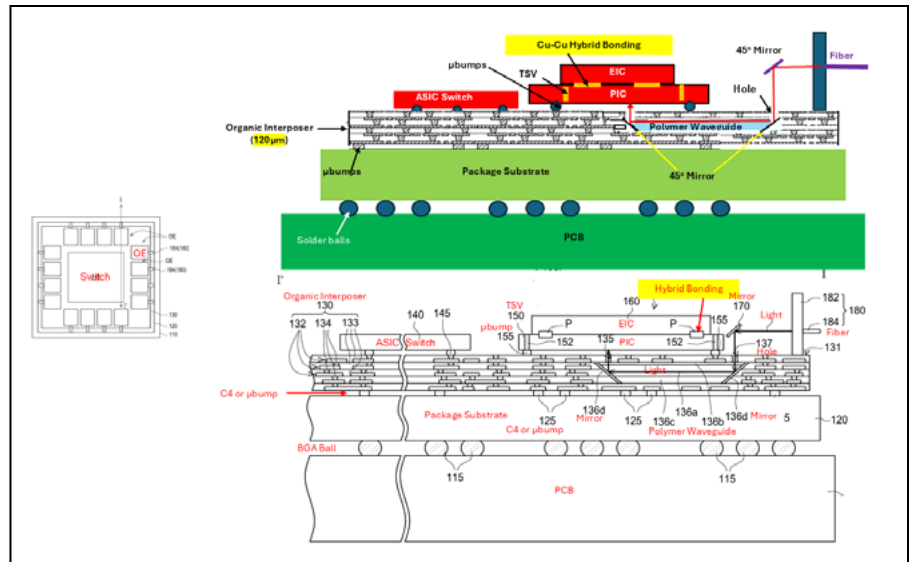


Figure 9: 3.5D heterogeneous integration of PIC and EIC using hybrid bonding on an organic interposer with polymer waveguides.

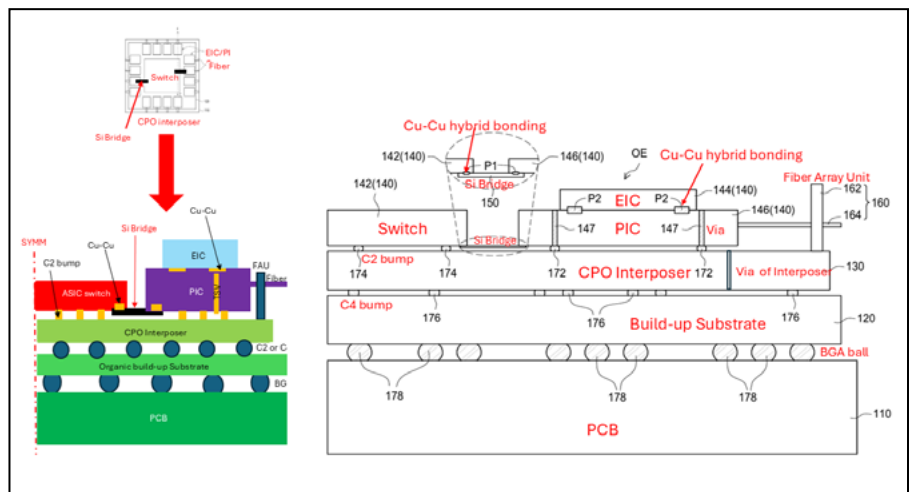


Figure 10: 3.5D heterogeneous integration of PIC and EIC and a switch with a Si bridge using hybrid bonding.

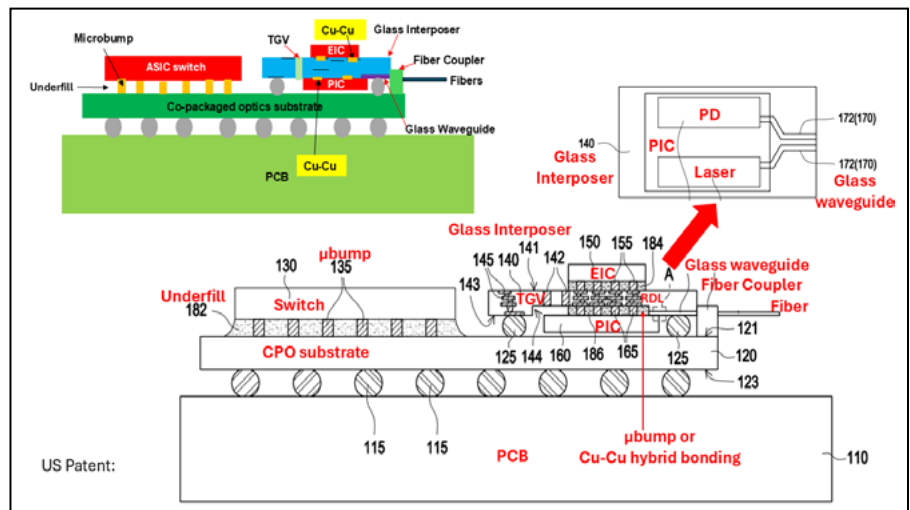


Figure 11: 3D heterogeneous integration of PIC and EIC with a glass interposer using hybrid bonding.

cavity of the substrate. The switch and the PIC/EIC stack are side by side attached to the CPO substrate. Compared to the CPO structure shown in [Figure 11](#), this CPO structure has better performance, but a higher cost.

For the receiver optical subassembly (ROSA) of a CPO with silicon photonics, the light from a fiber coupled to the silicon waveguide confines the light. Then the silicon resonator (with germanium) changes light to an optical signal. Finally, the PD, usually made of germanium and located in the PIC, changes the

For the transmitter optical subassembly (TOSA) of a COP with silicon photonics, the silicon modulator both injects and depletes the electrons and holes (charge carriers) of the electrical signal (voltage) of the switch in the silicon waveguide. While the silicon modulator processes the data, the laser driver of the EIC is the power and control engine for the light source itself. It provides a stable power supply and signal amplification before the light is shot out from the laser (usually made of InP) of the PIC to the fiber.

Thermal management of 2.5D IC integration with microchannels and Cu-Cu HB. **Figure 15** shows a thermal management scheme for a 2.5D IC integration with microchannels and Cu-Cu HB. It can be seen that the chiplets and the TSV interposer are etched with microchannels, and are dielectric-to-dielectric and metal-to-metal hybrid bonded together. The thermal performance of this case is better than that of **Figure 14**, but with a higher cost.

Some important results and recommendations are summarized as follows:

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[illegible]Chip Scale Review • Quarter 3 • 2026 [\[ChipScaleReview.com\]](https://ChipScaleReview.com) 37

- HB is an old flip-chip assembly technology that has been in HVM since 2016. Some examples of HB in older flip-chip assembly technology include: The CIS for smartphones by Sony, Samsung, etc.; and for automobiles by OMNIVISION, etc.; memory-on-logic and logic-on I/O for HPC by Jasminer, Samsung, AMD, Graphcore, Broadcom, NVIDIA (second half of 2026), Intel (second half of 2026), etc.; HBM by Samsung (2026 or 2027), SK Hynix (2026 or 2027), Micron (2027), etc.; GPU-bridge-CPU for notebooks by Apple, to 3D NAND flash by YMTC, and Kioxia-Western Digital, Samsung (to be shipped in Q4 2026), SK Hynix (to be shipped in early 2027), Apple iPhones (to be shipped in September 2026 in the China market), etc.
- Thirteen new applications with hybrid bonding have been proposed.
- In order to enhance performance and reduce package size, 3.5D IC integration with HB is strongly recommended.
- As of today, there are not many articles published on the quality and reliability (e.g., thermal cycling, thermal shock, mechanical vibration, mechanical shock, high-temperature storage, highly accelerated temperature, and highly-accelerated moisture resistance) of Cu–Cu HB. For HB to be more popular, these quality and reliability data are desperately needed.
- Thermal management of Cu–Cu HB (stacking chips) will be an important topic.
- We would like to know the answers to the following questions: 1) What is the effect of Cu–Cu bonding misalignment on the quality and reliability of Cu–Cu HB interconnect? and 2) What is the effect of bonding interface voids (size, location, and propagation) on the quality and reliability of a Cu–Cu HB interconnect?

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Biography

John H. Lau is a Senior Special Project Assistant at Unimicron Technology Corporation, Taoyuan City, Taiwan (ROC). He has more than 40 years of R&D and manufacturing experience in semiconductor packaging, 532 peer-reviewed papers (a principal investigator on 383), 52 issued and pending U.S. patents (a principal inventor on 36), and 25 textbooks. He is an ASME Fellow, IEEE Fellow, and IMAPS Fellow. He earned a PhD degree from the U. of Illinois at Urbana-Champaign. Email John_Lau@unimicron.com

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Through-glass via (TGV) etch comes to maturity for glass-core applications

By Venugopal Govindarajulu, Zia Karim [*Yield Engineering Systems*]

Through-glass vias (TGVs) play an important and critical role in advanced heterogeneous wafer packaging. These vertical electrical interconnections in 2.5D/3D packaging offer superior high-frequency integrity, excellent thermal stability, and low electrical/signal loss for high-performance computing (HPC) and artificial intelligence (AI) accelerators. Compared to silicon, glass offers distinct advantages—especially for radio frequency (RF) applications, and optical devices, where coefficient of thermal expansion (CTE) requirements are stringent. Panel-level TGVs require massive equipment for high-volume manufacturing (HVM) enablement up to 600 x 600mm panel sizes. TGVs require stringent processing to overcome micro cracks, voids, and critical dimension variations in a brittle glass substrate. For typical hour-glass type TGVs, the waist diameter (or the taper angle) is a critical specification that needs to be met as close as possible.

A wide choice of glass types that can meet the critical CTE requirements are available—therefore, it is important to understand the glass types and their effective chemistry for successful TGV formation. The laser plays a key role in defining the via shape, diameter and the taper angle (waist). To achieve a successful TGV, a clear understanding of the laser and the wet chemistry is required.

In this article, we discuss the role of wet etching chemistry by glass type, correlation to the waist diameter, hole opening uniformity, as well as critical dimension distribution vs. laser/chemistry. Typically, we used 510 x 515mm full panels for the process development as well as coupons for initial studies. Blanket coupons were used to do the etch rate studies, followed by laser samples for TGV formation studies.

Introduction

A detailed etch rate study with acidic and alkaline chemistries formed the basis of experiments on two widely-used

glass types (BF33 and EXG or SG). A range of temperatures were also studied to optimize the throughput, as well as the quality of the TGV formation. The acidic chemistry typically used with additives has a low temperature range, while the alkaline chemistry needs a higher temperature range to achieve reasonable etch rates. The concentration of the chemistry was also studied to optimize the etching performance. Bare glasses were used for etch rate studies, and laser-modified glasses were used for waist and via study experiments.

Glass-core processing challenges

Because of the increase in package sizes, high-frequency signal processing and mechanical strength and warpage issues, glass-core processing is getting very popular. These conditions were described in [1]. However, glass-core processing has been faced with many challenges that could probably become showstoppers to the implementation of glass-core substrates in advanced packaging for AI and HPC applications. These challenges were described in [1]. The challenges as

shown in **Figure 1** range from etching, annealing or curing, and metallization of redistribution layer (RDL) formation with Ajinomoto build-up film (ABF)/Cu warpage, created by asymmetric layers, as well as edge stress issues due to dicing and singulation [1].

Glass core processing, however, faces cracking and delamination issues for different sources of stress—either caused by glass/Cu CTE mismatch, or as a result of stress development from multilayer RDL, thermal cycling during processing, as well as defect formation from panel dicing. However, as indicated in **Figure 1**, TGV etch with good co-planarity, minimum CD variation, required waist, and consistent repeatability remained challenging due to aspect ratio, glass composition to get higher CTE, and laser modification types. This article will focus on such development and maturity using etch process development in conjunction with pre-processing (laser modification and clean), or post-processing (adhesion promotion layers, stress buffer layers, or metallization).

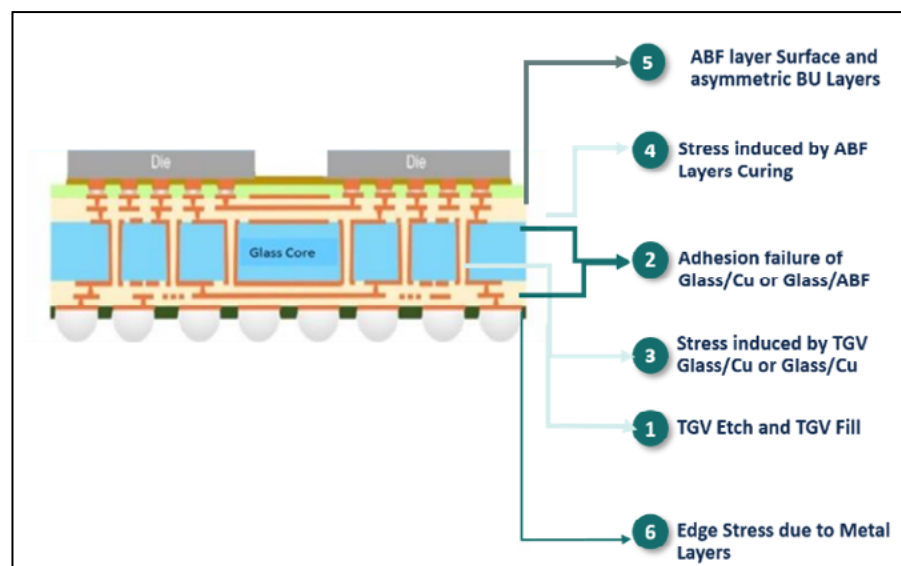


Figure 1: Glass-core processing challenges and showstoppers.

Experimental

The following sections discuss various aspects of the experimental process that we used.

Glass etch rate and waist DOE study. A detailed design of experiment (DOE) was performed to determine the highest waist opening per glass type. EXG glass needed acidic etching with low temperatures, which exhibited a low concentration. Additionally, low temperature is necessary

for a higher waist opening. This process pragmatically leads to a low-throughput issue. On the other hand, BF33 and OA11 glass types work well with alkaline chemistry in all temperature ranges, but at a higher chemical concentration. Both acidic chemistries and alkaline chemistries are developed using a mixture of available chemistries to get the best results for a particular glass type. **Figures 2a** and **b** show the etch rate by temperature and concentration.

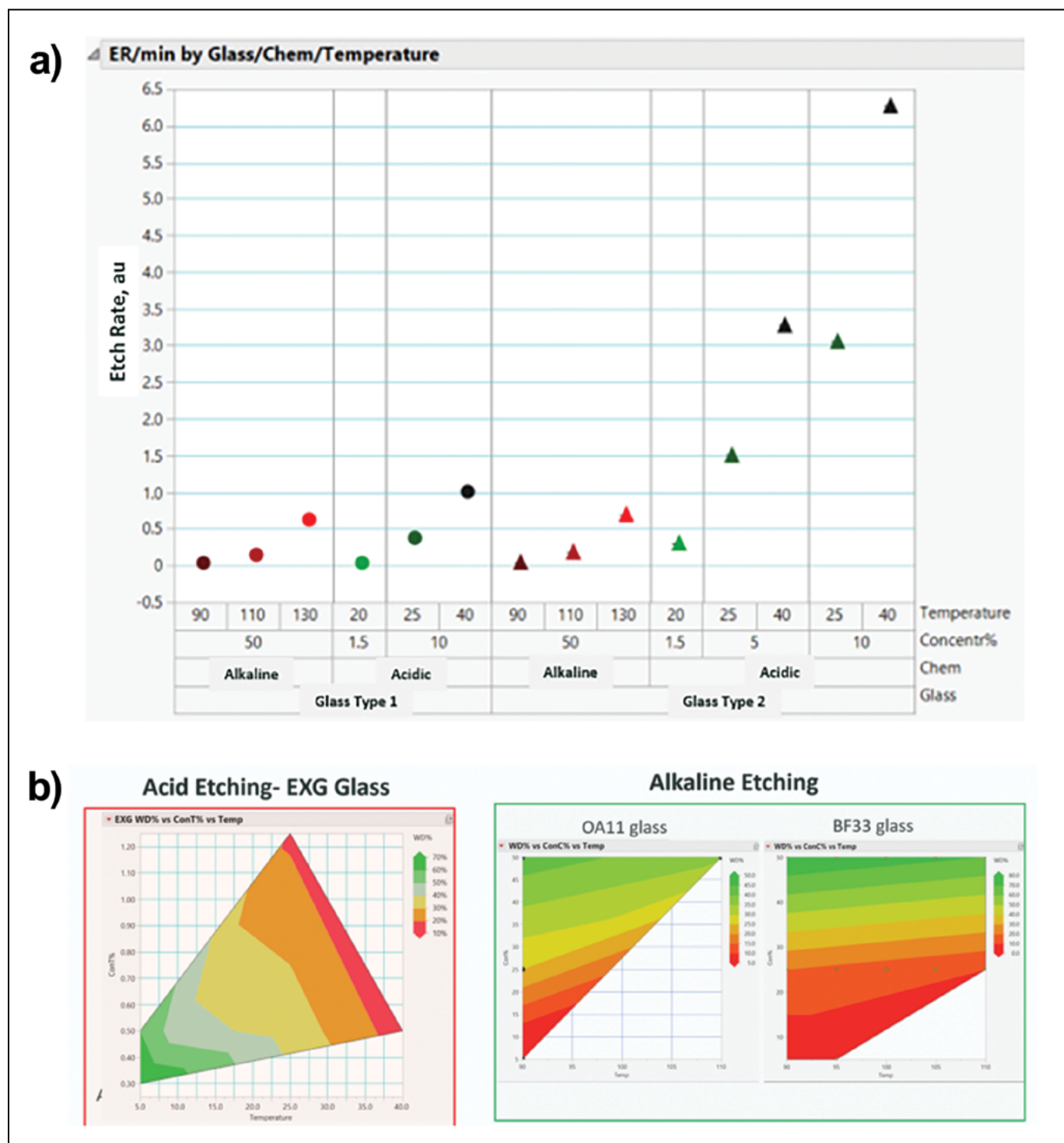


Figure 2: Etch rate studies: a) By glass type, chemistry and process conditions; and b) By glass type and chemistry.

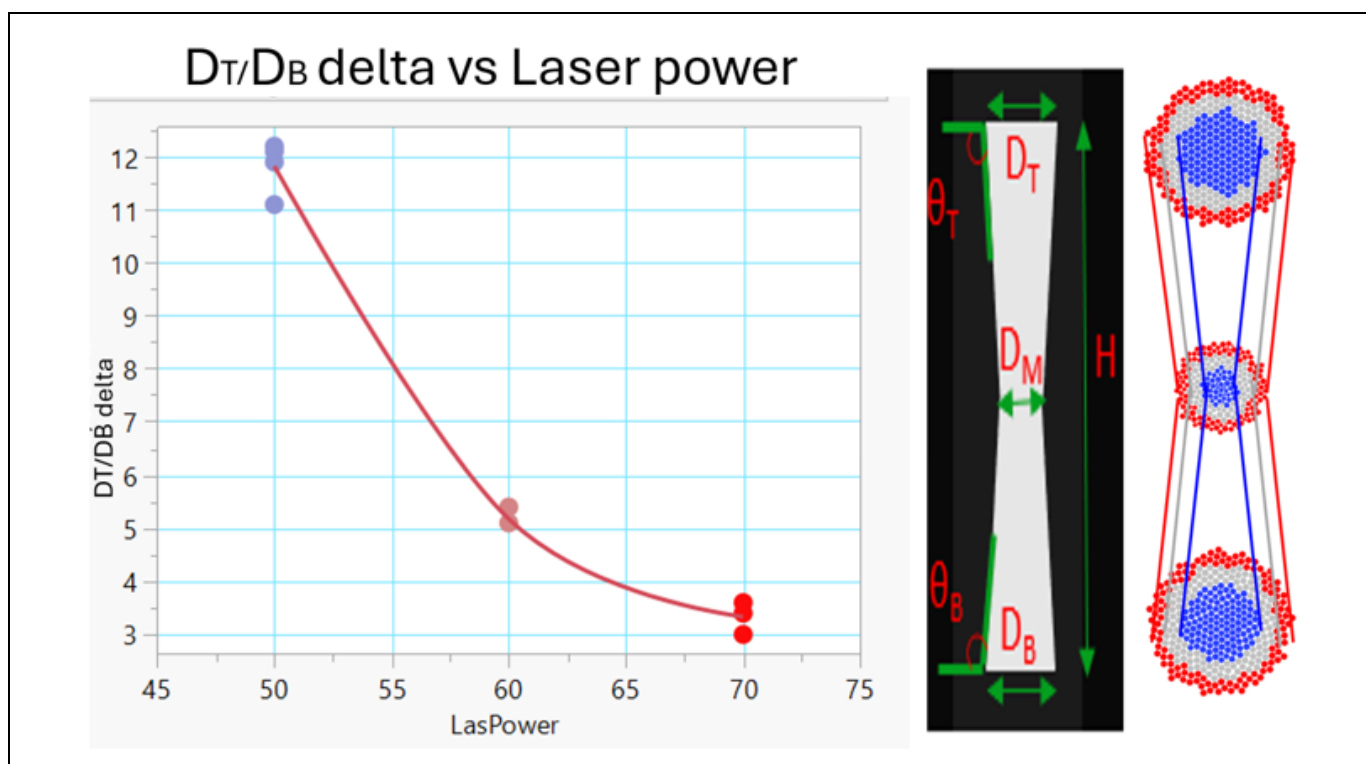


Figure 3: Top/bottom via delta vs. laser power trend.

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Top/bottom via variation study.

A laser power DOE was performed to optimize the top and bottom via diameter delta. A typical customer requirement is <5% variation in the via diameter on the top and bottom sides of the glass. A 40µm via hole used for experimental purposes in a 250µm-thick glass resulted in an aspect ratio >6. The top vs. bottom diameter via delta has a direct correlation to laser power as shown in **Figure 3**—the lower power results in a higher via delta. A cross-sectional scanning electron microscope (X-SEM) image of a sample also confirmed the delta as shown in **Figure 4a** for an acidic process. The via was clearly formed without any residue. Optical inspection (OM) mostly correlated with X-SEM results. Similar studies were performed for alkaline-based process showing a >90% waist as compared to the top opening and a >90% circularity in **Figure 4b** with no residue for the TGV process.

Laser vs. aspect ratio vs. temperature DOE. A detailed waist diameter DOE was performed on samples from two laser vendors using different values of aspect ratio (AR) for the glass etching process. AR

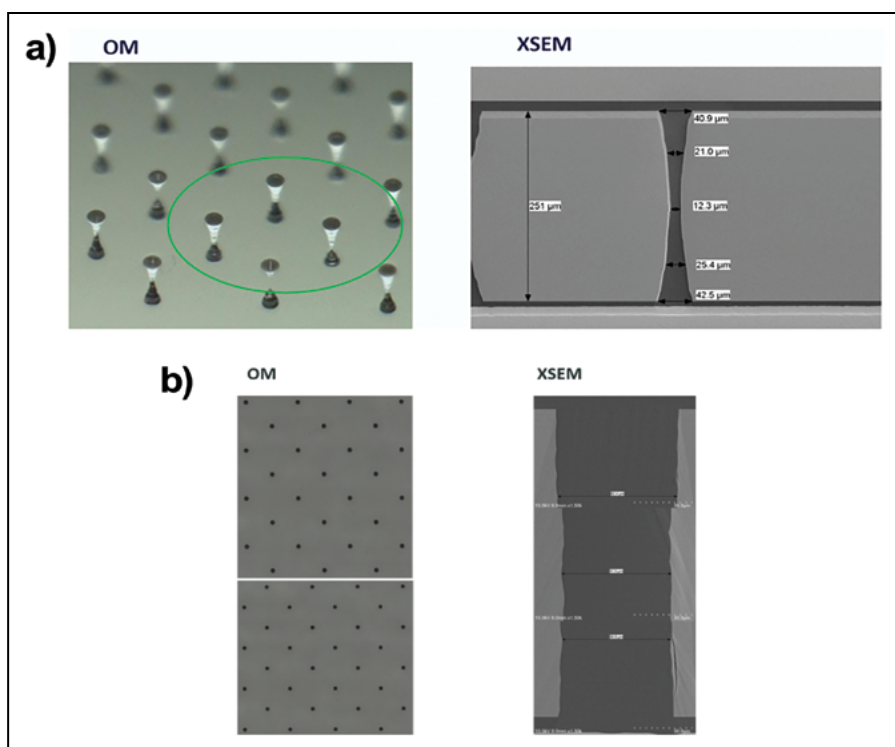


Figure 4: a) Acidic process TGV etch with good coplanarity and via profile; and b) Alkaline process TGV etch with good coplanarity and via profile.

values ranging from 10:1, 15:1, and 20:1 were used to measure the impact on the waist opening with respect to the process chemistry temperature. Alkaline chemistry used with BF33 glass at 90, 110 and 130°C showed a clear correlation between AR and operating temperature. The laser-to-laser difference was not significant, but it also demonstrates that laser optimization is critical to achieve a good waist opening to achieve a good top-to-bottom via delta shown in **Figure 3**. As shown in **Figure 5**, the lower aspect ratio with the lowest temperature resulted in the highest waist opening. This result was perfectly aligned with the etching model based on the thickness of the glass, via diameter and etchant temperature, etc.

Glass type vs. etchant. There are multiple glass types available from key glass manufacturers as shown in **Table 1**. The most commonly-used glass types were selected for laser+etch experiments. A library of glass type vs. optimized etchant was developed

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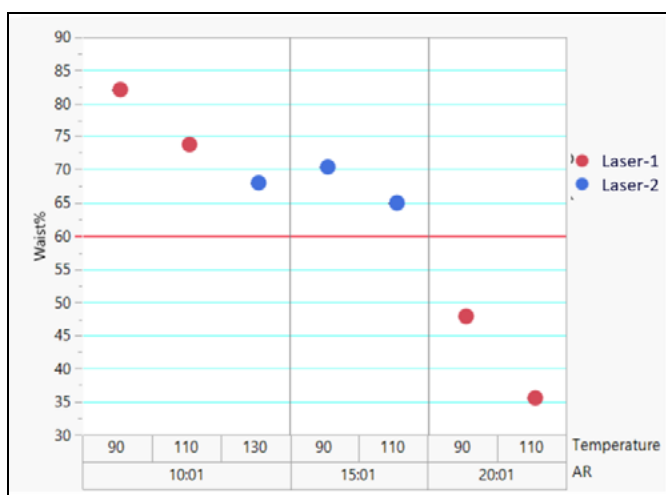


Figure 5: Waist opening trend by AR and temperature of the etchant.

Glass Types	Schott BF33	Schott D263	AGC EN1	Corning SG 3.3, 3.4 and 3.7	NEG OA-11	Corning EKG
CTE (20°-300°C) @ 10 ⁻⁶ /K	3.25	7.2	3.8	3.4-3.7	3.7	7.3
Etchant	Alkaline	Alkaline and Various	Alkaline	Acidic with additives	Alkaline	Acidic with additives
Post-etch Clean	Acidic clean	Acidic clean	Acidic clean	None	Acidic clean	None
TGV AR	4:1 -> 20:1 200um to 5 um via	>10:1	4:1 -> 20:1 200um to 20um via	>10:1	>10:1	4:1 -> 10:1 Typical 50um
Taper Angle	~1.2° Various including straight	Various	~2°	As low as 2.6° Various waist%		Various

Table 1: Glass types available from key glass manufacturers.

for our customers to have the capability to select the right glass type to meet their development needs. More detailed information can be shared based on a specific request.

Results and discussion

Detailed studies of glass types, etching rates with various chemistries, as well as two different laser vendors have been performed. The TGV via hole performance with respect to etchant type vs. glass type vs. laser vs. etchant temperature was established. A library of glass types and their performance has been established for our customers' reference and choice.

Summary

Since the publication of the etch process described in 2024 [2], chemistry development of alkaline and acidic types were made and experiments were devised that resulted in mature TGV etch processes on different types of glass with varying CTEs. These chemistries produce results regardless of glass types, as well as laser modification types. Consistent and repeatable etch processes with varying aspect ratios, waist requirements, and good CD variations were achieved. As a result, a data base has been established so that a matured process is produced to address glass-core substrate usage for HPC and AI applications.

Acknowledgments

We acknowledge the technical support from our YES Technology Center (YATC) at Chandler, AZ—especially Jeffrey Vu, Coby Tao, and Eric Nguyen. We also thank the laser modification suppliers for providing the laser conditions to correlate to the etch process. Acknowledgment also goes to various glass suppliers for providing different glass types of varying CTEs.

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Biographies

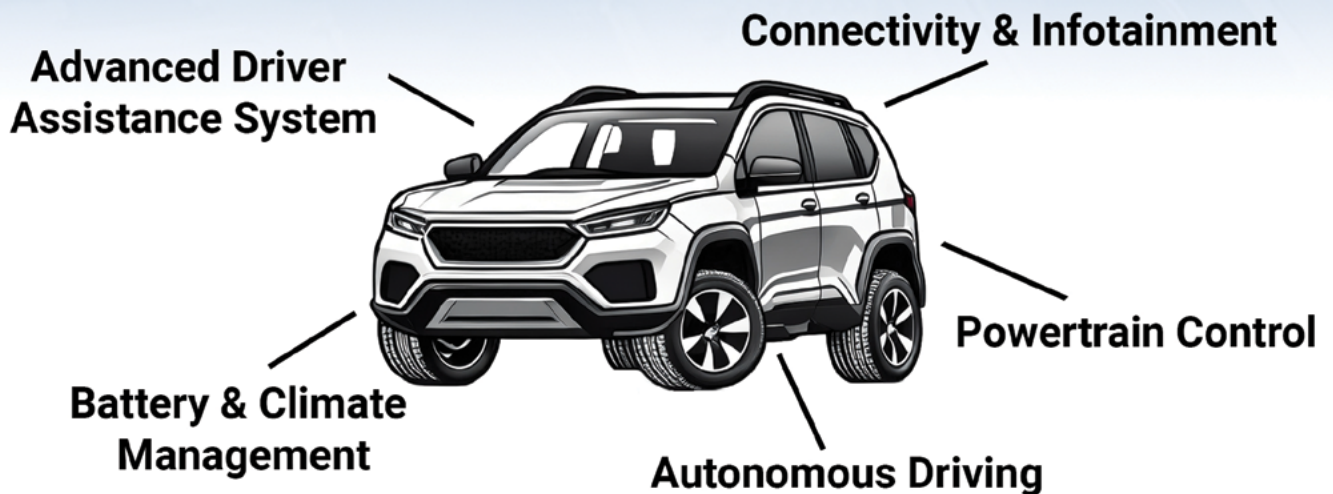
Venugopal Govindarajulu is Sr. Director of Technology at Yield Engineering Systems (YES), Chandler, AZ, responsible for wet process development for glass-core substrates. Prior to YES, he worked in Micron Utah and Global Foundries NY and Singapore for over 24 years. He has a Bachelor in Engineering degree from Bharathiar University, and a Master of Engineering from PSG College of Technology, Coimbatore, India. Email: vgovindarajulu@yes.tech

Zia Karim is CTO at Yield Engineering Systems (YES), Fremont, CA, since 2018. Before joining YES, Dr. Karim worked as VP of Business Development and Technology at AIXTRON/Genus for 15 years. He also held senior management positions at Applied Materials and Lam Research. He received his PhD in EE from Dublin City University, and BSc/MSc/Eng degrees from Bangladesh University of Eng and Tech. (BUET).



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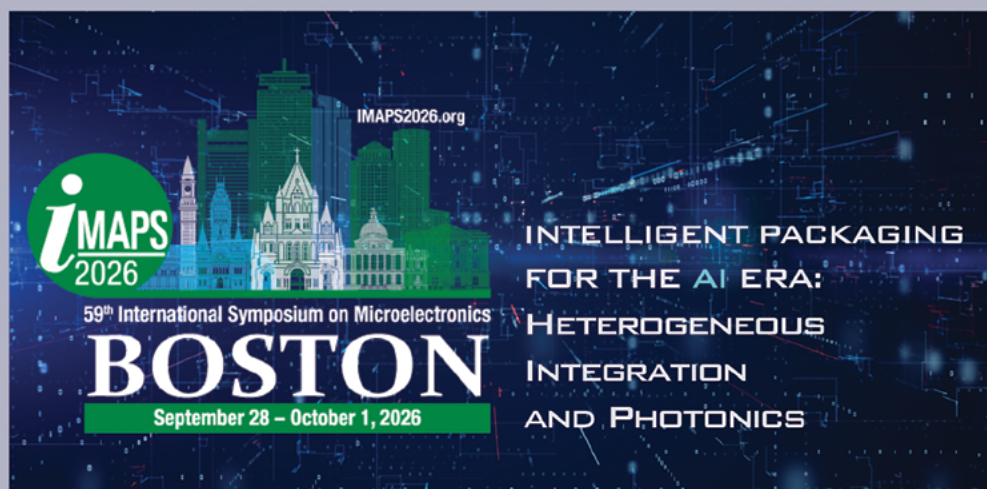
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IMAPS Symposium 2026: The premier event for microelectronics advanced packaging

By Karthik Dhandipandi [*Cerebras Systems; General Chair IMAPS 59th International Symposium on Microelectronics*]

On September 2–October 1, 2026, the 59th International Symposium on Microelectronics (IMAPS Symposium 2026) will bring together the world's leading experts, innovators, researchers, and industry professionals for one of the most comprehensive technical conferences dedicated to microelectronics and advanced packaging.

Centered on the theme, “Intelligent packaging for the AI era: Heterogeneous integration and photonics,” the symposium will showcase the technologies, materials, processes, and innovations driving the next generation of electronic systems. As artificial intelligence (AI), high-performance computing, advanced semiconductor packaging, and photonics continue to transform the industry, IMAPS Symposium 2026 will serve as the premier forum for knowledge exchange, collaboration, and professional development.

The event begins on Monday, September 28 with Professional Development Courses designed to provide attendees with practical, expert-led training on key industry topics. Monday afternoon features a panel: “Next generation measurement technique for domestic manufacturing: NIST and industry perspectives.” For high school students and parents, there will be a student-industry suite of sessions to introduce them to the microelectronics industry.

The 3-day technical conference program runs September 29–October 1 and features five technical tracks: 1) Distinguished keynote speakers (Qualcomm, Cerebras Systems, and Marvell Technology); 2) Expert panel discussions; 3) Technical paper presentations; 4) A poster

session; and 5) Extensive networking opportunities. The panel sessions will examine: “Hybrid bonding for Heterogeneous Integration” and “Packaging Challenges in the AI Era: Substrates and interposers shortages.”

In parallel with the conference, attendees can explore a dynamic, sold-out Exhibition Hall (September 29–30) featuring companies from across the microelectronics and advanced packaging supply chain. Exhibitors will showcase the latest products, equipment, materials, technologies, and services that are shaping the future of the industry.

Whether attending to advance technical expertise, discover emerging technologies, connect with industry leaders, or explore new business opportunities, participants will find IMAPS Symposium 2026 to be an essential event for staying at the forefront of microelectronics packaging innovation.

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35th SWTest Conference and EXPO: Sold out and new record attendance!

By Jerry Broz, PhD [General Chair, SWTest US and SWTest Asia Conferences, and VP at Delphon Industries]

The Semiconductor Wafer Test (SWTest) Conference and EXPO is the only premier annual technical event exclusively focused on the complex challenges and infrastructure behind wafer-level test and probe technologies. Marking its 35th anniversary, the 2026 conference convened from June 8-10 in Carlsbad, California. The milestone event was a sold-out success—drawing the highest attendance at the U.S.-based SWTest Conference and EXPO in its history.

This year's two-and-a-half-day conference brought together 778 international attendees from 18 countries for an exceptional and topical technical program. Some highlights included an Industry Vision Keynote, eight themed podium sessions ranging from photonics, to automotive challenges, to artificial intelligence (AI) applications for probe that featured 30 peer-reviewed presentations, and two sessions of 6 technical poster presentations. Alongside the technical program, the sold-out EXPO hosted 70 of the leading global suppliers for wafer-level test and infrastructure. With almost 50% of technologists, attendees and participants traveling from Asia, Europe, and the Pacific Rim, the 35th SWTest Conference was truly a multinational gathering of probe professionals to share knowledge, collaborate, and network within an intentionally casual, friendly environment.

Monday's plenary session kicked off with an inspiring Industry Vision Keynote from Dr. Radha Nagarajan, who is the Senior Vice President and Chief Technology Officer of Marvell Technology's Optical Engineering Group, where he manages the development of the company's optical platform products and technology. Speaking on "Connectivity scalability: Architecting the invisible backbone of the AI data center," Dr. Nagarajan detailed how explosive AI growth is driving unprecedented demand

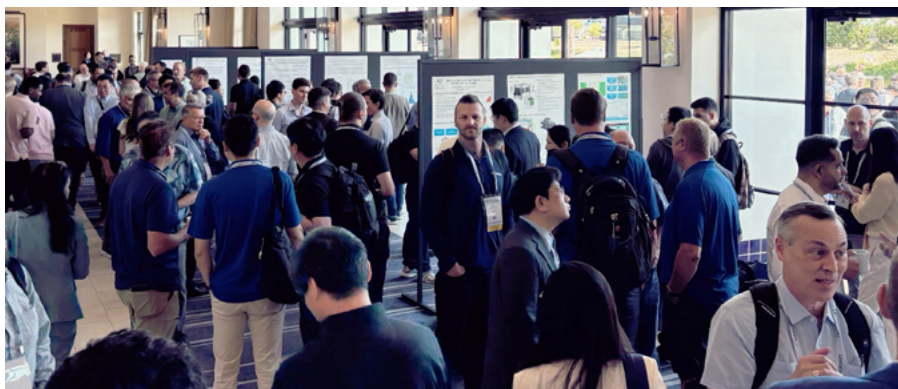
for semiconductor infrastructure, forcing tech giants to rethink various resource and power requirements of next-generation data centers. To overcome physical and energetic limitations, the industry is transitioning to complex, integrated hardware like silicon photonics and advanced 2.5D packaging. However, he emphasized that the viability of these systems hinges on a critical manufacturing reality: Overcoming high-bandwidth testing challenges through strict known-good die (KGD) and known-good optical (KGO) validation.

Over two-and-a-half days, the technical sessions focused on the key challenges facing probe technologists in research labs, low-volume settings, and high-volume testing environments. From this year's outstanding technical program, the Technical Program Committee identified the top presentations, as follows:

- **Best overall presentation.** Awarded to Saad Ahmed, Hamed Barghi, Karthik Subramanian, Thakshila Wickramaratne (Intel Foundry-US), and Jeremy Streifer, Ethan Caughey



During his Monday Industry Vision Keynote, Dr. Radha Nagarajan, Senior Vice President and Chief Technology Officer of Marvell Technology's Optical Engineering Group, discussed the critical shift of transitioning to silicon photonics and co-packaged optics for the modern datacenter. Advanced manufacturing techniques like 2.5D integration and fan-out wafer-level packaging are essential for creating the high-performance light engines required.



Showcasing 10 outstanding presentations from industry professionals, the SWTest 2026 poster sessions provided a dynamic environment for networking, collaboration, and meaningful connections among technologists, colleagues, and key suppliers.



With non-competing schedules, the technical program and EXPO gave attendees substantial time to engage with colleagues, customers, and suppliers during the extended breaks, daily meals, and evening social receptions.

- (FormFactor-US) for: “Micro bump probing: High-volume experience-driven capability demonstration and direction for advanced 3D/2.5D packaging.”
- **Best data presentation.** Awarded to the collaborative team of Francesco Casartelli, Raffaele Vallauri (Technoprobe-Italy) and Johann Heitzer, Oliver Nagler (Infineon Technologies-Germany) for their work on: “A new 300mm vertical probing solution enabling automotive microcontroller high-volume manufacturing and test.”

The Technical Program Committee also recognized several other outstanding contributions presented during the technical program:

- **Best presentation, tutorial in nature (tie).**
 - Kelvin Lo (Google-Taiwan) for: “Integer linear programming optimization for wafer sort touchdown reduction and mechanical risk mitigation;” and
 - Emmett Ricks (Micron-USA) for: “Benefits and challenges of high-temperature probe.”
- **Most inspirational presentation:** Monica Davis, Ethan Dwyer, Lakshmi-Anusha Condon (Teradyne, Inc.-USA), Alessia Galli (Technoprobe SpA-Italy) and Amit Agnihotri, Andy Chang (Marvell-

USA) for: “Achieving high-volume test for silicon photonic devices with a fully-integrated and automated solution.”

- **Best poster presentation.** Ai Heong Tan, Jiawei Lin, Tim Jin (Nexustest Pte Ltd-Singapore) for their work: “Enabling die-level KGD testing for CPO optical engine.”
- **“People’s Choice:”** Enrico Zschemisch and Kris Hublitz (Marvell-USA) for: “Marvell ATE test cell digital thermal feedback loop architecture & implementation” (voted in real-time by attendees via the mobile app).

The SWTest Program Committee is excited to announce that our long-time media partner, *Chip Scale Review*, will select at least one presentation from the 2026 program for publication as a featured full-length article in an upcoming issue.

On Tuesday, the impactful SWT-Crew mentoring initiative, as chaired by Karen Armendariz (Celadon), had record participation during their mentor-mentee matching event. SWTest is extremely proud to support this excellent program dedicated to career development by pairing women technologists with seasoned industry professionals. SWTest also promotes and supports student participation through the William Mann Student Travel Grant Program, which relies on vital funding raised during the annual charity golf tournament.

On Monday and Tuesday evenings, the SWTest EXPO floor had the “35th Anniversary Energy” as attendees networked, socialized, and connected with peers, suppliers, and customers. We welcomed many first-time participating multinational companies. A unique benefit of SWTest is that the EXPO and technical sessions never compete, allowing attendees to get the full value of both programs. This year’s sold-out exhibition featured 70 booths made up of the 30 Platinum, Gold, and Silver sponsors, and 40 exhibitors from the wafer probe and test communities.



Saad Ahmed (Intel Foundry-USA) and Jeremy Streifer (FormFactor-USA) received the Best Overall Presentation Award from Jerry Broz (SWTest General Chair) for “Micro bump probing: High-volume experience driven capability demonstration and direction for advanced 3D/2.5D packaging.”



Francesco Casartelli (Technoprobe SpA-Italy) and Johann Heitzer (Infineon Technologies AG-Germany) received the Best Data Presentation Award from Jerry Broz (SWTest General Chair) for “A new 300mm vertical probing solution enabling automotive microcontroller high-volume manufacturing and test.”

As the General Chair, I am pleased that our conference and EXPO continue to offer a diverse range of current and meaningful technical content combined with professional interactions. Throughout our event schedule, attendees are provided with substantial opportunities to engage and network



SWTest Technical Program and Steering Committee (L to R): Clark Liu (Taiwan Program Chair/TWMJC), Kenny Tang (TSMC), Geert Gouwy (imec), Mark Ojeda (consultant), Raffaele Vallauri (Technoprobe), Rey Rincon (Operations Chair), Jerry Broz (General Chair/Delphon Industries), Patrick Mui (JEM America/Program Chair), Karan Maniar (AEM), NyiNyi Thein (SanDisk), Alistair Laing (Micron), Matthais Schnaithmann (Feinmetall), Matt Zeman (FormFactor), and Joey Wu (Toward Technologies).
Not pictured: Davide Appello (Technoprobe), Karen Armendariz (Celadon), John Caldwell (MEC), Nobuhiro Kawamata (Japan Program Chair/FormFactor KK), BC Kim (Samsung), JY Kim (TSE), and Andrew Yick (Marvell Technology).

during extended breaks, daily meals, and evening social functions. I would like to take this opportunity to extend my sincere thanks to the sponsors, exhibitors, authors, speakers, session chairs, committee, and SWTest team members whose deep commitment made this a truly fantastic and record-setting milestone event.

Looking ahead, mark your calendars for the upcoming 7th SWTest Asia Conference and EXPO, which will be held from November 4-6, 2026, at the Hsinchu Sheraton. Abstract submission and registration are now open at <https://www.swtestasia.org/>, with discounted early-bird rates available until September 25, 2026. We invite you to participate in this Asia-centric probe technology forum to explore the latest industry advancements and network with global peers. The event is expected to showcase up to 55 prominent international suppliers from the probe and wafer test community.

Whether in San Diego or Asia, the SWTest Conference and EXPO provide invaluable opportunities for all wafer-level testing professionals from end users and suppliers, to engineers, and sales and marketing teams.





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2026 IEEE ECTC: Third consecutive record attendance shows advanced packaging is the enabler for HPC, AI, and more

By Michael Mayer (Associate Professor, University of Waterloo; General Chair 76th ECTC)

The 76th IEEE Electronic Components and Technology Conference (ECTC)—the premier international event for semiconductor packaging, components, and microelectronic systems—was held May 26-29 at the JW Marriott & The Ritz-Carlton Grande Lakes Resort, Orlando, Florida. It set a new attendance record of 2,730, unexpectedly surpassing last year's fabulous record of 2,518.

Here are some key ECTC 2026 program metrics:

- A record number of abstracts submitted: 918; with a record number of accepted papers: 419 presented in 36 oral and 5 interactive presentation sessions, including one dedicated to students. Highlights of the event and some of the noteworthy technical papers can be found at <https://ectc.net/press>. An archive of all the technical papers can be found at <https://ieeexplore.ieee.org/>.
- A series of 16 CEU-approved professional development courses were attended by a record 714 participants.
- There was also a record level of industry support, with 52 corporate sponsors and 136 booths in the sold-out exhibit hall.

A place to network

The world's leading industry players and top university researchers in semiconductor packaging and component technology came together to network with conference committee members, panelists, exhibitors, presenters and/or attendees. (See ECTC's flickr page for photos.) There were student engagement and competition programs, as well as a start-up competition designed to identify innovative ideas in photonics.

The ECTC 2026 technical program featured many of the critical technology advancements required for the advancement of artificial intelligence (AI) and high-performance computing (HPC), including advanced packaging technologies such as heterogeneous integration, hybrid bonding, co-packaged photonics, interposers, advanced substrates, wafer-level and fan-out packaging, 2.5D, 3D architectures, materials modeling, reliability, interconnections, and packaging for high-speed and high-bandwidth applications.

Program highlights

ECTC Keynote by Dr. Tien Wu, CEO of ASE. Dr. Wu's presentation was entitled: "Advanced Packaging & the Future of System Optimization." His keynote emphasized the transformative role of advanced packaging in system optimization as the semiconductor industry entered an AI-driven paradigm

shift. He explained that AI changes how information, patterns, applications, and industries evolve, while hardware has become the new bottleneck, and therefore, a central source of value and responsibility. Tien traced packaging from lead frames and ball grid arrays (BGAs) to chiplets, CoWoS®, heterogeneous integration, and wafer- or panel-level approaches, showing that packaging is now system-critical for power delivery, thermal management, bandwidth, photonics, reliability, and cost. He argued that the industry needs to look beyond the data center race and prepare for bifurcated roadmaps that also support high-volume, high-impact applications such as humanoids, edge AI, and implantable medical devices. Tien stressed that scalable solutions required density, performance, reliability, cost control, and ease of use together—not technology advancement alone. He also highlighted rising costs, capacity shortages, consolidation, and the need



76th ECTC Keynote by Tien Wu, PhD, CEO of ASE.

for collaboration across companies, regions, academia, consortia, and professional communities such as ECTC. His central message was that hardware and packaging engineers have become gatekeepers of progress, so the community needs to think long

term, collaborate broadly, and prepare for multiple roadmaps. His advice for students and young professionals is to choose meaningful work that contributes to the next major wave of technology.

Special sessions. In addition to the keynote talk, a series of special sessions

were presented during which panels of industry experts discussed technology status and roadmaps in these key areas:

- Quantum infrastructure for AI applications: Packaging challenges and roadmap;
- New packaging technologies enabled by panel-level integration;
- AI-enabled electronic design automation for multi-physics advanced packaging;
- Photonics-based systems for AI and exascale computing;
- System integration challenges of large-size and high-power components for high-performance computing and AI applications;
- Electrical-thermal-mechanical co-design in high-performance packaging;
- Enabling next-generation advanced packaging technology from wafer to panel;
- Innovative materials for advanced packaging: Materials for packaging, integration, and performance;
- 2026 IEEE EPS Seminar: “Redefining System Integration – The Rise of Organic Substrates in the Chiplet Era;”



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All technical sessions were extremely well attended.

- 2026 ECTC Plenary Session: “Efficiency Is Not Enough – Are We Solving the Wrong Problem in the Data Center Energy Use?” and
- 2026 IEEE EPS President’s Panel: “Data Centers in the Age of AI – Challenges and Solutions.”

Student engagement. Six finalist student teams competed in two categories for the opportunity to receive financial assistance to attend next year’s ECTC. Bachelors and Masters students submitted papers on the topic: ‘Low-cost Robust Thermal Solution for High Power AI/Datacenter Processor.’ The winning presentation was by Hiroyuki Sakuma, Dennis Y. Gao, and Lok Teng Cheung, from Georgia Institute of Technology.

PhD students competed in two topics: 1) “Materials, Interfaces, & Processes for Ultra-Scalable Interconnects;” and 2) “Electromigration Solutions for BGA Interconnects in AI-Focused Packages.” The winning presentation was by Li Ying and Sihang Shao, from Nanyang Technological University.

Other engagement opportunities included a student reception on Tuesday hosted by Texas Instruments where students had the opportunity to network and explore career options with industry professionals. A Young Professionals networking reception with senior members of the IEEE Electronics Packaging Society was also held.

Startup competition. Start-up companies pitched their innovative

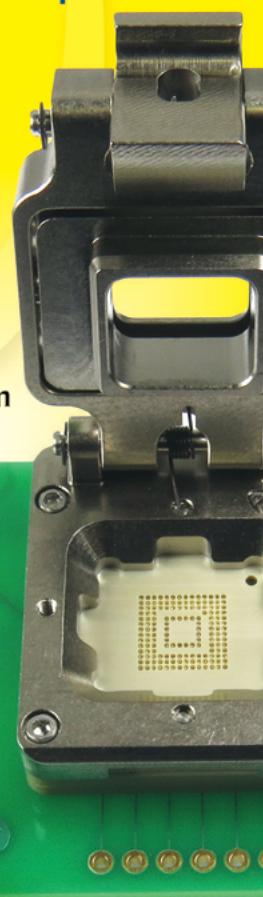
ideas to a panel under the theme: “The Light Age: Strategic Investment in Photonics to Power the Next Computing Era,” which was followed by audience Q&A, jury deliberation, and a networking event. The winning team was from NSC Innovation.

Heterogeneous integration roadmap (HIR) workshop. ECTC 2026 also featured a heterogeneous integration roadmap (HIR) workshop with four focused discussions: 1) Additive electronics manufacturing (AME) for advanced packaging; 2) Metrology for advanced packaging;

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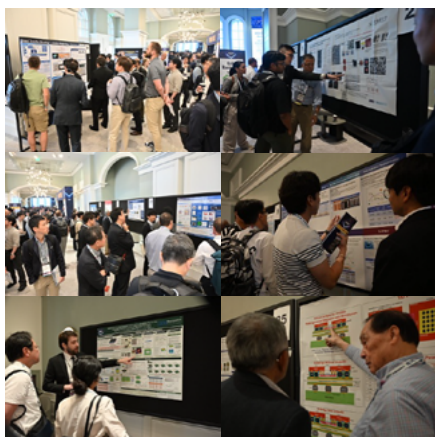
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Impressions from ECTC’s popular interactive sessions.



Many receptions allowed for ample networking.

Challenges, innovation, and industry impact; 3) Emerging technologies; and 4) Neuromorphic computing.

Professional development courses. ECTC 2026 offered 16 professional development courses (PDCs) in addition to the main conference program. These four-hour courses—taught by world-class experts—enabled participants to broaden their technical knowledge base. Attendees were awarded either CEU or PDH credits (continuing education units or professional development hours, respectively).

Looking ahead

ECTC 2026 had a record-setting year, and the variety and technical depth of the work presented is evidence of the tremendous amount of innovation taking place in advanced chip packaging. It's an exciting time to be in this industry, and we can't wait to see what's in store for next year when ECTC 2027 takes place in Denver, CO, June 1-4, 2027. The ECTC committee looks forward to seeing you in Denver.

About ECTC, EPS & IEEE

The ECTC technical program addresses new developments, trends

and applications for a broad range of topics, including components, materials, assembly, reliability, modeling, interconnect design and technology, device and system packaging, heterogeneous integration, wafer-level packaging, photonics and optoelectronics, IoT, 5G, quantum computing and systems, 2.5D and 3D integration technology, and other emerging technologies relevant to electronics packaging.

The IEEE's Electronics Packaging Society (EPS) sponsors ECTC. EPS is the leading international forum for scientists and engineers engaged in research, design and development of revolutionary advances in microsystems packaging and manufacturing. It encompasses all aspects of packaging and integration of electrical, electronic, optoelectronic, biological, micromechanical and sensing components.

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