Chip Scale Review®

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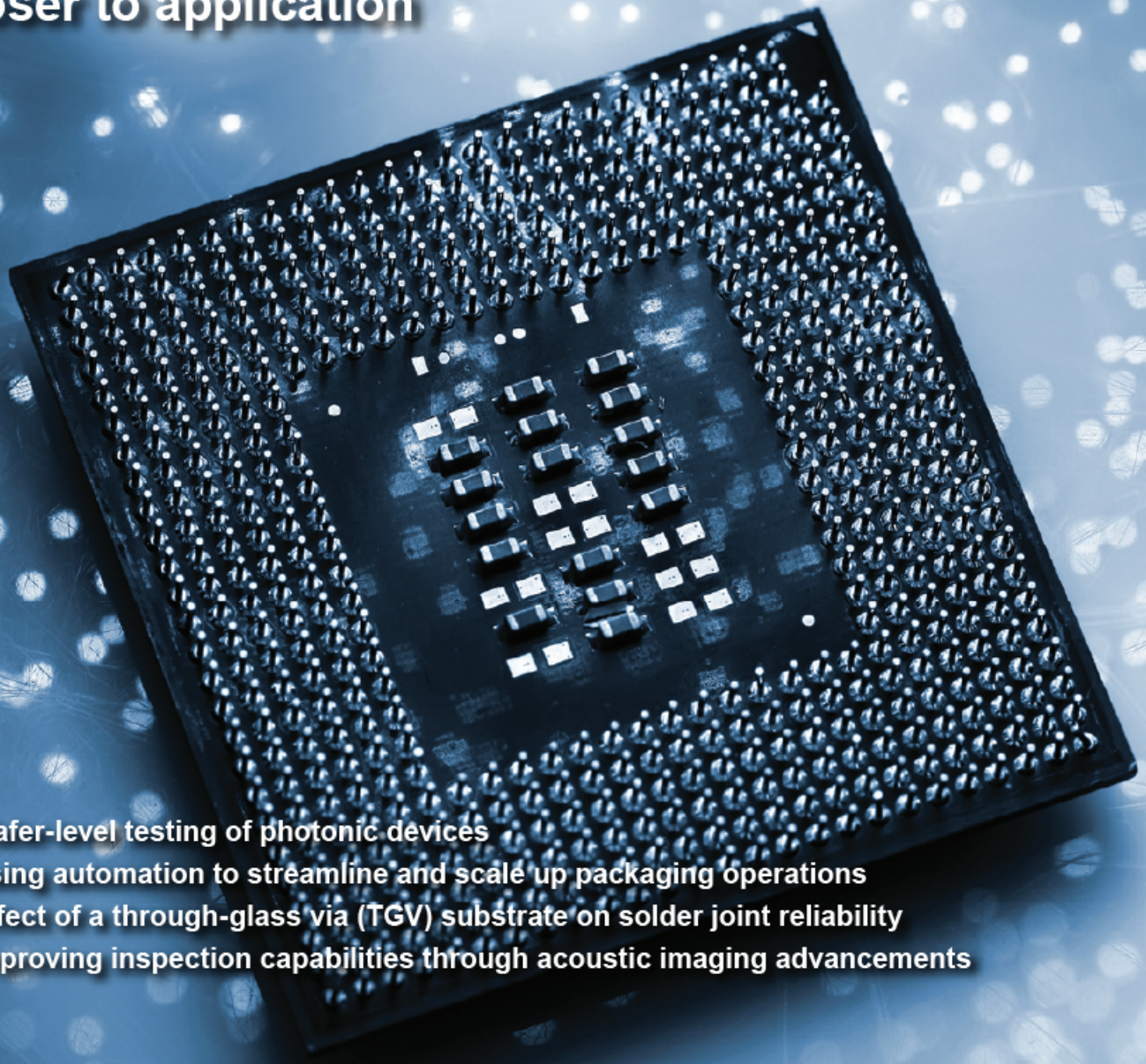
The Future of Semiconductor Packaging

Volume 29, Number 5

September • October 2025

From lab to fab: Bringing MEMS vapor cells closer to application



- Wafer-level testing of photonic devices
- Using automation to streamline and scale up packaging operations
- Effect of a through-glass via (TGV) substrate on solder joint reliability
- Improving inspection capabilities through acoustic imaging advancements

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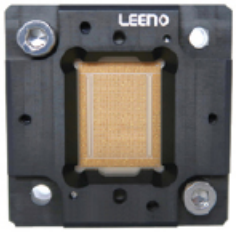

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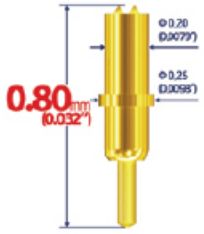

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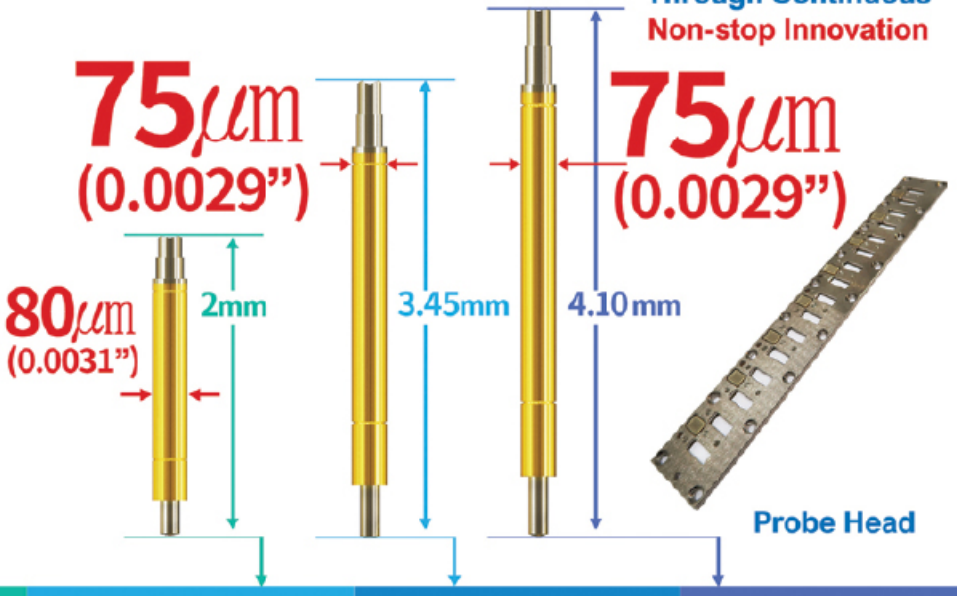

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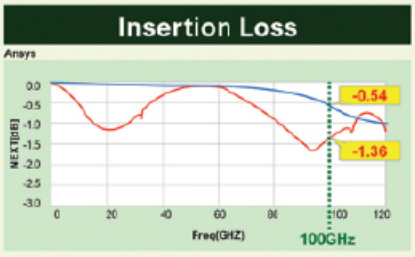

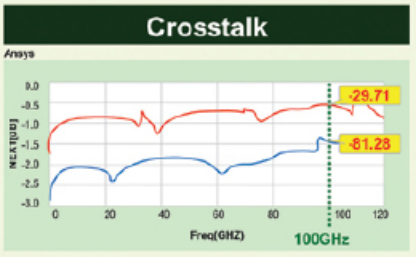

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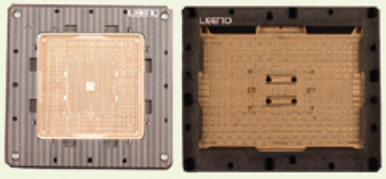

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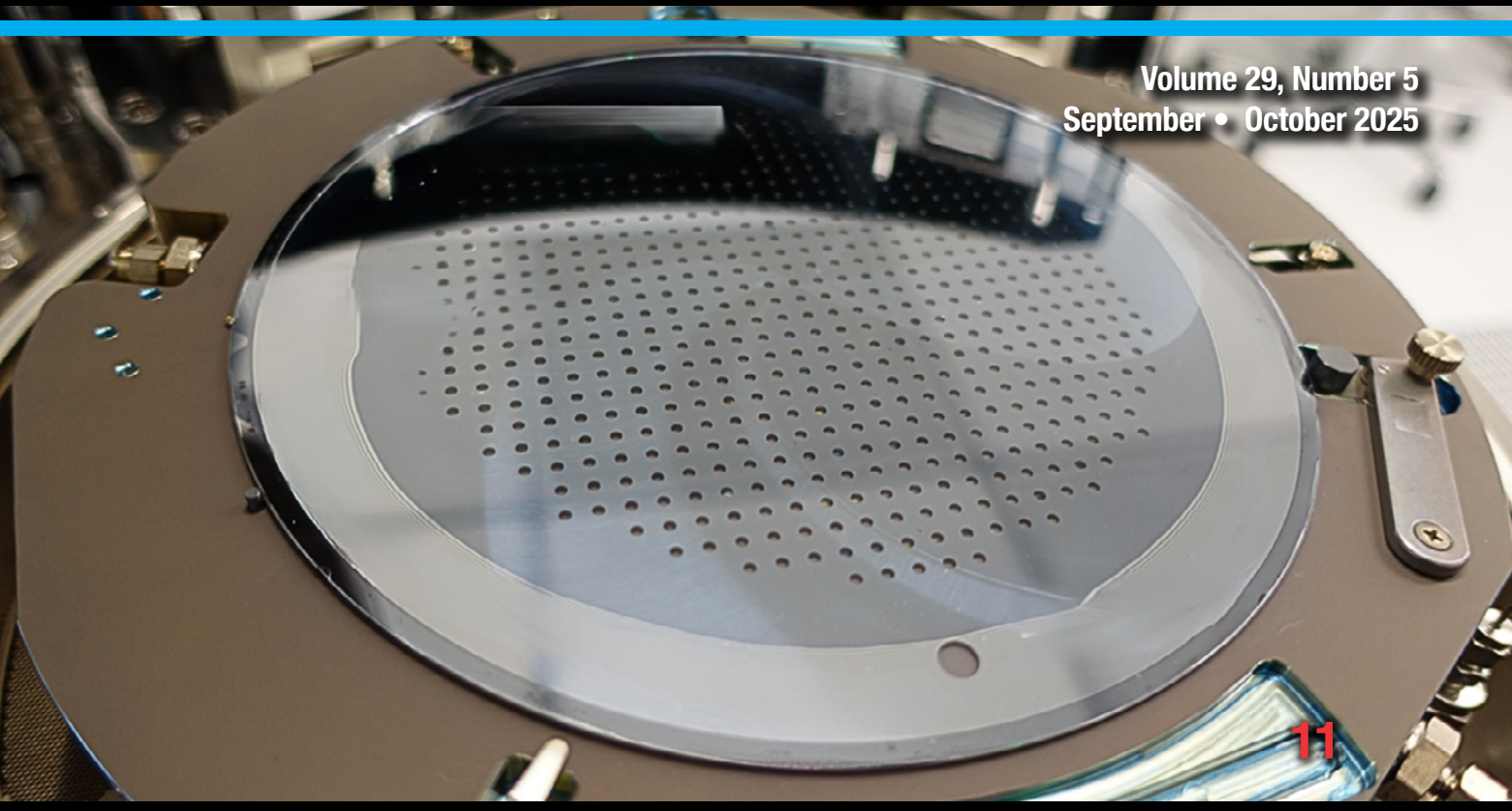

The advantages of quantum sensing over classical methods are several: 1) Reducing fabrication costs; 2) Enhancing yield; and 3) Developing scalable manufacturing methods. The cover article uses the example of MEMS vapor cell fabrication and integration into a gyroscope measurement setup. Such atomic gas vapor cells are the core components of optically-pumped quantum devices and represent the forefront of precision sensing technology. As such, they enable the development of compact, high-performance instruments.

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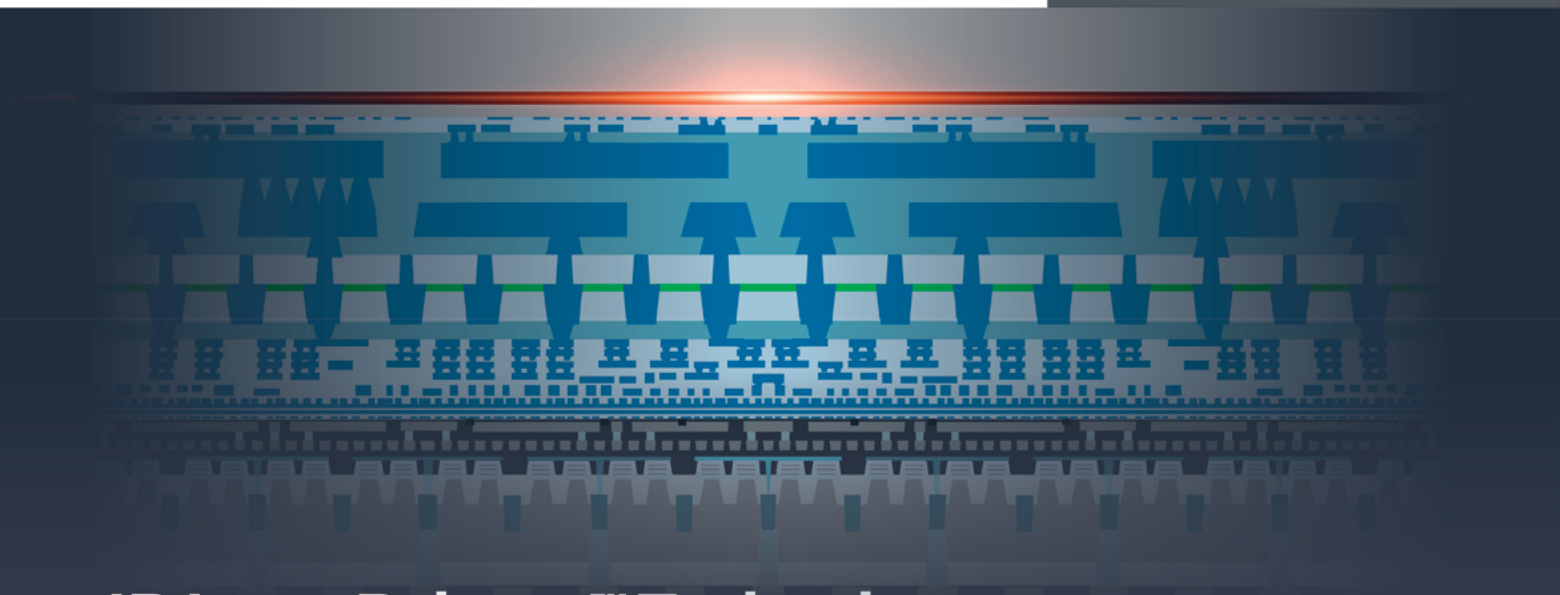

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Publisher
knewman@chipscalereview.com

Lawrence Michaels
Managing Director
Editor-in-Chief
lmichaels@chipscalereview.com

Debra Vogler
Senior Technical Editor
debravogler@me.com

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P.O. Box 2165
Morgan Hill, CA 95038
Tel: +1-408-846-8580
E-Mail: subs@chipscalereview.com

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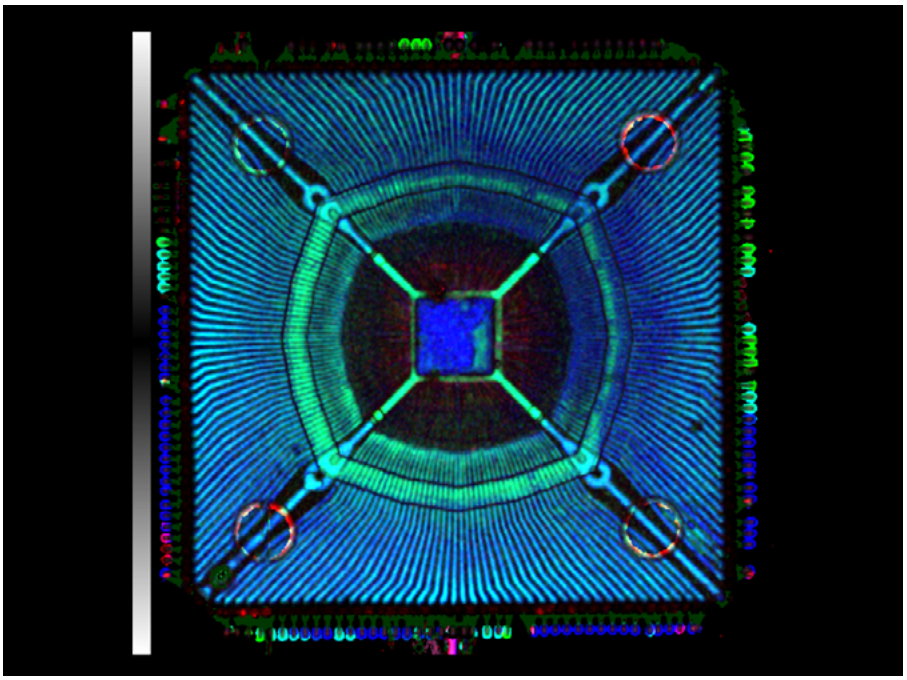

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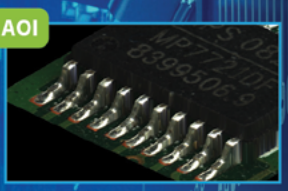

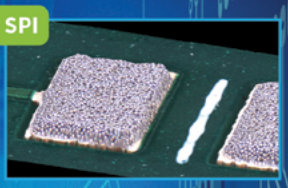

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Using automation to streamline and scale up packaging operations

Chip Scale Review asked Aerotech's Justin Bressi to discuss the use of automation to streamline and scale up packaging operations.

CSR: How is advanced packaging meeting the challenges faced by the slowdown of Moore's Law with respect to traditional transistor scaling at the same time that artificial intelligence (AI) and high-performance computing (HPC) are presenting additional challenges for the industry?

JB: Advanced packaging continues to push the frontier of what is possible in semiconductor manufacturing, enabling the industry to address the challenges of AI and HPC applications. Chipmakers must work closely with the entire ecosystem, including providers of fundamental subsystems like precision motion control, to solve the complex challenges posed by these emerging technologies.

CSR: How is automation helping manufacturers scale up and streamline packaging operations—particularly now that the once distinct line between front-end and back-end semiconductor manufacturing has blurred in recent years?

JB: While traditional packaging was once a purely "back-end" process focused on simple protection and connectivity, both mature and emerging advanced packaging processes now have many of front-end semiconductor manufacturing's characteristics and stringent demands. This fundamental shift is driven by multiple factors, including processes like fan-out wafer-level packaging (FOWLP), where some packaging processes are completed before the wafer is diced. Additionally, the need for higher performance demands tighter integration, relying on complex architectures like heterogeneous integration and 3D stacking, where multiple dissimilar dies from different process nodes, or even different materials, are brought together into a single, highly-integrated package. These new methods and architectures require a level of precision that was previously exclusive to the front end, making the packaging process an integral part of system performance and functionality.

CSR: What new kinds of automation are needed when scaling up advanced packaging operations?

JB: In many cases, simple, low-precision pick-and-place robotics are no longer adequate when scaling up advanced packaging operations. Manufacturers now require sophisticated automation systems capable of nanometer-level positioning and dynamic control traditionally reserved for front-end processes. These systems provide the high-speed, high-precision capabilities needed to handle everything from wafer-to-wafer bonding to die-to-interposer assembly with the near-flawless accuracy required to achieve satisfactory yields. Without this higher level of automation, the intricate alignments and delicate forces required for modern processes like hybrid bonding would be impossible to achieve at a scale that meets both the yield targets necessary to be commercially viable, and the intensely demanding throughput targets of semiconductor operations. Process flexibility is also often crucial, as chip manufacturers need to be able to adapt to evolving designs and requirements from their end customers. This need for flexibility puts additional demands on the automation systems, requiring a level of system robustness to support a wide variety of operating parameters.

CSR: What does the shift to advanced packaging mean for semiconductor production in Taiwan?

JB: The shift to advanced packaging is reshaping the landscape of semiconductor production in Taiwan, with TSMC at the epicenter of this transformation. For decades, Taiwanese chipmakers, particularly TSMC, operated as pure-play foundries, focusing almost exclusively on the "front-end" processes of designing and fabricating wafers. Back-end packaging was traditionally done by outsourced semiconductor assembly and test (OSAT) providers. However, the advent of new advanced packaging architectures like TSMC's dominant Chip-on-Wafer-on-Substrate (CoWoS®) has fundamentally altered this business model. These integrated, high-density packages require a level of precision and process control that is a natural extension of front-end fabrication, not a distinct back-end activity. This has meant a substantial shift in strategy and investment for leading Taiwanese manufacturers.

CSR: Bringing significant advanced packaging capabilities in-house surely requires substantial investments in R&D. Could you elaborate on what is required?

JB: Indeed, to enable the new chip architectures, Taiwanese manufacturers made substantial investments in R&D, new equipment and highly specialized expertise. While collaborations with OSATs still exist for certain processes, the most cutting-edge advanced packaging processes are increasingly being integrated directly into the foundry's workflow to ensure the highest levels of quality, yield and performance. This increasing level of vertical integration provides tighter control over the entire supply chain, which is crucial for meeting the demanding specifications of HPC and AI chips.

CSR: Whenever new processes or methods are introduced, the industry usually needs to go through a period of time when standards or new equipment needs to be developed. What is your assessment of these needs?

JB: Unlike mature front-end processes or CoWoS®, many emerging advanced packaging techniques are novel and lack fully-standardized, off-the-shelf equipment. This creates a major opportunity for innovation. Manufacturers in Taiwan are

actively collaborating with local equipment makers to co-develop the bespoke tools needed for these new processes. This strategic partnership not only accelerates the development of advanced packaging technologies like CoWoS®, but also strengthens Taiwan's entire semiconductor ecosystem, building a resilient supply chain that reinforces the island's dominance in the future of chip manufacturing. Because many of these new processes require positioning systems with performance close to that of front-end semiconductor equipment— including requirements for extreme precision and dynamics—we have been working with manufacturers in Taiwan to provide cutting-edge motion control solutions.

CSR: What is the role of precision motion systems in meeting the evolving demands of advanced packaging?

JB: Advanced packaging processes share many of the demanding characteristics of front-end processes, so their enabling motion control systems must meet incredibly stringent specifications. The need for precise alignment, stability and high dynamics is fundamental to many of these processes, from wafer bonding to heterogeneous die stacking, which are simply not possible or scalable without equipment that relies on cutting-edge motion control engines for critical process steps.

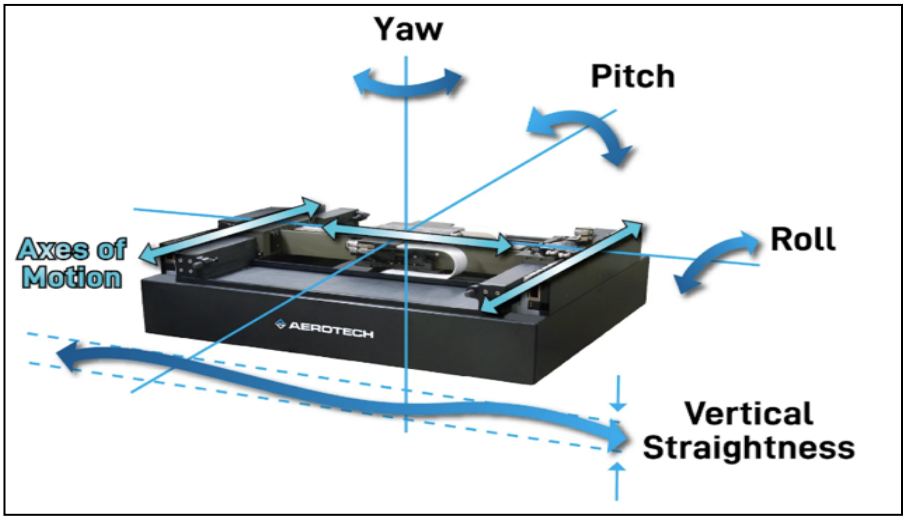

Figure 1: To achieve near-perfect bonding without discontinuities or die-killing voids and gaps, processes like hybrid bonding require alignment in all six degrees of freedom: X, Y, Z, and the three rotational axes.

One of the most important requirements is nanometer-level positioning accuracy and stability. Processes like hybrid bonding require alignment in all six degrees of freedom—X, Y, Z, and the three rotational axes—to achieve near-perfect bonding without discontinuities or die-killing voids and gaps (Figure 1).

Modern systems typically use technologies like air bearings and advanced servo controls to minimize geometric error motions and achieve exceptional in-position stability, often down to a few nanometers. This extreme precision is necessary to assemble advanced node chips that increasingly rely on shrinking pitches and higher-density interconnects to achieve cutting-edge performance.

Beyond precision positioning, high dynamics and force control are also essential for meeting throughput targets. The demand for rapid step-and-settle performance and high-speed movement is paramount in a high-volume manufacturing environment. Advanced motion controllers are engineered to enable aggressive servo tuning and sophisticated feedforward controls that minimize dynamic errors during high-acceleration moves. Furthermore, delicate

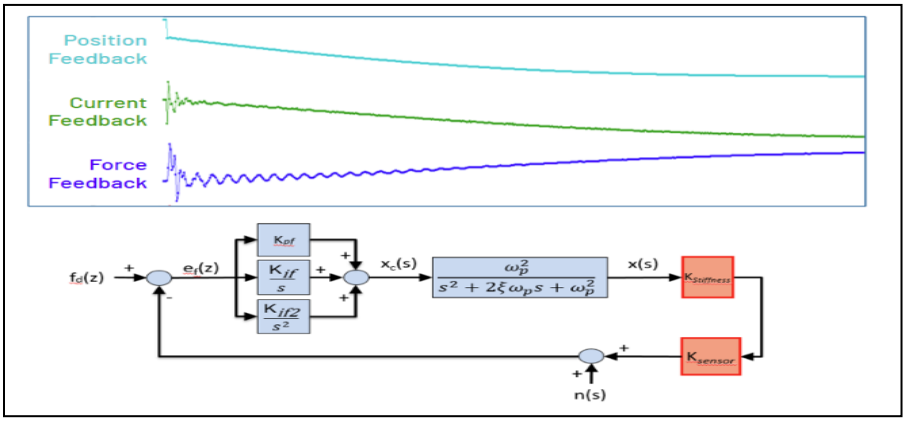

Figure 2: Integrated force feedback and sophisticated servo loops are needed to accurately track commanded force for delicate processes such as chip stacking.

processes like chip stacking require precise control over the applied press force. To meet these needs, integrated force feedback and sophisticated servo loops are used to accurately track commanded force, ensuring the integrity of the bond without damaging the delicate components (**Figure 2**).

Finally, the entire system must operate reliably within demanding environments like cleanrooms and ultra-high vacuum (UHV) chambers while also managing unwanted vibration and internal heat dissipation. Precision motion systems mitigate these environmental factors with specialized methods and materials, passive and active isolation systems, and thermal compensation techniques. By integrating these capabilities, precision motion systems become more than just components; rather, they are a mission-critical subsystem of the overall process tool, providing the performance and reliability needed to enable the most advanced semiconductor technologies.

CSR: How can local chipmakers adapt to fast-changing requirements?

JB: In an environment where technological requirements are evolving at a breakneck pace, adaptability is the most valuable asset for any chipmaker. Advanced packaging requires constant innovation to keep up with new architectures and tighter integration demands. This creates a significant challenge for chipmakers who must not only master today's technology, but also prepare for tomorrow's. Their success hinges on two key elements: 1) Robust feedback loops in process development; and 2) Strategic collaboration with key suppliers and capital equipment original equipment manufacturers (OEMs).

By bringing key advanced packaging capabilities in-house, companies can shorten the feedback loop between R&D, and design and manufacturing. This allows them to experiment with novel processes and quickly iterate on new architectures, providing the agility needed to respond to sudden shifts in technology.

Strategic collaboration with key capital equipment partners and suppliers is crucial for staying ahead of the curve. By working closely with equipment manufacturers, chipmakers can co-develop bespoke tools and processes needed for emerging technologies that don't yet have off-the-shelf solutions. This approach leverages the specialized expertise of their supply chain, allowing for faster development cycles and a more resilient overall ecosystem.

Biography

Justin Bressi is a Business Development Manager at Aerotech Inc. He has over 10 years of experience in the motion control and automation industry and holds a Master's degree in Business Administration and a Bachelor's degree in Mechanical Engineering from the University of Pittsburgh. Email: jbressi@aerotech.com

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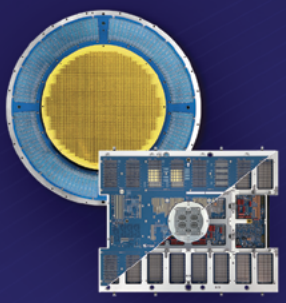

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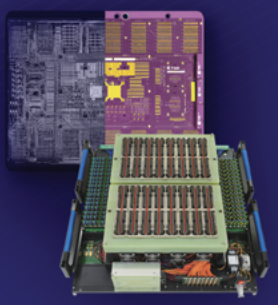

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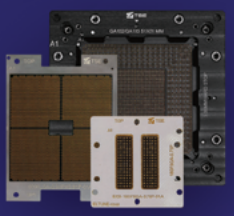

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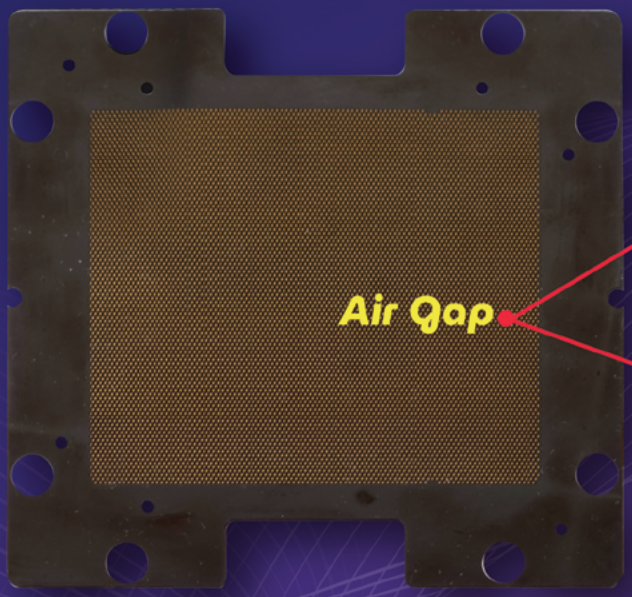
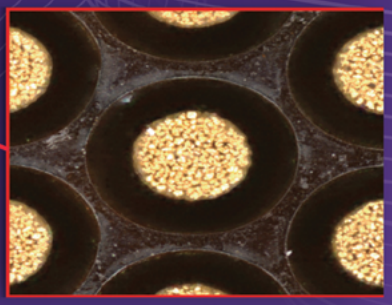


<Section View>



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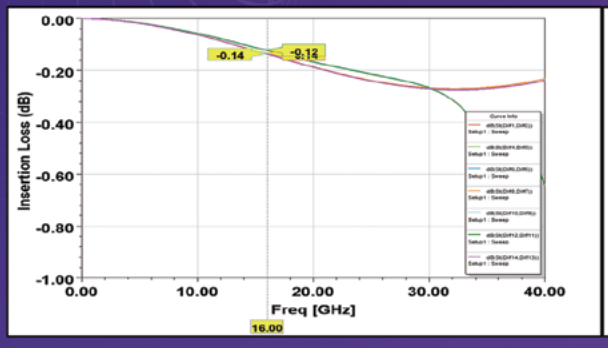

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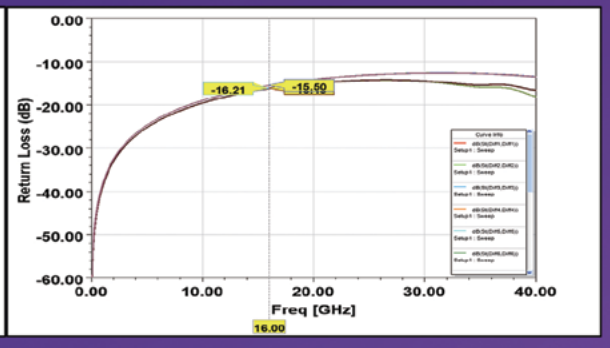

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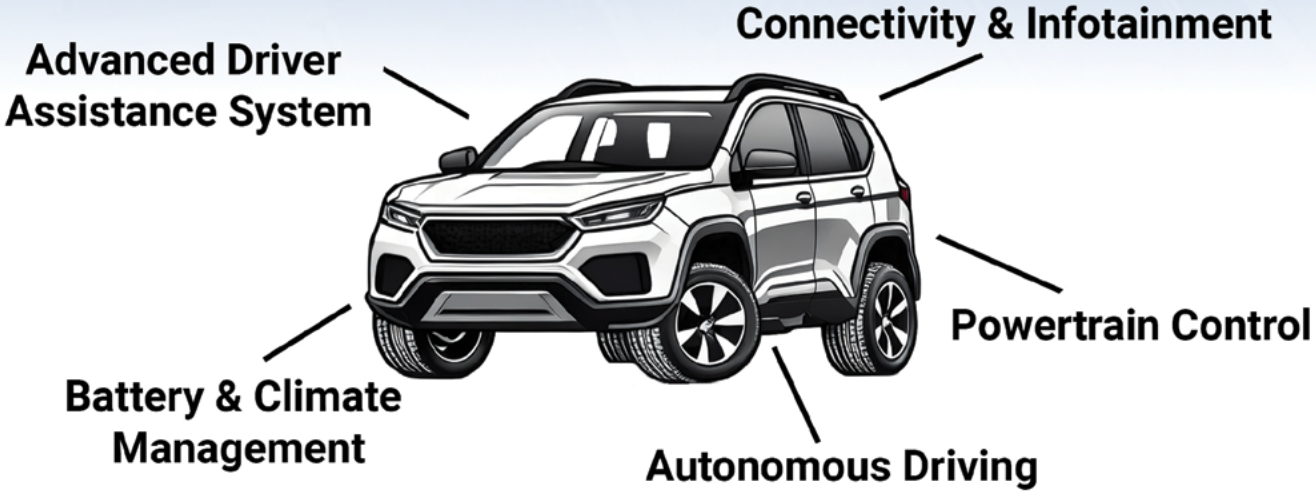

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From lab to fab: Bringing MEMS vapor cells closer to application

By Gudrun Bruckner [Silicon Austria Labs GmbH, Heterogeneous Integration Technologies, Villach, Austria]; Janine Riedrich-Möller [Robert Bosch GmbH, Advanced Technologies and Micro Systems, Renningen, Germany]; Thomas Grömer [EV Group, St. Florian am Inn, Austria]

Quantum sensing offers several advantages over classical methods and is being extensively researched for applications like magnetometers, gyroscopes, and atomic clocks. The motivation behind this work stems from common industrial challenges: 1) Reducing fabrication costs, 2) Enhancing yield, and 3) Developing scalable manufacturing methods. In order to transition these innovative principles from laboratory research to industrial fabrication and real-world applications, it is essential to not only understand the underlying physics, but also to consider industry requirements and available manufacturing technologies. This article uses the example of microelectromechanical systems (MEMS) vapor cell fabrication and their integration into a gyroscope measurement setup to highlight the effectiveness of collaboration between research organizations and industry in developing new solutions for commercialization. Atomic gas vapor cells are the core components of optically-pumped quantum devices and represent the forefront of precision sensing technology. They enable the development of compact, high-performance instruments.

The applications of MEMS-based rubidium vapor cells are diverse and expanding. They are a critical component in miniature atomic clocks, which, compared to traditional quartz oscillators, offer superior time-keeping capabilities in a small, low-power package, making them ideal for portable communication and navigation systems. In the field of magnetometry, these cells are used to create highly-sensitive magnetometers capable of detecting minute magnetic fields, with applications ranging from biomedical imaging, such as magnetoencephalography, to geophysical surveying. Compared to superconducting quantum interference devices (SQUIDs), vapor cells provide similar sensitivity, while offering a major advantage: They operate at accessible temperatures slightly above room temperature, thereby eliminating the need for the extensive cryogenic cooling required by SQUIDs. Additionally, the principles of atomic spin precession are being harnessed to develop atomic gyroscopes that promise unprecedented precision in rotation sensing for inertial navigation systems.

A process called optical pumping is used to prepare the atoms in a specific spin-polarized state. This is achieved by illuminating the atomic gas vapor with polarized laser light that selectively excites atoms and leads to a net magnetization of the atomic ensemble. Once polarized, the atomic spins precess at a characteristic frequency, known as the Larmor frequency, when subjected to an external magnetic field. This precession can be optically detected as a change in the absorption or polarization of a probe laser beam, allowing for highly-sensitive measurements of the magnetic field or rotation.

The atomic gas used in vapor cells typically consists of a mixture of several gases, including an alkali vapor—such as rubidium—and noble gases like xenon, and nitrogen, all confined within a small, sealed cell. Each component in the mixture serves a specific function, and optimizing the gas composition is essential for achieving high sensitivity. Xenon isotopes such as Xe-129 and Xe-131 possess nuclear spin and exhibit long relaxation times, making them ideal for precision sensing. Alkali atoms like rubidium can be optically pumped and transfer their polarization to xenon nuclei via spin-exchange interactions. Nitrogen enhances the efficiency of optical pumping by quenching excited states of the alkali atoms, thereby preventing radiation trapping. Together, these components form a system capable of suppressing magnetic field noise and isolating the rotational signal in gyroscopes. In addition to the composition of the gas, the operation temperature, gas pressure and cell geometry are to be considered. A detailed overview of various gyroscope strategies and properties of gas mixtures can be found in [1].

MEMS vapor cell fabrication

A key challenge in the fabrication process is the encapsulation of volatile and reactive rubidium metal, along with the high cost of xenon isotopes used in the gas mixture. Advances in microfabrication have significantly improved the state-of-the-art in vapor cell technology. Instead of traditional glass-blown cells—that are difficult to scale for commercial applications—modern vapor cells are fabricated using a layered structure of glass, structured silicon, and another glass wafer. This approach leverages MEMS-compatible processes such as photolithography, deep-reactive ion etching (DRIE) of silicon, and anodic bonding for hermetic sealing. These techniques have resulted in robust, reliable devices. Furthermore, wafer-scale fabrication now enables the mass production of highly-integrated vapor cells, paving the way for scalable and cost-effective quantum sensors.

Miniaturization and wafer-level production are now possible and enable upscaling. However, there are still two main challenges to be addressed. While the spin-exchange optical polarization between rubidium and Xe-129 enhances the signal-to-noise ratio of the atomic gyroscopes, xenon is a trace gas in the Earth's atmosphere and isotopically-pure xenon gas is very expensive, contributing

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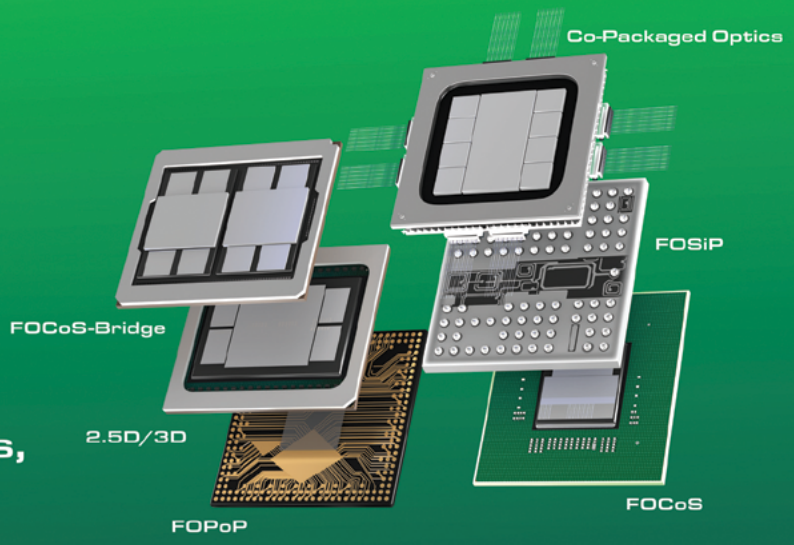

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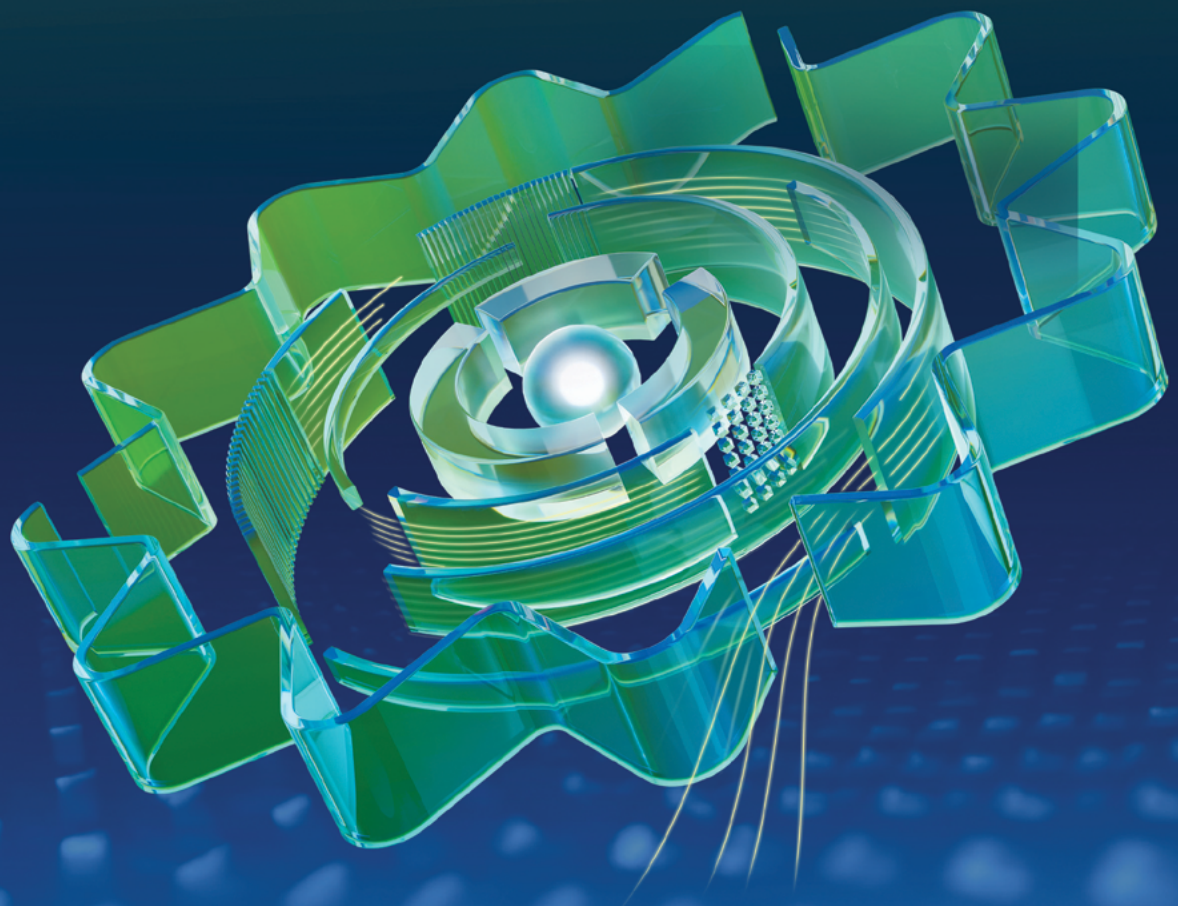

significantly to the total cost of the vapor cells. The handling of rubidium and the high cost of xenon hinders the widespread implementation of these types of cells. Instead of looking for other gas compositions, we addressed these blocking points by developing a new gas filling method for the vapor cells that minimizes the amount of the required xenon gas, while providing full control of the other required parameters, namely rubidium deposition, gas composition and cell pressure.

In a standard wafer bonding process, the gas lines are connected to the bonding chamber and the whole chamber volume is evacuated and purged several times before the chamber is filled with the final gas and the cells are sealed by anodic bonding between the capping glass and the silicon wafer. This process requires a substantial amount of xenon gas, with significantly higher consumption than would be necessary to fill the cells alone.

The innovative process flow is depicted in **Figure 1** (see also [2]). The realization of this idea was only possible by combining the understanding of the required physical parameters with the know-how and willingness to cooperate. It required a redesign of the bond chuck that included re-evaluation of applied materials and required surface quality, a modification of the wafer bonding equipment and the installation of an enhanced gas control system. A detailed description can be found in [3].

One key idea for the xenon filling is to separate the atomic gas flow from the gas control circle of the chamber and to guide the atomic gas directly from the chuck to the cells before sealing them. While the underlying idea seems relatively simple, it requires a deep understanding of the flow dynamics during filling and the continued aligned gas flow control of both gas circuits. As one bonding step involves bending of the capping glass, mechanical properties of the glass must be considered to allow said bending, while at the same time it must sustain any over pressure in the gas filling circuit relative to the bonding chamber.

The described process flow combines established processes like structuring of silicon by etching and Taiko grinding in an innovative way, and also introduces completely new approaches like the laser opening of the glass for the gas inlet. Here are some aspects that demonstrate the cross-disciplinary solutions. The numbers in parentheses listed in the remainder of the article refer to the process flow numbering in **Figure 1**.

(1) The first anodic bonding step is state of the art, but for symmetry reasons a thin glass was used. (2, 3) During Taiko grinding and later etching, care must be taken so that the surface of the outer bonding ring is not impaired by scratching

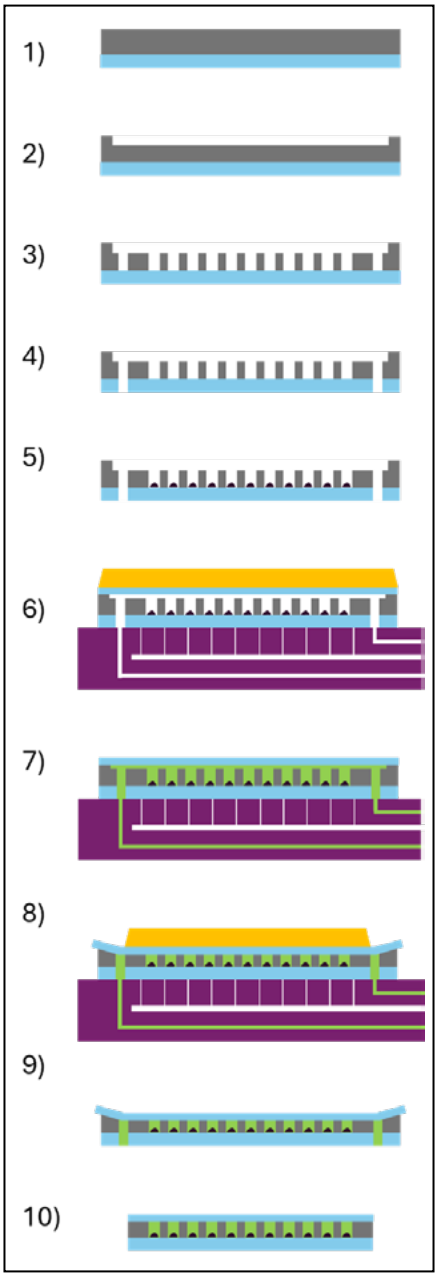

Figure 1: Process flow for the fabrication of MEMS vapor cells: 1) First anodic bond; 2) Taiko ring grinding; 3) Structuring of cavities; 4) Opening of glass with laser; 5) Deposition of Rb; 6) Second anodic bond of cover glass; 7) Xe gas filling; 8) Third anodic bond; 9) Edge trimming; and 10) Flat wafer stack.

or etching because that would interfere with the second anodic bond in step (6). As an alkali metal, rubidium is known for its reactivity with air and water. Instead of filling the cells directly with rubidium, we used a method similar to one described by other authors and dispensed an alcoholic solution of RbN_3 and dried it slowly to insert a defined amount of RbN_3 into the cell. The dried RbN_3 stays in the cell and does not interfere with the gas filling in step (7). The Rb atoms will only be released by UV-laser decomposition into Rb and N_2 any time after the cells have been closed. As described above, the nitrogen from this reaction is beneficial for the optical pumping. (6) The second anodic bond in combination with the opening of the glass results in a gas flow circuit that is separated from the volume of the bond chamber and the vacuum system used to hold the wafer stack. (7) Filling the cells with the precious xenon gas can now be done without filling the whole bonding chamber. The xenon only flows from the chuck to the wafer and through the cells.

An elaborate simulation was done considering flow dynamics, as well as mechanical and temperature aspects, to fully fill all the cells without breaking the cover glass. Two-way coupled fluid-structure interaction (FSI) simulations in ANSYS Fluent were essential to accurately determine the time required to fill the MEMS cells because fluid flow and structural deformation influence each other dynamically. All structural analyses were conducted within Fluent using intrinsic FSI. Due to the significant deflection of the glass plate, a nonlinear elasticity model was applied. Because the domain geometry evolves over time with the movement of the glass plate, a dynamic mesh with smoothing was employed to accurately capture the gas behavior. Additionally, mechanical finite element simulations in ANSYS Mechanical were performed to assess the maximum deformation and stress in the glass under its own weight and the processing pressure.

Figure 2 shows how the xenon propagates through the individual cells, starting from the inlet point. The exact filling time depends on the geometry of the wafer stack. Complete filling is reached in less than 100s for a 200mm wafer and cylindrical cells with 2mm diameter and 1mm height. Careful timing is needed

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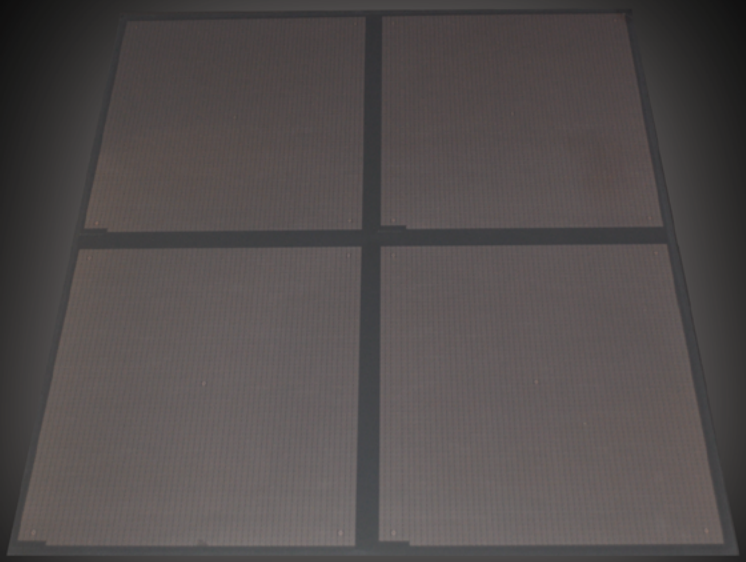

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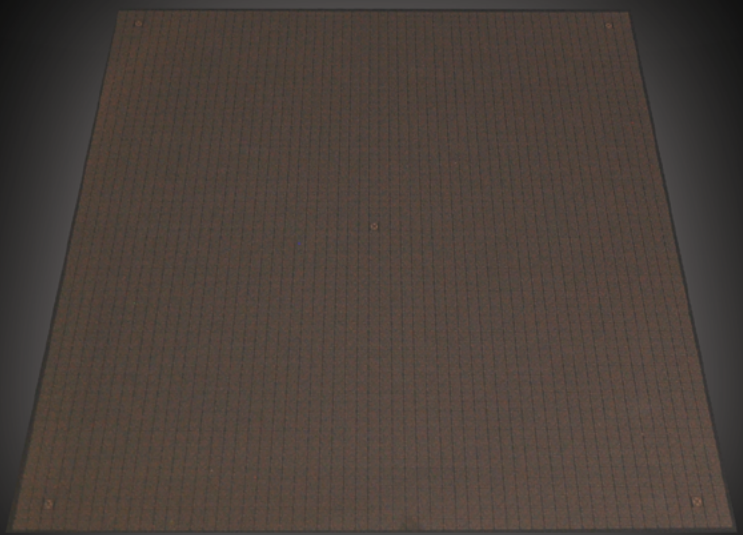

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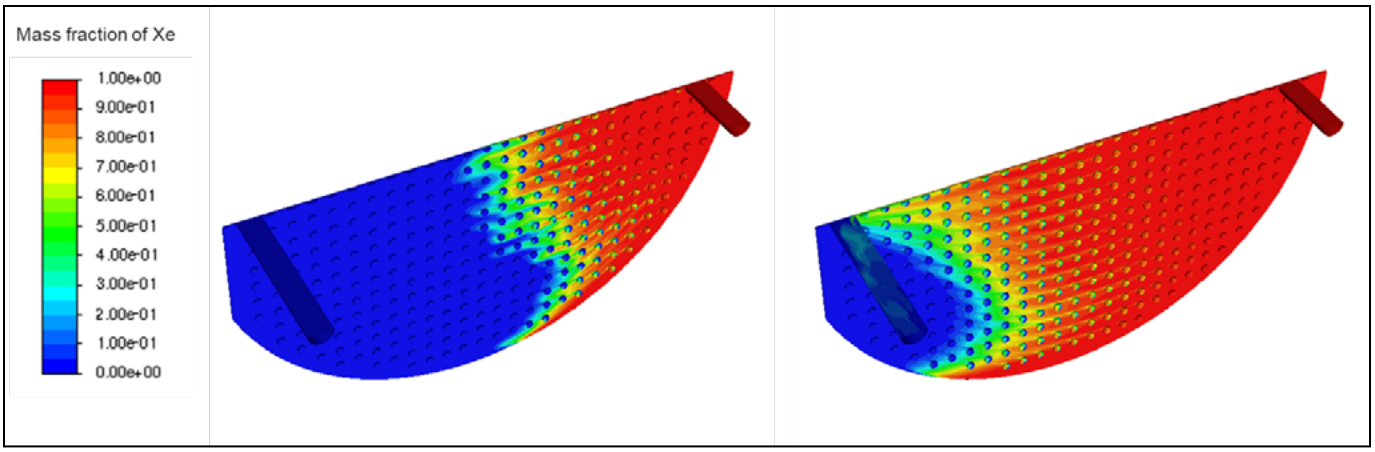

Figure 2: Simulated mole fraction of xenon during gas filling between inlet (red) and outlet (blue) after 10ms and 20ms (because of symmetry, only half a wafer is shown).

during the filling to control the time-dependent pressure difference among the bonding chamber, cells and vacuum chuck. Figure 3 shows the redesigned chuck with connected gas lines.

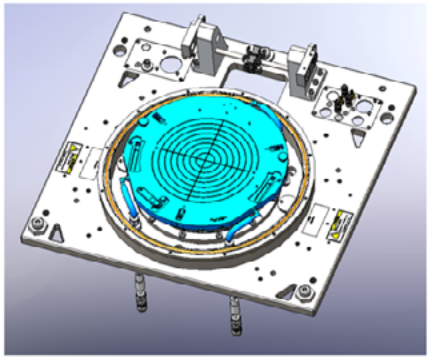

Figure 3: Redesigned chuck with incorporated gas line.

(8) The third anodic bond is realized by bending the glass capping wafer with a pressure plate so that the cells are closed and therefore decoupled from the gas flow in the chuck. (9) Edge trimming releases the flat inner part of the wafer stack and allows for further wafer-level processing, like lithography and metal deposition, to add heaters or coils to the cells. After all wafer-level processes are finished, standard dicing methods can be used to separate the cells. Figure 4 shows a bonded wafer and samples of separated MEMS vapor cells.

Gyroscope setup

As discussed, vapor cells are applicable in diverse sensor technologies. Our research utilized vapor cells containing rubidium, xenon, and nitrogen, configured for gyroscopic measurements as envisioned in autonomous vehicles (see Figure 5).

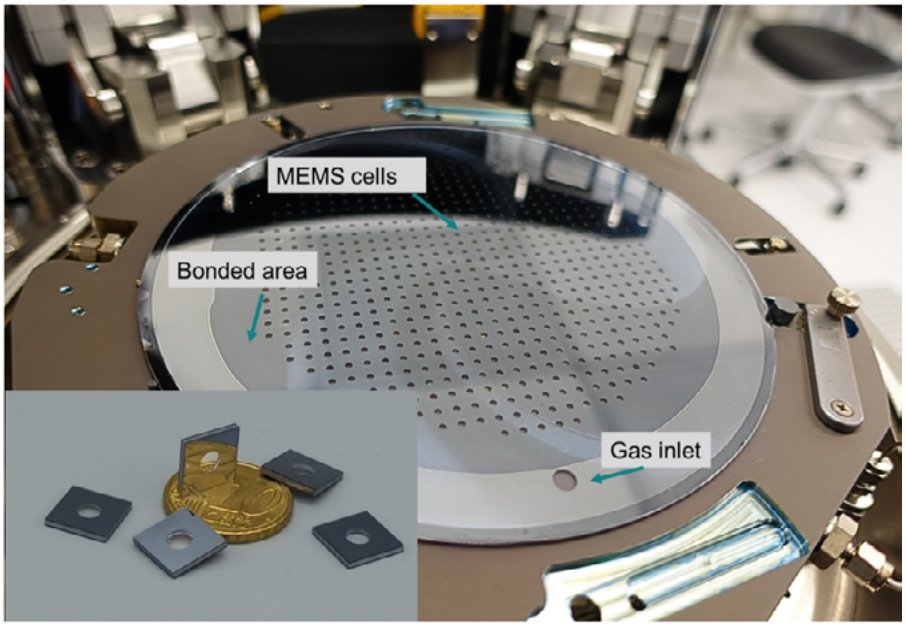

Figure 4: Bonded wafer and samples of separated MEMS vapor cells.

Figure 5: Envisioned future mobility solutions using high-performance inertial sensors. Photo: Courtesy Robert Bosch GmbH

The main components of the setup are illustrated in Figure 6. The heated vapor cell is encompassed by a three-axis coil system and magnetic shielding. A pump laser beam at 795nm orients the atomic spins. Spin precession is detected by a probe laser beam of the same wavelength via the Faraday effect, utilizing a polarizing beam splitter and a balanced photodetector. A lock-in amplifier-based signal processing scheme permits the separation of the rubidium signal from the xenon signal and the extraction of the rotation rate.

Thermalization of the vapor cell

The sensor design includes a heater for temperature stabilization of the vapor cell. A cell holder made of polyether ether ketone (PEEK) material enables thermal decoupling of the vapor cell from the environment. All mechanical components must be nonmagnetic, serve as housing and thermal insulation for the laser and vapor cell, and simultaneously provide precise, passive alignment references for the optical assembly.

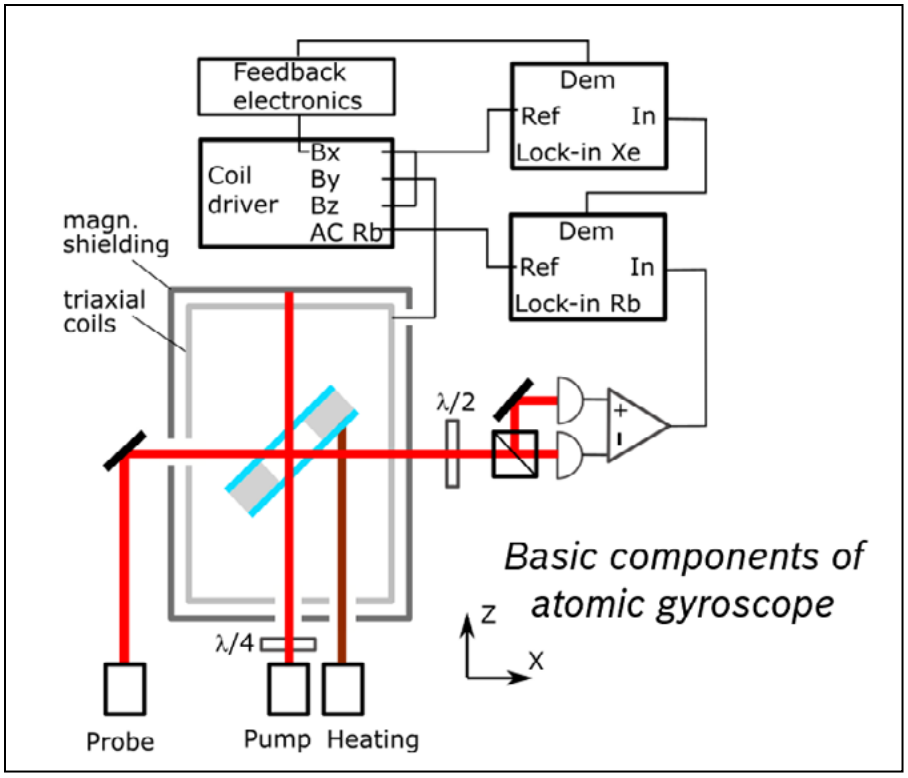

Figure 6: Main components of a vapor cell-based atomic gyroscope.

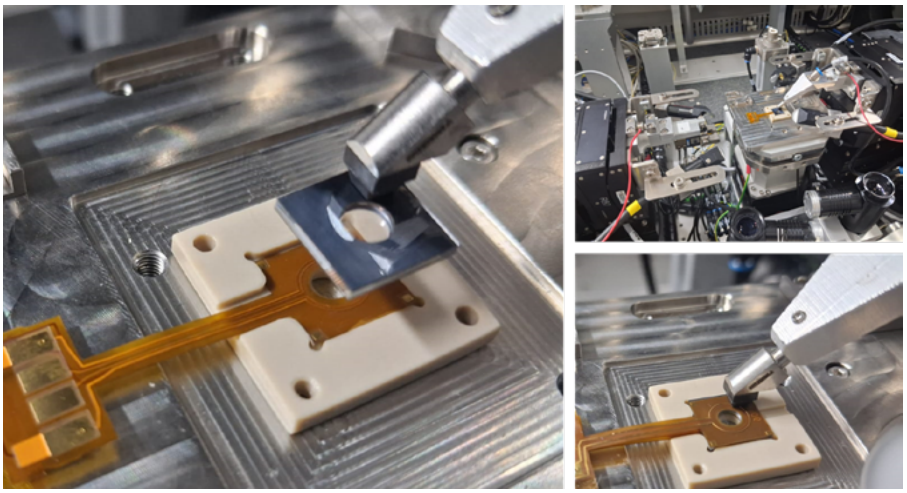

Figure 7: Automatic assembly of heaters and MEMS cell into a peak housing with Ficontec CL 1500.

In our setup, the vapor cell is heated by resistive elements. While the heating elements for the vapor cell could have been fabricated by applying lithography at the wafer level, we have decided to use printing technology on flex prints. The design of each heater cancels out magnetic fields from heating currents and the usage of two heaters on both sides of the cell ensures a more homogeneous temperature across the cell than could be realized by a single-sided lithographic process. In addition, high-temperature flex prints serve as electrical contacts, so that no additional wire or flip-chip bonding is needed to contact the heating circuits electrically. Finally, a temperature sensor is included on the flex print for even better temperature control. Figure 7 shows the automated assembly of the cells and heaters into a PEEK housing with the dedicated assembly machine Ficontec CL1500.

Summary

Beyond introducing an innovative approach for fabricating MEMS vapor cells, this study highlights the critical importance of multi-disciplinary co-design and collaboration.

Extensive simulations were needed not only for the optical design and thermal control of the laser and the vapor cells, but also for covering the multi-physics behavior (mechanical, fluidic, thermal) during gas filling. Apart from using MEMS fabrication, we opted for the combination of different fabrication technologies, despite not all of them being at wafer level and high throughput like the dispensing of RbN_3, or using printing technology for heating the vapor cells. The heterogeneous approach allowed us to take advantage of the various technologies.

The need to have a sealed gas inlet for the filling gas between the chuck and the wafer, and the separation of the gas circuits, required a thorough design review of the bond chuck and modifications of the wafer bonder itself. These changes were only possible because of the close cooperation between scientists, machine manufacturers and users.

Building a gyroscope out of the vapor cells can be seen as fabricating a quite complicated advanced package. Achieving the initial concept required a comprehensive, end-to-end design methodology—encompassing simulation, design, equipment adaptation, process control and testing—underscoring the value of integrated efforts across multiple domains.

Acknowledgments

This work was a team effort, and the authors want to thank co-authors Ali Roshanghias (Silicon Austria Labs), Augusto Daniel Rodrigues (Silicon Austria Labs), Jaroslav Kaczynski (Silicon Austria Labs), Martina Hübner (Robert Bosch GmbH) and Tino Fuchs (Robert Bosch GmbH). The authors would also like to thank their fellow team members at Silicon Austria Labs for their contributions: Younes Ashouri-Shokri, Jochen Bardong, Giovanna Grosso, Markus Zauner, Manoj Jose, Abinash Pradhan and Muhammad Khan. This work has been jointly supported by Robert Bosch GmbH, and by Silicon Austria Labs (SAL), owned by the Republic of Austria, the Styrian Business Promotion Agency (SFG), the federal state of Carinthia, the Upper Austrian Research (UAR), and the Austrian Association for the Electric and Electronics Industry (FEEI).

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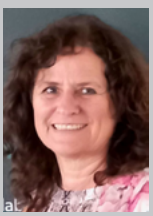

Biography

Gudrun Bruckner is Staff Scientist at Silicon Austria Labs at the Heterogeneous Integration Unit in Villach, Austria. She has extensive experience in research related to sensing technologies for harsh environments. Currently, she leads research projects in the field of integration and packaging, with a particular focus on photonic assembly. She earned her PhD in Physics from the University of Vienna, Austria.
Email: gudrun.bruckner@silicon-austria.com

Wafer-level testing of photonic devices

By Philipp Dietrich, Andrés Machado, Florian Rupp, Roman Zvahelskyi [Keystone Photonics GmbH]

High-volume manufacturing of optical communication infrastructure is limited by the lack of scalable manufacturing approaches. Following the footsteps of microelectronics by using wafer-scale fabrication processes has been a successful strategy for the manufacturing of the photonic integrated circuits themselves. However, subsequent steps common to microelectronic devices like cost-efficient packaging and high-throughput wafer-level testing, are missing and hamper the scalability of photonic device production.

To understand the fundamentally different challenges one finds in photonics compared to microelectronics, one must first take a deeper look at the various approaches to producing integrated photonic devices (**Figure 1**). The more conventional approach is exemplified in optical transceivers, which typically contain an array of lasers and are directly connected to single-mode fibers (SMFs). These transceivers have an electrical plug that allows simple exchange and therefore, show good in-field serviceability. Conventional transceivers with an electrical plug have the inherent disadvantage of requiring long electrical traces that induce high electrical loss and require transceiver-integrated digital signal processing (DSP). There is a lively discussion within the industry on how long pluggable transceivers will be competitive in terms of energy efficiency. Removing the power-hungry DSP is a logical, key step forward that can only be achieved by reducing the electrical trace length before the optical I/O [1]. Co-packaged optics (CPO) has therefore emerged as the clear approach for the long term [2]. However, the increased difficulty of exchanging or servicing such tightly-integrated modules is a real hurdle, and places stringent requirements on the reliability of CPO modules. These concerns are often addressed by removing the laser source from the package and making it hot-swappable and connecting SMFs with an optical plug.

How is photonics different from microelectronics

At first sight, the described CPO implementations appear to be relatively similar to their copper equivalent. One simply requires efficient packaging and testing implementations—ideally at the wafer level—to enable scalable mass production. However, a copy-and-paste approach from microelectronics fails at this point. While an electrical trace can be coupled with relatively large electrical interfaces—such as bumps or pads in the range of a few tenths of microns—photonics is different. To enable fast data rates at sufficient distances, optical waveguides must be single mode, i.e., they must give light only one possible way to propagate. As a consequence, light must be confined sub-micrometer scales. While spot-size converters may—with significant technical complexity—enable some degree of mode field expansion, the dimension of optical coupling interfaces will remain in the sub-10µm range. Therefore, both optical

Accuracy	Electrical	SMF interface	Laser interface	Optical plug
Size	50 µm	10 µm @ 1/e²	2.5 µm	40 µm
Position	20 µm	2 µm @ 1 dB	0.5 µm	8 µm
Angular	-	2° @ 1 dB	8°	0.5°

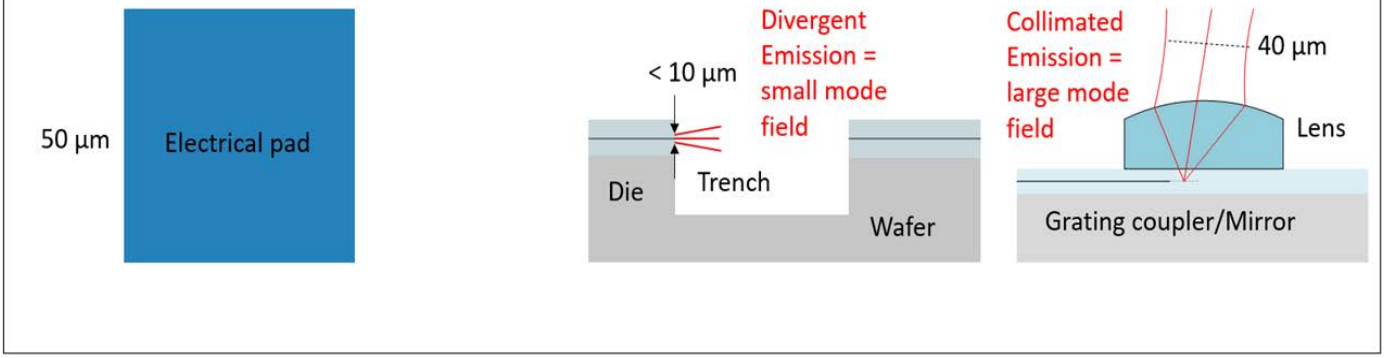

Figure 1: Size comparison of a typical electrical pad (blue) and optical mode-fields of a single-mode fiber (SMF) interface and the laser interface of a photonic chip. The accuracy requirements for the pad are in the range of 20µm, whereas photonic chips require accuracies in the micrometer- or sub-micrometer range. Beam expansion—as in optical plugs—will lead to relaxed positioning requirements, but with more stringent angular positioning requirements.

packaging and optical testing require, in a straightforward implementation, the ability to position components with sub-micrometer accuracy, introducing significantly more complexity than what is required for microelectronics. One may argue that this problem can be solved by expanding the mode fields using beam expansion, as is done in TSMC's compact universal photonic engine (COUPE) [3]. However, this only shifts the requirements from translational accuracy into equally stringent constraints for the angular positioning.

As a compounding factor, testing at the wafer level is particularly critical in the photonics industry, because it allows for the screening of chips before they undergo costly packaging steps. Unlike in microelectronics, packaging accounts for a disproportionately large share of the overall component cost in photonics (**Figure 2**).

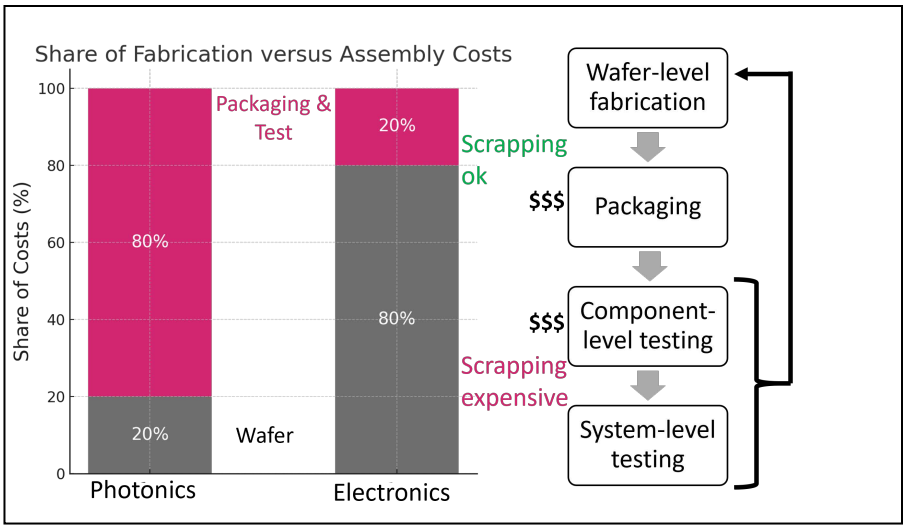

Figure 2: The relative cost of packaging and testing is significantly higher in photonics than it is in electronic manufacturing processes. Therefore, selecting known-good dies early in the fabrication process, ideally at wafer level, is particularly critical in photonics.

Leveraging in situ micro-printing optical testing

In summary, wafer-level optical testing is crucial for the scalability of photonic manufacturing and demands precisely-positioned micro-optics with sub-micrometer, or sub-0.1°, alignment in order to couple into expanded beams trenches or V-Grooves. The high accuracy requirements of photonic components cannot simply be met with conventional active-alignment technology because of the variation of optical fiber arrays and the geometrical constraints when coupling several optical lines at once. Typical pick-and-place micro-optical elements would not fit into V-Grooves or trenches with dimensions of 100µm and below. These intrinsic difficulties, however, can be convincingly addressed by utilizing 3D-printed micro-optics to control the direction and size of light entering and exiting photonic devices.

In situ 3D micro-printing (**Figure 3**) has already been successfully employed in photonics, especially in the field of optical packaging [5]. It has been demonstrated to be a reliable and reproducible method for low- and mid-volume production. The use of micro-printing for optical testing was first demonstrated at the Karlsruhe Institute of Technology [6,7] and is routinely used in a variety of industrial applications [8,9] with a focus on wafer-level testing.

The inherent advantage of the technology lies in its ability to combine

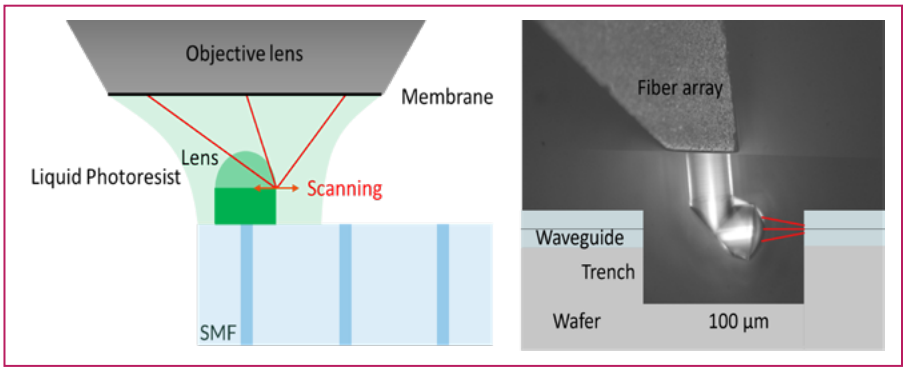

Figure 3: In situ 3D-micro printing using two-photon polymerization. A freeform micro-optical device is fabricated at the device facet of fiber arrays and other components by curing a liquid photoresist. With an in-built detector, sub-micrometer alignment to the mode field of optical components is possible. The free-form capability of the technology allows the creation of probes that fit into trenches of photonic wafers.

sub-micrometer accurate alignment to optical components (such as fiber array cores) with the precise fabrication of 3D freeform structures. As a 3D-printing system is used to both localize and print optical structures, feature alignment is almost exact, which highly benefits reproducibility [9]. This can be seen in the mode field size distribution shown in **Figure 4**, which demonstrates repeatability with a 3σ variation of 6%, resulting in negligible coupling loss variations (**Figure 4**). Consequently, 3D micro-printing can be seen as a pivotal technology to fabricate optical probes for wafer-level testing.

Summary

The use of micro-optics provides an order-of-magnitude improvement over existing solutions in a broad range of applications and can be considered a key enabling technology for scaling artificial intelligence (AI) infrastructure. A broad range of innovations have been applied in industrial settings, including: 1) Scalable fabrication of optical probes with 64 channels and beyond; 2) Features for automated alignment and calibration; 3) Ultra-fine pitch arrays to measure devices down to 20µm pitch; and 4) Smart probes with integrated distance sensors to avoid wafer crashes and increase throughput [9]. These advances are complemented by the possibility of seamless integration into existing wafer-level testing solutions through auto-alignment features as well as mechanical interfaces [8] for prober integration. Furthermore, applications for double-sided testing can be supported [10] and may enable novel approaches using optical plugs.

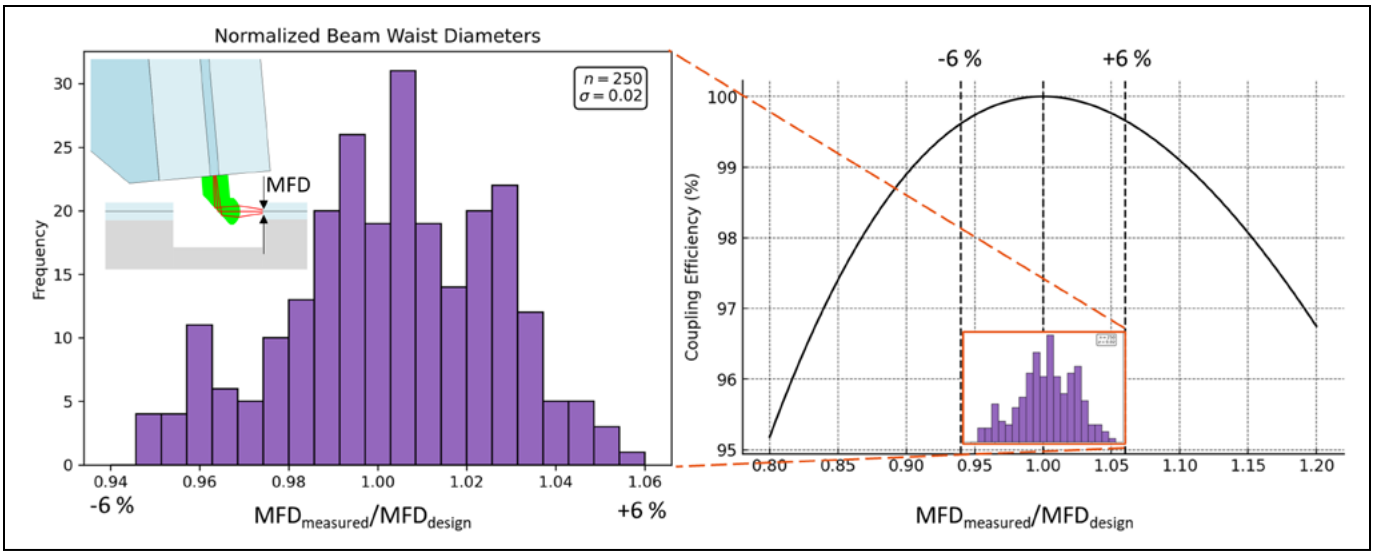

Figure 4: The mode-field diameter (MFD) of optical probes is a key figure of merit for performance variation of optical probes. Commercially-available optical probes provide low enough MFD to reduce coupling performance variation to less than 1%.

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Biographies

Philipp Dietrich is a co-founder and CEO of Keystone Photonics, Karlsruhe, Germany. He has ten years of industry experience in commercializing innovative products and solutions based on additive micro-fabrication. He is also a co-founder of Vanguard Automation, a company providing industry-grade machines and processes for photonic integration based on additive microfabrication and was recently acquired by Mycronic. He received his PhD from the Karlsruhe Institute of Technology for his work on the fabrication and application of functional microstructures. Email philipp.dietrich@keystone-photonics.com

Andrés Machado leads Research and Development at Keystone Photonics, Karlsruhe, Germany. He focuses on the development of new applications of freeform micro-optics, automated optical characterization, and optimization in micro 3D-printing. He holds a MSc in Physics from the Karlsruhe Institute of Technology.

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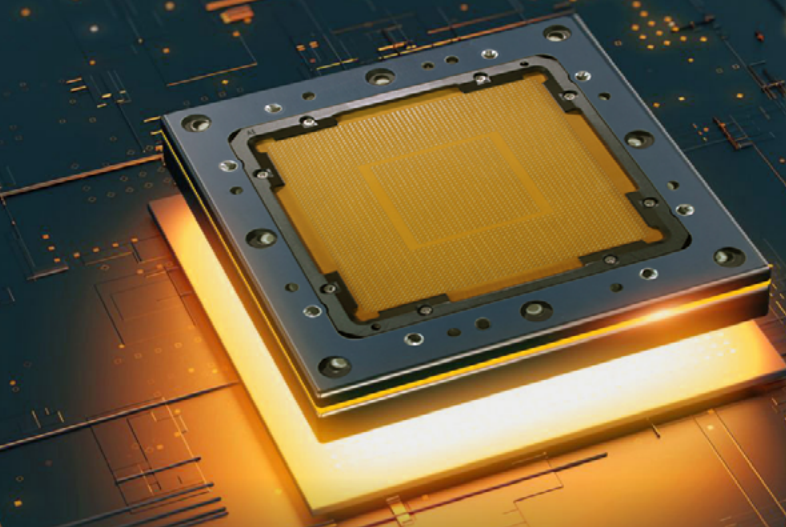

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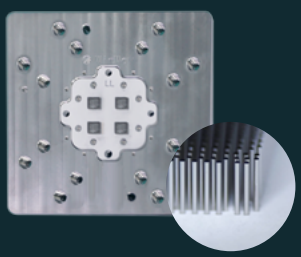

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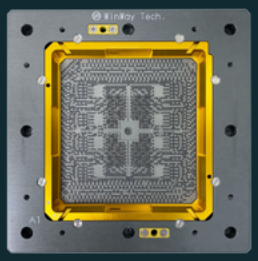

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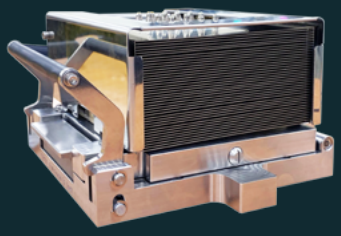

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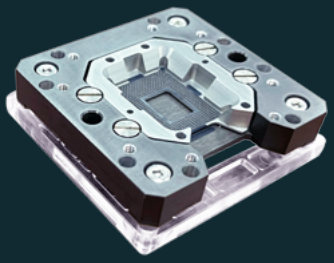

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Improving inspection capabilities through acoustic imaging advancements

By Bryan Schackmuth [Nordson, Test & Inspection]

The semiconductor manufacturing industry has exacting needs during the inspection process, requiring a precise approach to productivity and quality control. Higher throughput and resolution rank near the top of manufacturers' needs, as does defect detection with pinpoint accuracy. Additional requirements may include inspection systems and solutions that do not suffer from extensive maintenance downtimes, and a smaller machine footprint to maximize the efficiency of expensive cleanroom space.

The requirements noted above are why acoustic inspection is becoming a key tool in the semiconductor wafer and package inspection toolbox. Semiconductor devices are becoming more complex, increasing their value throughout the manufacturing process. This creates a need for a 100% inspection at all stages. Options like optical, infrared and X-ray are important methods to help ensure package reliability, however, advancements in acoustic imaging are changing inspection capabilities.

Challenges with packaging advancements and current inspection solutions

Wafer defects tend to be small—for example, a small 10µm delamination between two layers meant to be bonded together. If there is a small defect anywhere in the chip as it gets processed, this can often lead to a bubbling or blistering effect that can expand under grinding or polishing. Certain defects that escape the inspection process can be exposed to environments where they can grow over time, necessitating the need for a more intensive inspection process. When these small defects escape the production process, they can lead to expensive field failures (**Figure 1**).

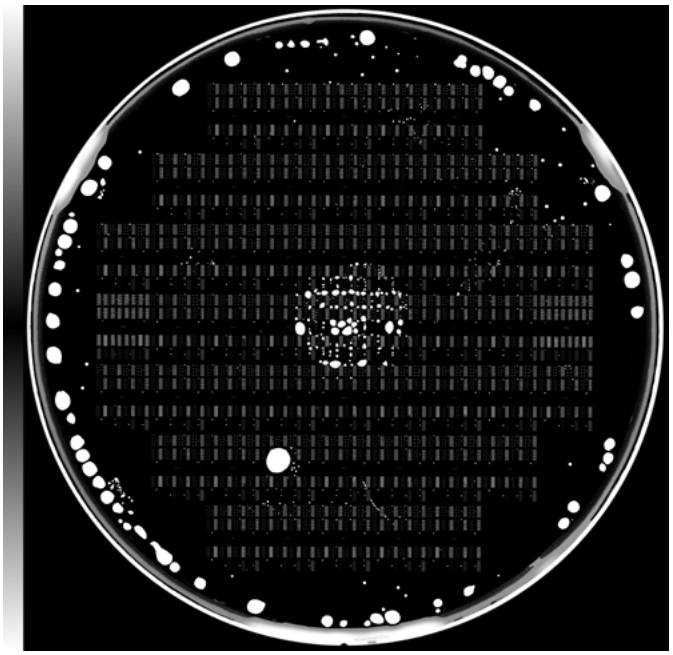

Figure 1: Wafer defect example.

In addition to the considerations above, the advanced packaging market continues to grow significantly. Whether it's system-in package (SiP), fan-out (FO), wafer-level package (WLP), or heterogeneous packaging, the market is driving manufacturers to put as much as possible into the smallest form factor. With that complexity comes the potential introduction for defects at different stages of manufacturing. As such, there's a high cost of failure, necessitating a more advanced inspection of these devices. The sooner inspection happens in these earlier stages, the better. Advanced acoustic microimaging can help to screen out defects to improve yield and guard against further processing of a known defect.

Historically, a wafer was essentially two dimensions (X and Y) and one layer of metallization for the chip. Advanced packaging is now moving into the third dimension. An example of this is stacking devices, so each layer features a bond. It could be as simple as silicon-on-insulator (SOI), which is just two bonded wafers. Or it could be the more complex high-bandwidth memory (HBM) devices with multiple layers that can include the stacked die and through-silicon vias (TSVs). Advanced acoustic imaging is needed to look at these different applications and determine if there are defects, then map them out and provide that information to the customer.

Because of the complexity, variation, and miniaturization of advanced packaging, there is pressure to increase inspection, particularly at high resolution, to effectively detect defects. Manufacturers are seeking to deliver higher throughput, with a requirement to scan more samples during inspection.

As many manufacturers know, an X-ray based solution is good at seeing variation in density because of a smaller resolution—X-rays can easily spot a solder ball, wire bond, or a via—which is why it is ideal for sampling. However, an X-ray cannot see a thin delamination or crack, because that would be too thin for it to detect. Optical solutions are best for surface-level defects but are incapable of looking inside a wafer the way an X-ray or acoustic solution can. **Figure 2** shows examples of all three inspection solutions. Meanwhile, infrared options may struggle with highly-doped wafers.

An acoustic solution excels because of the use of ultrasound. Typically, an acoustic solution should operate anywhere from 15MHz up to about 300MHz to effectively look inside objects, detect defects, and characterize material properties and changes in semiconductor devices. Additionally, ultrasound will not travel through air. If an air gap is hit during inspection, it offers 100% reflection by sending back a big signal. Even down to hundreds

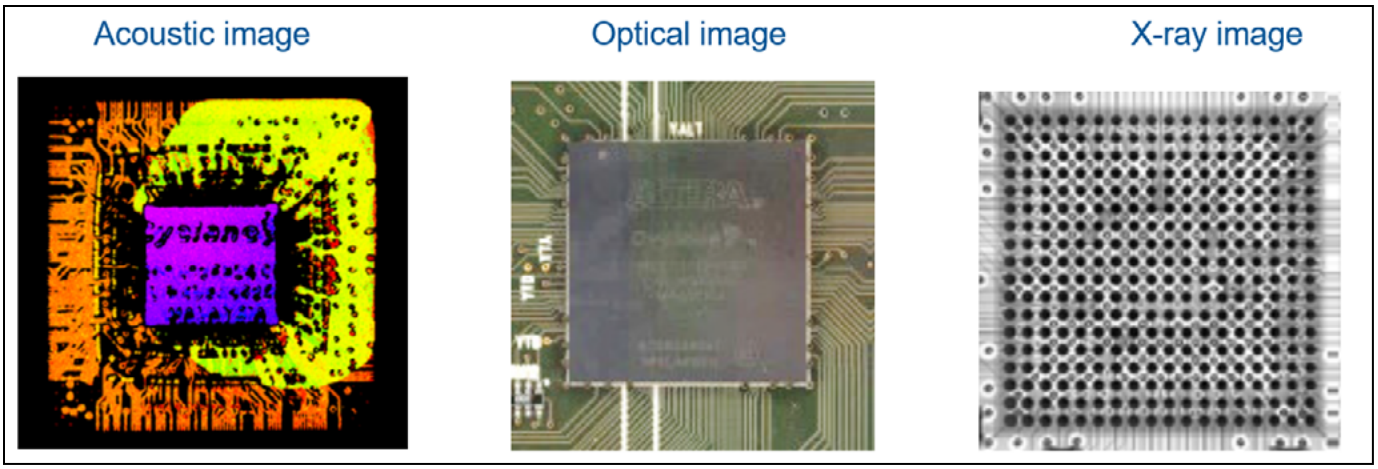

Figure 2: Acoustic (AMI)/optical/X-ray inspection examples.

of angstroms, the thickness of an air gap is enough to stop the ultrasound, making it a very good technique for bond evaluation.

There are challenges with traditional scanning methods in acoustic inspection stemming from water use. Because the transducer scans samples in a tank or bath, water may enter the sample through cracks and defects (**Figure** 3). To ensure the wafer's integrity, and to safeguard it from particles and reduce drying time, water must be filtered and constantly changed. Additionally, separation can occur when bonded wafers don't properly anneal before scanning, which can lead to separation.

Acoustic technology that improves the inspection process

Given the inspection complications noted above, we set out to create an acoustic micro-imaging machine implementing a technology that enhances and accelerates inspection efforts. The SpinSAM™ acoustic micro-imaging (AMI) inspection system features proprietary technology that combines breakthrough scanning capability with defect capture and image quality to enhance productivity and accuracy for 100% semiconductor inspection geared to high-end devices. The system offers high throughput and sensitivity, enabling precise defect detection in wafer-based assemblies using waterfall technology to limit exposure, as well as an advanced, spin scan method. However, it is not meant to be a competitor to optical, infrared and X-ray solutions; rather, it complements the inspection machines already in a high-volume manufacturing (HVM) environments so it can be effectively deployed according to application and needs.

Because of the complexity of wafer-level and advanced packaging, and the wafers themselves, the cost of field failures is extremely high, driving the need for increased inspection. The SpinSAM™ offers 100% inspection on these samples—for example, identifying defects at the various layers in a stacked die, whether 8-stack or 16-stack (**Figure 4**). Some applications require the use of a carrier wafer and temporarily bond it to a processed wafer. The carrier wafer acts like a substrate for the actual wafer. If the temporary bond is ineffective, it could potentially induce defects into the sample during the chemical mechanical polishing (CMP) process. Our solution can inspect that temporary bond to expose defects before it moves forward in the production process.

Benefits of ultrasound technology include its nondestructiveness, its sensitive technique for bond evaluation, and its ability to penetrate most materials. At a lower frequency, such as 15MHz,

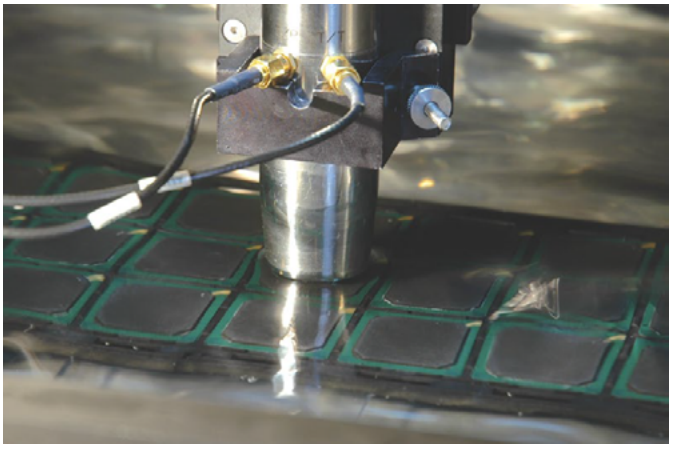

Figure 3: Acoustic scanning in bath example.

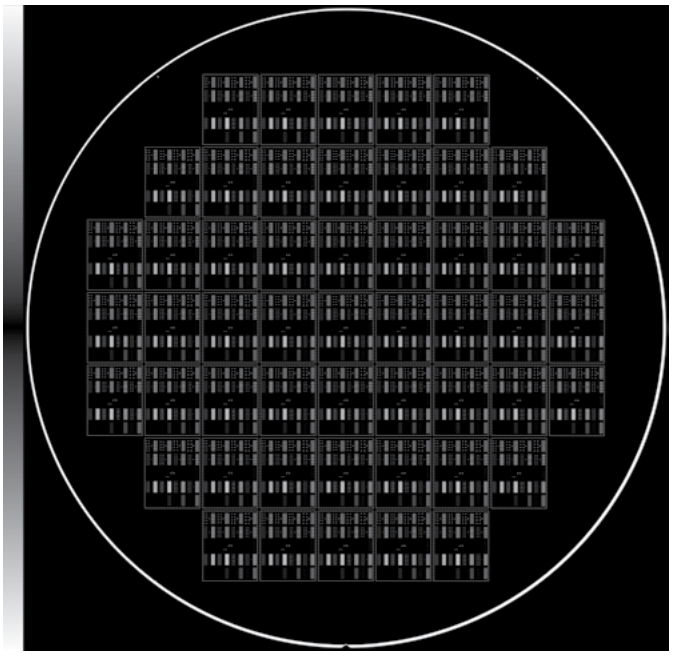

Figure 4: Wafer-level inspection example using SpinSAM™ technology.

ultrasound will have more penetration, meaning it can go through a thicker sample with a resolution of approximately 130µm. A higher frequency will result in a better resolution down to 9µm for 300MHz, but the inspection will have less penetration. The balance of penetration and resolution is dependent on the application.

Because ultrasound doesn't travel through air, something is needed to couple the ultrasound to the sample. Gel is used in a medical environment, acting as a surface contact-type transducer. For semiconductor applications, however, the sample cannot be touched in acoustic imaging, so deionized water is used for its safety and availability. The sample can be placed in a water bath such as a water tank, or a waterfall, which is the approach used by our solution. A specialized transducer water coupling decreases the amount of water that's hitting the surface of the wafer (**Figure 5**). Instead of immersing the sample, water is cascaded or jetted specifically in the area being inspected to minimize exposure. For example, defects exposed to the outside edge could lead to water contamination inside the sample. A waterfall approach helps to minimize that chance.

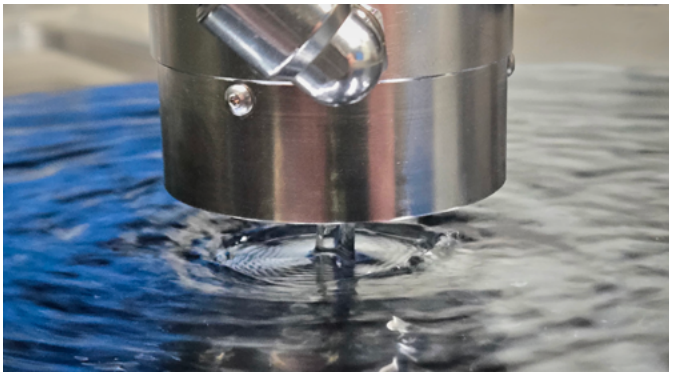

Figure 5: SpinSAM™ transducer technology: Inspecting a wafer.

The main driver behind creating our advanced technology was the opportunity to optimize throughput, then taking it a step further by focusing on wafers per hour, and per footprint to maximize the throughput in the smallest footprint. Our solution functions at 100µm resolution and about 41 wafers per hour, with the capability to go down to a 10µm resolution, besting the capabilities of a traditional raster scan (**Figure 6**).

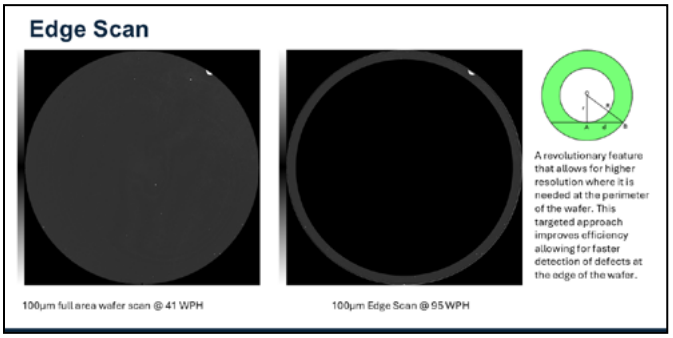

Figure 6: Wafer edge inspection example.

Wafer edge inspection is valuable for manufacturers. The coefficient of thermal expansion during the bonding process is more extreme at the edges, which is where manufacturers are likely to find more defects. However, the center of the wafer is unlikely to see as many defects as it does not experience the same stresses as at the edge of the wafer. The SpinSAM™ is well suited to doing a lower resolution scan in the center, then maximize the resolution towards the edge to see edge defects.

Finding defects early in the process can be crucial for most manufacturers. As such, this technology isn't meant for final package inspection. For example, if there's a thousand die on the wafer, manufacturers can use the acoustic microscope to pick out those defect parts and reject them—which saves time, effort and money during final assembly.

The growth of acoustic imaging technologies

Traditionally, the type of scanning that has been done for acoustic microscopes is an XY raster scan, not unlike an inkjet printer scanning back and forth over paper as it prints. In a traditional raster scan system a transducer generates the ultrasound, moves to the left and stops, then accelerates to the right and stops, going back and forth to provide a scan. It generates a square scan area for a circular wafer, which means areas outside the wafer at the corners are unnecessarily scanned. The time lost during turnaround adds up over time, using more energy to accelerate and decelerate. Additionally, raster scanning tends to feature a gantry mechanism over the wafer, which results in additional moving parts on top of the wafer. This can be detrimental for particle generation because of the bearings, belts or motors moving over the wafer's surface, which can lead to particle contamination on the wafer surface.

Our solution improves upon the raster scan process with new spinning technology (**Figure 7**). With this acoustic imaging system, a rotational or spinning scan starts in the middle, then moves to the edge as the wafer spins, this provides a more efficient inspection, maximizing the data acquisition time to just the area of the wafer. There is only one transducer per wafer inspection, which means that there is no image stitching, or one transducer per wafer for a uniform image. This technology allows for minimal movement over the surface of the wafer with no mechanical scanner above the wafer.

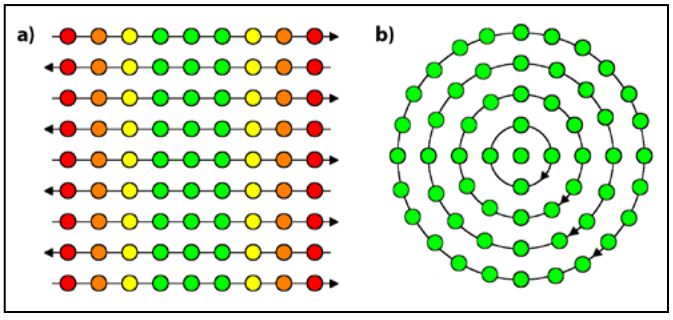

Figure 7: a) Raster scanning vs. the b) SpinSAM™ scanning method.

The spinning scan is also capable of doing either a perimeter scan, or an edge scan. Instead of scanning the whole wafer, manufacturers can scan a portion of the outer edge, which would be impossible with a traditional raster scan. This is especially important for manufacturers who find most defects at the edge of the wafer. A partial scan allows

for selectable parameters to see how much of the edge to scan. There's no time loss because the scan is continuous, making it more energy efficient in the process.

With our new technology, the frequency of the scans has improved to a higher frequency. Generally, use of a lower frequency results in a lower resolution, however it can go through more material. A higher frequency results in a higher resolution, but it can't go through as much material. Our solution has an improved transducer design along with an optimized frequency and lens shape that, in turn, optimizes the focal spot so it can get that much higher resolution (**Figure 8**). Improvements have also been made to the radio-frequency (RF) chain that generates the ultrasound, thereby maximizing the output of the signal while minimizing the signal to noise ratio.

The use of acoustic inspection allows end users to isolate layers within the wafer sample. So as the ultrasound travels, it travels in time so manufacturers can pick regions of time to observe. If they see a trend of defects occurring at the base layer or the deepest layer, the system allows for the opportunity to go back in the process to discover what's causing these defects. Perhaps it only happens in one layer, or never in the upper layers—just the lower layers. Maybe they have unintended particle generation that puts particles at the edge of the wafer during that process and those particles then cause the defects. The acoustic imaging technology deployed by the SpinSAM™ can empower manufacturers to maximize their early processes to minimize defects in the future.

The future of inspection tech

The advancement of acoustic imaging is constantly changing, with the capability for upgrades that can be implemented in current machines. Our solution features four scanners with four scan stages to maximize the throughput. For example, the system includes an equipment front-end module (EFEM) that loads wafers into the four scanners. Because there are four transducers used during the inspection, slight variation in the output can occur across the four scanners. Global tool matching serves as a matching network, looking at the signal of all four transducers using a reference wafer to calibrate each of the four scanners. That reference measurement is then used to harmonize the output signal on each scanner to ensure amplitude signals are consistent. This can be useful for manufacturers with labs in different countries. If a manufacturer has a system in Singapore running a wafer and that same system also in Taiwan running a same wafer, manufacturers can achieve the same recipe, system, wafer, and result. This ensures multinational companies can use the same data set or the same parameters and not have to change or modify depending on the system.

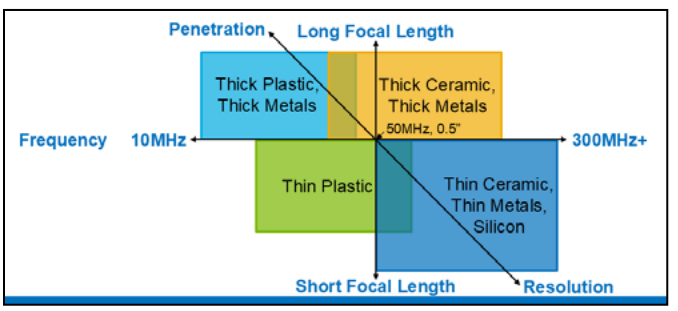

Figure 8: Transducer technology.

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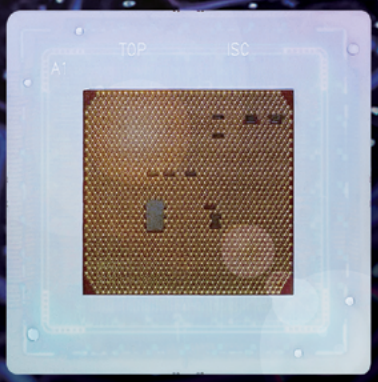

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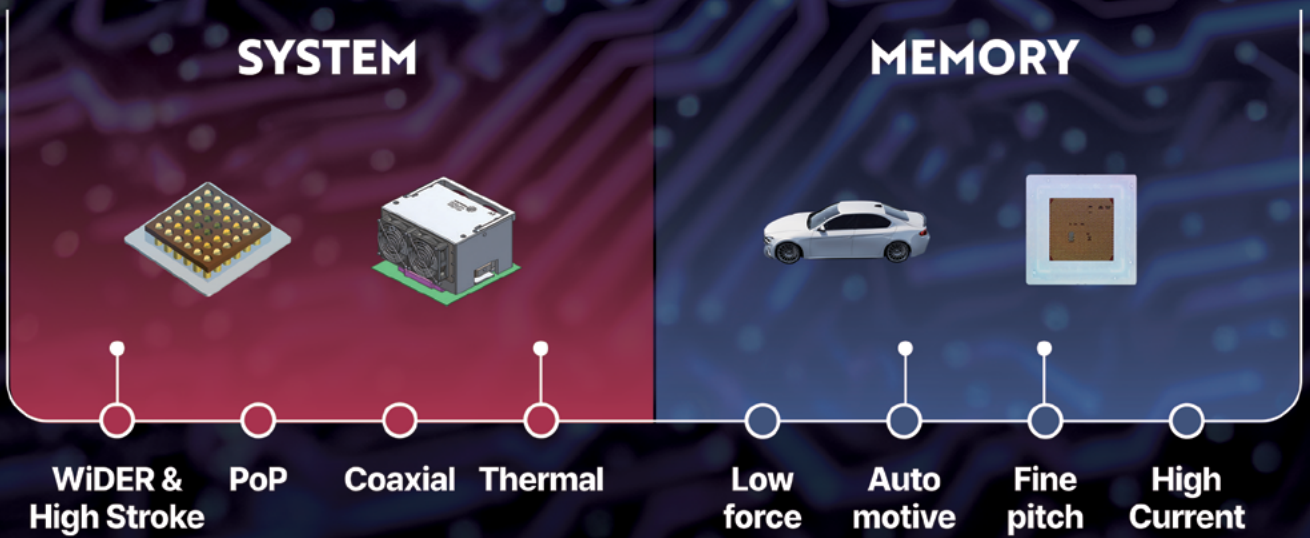


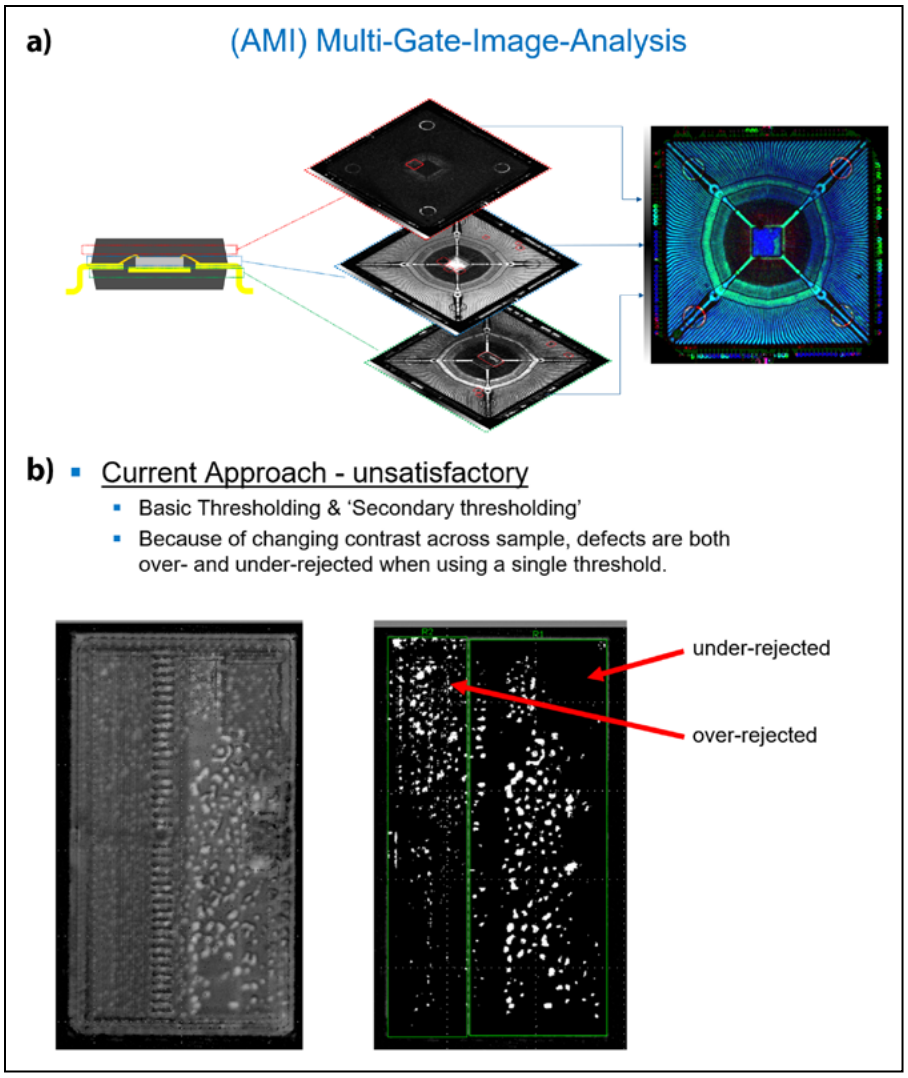


Figure 9: a) AMI: Multi-gate-image-analysis; b) Image analysis and accurate defect capture.

Maintenance downtime can also be challenging for manufacturers. Systems that feature modular design can mitigate downtime issues related with regular or extended maintenance. In the case of our solution, each of the previously mentioned scanners is actually a scan module. There's also another RF module that generates the ultrasound. With a modular design, manufacturers can take one scanner offline to do preventive maintenance or servicing, but the remaining three scanners will continue to run. With traditional preventive maintenance, the whole machine would go out of commission, causing manufacturers to lose 100% of their throughput. A modular design makes for easier service while minimizing system downtime.

The SpinSAM™'s modularity also applies to the system's scanning capabilities. Whereas most systems rely on multiple transducers to scan a single wafer, this system relies on independent scanners that allow for one wafer to be scanned at 100µm, and another to be scanned at only 50µm, with the capability to scan up to four wafers at the same time.

Machine learning (ML) and artificial intelligence (AI) are also being developed to integrate in advanced acoustic imaging systems, while also informing inspection and metrology systems. Our system has already introduced multi-gate image analysis, or MGIA (**Figure 9**). There are applications where, if a manufacturer sets a threshold, the system will either reject too much, or won't detect the defect. But with AI and ML, the system can be taught what constitutes a defect. Then, over time with machine learning, manufacturers can build up a robust model to isolate defects without overkill or underkill. The MGIA is multi-gate—meaning multiple images. This offers the capability to take three images, stack them together, and analyze them as a whole package. This has been useful for the more complex structures that are common for today's manufacturers.

Lastly, another common issue for manufacturers is wafer warpage. Current solutions can allow for ±1mm of warpage using a vacuum stage to hold the wafer. Warped wafer handling can be addressed by changing the focus of the transducer to accommodate for the variation of the warpage of the wafer. The implementation of mechanical- or software-based solutions can minimize the effect of the warpage.

Summary

As the semiconductor space continues to expand and the needs of acoustic inspection imaging advance with that growth, the technology will continue to be explored to exceed expectations while streamlining the inspection process. While the goal is always to enhance productivity and processes while improving yields for today, there is always an eye to the future to ensure manufacturers are always on the cutting edge and growing with the times while maximizing the cost of ownership and quality standards.

Biography

Bryan Schackmuth is Senior Product Line Manager and the Senior Product Line Manager for Acoustic Technologies at Nordson Test & Inspection, Elk Grove Village, IL He oversees the development and implementation of advanced acoustic inspection systems tailored for the semiconductor market. Email Bryan.Schackmuth@nordson.com

Effect of a through-glass via (TGV) substrate on solder joint reliability

By John H. Lau [Unimicron Technology Corporation]

In this study, the effect of a glass-core substrate on solder joint reliability when used on a printed circuit board (PCB) is investigated. The advantages and disadvantages of a glass-core substrate vs. an organic-core substrate, through-glass vias (TGVs), and redistribution layers (RDLs), will be briefly mentioned first.

Advantages and disadvantages of glass packaging

The advantages of glass-core packaging compared with organic-core packaging are: a) Ultra-high flatness for improved depth of focus for lithography; b) Dimensional stability needed for extremely tight layer-to- layer interconnect overlay; c) Higher interconnect density; d) Higher mechanical stability for ultra-large form-factor packages with high assembly yield; e) Improved flexibility in setting design rules for power delivery and signal routing; f) Better power delivery solutions while achieving high-speed signaling; g) Higher tolerance for higher temperatures; and h) Higher ability to seamlessly integrate optical interconnects.

The disadvantages of glass-core packaging compared with organic-core packaging are: a) Higher material cost; b) Higher processing (production) cost; c) Higher yield loss; d) Fragility (easy to break); e) Handling; f) Difficulty in making TGVs; g) Glass (softens) at high temperatures; and h) Special and expensive equipment.

Glass-core substrate vs. glass-core interposer

Some of the glass packaging is shown in **Figure 1**. It can be seen that the organic-core build-up package substrate (**Figure 1a**) has been replaced by the glass-core build-up package substrate (**Figure 1b**). Also, the traditional through-silicon via (TSV) interposer [1] has been replaced with the TGV interposer (**Figure 1c**)—a 2.5D IC integration. It can be seen that a TGV glass-core interposer that is supporting chips is also supported by an organic-core substrate as shown in **Figure 1c**. Finally, a chip is embedded in the glass-core build-up package substrate—i.e., a 3D IC integration (**Figure 1d**).

Through-glass vias (TGVs) and RDLs

The fabrication process of a TGV is very different from that of a TSV. Most of the TSVs are fabricated by the deep reactive-ion etching (DRIE) process [2]. However, today, most of the TGVs

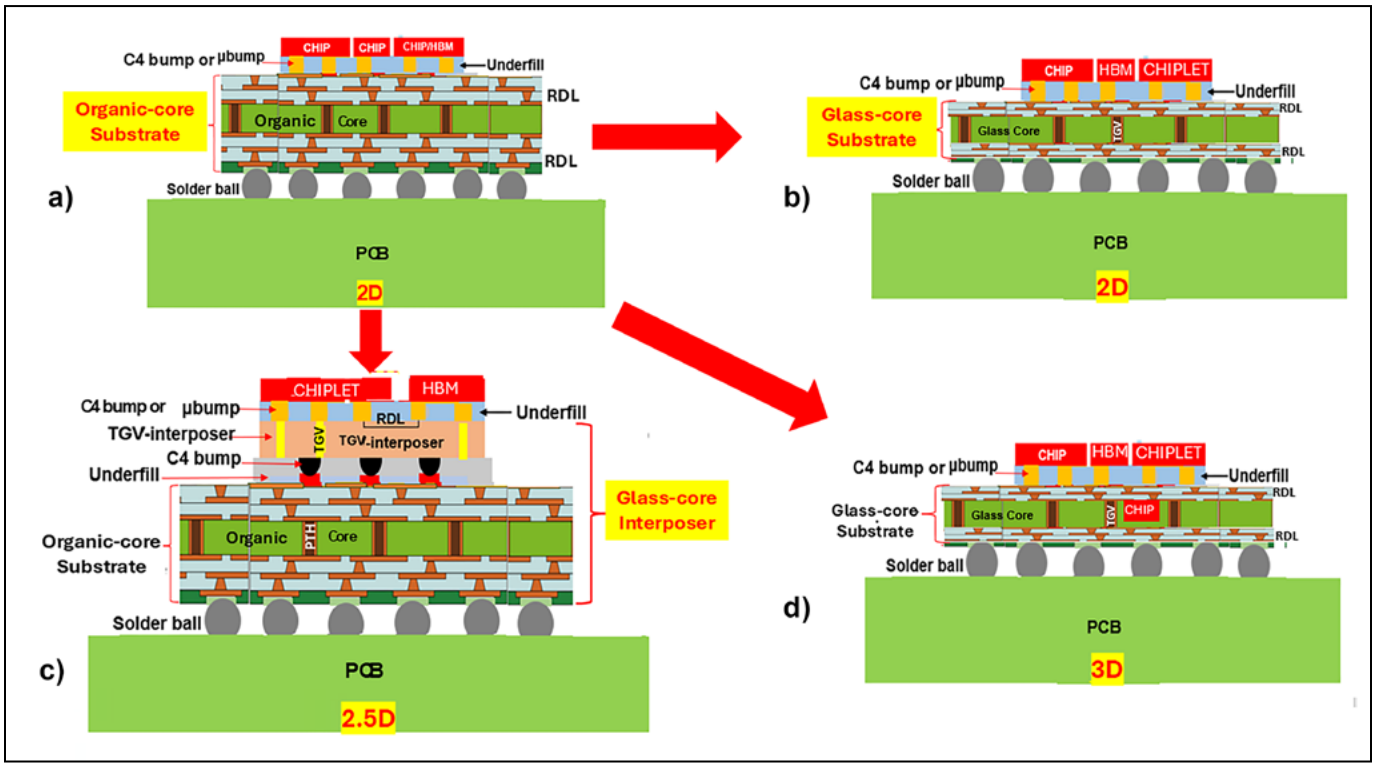
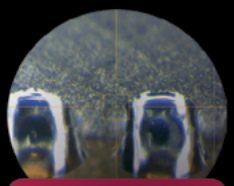


Figure 1: a) Organic-core substrate; b) Glass-core substrate; c) Glass-core interposer; and c) 3D IC integration with glass-core substrate.

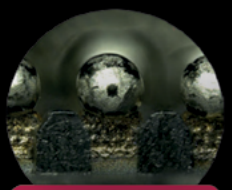
BALL PLACEMENT & LASER SOLDERING

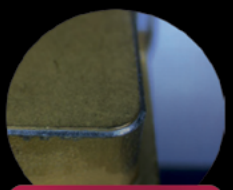

3D-Soldering

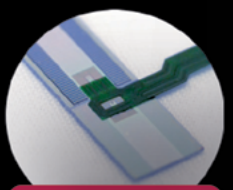

Solder Stacking


Wire Soldering


BGA Soldering


Pre-Soldering of SMD Connector Elements


Lid Sealing for Connectors & IR-Sensors

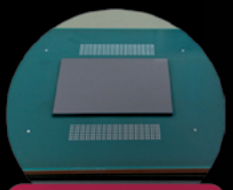

Flex to Chip Soldering

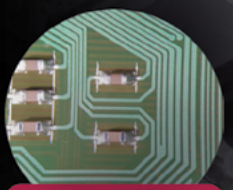

Through Hole Soldering

LASER ASSISTED BONDING (LAB, LCB, LAR)


3D Multi Layer Stacked Packaging


Optoelectronic Device Assembly


CPU on Interposer Assembly

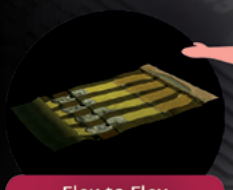

SMD Capacitor Assembly

SOLDER & CHIP REPAIR


BGA Rework


Interconnects of Camera Module


BGA Package Assembly onto Substrate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are fabricated by laser drilling such as the laser-induced deep etching (LIDE) process developed by LPKF Laser & Electronics AG in 2017 [3-6]. The most commonly used glass materials are the SCHOTT AF 32 alkali-free flat glass, and the CORNING HPFS 7980 high-purity non-crystalline fused-silica glass. Both materials have low coefficients of thermal expansion (CTE) that are close to that of silicon.

The process flow for fabricating the TGV is shown in **Figure 2a**. It can be seen that the vias are formed by high-speed laser, and the modified area of the glass is removed by anisotropic wet chemical etching, e.g., hydrofluoric acid (HF) or sodium hydroxide (NaOH). **Figure 2b** shows an image of a typical TGV. It can be seen that there is a taper angle on the TGV. This taper is due to the rate of the circulation and temperature of the etching solution, and the concentration difference of the etching solution. These process attributes result in making the outer ionizer move inward and be replenished as shown in **Figure 2c**. The higher the etching rate, the larger the taper angle. It is followed by the metallization of the seed layer, which can be materials such as Ti/Cu, electroless Cu, etc., as shown in **Figure 3a**. Then, electroplated Cu is used to fill the via as shown in **Figure 3b**. **Figure 3c** shows an image of Cu-filled TGVs. The process flow for fabricating the RDLs (build-up layers) of the glass core is very similar to the process flow used for RDLs of the TSV interposer. For L/S≥2µm, the dielectric materials are either a photo-imageable dielectric (PID), or an Ajinomoto build-up film (ABF); and for L/S<2µm, the dielectric material is SiO_2. For L/S≥10/15µm, the dielectric material can be resin. **Figure 4** shows the scanning electron microscope (SEM) images of the Cu-filled TGV with RDLs (build-up layers).

Motivation

So far, reliability issues using glass-core substrates have not been sufficiently discussed in the literature. In this study, the solder joint reliability when a glass-core substrate is used is presented. **Figure 5** shows the structures under consideration. **Figure 5a** is for a flip-chip device on an organic-core substrate, while **Figure 5b** is for a flip-chip device on a glass-core substrate. Today, in

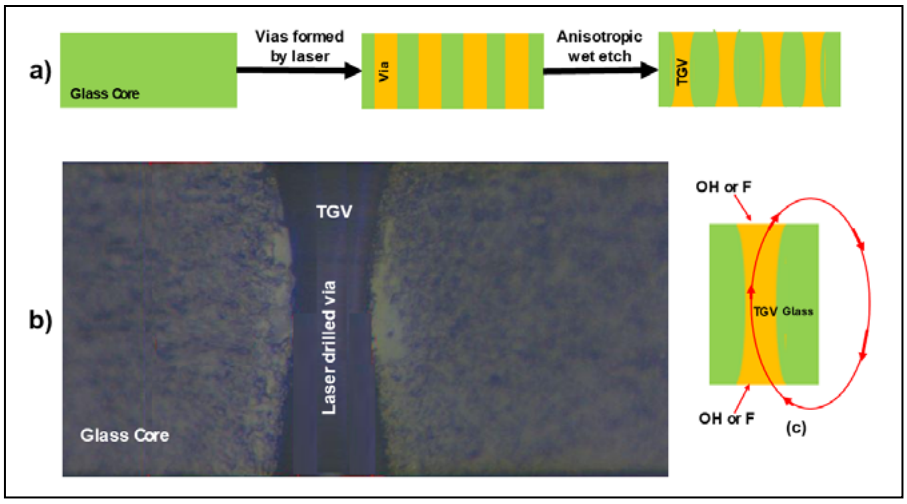

Figure 2: a) TGV process flow; b) SEM image of a TGV; and c) Etch solution mechanism.

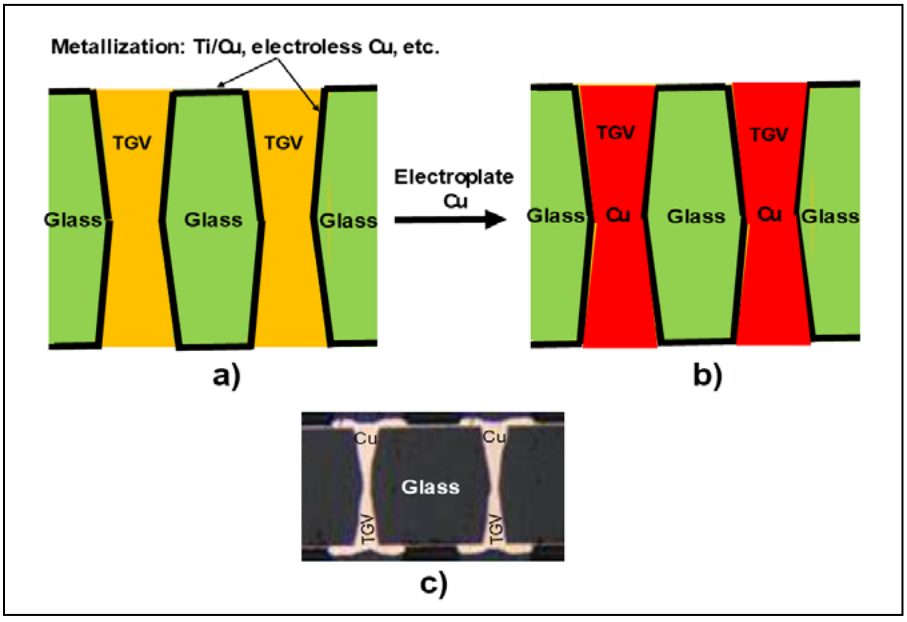

Figure 3: a) TGV sidewall metallization; b) Cu plating; and c) An image of Cu-filled TGV.

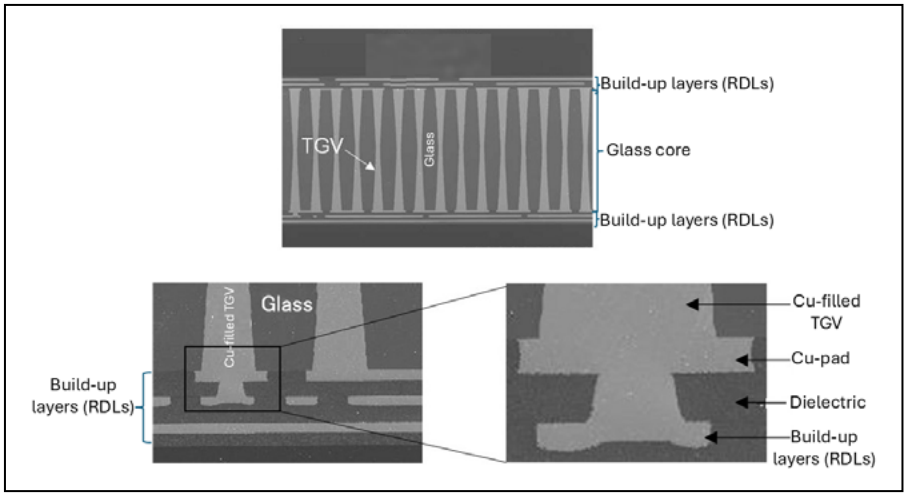

Figure 4: SEM image of a glass-core substrate with TGV and RDLs (build-up layers).

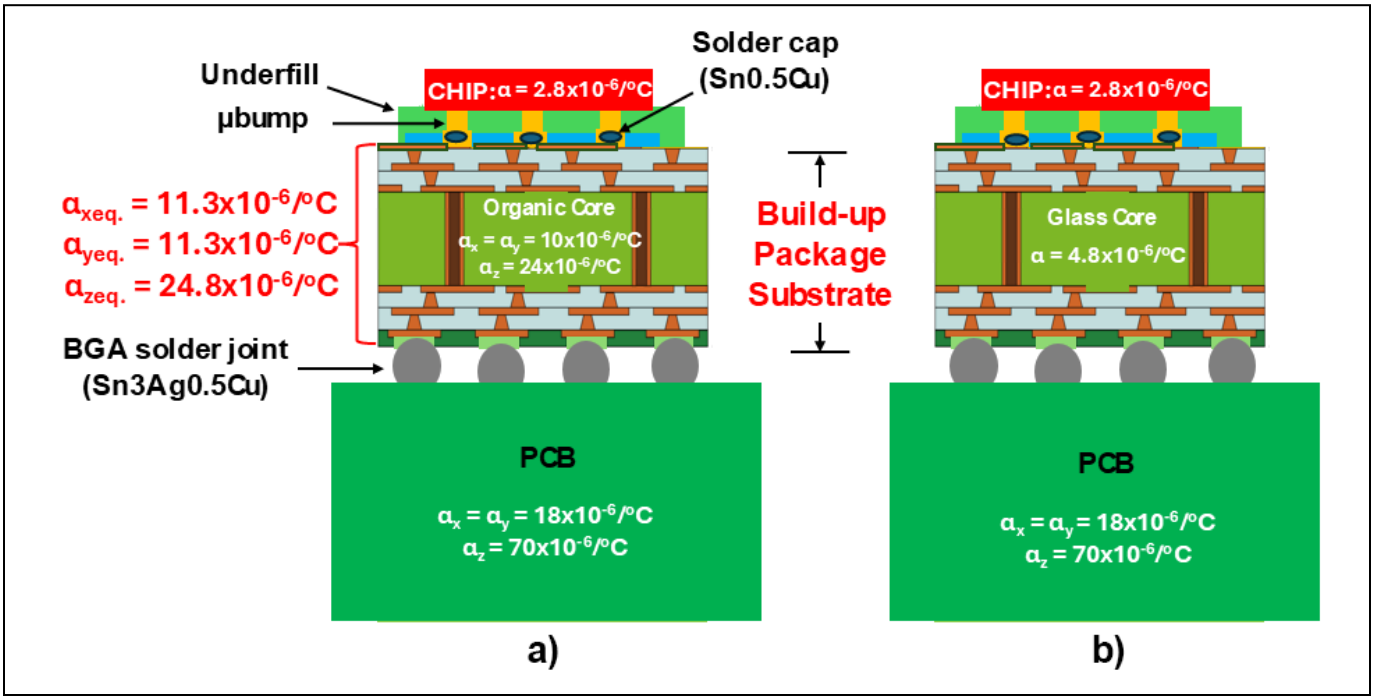

Figure 5: a) Flip-chip on an organic-core substrate; and b) Flip-chip on a glass-core substrate.

order to make the µbump solder joint reliable between the chip and the build-up package substrate, the coefficient of thermal expansion (CTE) of the glass-core substrate is made to be as close as possible to that of the Si chip. In this case, the thermal expansion mismatch between the glass-core build-up package substrate and the PCB is increased, and the ball grid array (BGA) solder joint reliability is questionable! The objective of this study is to point out that the CTE of the glass core should not be close to that of the silicon chip ($2.8x^{-6}$/°C), but rather to that of the PCB ($18.5x^{-6}$/°C).

The structure

In this study, the solder cap of the µbump is made of Sn0.7Cu (melting point = 227°C) and the solder of the BGA solder joint is made of Sn3Ag0.5Cu (or SAC, and the melting point = 217°C). Both solders obey the Anand constitutive model [7], i.e., the thermal-fatigue reliability of the solder joints was examined using a nonlinear model based on temperature, which was corroborated by a time-dependent finite element analysis.

Figure 6 schematically shows the structures under consideration. The silicon chip (10mm × 10mm × 350µm) is supported by a build-up package

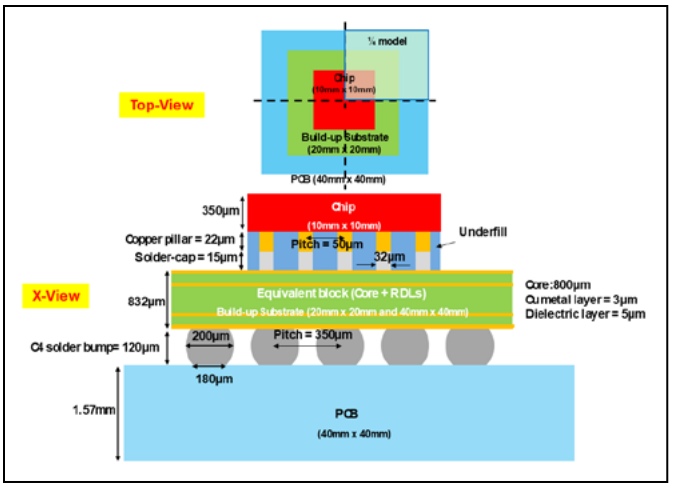

Figure 6: Top view and cross-section view of the structure.

substrate (20mm × 20mm × 832µm), which is fabricated by using a conventional material such as the organic core (800µm-thick), and the new glass core (800µm-thick) material. There are two build-up layers on the core's top and bottom sides that are fabricated by a PID for the dielectric layer (5µm-thick) and electrochemical deposition (ECD) Cu for the metal layer (3µm-thick).

Because of the double symmetries of the structure shown in **Figures 5** and **6**, only a quarter of the structure is modeled. **Figure 7** shows the chip, package substrate, PCB, µbumps and BGA solder joints. Finer meshes are used for the critical locations (higher stress/strain areas) such as corner µbumps connecting the chip and the build-up package substrate, and the corner BGA solder joints connecting the build-up package substrate and the PCB.

Because the focus of the present study is on the solder joint reliability, in order to simplify the modeling and save the computing time, the organic and glass build-up package substrates are modeled as an equivalent block. For both structures, the number of elements, the distribution of mesh sizes, and the modeling are the same, except for the effective material properties of the equivalent block.

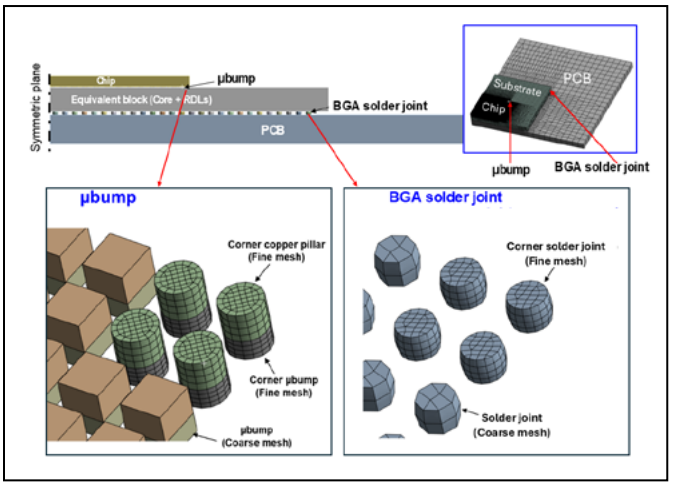

Figure 7: Finite element modeling of the structure.

Material properties

Table 1 shows the material properties for modeling. All the materials are assumed to be constant except solder (Sn3Ag0.5Cu), which is time and temperature dependent. Also, the solders, Sn3Ag0.5Cu and Sn0.7Cu, obey the Anand viscoplasticity constitutive equation [7]. There is a total of nine (9) constants (parameters) of the Anand equation (model), namely A, Q, ξ, m, n, h_0, α, and s_0. For Sn3Ag0.5Cu (SAC) and Sn0.7Cu [7], these constants are shown in **Table 2**.

Materials	Young's modulus (GPa)	Poisson's ratio	CTE ($10x^{-6}$/°C)
Silicon	131	0.278	2.8
µbump (Sn0.7Cu)	30	0.3	22
C4 bump (SAC305)	49 - 0.07T(°C)	0.3	21 + 0.017T(°C)
PCB	$E_x = E_y = 22$; $E_z = 10$	0.28	$\alpha_x = \alpha_y = 18$; $\alpha_z = 70$
Underfill	4.5	0.35	50
RDL (Dielectric)	2.0	0.3	60
RDL (Copper)	121	0.34	16.3
Glass core	72	0.29	4.8
Organic core	24	0.3	$\alpha_x = \alpha_y = 10$; $\alpha_z = 24$
Equivalent block (Glass core + RDLs)	71	0.29	6.3
Equivalent block (Organic core + RDLs)	25	0.3	$\alpha_x = \alpha_y = 11.3$; $\alpha_z = 24.8$

Table 1: Material properties.

Anand Model		
Parameters	**SAC305**	**Sn0.7Cu**
s_0 (Pa)	$18.07x10^6$	$33.8x10^6$
Q/R (K)	9096	5276
A (s^{-1})	3484	9875
ξ	4	2
m	0.2	0.176
h_0 (Pa)	$1.44x10^{11}$	$61987.3x10^{11}$
$\hat{s}$ (Pa)	$26.4x10^6$	$65.2x10^6$
n	0.01	0.003
a	1.9	1.03

Table 2: Anand model parameters for Sn0.7Cu and Sn3Ag0.5Cu.

Thermal boundary condition

The temperature boundary condition is shown in **Figure 8**. It can be seen that the temperatures are −40°C↔85°C, and the dwell-time at hot, dwell-time at cold, ramp-up time, and the ramp-down time are 15m each.

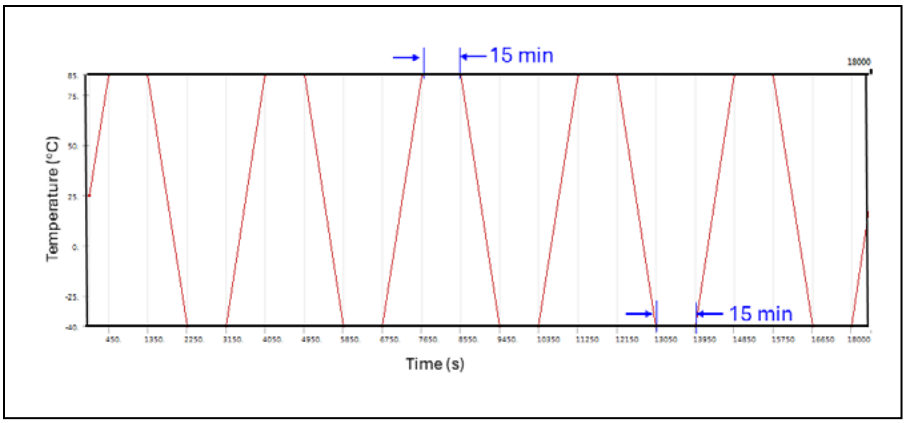

Figure 8: Temperature boundary condition.

Thermal-fatigue life of solder joints

As shown in [7], a simple thermal-fatigue life equation for the lead-free solder joints is given by

$$N_f = \Sigma_j \alpha_j \left[\frac{\Sigma_i \Delta W_i x V_i}{\Sigma_i V_i}\right]^{\beta_j}$$

where N_f is the thermal fatigue life of the solder joint, and α_j and β_j (which is a negative value) are constant to be determined by experiments such as the isothermal fatigue tests for a specific component/package and solder joint. ΔW_i is the accumulated inelastic strain energy density per cycle in the ith element determined from finite element simulations and V_i is the volume of that ith element. It can be seen that the larger the accumulated inelastic strain energy density per cycle the smaller (shorter) the thermal fatigue life of the solder joint.

Accumulated inelastic strain in µbump solder joints between the chip and substrate [8]

The accumulated equivalent inelastic strain contour distributions at the corner µbump solder joints of the flip-chip assembly comprising the organic-core and glass-core package substrates, respectively, at 450s (85°C), at 2250s (−40°C), and at 18000s (25°C), are shown in **Figures 9a** and **9b**. It can be seen that the maximum inelastic strain at the corner µbump solder joint, for both cases, occurs at a small local area, and the values are 2.2% at 450s (85°C), 6.6% at 2250s (−40°C), and 44.6% at 18000s (25°C) for the flip-chip on organic-core substrate. The values are 1.1% at 450s (85°C), 3.2% at 2250s (−40°C), and 21.8% at 18000s (25°C) for the flip-chip on glass-core substrate. Comparing these values for both package substrates, it can be seen that the maximum equivalent inelastic strain at the corner µbump with the glass-core substrate is smaller than that with the organic-core substrate.

Figures 10 shows the inelastic stain time-history in the corner µbump solder joint with the organic-core and glass-core substrates. It can be seen that the strain is smaller in the glass structure. This is because the thermal expansion mismatch between the glass-core substrate and the silicon chip is smaller than that between the organic-core substrate and the silicon chip.

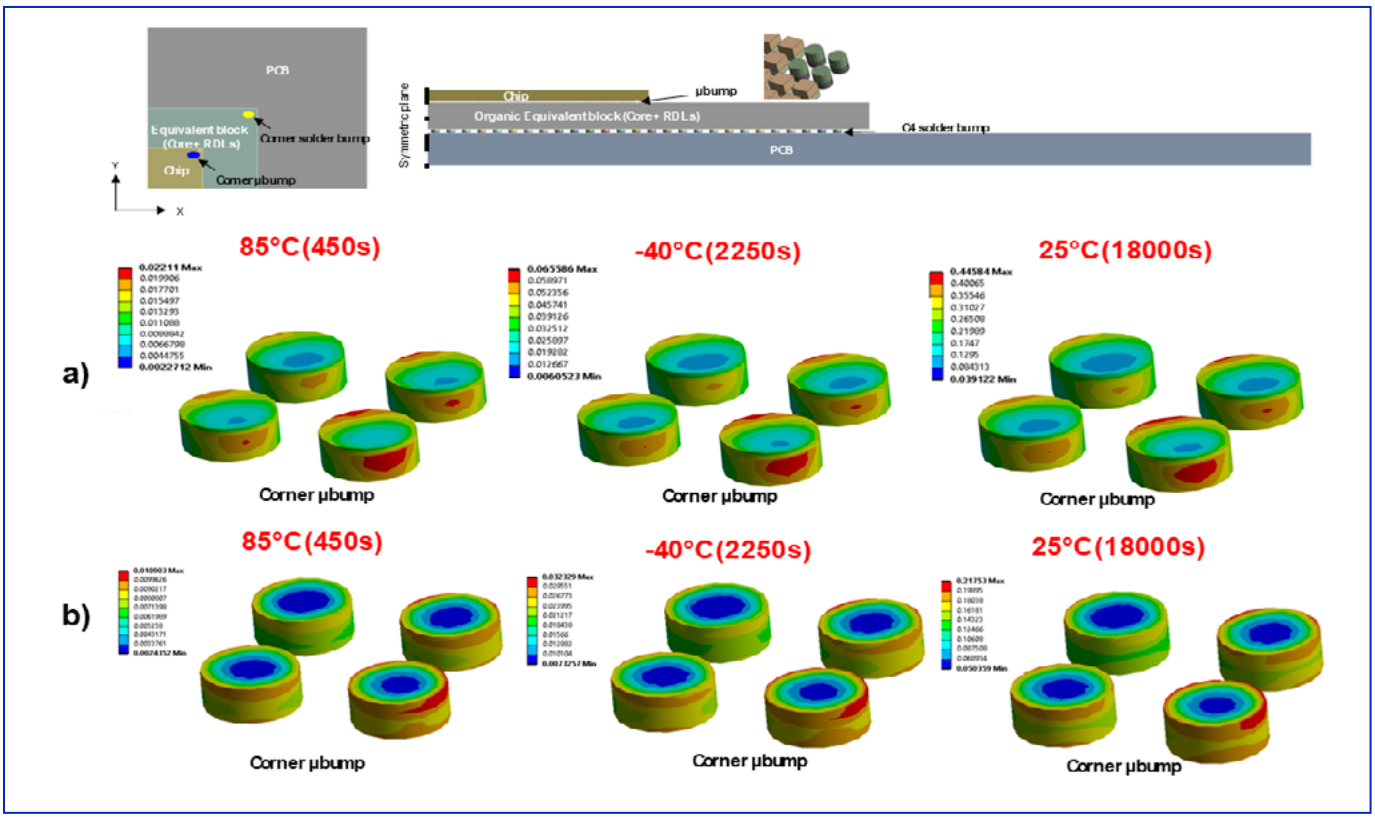

Figure 9: Maximum accumulated inelastic strain in a corner µbump solder joint of a structure with: a) An organic-core substrate; and b) A glass-core substrate.

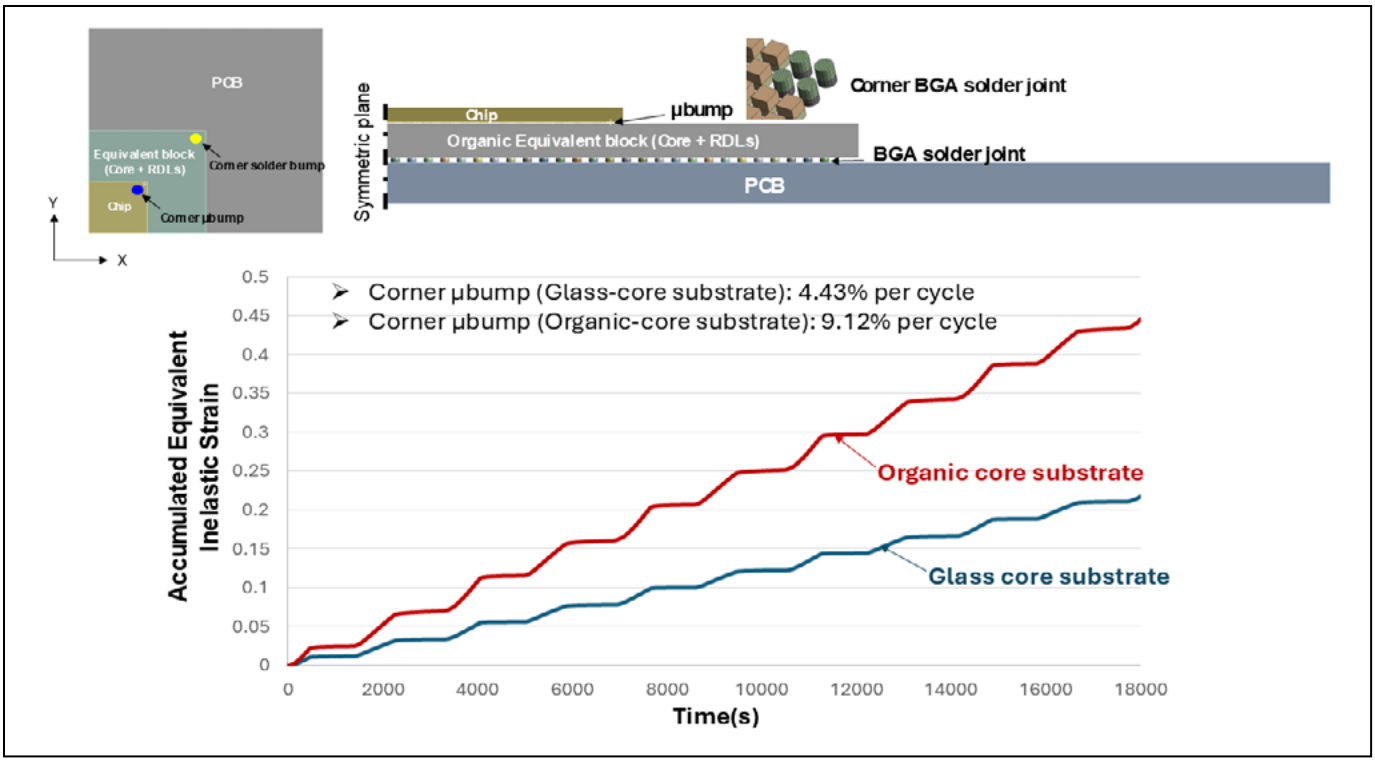

Figure 10: Maximum accumulated inelastic strain vs. time history in a corner µbump solder joint of structures with organic- and glass-core substrates.

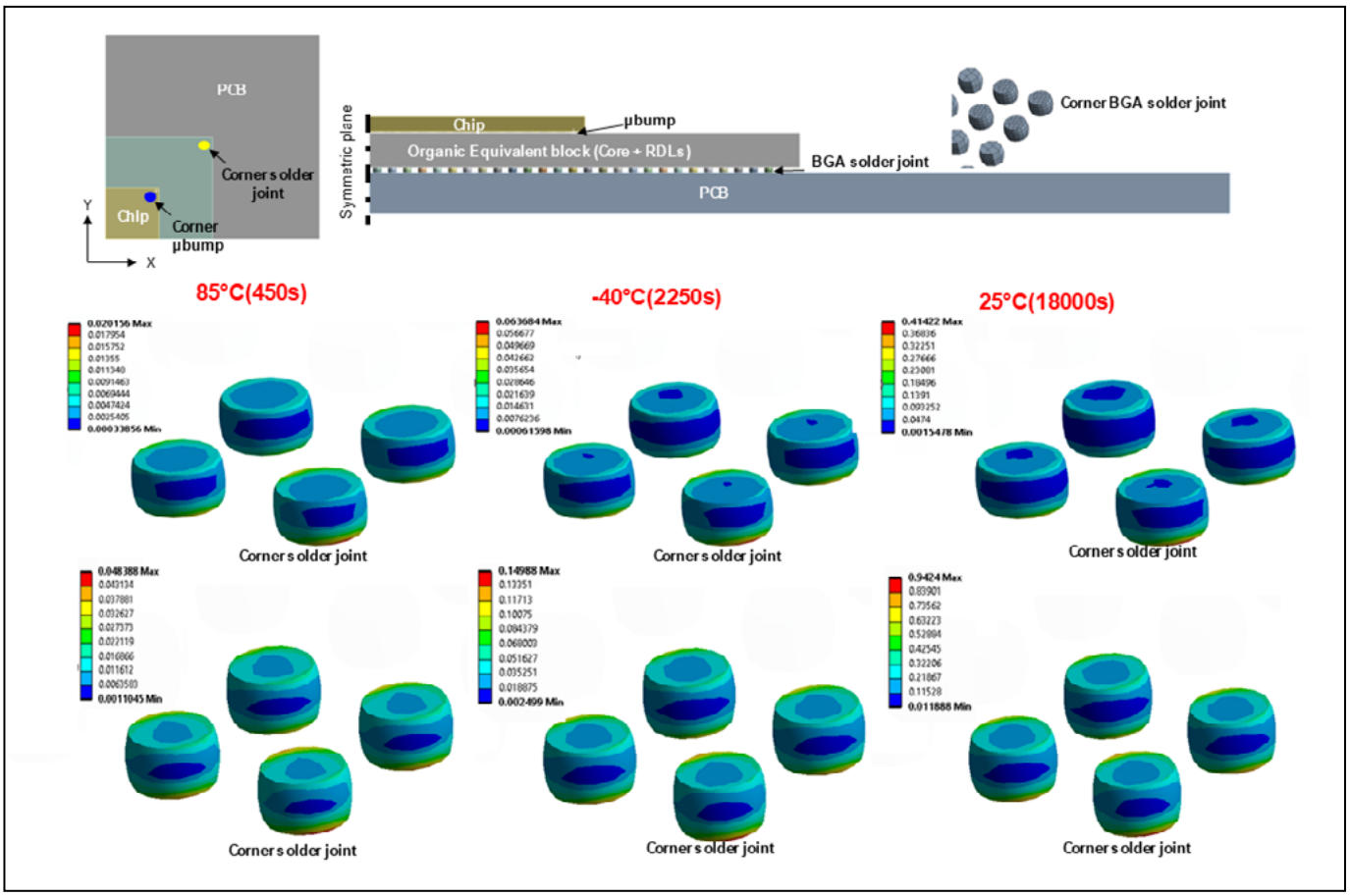

Figure 11: Maximum accumulated inelastic strain in a corner BGA solder joint for a structure with: a) An organic-core substrate; and b) A glass-core substrate.

Accumulated inelastic strain in BGA solder joints between the substrate and PCB [8]

Figure 11 shows the accumulated equivalent inelastic strain contour distributions at the corner BGA solder joint of the flip-chip assembly made of the organic-core and glass-core package substrates, respectively, at 450s (85°C), at 2250s (−40°C), and at 18000s (25°C). It can be seen that, for both substrates, the maximum inelastic strain at the BGA corner solder joint occurs at a small local area, and the values for organic-core substrate are 2.0% at 450s (85°C) and 6.4% at 2250s (−40°C), and 41.4% at 18000s (25°C), while for the glass-core substrate, the values are 4.8% at 450s (85°C),15.0% at 2250s (−40°C), and 94.2% at 18000s (25°C). Comparing these values, it can be seen that the maximum equivalent inelastic strain at the corner BGA solder joint with the glass-core substrate is larger than that with the organic-core substrate.

Figure 12 shows the maximum accumulated inelastic strain vs. time history for the corner BGA solder joint for structures made of the organic-core and glass-core substrates. It can be seen that the maximum accumulated inelastic strain in the corner BGA solder joint is larger with the glass-core substrate. This is because the thermal expansion mismatch between the glass-core substrate (α=6.3×10−6/°C) and the PCB ($\alpha_x=\alpha_y$=18×10−6/°C, α_z=70×10−6/°C) is larger than that between the organic-core substrate ($\alpha_x=\alpha_y$=11.3×10^{-6}/°C, α_z=24.8×10^{-6}/°C) and the PCB.

Summary

Some important results and recommendations are summarized as follows:

- The thermal-fatigue reliability of flip-chip µbump solder joints on glass-core build-up package substrates and BGA solder joints on a PCB has been investigated. For comparison purposes, the same structure with the conventional organic-core build-up package substrate has also been studied.
- The solder cap of the µbump is made of Sn0.7Cu and the BGA solder joint is made of Sn3Ag0.5Cu. Both solders obeyed the Anand viscoplasticity constitutive equation.
- The maximum accumulated equivalent inelastic strain in the µbump solder joint is smaller in the structure with the glass-core substrate than in the structure with the organic-core substrate. This is because the thermal expansion mismatch between the Si chip and the glass-core substrate is smaller than that between the Si chip and the organic-core substrate.
- The maximum accumulated equivalent inelastic strain in the BGA solder joint is more than two times larger in the structure with the glass-core substrate than in the structure with the organic-core substrate. This is because the thermal expansion mismatch between the glass-core substrate and the PCB is larger than that between the organic-core substrate and the PCB.
- In packaging under thermal conditions, underfill is usually

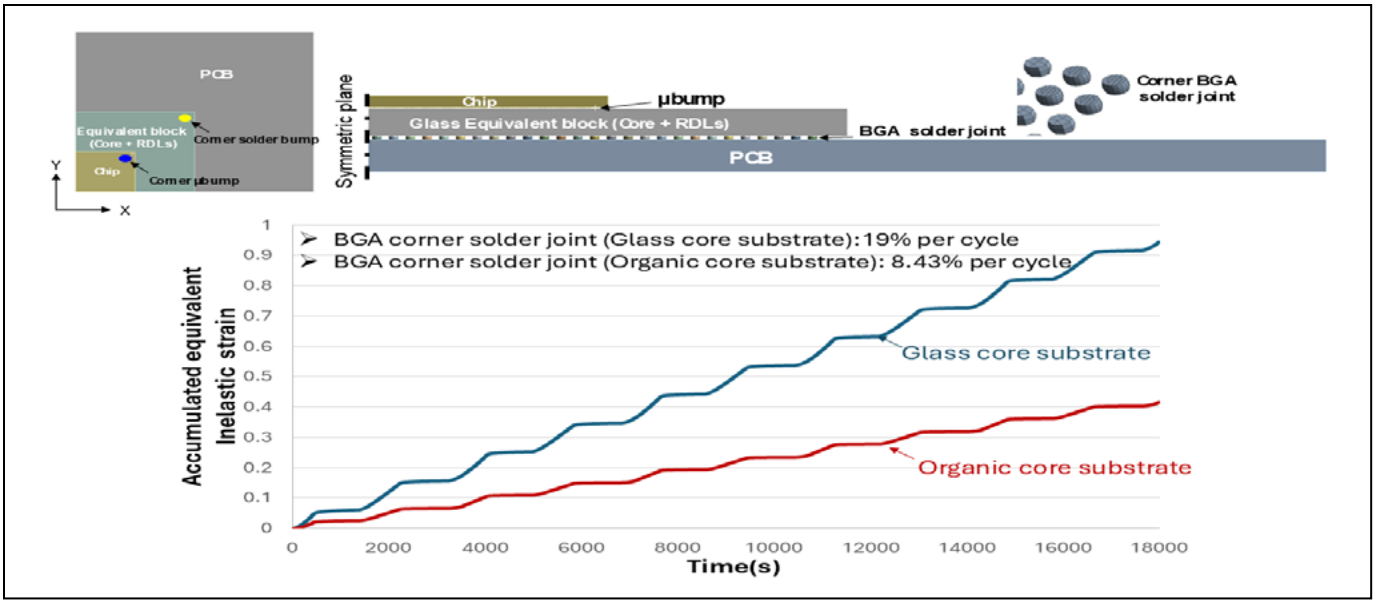

Figure 12: Maximum accumulated inelastic strain vs. time history in a corner BGA solder joint for structures with organic- and glass-core substrates.

needed for silicon chips on a package substrate to ensure the µbump solder joint reliability (**Figures 5**). However, underfill (because it is non-reworkable) is seldom used as a package substrate on a PCB. In order to have a reliable BGA solder joint, therefore, the thermal expansion mismatch between the package substrate and PCB should be as small as possible—especially for large package substrates. Unfortunately, today the glass package substrate is heading in the wrong direction. For example, the glass CTE is

getting closer to the silicon CTE (α=2.8×10^{-6}/°C) and farther away from the PCB CTE (α=18.5×10^{-6}/°C). When choosing the material properties, such as the CTE of a glass substrate, it is recommended that care be taken when considering the thermal expansion mismatch between the glass substrate and the PCB—especially for large glass substrates. As a matter of fact, the CTE of the glass substrate should be closer to the PCB CTE because there is underfill protection of the µbump solder joint on the glass substrate, but there is no underfill protection of the BGA solder joints on the PCB—especially for large glass package substrates.

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Biography

John H. Lau is a Senior Special Project Assistant at Unimicron Technology Corporation, Taoyuan City, Taiwan (ROC). He has more than 40 years of R&D and manufacturing experience in semiconductor packaging, 532 peer-reviewed papers (a principal investigator on 380), 53 issued and pending U.S. patents (a principal inventor on 34), and 24 textbooks on semiconductor packaging. He is an ASME Fellow, IEEE Fellow, and IMAPS Fellow. He earned a PhD from the U. of Illinois at Urbana-Champaign. Email John_Lau@unimicron.com

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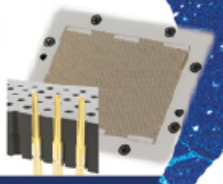

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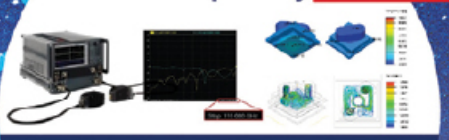

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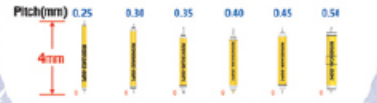

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