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The Future of Semiconductor Packaging

Volume 29, Number 3

May • June 2025

Efficient PIC testing enables data center capacity expansion for optical connectivity

- Examining the drivers of advanced packaging
- IC chip obsolescence solutions: Package converters
- Glass-based 3DHI transmit and receive system-in-package
- Integrated stress analysis: A critical capability for next-gen 3D IC design
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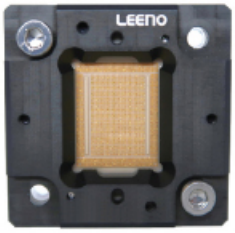

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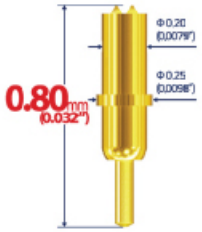

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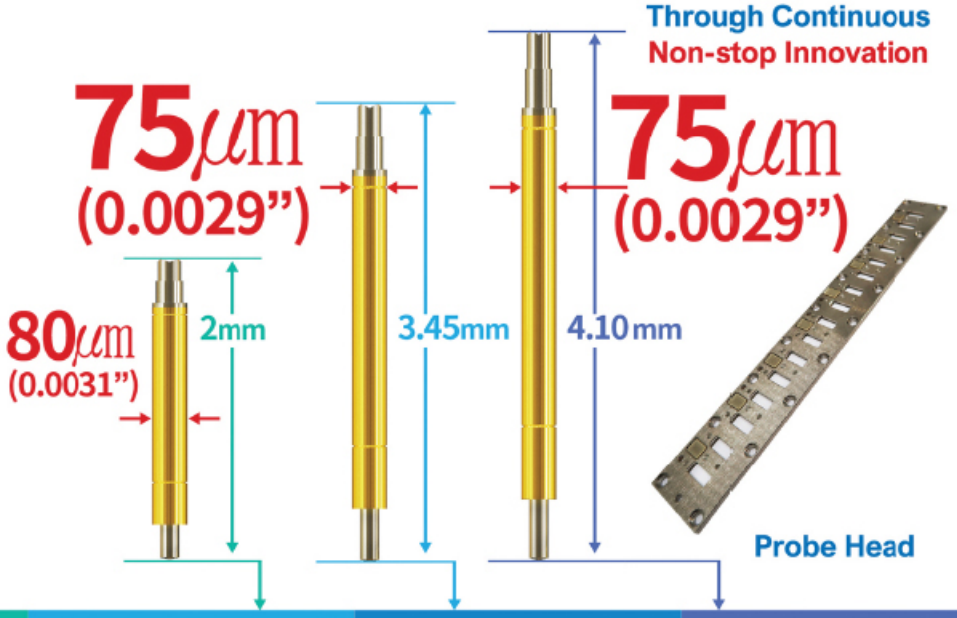

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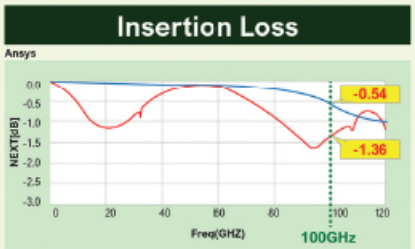

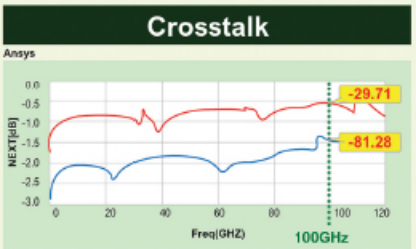

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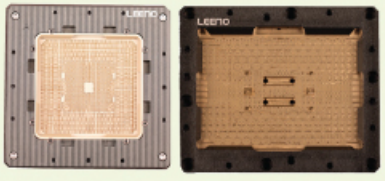

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The growing size of AI clusters is pushing data centers to their physical limits, necessitating the development of multi-site AI clusters to distribute workloads. These clusters rely on coherent ZR optics for high-speed data transfer, which is why it is imperative to increase the yield of such cutting-edge optical modules. This increase in yield can be enabled by using efficient PIC testing.

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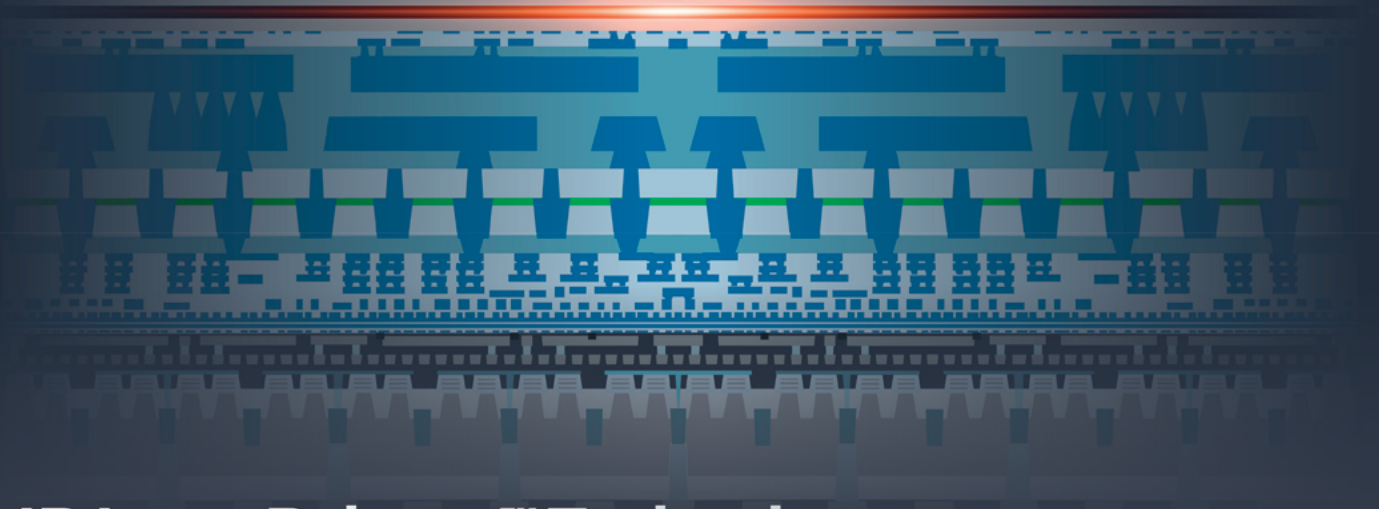

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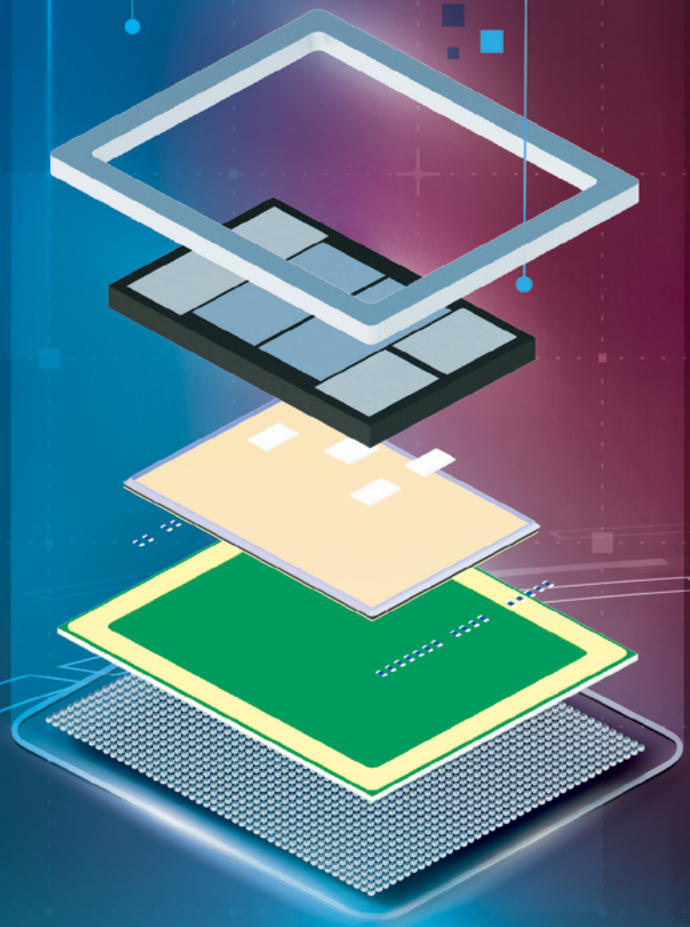

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Examining the drivers of advanced packaging

Chip Scalę Review asked MacDermid Alpha's, Eric Gongora, to address the drivers of advanced packaging. His responses cover heterogeneous integration, thermal management of HPC applications, and other topics.

CSR: The introduction of high-performance computing (HPC), artificial intelligence (AI), and advanced memory devices has driven rapid change within the semiconductor industry, moving beyond technologies of the mobile era. How has this rapid shift impacted the advanced packaging industry?

Gongora: There is a shift toward high-density, high-bandwidth architectures in advanced packaging. This is rendering traditional flip-chip and system-in-package (SiP) mobile packages insufficient for today's high-performance computing (HPC) applications. Advanced packaging must adapt to support higher I/O density, ever-higher bandwidths, and lower latency. This shift is driving the adoption of 2.5D (silicon interposers), fan-out redistribution layer (RDL), and 3D stacked memory.

Heterogeneous integration adoption

CSR: What role does heterogeneous integration play with respect to advanced packaging?

Gongora: Heterogeneous integration (HI) has been adopted as the advanced package of record for AI accelerators, graphic processing units (GPUs) and central processing units (CPUs) (**Figure 1**). HI combines logic, memory and radio frequency (RF) components within tight proximity and functional interconnect layers within the package. This advanced packaging shift has accelerated the use of chiplets that are connected through advanced interconnects (e.g., embedded multi-die interconnect bridge (EMIB), Intel's Foveros technology, chip-on-wafer-on-substrate (CoWoS), embedded bridge in organic substrate, Si or RDL layers).

The interconnect metric for HI layers at the package level are the number of I/Os per millimeter squared. This new metric is the driving force behind ultra-fine through-silicon via (TSV), hybrid bonding and tight-pitch embedded silicon bridge and substrate bridge interconnects. For high-bandwidth memory (HBM) and logic-memory stacking, TSV technology and hybrid direct bonding are becoming critical enablers. Hybrid bonding offers sub-µm interconnects, improving performance for AI processors, however, total cost of ownership is impacting faster adoption.

Figure 1: HPC and AI innovations are driving the shift to high-density, high-bandwidth architectures in advanced packaging.

Thermal management of HPC applications

CSR: What packaging challenges need to be addressed with respect to thermal management of HPC applications?

Gongora: Thermal and power management challenges increase with the introduction of HPC and AI technologies. AI chips generate a tremendous amount of heat, so advanced packaging must now incorporate thermal management solutions like embedded heat spreaders, liquid cooling channels, and through-mold power and ground vias.

Furthermore, advanced packaging is no longer limited to back-end processes. In this new HI environment, advanced packaging has become a core enabler for system-level performance, and equal in strategic importance to front-end manufacturing, development and device design.

Closer collaboration

CSR: What trends are you seeing in collaboration across the ecosystem among material suppliers, equipment manufacturers, and design houses?

Gongora: As the industry transitioned from mobile to HPC and AI technologies, the business strategy also shifted. During the adoption of system in package (SiP) (for mobile technology), outsourced semiconductor assembly and test (OSAT) companies were driving the ecosystem to maintain lower packaging costs. Supply chain dynamics have since shifted; OSATs and integrated device manufacturers (IDMs) have significantly increased their respective investment in advanced packaging R&D. Traditional fabless companies now collaborate with packaging houses early in the design stage. Similarly, IDMs, fabless and original equipment manufacturers (OEMs) are now also working closer together—earlier in the silicon and package development phase—on plating chemistries that enable next-generation HI technologies.

Shifts in the packaging ecosystem

CSR: What trends do you see in the packaging ecosystem?

Gongora: At a certain point, we expect OSATs to play a more traditional role as the need for lower-cost HPC packaging solutions gain traction. The advanced packaging segment will become more segmented via a cost and performance trade-off. The highest-performing HI packages will continue to support the

highest-cost interconnect technologies. Advanced packaging for standard desktop and laptop computing will shift to lower-cost performance trade-off options.

Material science across the ecosystem requires significant collaborative engagement. We have shifted from a traditional chemistry supplier to a material science solution provider, meeting the evolving need for plating technologies. We now develop chemistry side by side with customers, OEMs, and tool vendors.

The role of electroplated metals: now and in the future

CSR: How important are plating technologies in relation to CoWoS, 2.5D and 3D ICs for today's semiconductor applications—and what about future developments?

Gongora: Copper plating technologies play a pivotal role in advancing modern packaging architectures, becoming increasingly essential as the industry progresses toward finer features, higher densities, and more complex HI package designs (**Figure 2**). Driven by performance demands, this level of integration continues to push the boundaries of both chemistry and physics.

Copper plating is essential for forming RDLs, TSVs, and fine-pitch bumps that interconnect chiplets in 2.5D and 3D packages. Uniform, void-free copper fill is the requirement for meeting dimensional precision, as well as for the reliability demands of HPC applications. Electroplated materials also aid in stress management; nickel or new alloy barrier metals help prevent intermetallic growth and fatigue, thereby improving long-term reliability.

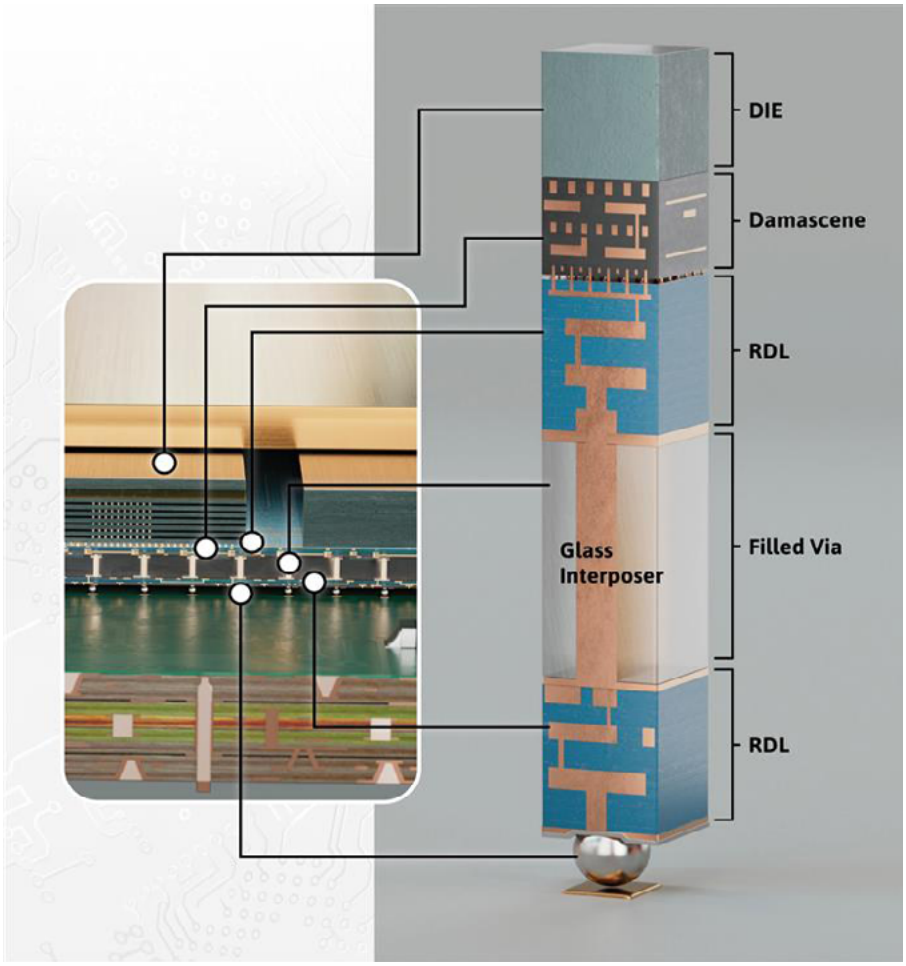

Figure 2: Cross-section of an advanced packaging structure. Our electroplating materials support production across these layers, enabling current and next-generation packaging technologies. SOURCE: MacDermid Alpha

Uniform plating across wafer-scale interposers (CoWoS) and 3D die stacks directly impacts yield and performance. For signal integrity and power delivery, stable copper plating ensures low resistance, high current-carrying capacity, and impedance control are key to enabling high-speed data transfer between HBM and logic. Additionally, copper plating supports thermal management. In 3D ICs, features like copper pillars and thermal vias help dissipate heat, which is increasingly important as power densities increase in next-generation HPC systems.

As 2.5D and 3D ICs move toward sub-2µm line/space RDLs, copper plating processes must adapt as well. Super-conformal plating and advanced additive chemistries are critical for filling ultra-fine features with precision. Future designs will require thinner copper RDLs (~0.5µm) with improved adhesion and lower stress. Additionally, exploring materials like cobalt, tin-silver alloys, and graphene will boost resistivity, thermal performance, and electromigration resistance.

Hybrid bonding, chiplet integration, and heterogeneous materials will demand customized plating stacks (e.g., Cu/Ni/Au) and compatible surface finishes. New architectures, such as backside RDLs in 3D ICs, will increase the need for ultra-fine, low-temperature plating techniques.

As bump pitches drop below 20µm, plating must offer tighter control and lower defect rates. Semi-additive processes (SAP) and eco-friendly chemistries will be key to scaling high-volume, advanced packaging.

Plating remains essential to electrical, thermal, and reliability performance in CoWoS, 2.5D, and 3D ICs, and is a critical enabler as Moore's Law slows and advanced packaging takes the lead in semiconductor innovation.

Alpha particle sensitivity: A serious issue

CSR: As advanced packaging architectures like 2.5D and 3D ICs continue to gain prominence, sensitivity to alpha particle emissions increases. How important are low alpha materials for ensuring high reliability and performance in this space?

Gongora: The use of 2.5D and 3D ICs is growing, enabling the stacking of multiple advanced-node logic and memory

dies into a single package. Packaging these higher density circuits, such as cache memory and control logic, increases alpha particle sensitivity.

A single particle hitting a sensitive node can cause soft errors (bit flips), single-event upsets, and system-level failures in data sensitive applications. The issue is exacerbated with advanced nodes of 5nm, 3nm and lower. RDLs must be low alpha certified to prevent error risks.

Foundries and OSATs now require ultra-low alpha (ULA) emission testing as part of the package qualification process for packaging materials. The industry is progressing from <0.002 cts/khr-cm^2 to <0.001 cts/khr-cm^2 due to the reliability and performance required for HPC, AI and automotive devices.

Overcoming alpha particle emission problems

CSR: What have you done to address the challenges of alpha particle emission?

Gongora: We have developed a new ultra-low and super ultra-low alpha count tin for tin solder bump and tin cap on copper pillar applications. This innovative technology addresses the growing problem of soft errors caused by alpha emissions in next-generation semiconductors. The technology is crafted from high-purity tin materials, meeting the highest standards in the industry. The portfolio includes tin methanesulfonic acid (Sn-MSA) and soluble tin anodes. These leverage our vertically-integrated supply chain and advanced purification processes to deliver exceptional quality and performance.

The evolution to hybrid bonding

CSR: What are the biggest challenges in the roll out and development of hybrid bonding? How is MacDermid Alpha working to meet these challenges from a chemistry perspective?

Gongora: Advanced packaging bonding technology has rapidly transitioned from die and wire bonding to flip-chip bonding to thermo-compression bonding (TCB), and now, to hybrid bonding (**Figure 3**). TCB was qualified for high-volume manufacturing (HVM) in 2014. Led by Intel [1], it is now a widely-adopted bonding technology for 2.5D

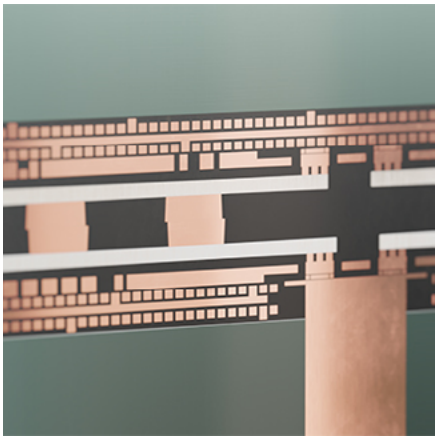

Figure 3: Hybrid bonding in use—interconnecting with precision. SOURCE: MacDermid Alpha

and 3D ICs. Sony was the first to qualify and ramp wafer-to-wafer hybrid bonding in 2016 [2].

Aside from current wafer-to-wafer applications and complementary-metal-oxide semiconductor (CMOS) image sensors, die-to-wafer hybrid bonding integration remains 2 to 3 years away from broader adoption for high-density (HI) packaging, yet it is essential for enabling next-generation packaging technologies. Die-wafer bonding provides inherent flexibility for bonding multiple advanced node chiplets within a single package. The main challenges of hybrid bonding adoption for HVM include: 1) Surface cleanliness; 2) Copper oxide control; 3) Bond pad surface planarity and roughness; and 4) Die-to-wafer bonding alignment. Additionally, the yield and throughput combination leads to early adopter total cost of ownership (TCoO) concerns.

Meeting these new requirements

CSR: How are you going to meet the new requirements needed to implement hybrid bonding?

Gongora: We are partnering with key tier-one suppliers in developing ultra-thin copper films. There is significant ongoing collaborative progress toward developing nano-twin and fine-grain copper structure technology. These are designed to refine the grain structure and behavior during bonding and post-thermal exposure to meet the requirements of current technology leaders.

FOPLP adoption

CSR: How close is panel-level packaging to mainstream adoption, and what challenges still need to be overcome?

Gongora: Fan-out panel-level packaging (FOPLP) first arrived around 15 years ago, but has maintained slower industry adoption and remained largely a low-cost option for smaller body size wafer-level chip-scale packages (WLCSPs). Panel uniformity for with-in-package (WIP) is driven by the equipment design.

FOPLP starts at 300mm^2 with plans to scale to larger panels (e.g. 510mm x 515mm, >600mm^2) and finer RDL pitches (e.g., 2/2 to 1/1). These accommodate more advanced pitch chiplets. The scaling is occurring in two directions where the panel and unit size are increasing while the pitch, line/pace and µ-via dimensions are decreasing. This scaling brings unique challenges, much like wafer scaling; however, in FOPLP, the lack of panel size standardization further increases technical complexity.

Implementation in HPC

CSR: How should panel-level packaging be implemented in HPC applications?

Gongora: There is a resurgence in panel-level packaging efforts in the HPC space to address and reduce the cost per mm². As the silicon interposer size has increased from 70mm^2 to 100mm^2, the utilization per wafer is driving higher package cost through wasted silicon and the manufacturing utilization hit. Therefore, there is a drive towards panel-level packaging as a lower cost option to displace the silicon interposer.

FOPLP is now mainstream, but has the potential to expand its market further in the HPC space. An option from round silicon to square organic interposer will drive the development cycle for chip-on-panel-on-substrate (CoPoS) faster than we have seen in standard FOPLP. This drive will lead to advancements in higher adoption rates for FOPLP. The main factors that impact FOPLPs broader adoption for HPC are warpage control, uniformity, and finer line/space needs along with higher layer counts. We are researching ways to improve not only with-in-unit (WIU) uniformity, but also WIP uniformity while continuing to enable µ-via and trace uniformity through our leveler technology.

Sustainability goals

CSR: What sustainability trends are emerging in advanced packaging, particularly in terms of materials and energy usage?

Gongora: As advanced packaging becomes more central to semiconductor performance, the industry is implementing sustainability goals, driven by regulatory changes, corporate environmental, social, and governance (ESG) targets and customer expectations. Some of these key trends are material innovation, e.g., green mold compounds, and low-volatility underfills. Lead-free solder and halogen-free materials are now standard for WLP, FOWLP, and 2.5D packages.

Energy efficient process improvements like hybrid bonding copper plating chemistry require lower thermal budgets compared to traditional bump reflow processes. Low-temperature copper-copper bonding (<200°C) is in development for 3D-stacking for next-generation HBM stacks.

Waste reduction initiatives in the wafer fabs include complete water recycling via closed-loop systems, along with materials like photoresist and plating chemicals being reclaimed rather than discarded. TSMC developed the first complete copper and tin chemistry reclaim system in Taiwan [3].

The shift toward panel-level packaging for interposer use in CoPoS enables material savings: from using 300mm silicon wafers to larger panel substrates >500mm^2 through improved material utilization and reduced packaging costs per device. Panel-level packaging reduces silicon waste, improving sustainability.

Sustainability is now a competitive differentiator in advanced packaging. Companies that innovate towards lower energy and greener materials may win both market share and loyalty among AI, HPC, and automotive customers that have aggressive ESG goals.

References

1. P. Garrou, "Intel and ASM look to TCB," (2015) https://sst.semiconductor-digest.com/2015/11/intel-and-asm-look-to-tcb/
2. M. LaPedus, "Bumps vs. hybrid bonding for advanced packaging," (2021) https://semiengineering.com/bumps-vs-hybrid-bonding-for-advanced-packaging/
3. "TSMC's innovation of recycling copper waste liquid generates millions of dollars as green value every year," https://esg.tsmc.com/en-US/articles/127

Biography

Eric Gongora is VP of Wafer Level Packaging at MacDermid Alpha Electronics Solutions, West Haven, CT. He has over 25 years of expertise in the semiconductor industry, including 15 years in the OSAT sector, following positions at Motorola and General Electric. He holds a BSc in Mechanical Engineering from the U. of Florida and an MBA with a focus on technology from Arizona State U. Email Eric.Gongora@MacDermidAlpha.com

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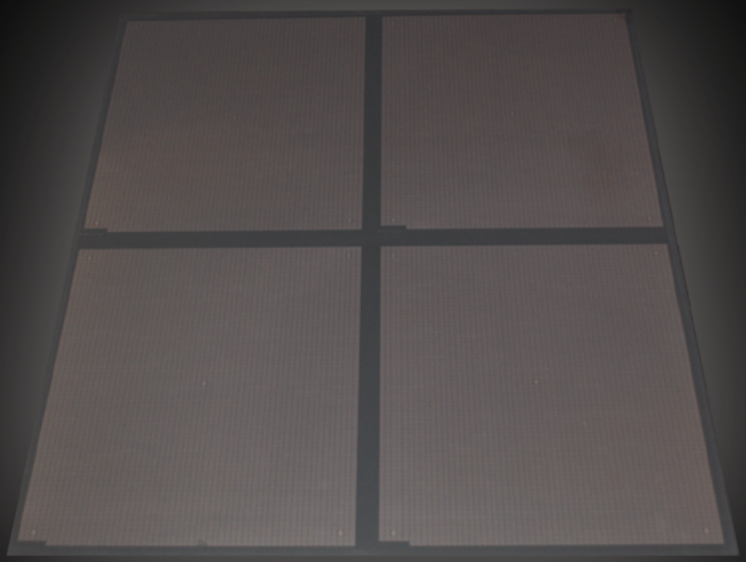

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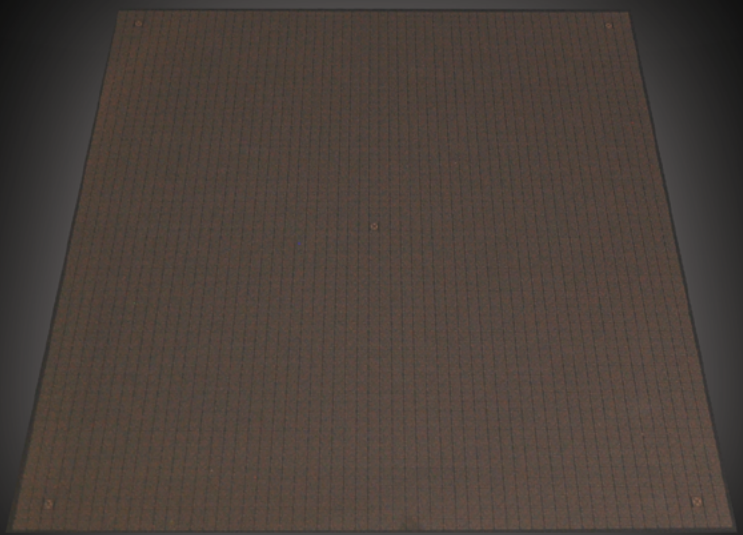

Current optimized format

full 600mm active area for
maximum utilization

IC chip obsolescence solutions: Package converters

By Ila Pal [Ironwood Electronics, Inc.]

An obsolete integrated circuit (IC) chip is an electronic component that is no longer being manufactured or actively supported by its original manufacturer. This can be due to various factors like technological advancements, shifts in market demand, or manufacturing issues. Progress in semiconductor technology often leads to the development of newer, more efficient, and smaller ICs, making older ones less desirable for new designs. Changes in consumer demand or industry needs can cause certain ICs to become less relevant or necessary. Problems with production, supply chains, or component availability can also lead to obsolescence.

Finding replacement ICs can be difficult and expensive, as obsolete parts are often only available through specialized distributors or second-hand markets. Equipment or systems relying on obsolete ICs can face challenges in repairs and replacements, potentially leading to downtime and increased costs. When an IC becomes obsolete, designers may need to find compatible replacements or redesign circuits to utilize newer ICs. Unavailability of chips affects primarily military electronics because the average life cycle of military hardware sometimes exceeds 10 years. Chip unavailability also affects the medical industry because any changes require a long approval process and scrapping of expensive base components. A complete redesign is generally not an option because it consumes many design resources, approval loops, validation cycles, revised manufacturing costs, etc. Substitute devices and adapting to the situation by using alternate devices are the best possible options for a chip obsolescence problem.

Package converters

IC package conversion involves using adapters or converters to allow the use of ICs with different physical package types on the same circuit board. This is useful when a specific IC package is discontinued, when you need to test or prototype with different packages, or when you want to use a substitute device without redesigning the entire board. Substitute devices come in alternate packaging formats that require a simple package converter. Converting the footprint of an IC package to that of another type or size of package is required in many situations. The semiconductor industry is moving away from older through-hole packages such as the dual-inline package (DIP), pin grid array (PGA), etc., and replacing them with surface mount technology (SMT) packages such as the quad flat pack (QFP), ball grid array (BGA), chip-scale package (CSP), wafer-level packaging (WLP), quad flat no-leads package (QFN), etc.

Often a manufacturer will suddenly find a device that has been bought for years is no longer available in the package for which the system board is designed. Until the board is redone, a package converter is needed to fulfill the immediate requirement. Very often these adapters are a simple 1:1 pin mapping from the new package to the old. A few examples of package converters and how they can solve chip obsolescence issues are considered below.

QFP to PGA converter

In the QFP to PGA converter scenario, the Actel 1280KL chip packaged in a 176-pin PGA package was obsolete. The alternate IC Altera 9480, however, is available in a 208-pin QFP package. A unique technology used in the custom package converter for the Altera 9480 allows the 208-pin QFP package to connect to a target board designed for an Actel 1280KL chip, which is packaged in a 176-pin PGA package without compromising real estate. Most of the signals are 1:1 with excess power and ground pins along with a few "no connect" pins. A printed circuit board (PCB) was designed with a QFP pattern on the top side and a PGA pattern on the bottom side. Because the pattern overlaps, the PGA can't be a through-hole design, so the result was control depth hole technology. The control depth press terminal pins keep the real estate required to make the conversion at a minimum. Conventional through-hole terminal loading would require an offset as the patterns for the QFP and the PGA. The control depth pressed PGA interface pins in this custom adapter can be located directly beneath the QFP pad array because they do not penetrate the adapter board top surface. The QFP to PGA package converter shown in **Figure 1** has JTAG testing support in the form of a 0.1" center terminal header strip.

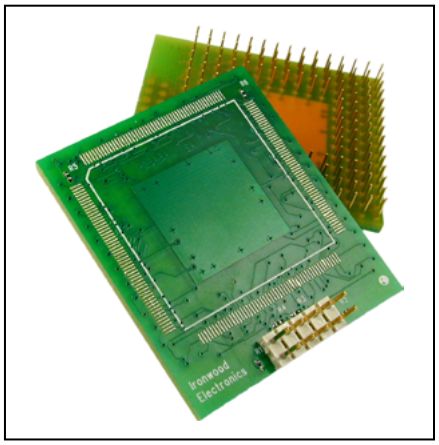

Figure 1: A QFP to PGA package converter.

QFP to QFP converter

In this next example, a target system developed for the Texas Instruments PCI2031, which is packaged in a 176-pin QFP package, can accommodate the Intel 21152 package through a custom package converter. The custom package converter (**Figure 2**) is a two-piece pluggable adapter. A low-mass surface-mount foot solders to the target board with standard reflow processes similar to those used to solder the actual QFP chip. A set of terminal pins on the foot interconnect to four peripheral leadless contacts on the edge of the PCB, which solder to the QFP target board pads. The low-cost leadless contacts are

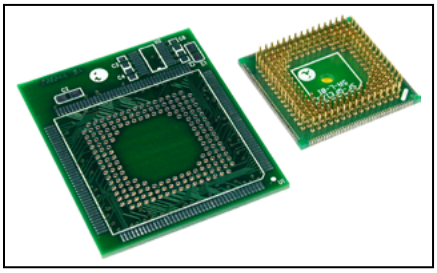

Figure 2: A two-piece pluggable adapter acts as a custom package converter to accommodate the Intel 21152 package.

similar to a leadless chip carrier (LCC) chip, but are designed to solder to the smaller pitch QFP pads. The top adapter, which plugs onto the foot, contains an SMT land pattern for the Intel 21152. The top adapter board has support for an IDT 1 to 10 clock driver (3.3v) and bypass capacitors.

SOIC to QFP converter

In this example, an 80QFP device was obsolete and replaced by a Micrel 20SO package with additional capacitors and resistors. As in the previous example, a two-piece pluggable solution is not feasible due to height constraints. If adapter height is critical, a solder column or bottom termination design (as shown in **Figure 3**) is the best solution. The total height of the adapter is dependent on the height of the components surface mounted to the top, but are typically less than 0.2" (5mm).

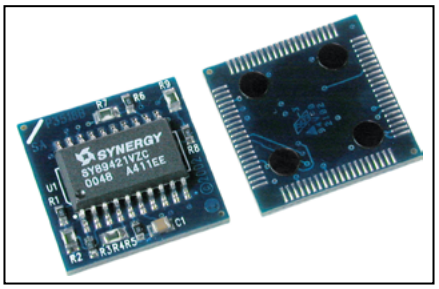

Figure 3: A solder column adapter converts an obsoleted 80QFP device pattern to a Micrel 20SO package with additional capacitors and resistors.

with right peripheral row distance where the device will be soldered. On the backside (to be specific—the edge), pads with side castellation were designed for soldering down to the target PCB. The compact design (shown in **Figure 4**) is ready for production: It can be loaded into tubes, placed in trays, or in a tape and reel for pick and place equipment.

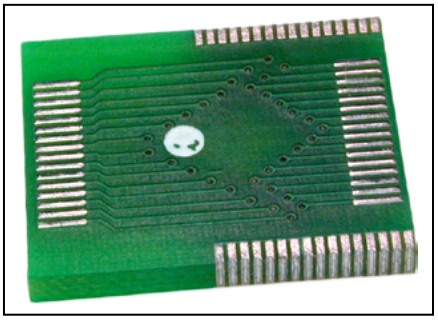

Figure 4: A "fix" adapter corrects the pad location for a 32-pin SOIC device.

SOIC to SOIC converter

Fixing a target board problem because of a wrong device pin out or wrong pad location is another function of package converters. To err is human, to adapt is divine. Package converters—often called "Fix adapters" due to this particular scenario—can be made in many configurations and are usually specific to the mistake that was made. In this next example, the target PCB was designed for a 32SOIC device with two peripheral rows that were at the wrong distance. To fix that problem, a PCB was designed

Summary

When availability or performance of a given IC becomes an issue, using a package converter with substitute device(s) without redesign of the target system is the most economical option with respect to both time and cost considerations. Technology advancements, such as solder column, J-lead, edge castellation, micro- blind/buried vias, flex PCBs, and embedded capacitor/resistor enable adapters to solve any type of constraints faced by end products. Parts can be manufactured as Restriction of Hazardous Substances (RoHS)- or non-RoHS compliant depending on end-usage restrictions. Simple or complex adapters increases the average component life cycle to align with the end product life cycle, which is a must for military and medical electronics applications.

Biography

Ila Pal is CTO at Ironwood Electronics Inc., Eagan, MN, USA. He holds an MS degree in Mechanical Engineering from Iowa State U., Ames, and an MBA from the U. of St. Thomas, Minneapolis. He has received patents, presented papers, published articles, and has spent more than 30 years developing new technologies in the packaging and interconnection field. Email ila@ironwoodelectronics.com

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Efficient PIC testing enables data center capacity expansion for optical connectivity

By Andrew Yick [Marvell]

The surge in compute nodes driven by artificial intelligence (AI) networks has led to an unprecedented increase in demand for optical connectivity solutions for data centers. Ethernet optics experienced a staggering 60% growth in 2024, and this upward trend is expected to continue in 2025 [1]. AI bandwidth capacity has further driven an explosion in dense wavelength division multiplexing (DWDM) data center interconnect (DCI). DCI is a networking technology that links multiple regional data centers together, enabling them to operate as a single entity. Recent growth in the DCI segment has been propelled by the sale of 400G ZR/ZR+ transceivers used to interconnect data center clusters. The number of DCI ports is expected to triple from 2024 to 2028 with upcoming 800G and 1.6T ZR/ZR+ solutions [1].

The growing size of AI clusters is pushing data centers to their physical limits, necessitating the development of multi-site AI clusters to distribute workloads. These clusters rely on coherent ZR optics for high-speed data transfer, scalability, and data integrity, essential for large-scale processing and real-time AI applications [2]. Therefore, increasing the size of AI clusters by interconnecting compute nodes scattered across data centers within a metro area or region via DCI is a top priority.

Marvell's 800G ZR/ZR+ silicon photonics module, COLORZ® 800, incorporates our 5nm CMOS Orion™ coherent digital signal processor (DSP). The module is built on an innovative, field-proven silicon photonics engine comprising industry-leading drivers and transimpedance amplifiers (TIA) operating at 128GBaud integrated directly on the photonic substrate [3].

Shifting yield to the left

At the 2024 Semiconductor Wafer Test (SWTest) Asia Conference and EXPO, numerous presenters highlighted the need to shift yield left to the wafer level as device complexity and integration levels increase. Cutting edge optical modules are no different. Three levels of test in the manufacturing of optical modules described below are identified in **Figure 1**. Level 1 involves testing the constituent known good die (KGD) at the wafer level before their subsequent assembly. Level 2 involves integrating the KGD components onto the silicon photonic integrated circuit (PIC) to form a multi-chip module. At this stage, a fiber pigtail is aligned to complete the optical engine. At Level 3, the optical engine is incorporated into the optical module along with a digital signal processor (DSP), printed circuit board (PCB), microcontroller, and other passive components.

As the level of integration increases from wafer-level KGD to optical light engines and full optical modules, the cost of yield scrap loss rises significantly. If a component does not perform as expected in the module, rework options may be limited or unavailable. Therefore, ensuring true KGD at the wafer level is essential. Another aspect to consider is that there is significantly more test capacity available at the wafer KGD

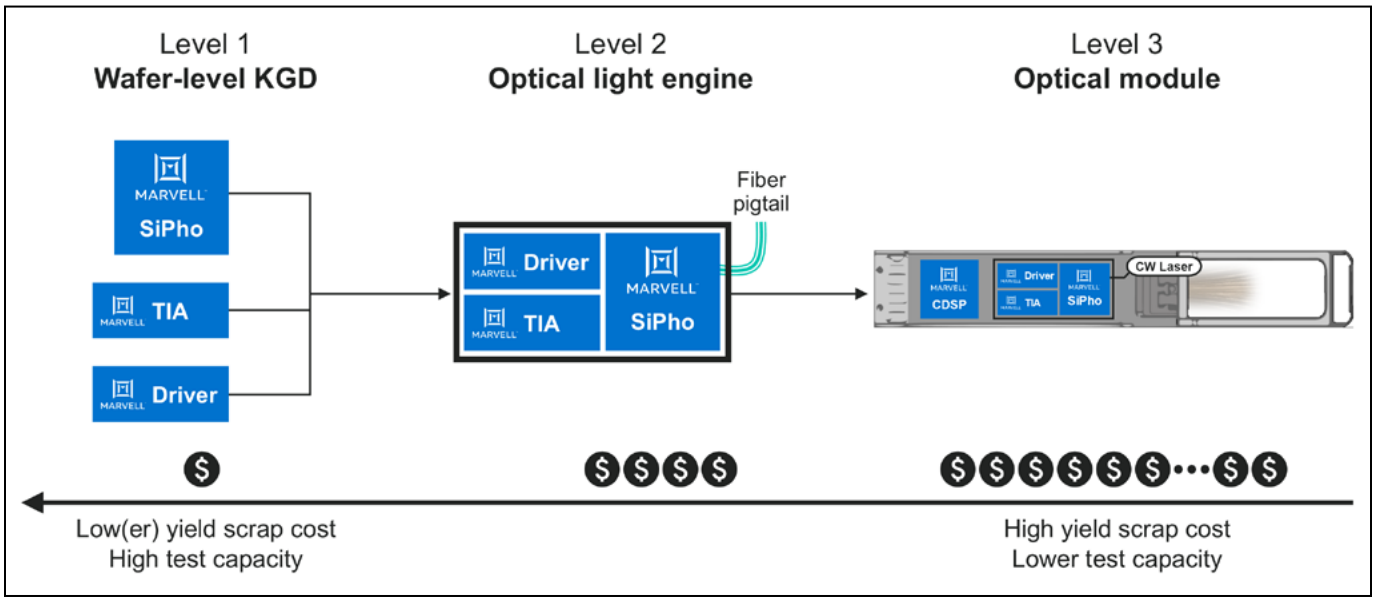

Figure 1: Manufacturing test at three assembly integration levels.

levels compared to the module level. At the module level, test times are generally longer and the costs for scaling capital equipment are higher.

Monolithic electrical-optical probe card

As we shift yield to the left, efficient opto-electrical testing of the PIC becomes critical. This necessitates hardware that offers similar efficiency and ease-of-use as pure electrical testing. The integrated ultra-fast opto-electrical (UFO) probe card we developed with Jenoptik offers alignment-insensitive test solutions for PIC wafer-level tests. The probe card solution comprises an electrical probe head that is monolithically-integrated with the optical fiber array into a single card. This solution is alignment-insensitive to the accuracy of a wafer prober due to the shaped intensity output profile of the optical beam [4]. In general, higher coupling loss is traded for better alignment tolerance. No active alignment using fine-positioning optomechanics is required. All test measurements were conducted using surface grating couplers.

The latest UFO probe card features two significant advancements, shown in **Figure 2**. A vertical pin probe head with a lower support cutout was successfully developed in collaboration with industry-leading probe partners. This design offers significant advantages over previously implemented cantilever probes by allowing denser and more random electrical placement and enabling probing on bumps. Polarization-maintaining fibers (PMF) were integrated, therefore, eliminating the necessity for a polarization controller. This innovation simplifies tuning and more accurately replicates the actual device under test (DUT) use case. Previous implementations used single-mode fiber (SMF). The PMF fiber array unit (FAU) polarization orientation is aligned with the transverse electric (TE) grating coupler.

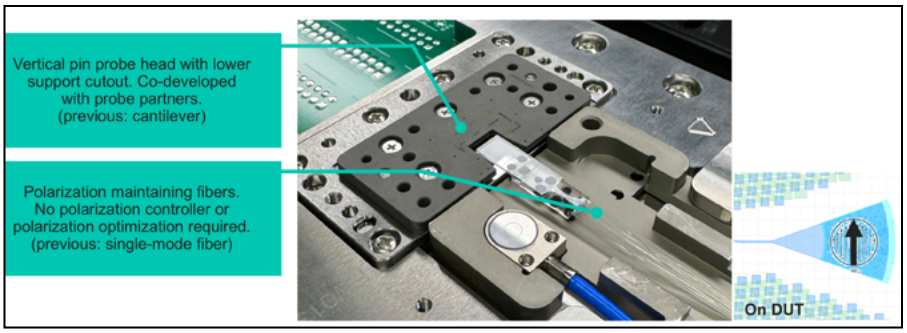

Figure 2: Monolithically-integrated opto-electrical probe card.

Lab vs. line setup

Comparison between lab and production line setups reveals several key differences. The engineering lab uses active alignment with hexapod and piezo optomechanics, while the production line employs passive integrated probe card optics. In terms of optical mode, the engineering measurement involves finely-coupled standard SMF or PMF modes, while the production line measurements use an expanded mode beam. The probers differ as well, with the engineering lab using an MPI TS2000 prober and the production line using a more standard UF200 production model.

The simple configuration of the production line allows plug-and-play efficiency, eliminating the need for a test engineer to be physically present at setup. Conversely, the engineering setup necessitates both engineer and technician participation for hardware installation and alignment.

A PCI eXtension for Instrumentation (PXI)-based tester system was selected because it incorporates direct current (DC), optical, and radio-frequency (RF) instruments, making it ideal for low pin-count devices with reduced capital expenditure (CapEx) and maintenance costs. This is in contrast to recent integration with larger automatic test equipment (ATE) testers [5]. Unlike ATE testers that need external optical instruments and additional racks, this cabled-in PXI system is a single, customizable unit that combines all necessary instruments.

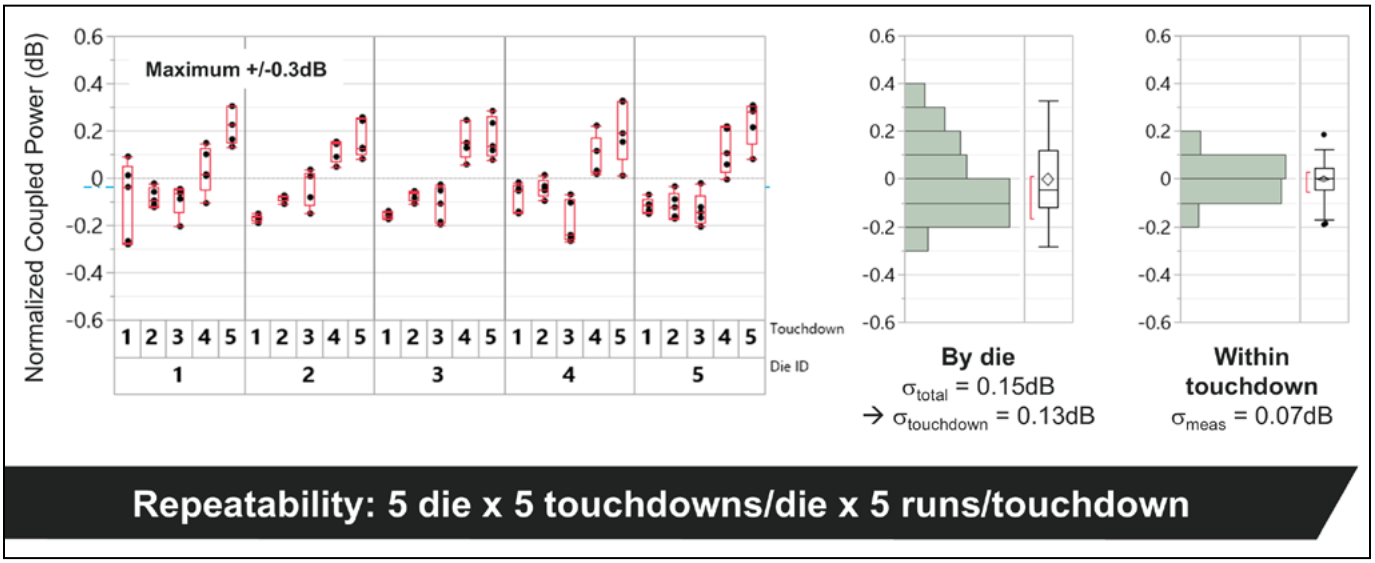

Figure 3: Production line passive optical coupling repeatability analysis.

Production line optical repeatability

Figure 3 shows optical coupling repeatability data collected using a standard UF200 prober, looping 5 die with 5 touchdowns and running the test program 5 times per touchdown. The maximum deviation between die and touchdowns is ±0.3dB, with a standard deviation of σ_{total}=0.15dB. Within a single touchdown, the measurement repeatability is σ_{meas}=0.07dB; from this value, touchdown repeatability of $\sigma_{touchdown}$=0.13dB is calculated, which aligns closely with previously demonstrated results [4]. These results confirm that the monolithic probe card delivers optical repeatability performance on par with a fully active-aligned system, proving its suitability for precision parametric measurement of optical PICs.

Key optical measurement parameters for PICs include Vπ: the half-wave voltage of the Mach-Zehnder modulator [V], extinction ratio (ER): the ratio of maximum to minimum Mach-Zehnder intensity [dB], chip loss: the ratio of optical power lost through the chip [dB], bias point: the phase of the null bias from zero heater power [degrees], and phase tuning rate: the heater power required for a 2π phase shift [mW]. These measurements are shown in normalized form in **Table 1** to maintain the confidentiality of design specifications.

Table 1 presents a comparison between the measured optical parameters and the total standard deviations for both the lab solution and the production line solution. The data shows that, regardless of the optical parameter—Vπ, chip loss, bias point, or phase tuning rate—the standard deviations of the measurements are similar between the two locations. Excellent measurement repeatability for key parameters is obtained for passive alignment versus active alignment.

Production data insights

The Vπ measurement is so highly accurate that it enables even the characterization of the Vπ shift over the C-band from 1530 to 1565nm. **Figure 4** shows a 2.26% increase in mean Vπ, collected over a wafer population, which closely matches the theoretical 2.29% increase due to wavelength scaling of a fixed-length modulator.

Having established the repeatability of the solution, the measurements between the lab and the production line are compared. **Figure 5** shows

	Engineering lab: Hexapod	Production line: Monolithic probe card		
Parameter	σ_{total}	σ_{total}	σ_{meas}	$\sigma_{touchdown}$
Vπ	0.78%	0.76%	0.55%	0.52%
Chip loss	0.054 dB	0.030 dB	0.019 dB	0.023 dB
Bias point	1.80°	1.50°	0.41°	1.44°
Phase tuning rate	0.50%	0.29%	0.14%	0.25%

Table 1: Measured optical parameters vs. total standard deviations comparison.

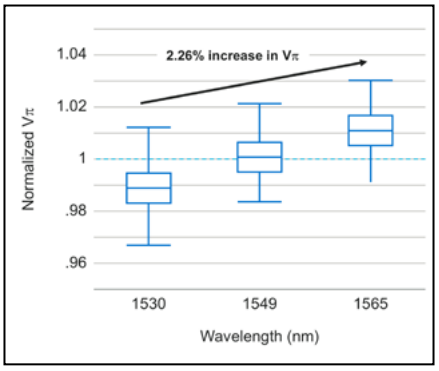

Figure 4: Modulator Vπ measurement shift over wavelength.

two parameters: normalized Vπ and chip loss. The absolute mean of the Vπ populations are within 0.68%, meaning that if the Vπ value was 10V, the mean values differed by less than 0.068V. Furthermore, the root-mean square error (RMSE) sigma was only 1.38%, indicating that 95% of the data points fall within 2.7% of the fitting line. A similar correlation is observed for chip loss. The absolute means of the chip loss populations are within 0.06dB. Furthermore, the RMSE sigma was only 0.10dB, indicating that 95% of the data

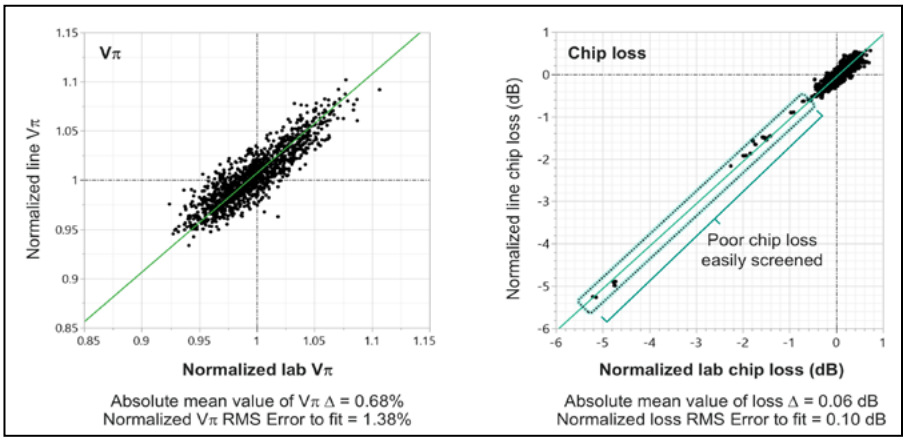

Figure 5: Lab to production line optical measurement correlation: a) (left) Normalized lab Vπ vs. Normalized line Vπ; and b) (right) Normalized lab chip loss (dB) vs. Normalized line chip loss (dB).

	Engineering lab repeatability	Production line repeatability	Engineering lab to production line correlation		
Parameter	σ_{total}	σ_{total}	RMSE	Absolute mean Δ	R^2
Vπ	0.78%	0.76%	1.38%	0.68%	0.79
Chip loss	0.054 dB	0.030 dB	0.10 dB	0.063 dB	0.95
Bias point	1.80°	1.50°	5.9°	---	0.99
Phase tuning rate	0.50%	0.29%	0.53%	0.10%	0.92

Table 2: Engineering and production site optical measurement correlation.

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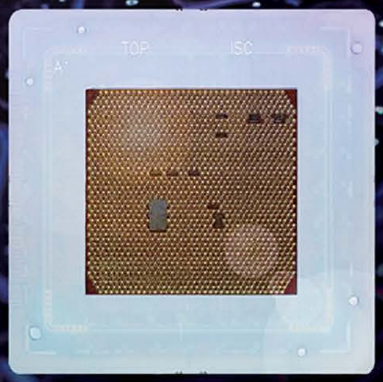
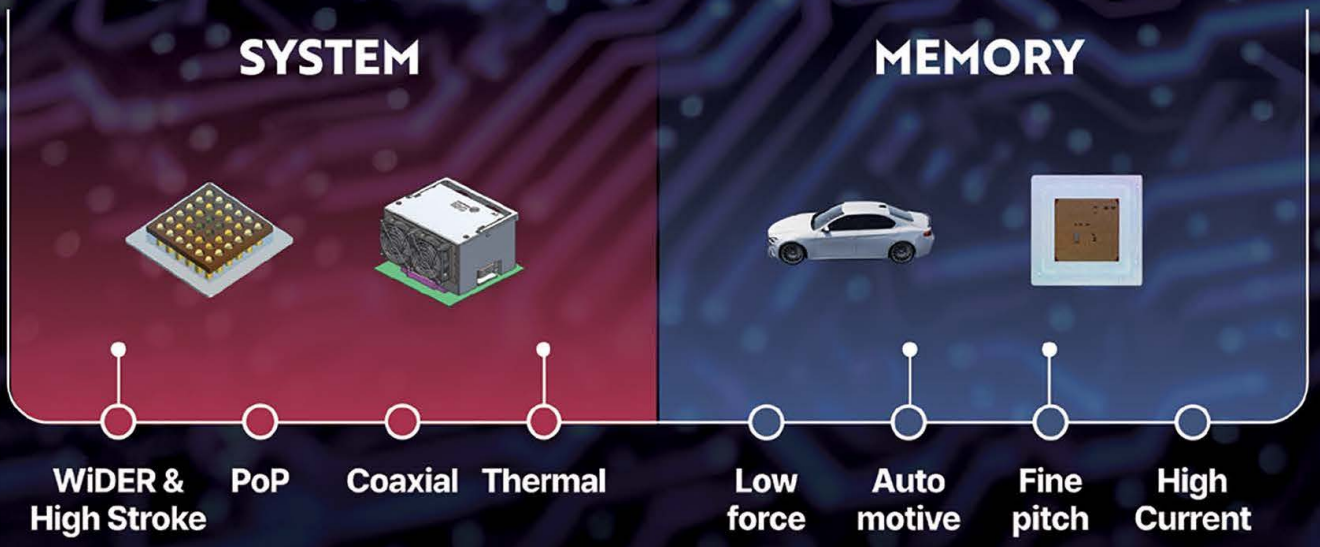


Capable of Mass Production : From Validation To SLT



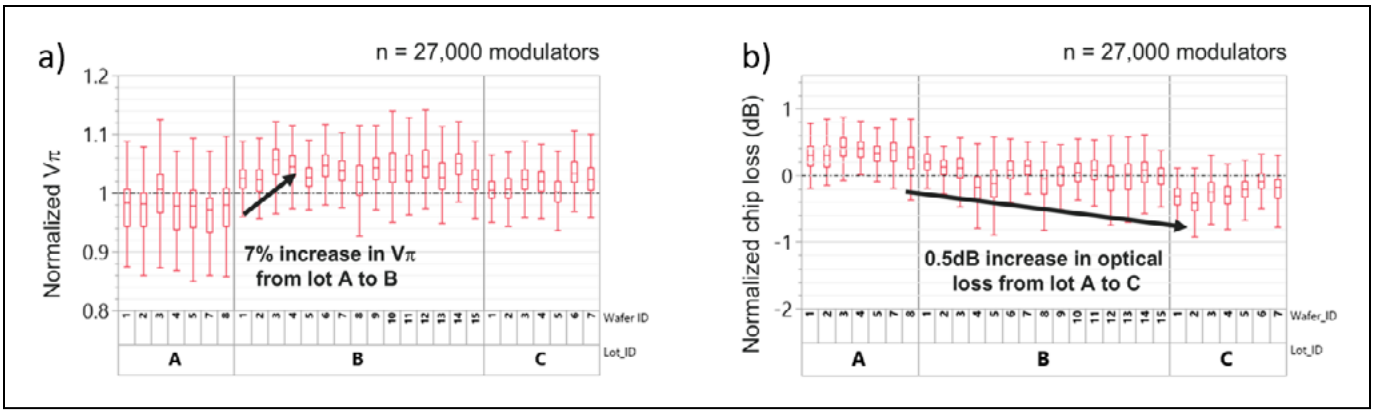


Figure 6: Production lots optical measurement shifts vs. process: a) (left) Graph shows a 7% increase in Vπ from lot A to B; and b) (right) Graph shows a 0.5dB increase in optical loss from lot A to C.

points fall within 0.20dB of the fitting line. Most importantly, poor chip loss outliers can be easily identified and screened to prevent their incorporation into optical engines.

Table 2 summarizes the measurements between the engineering and production sites. The RMSE of the correlation fit between the two sites, compared to the repeatability of the measurements themselves, is very close. This indicates that the correlation variation is comparable to the measurement repeatability. Additionally, the absolute mean delta between the two sites is also very small with strong R^2 correlation values. It should again be noted that the engineering measurements use active hexapod alignment versus the production passive optical coupling, yet the measurement correlation relative to repeatability is excellent.

Figure 6 analyzes datasets from 27,000 modulators, showing process shifts and optical parametric differences between production lots A, B, and C. **Figure 6a** maps a 7% increase in Vπ due to process shifts from lot A to lot B. **Figure 6b** maps a 0.5dB increase in optical loss for the same three lots moving from lot A to lot C. This data serves as an early optical warning for yield crashes or maverick lots, preventing low-performing die from integration and expediting backup lots if needed. It also shortens process or design improvement cycles at the fab, expediting yield feedback without waiting for final module characterization.

Figure 7 shows the same three lots and data for the normalized extinction ratio versus the test lower limit. Most lots exhibit a high yield. However, PICs that do have low extinction ratios can be identified and eliminated before TIA, driver, and fiber attach assembly. This process improvement increases the final yield on certain optical engine lots by up to 20%.

The yield shift-left is meaningful only if the subsequent assembly-level data correlates with the wafer-level KGD. The capability to record and monitor individual PIC fuse identifications from the die level to the optical engine level ensures precise traceability and quality control throughout the production process.

Figure 8 illustrates that our wafer-level Vπ measurements accurately predict light engine Vπ even after the assembly process, indicating a good correlation between KGD testing and pigtailed light engine performance. The absolute mean of the Vπ populations are within 0.44% with a RMSE sigma of only 2.63%. By employing appropriate wafer-level

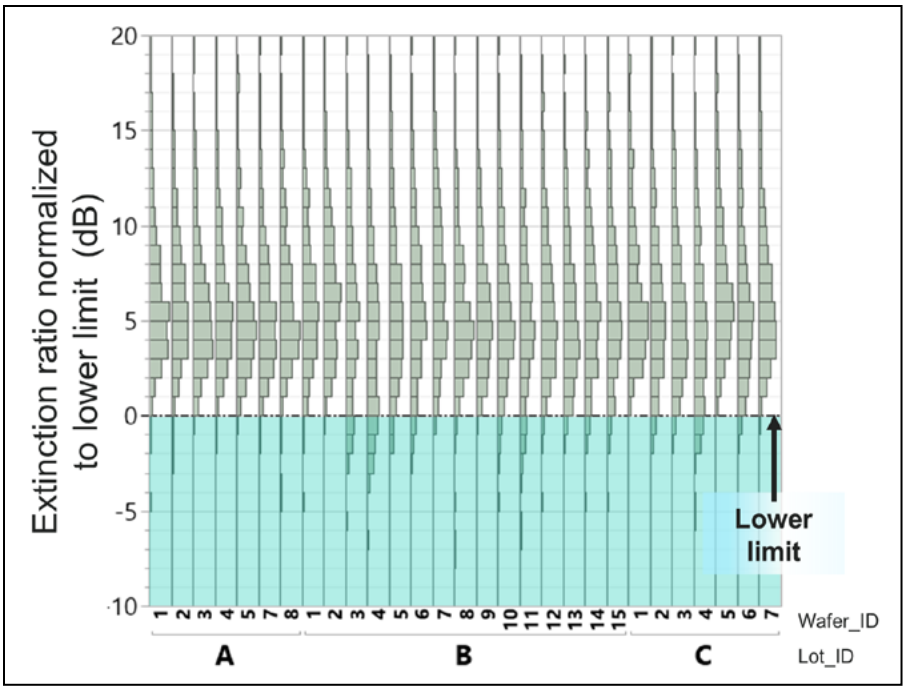


Figure 7: Production lot modulator extinction ratio shifts vs. process.

Parameter	RMSE	Absolute mean Δ	R^2
Lab to line	1.38%	0.68%	0.79
Line to light engine	2.63%	0.44%	0.57

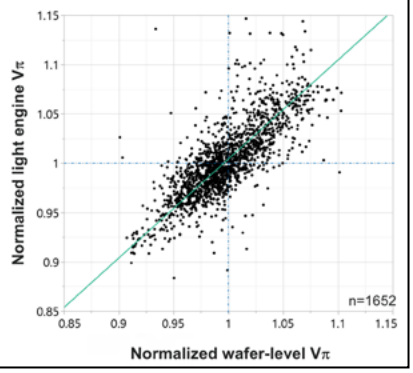


Figure 8: Wafer-level to optical light engine measurement correlation.

binning, we can effectively reduce light engine yield loss, ensuring that only the highest-performing KGD advance through assembly stages.

Summary

Compared to active alignment, a passive monolithic optical probe card has demonstrated similar measurement repeatability and capability for key PIC optical parameters when compared to active alignment. This similarity in performance metrics between the two methods reinforces the robustness of a passive probe solution to generate KGD.

Furthermore, we observed excellent measurement correlation between the engineering lab and the production line, with plug-and-play deployment at the outsourced semiconductor assembly and test (OSAT) level. This seamless integration underscores the reliability and efficiency of the measurement process, ensuring that the transition from development to full-scale production is smooth and efficient.

Additionally, the opto-electrical testing capability provides an early warning to wafer-level process changes and maverick lots, effectively shifting yield left to KGD. This screening prevents low-performing die assembly and speeds up process improvement cycles by providing quick yield feedback without waiting for final module characterization.

Acknowledgment

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References

1. S. Baleva, C. Cao, V. Kozlov, J. Lively, I. Lomtev, R. Rubenstein, T. William, LightCounting: "Optical Communications Market Forecast," Oct. 2024.
2. N. Kucharewski, "The evolution of AI interconnects," Retrieved from https://www.marvell.com/blogs/the-evolution-of-ai-interconnects.html; March 17, 2025.
3. "Marvell launches industry's first 800G ZR/ZR+ modules for data center interconnect," Marvell news release, Aug. 23, 2023; https://www.marvell.com/company/newsroom/marvell-launches-industrys-first-800G-zr-zr-plus-modules-for-data-center-interconnects.html
4. T. Gnausch, "UFO Probe™ Card: New dimensions in wafer-level test of photonic integrated circuits," SWTest 2022, Carlsbad, CA.
5. G. Bappi, T. Gnausch, "Novel direct probe solution for opto-electronic wafer-level PIC testing," SWTest 2024, Carlsbad, CA.

Biography

Andrew Yick is the Senior Director of Product and Test Engineering at Marvell in Westlake Village, California. He leads Marvell's Product and Test Engineering teams, driving the production of cutting-edge broadband analog devices such TIAs, drivers, and silicon PICs. His expertise spans from DC to 110 GHz, all the way to light speed. He has over 20 years of industry experience and received his PhD in Electrical Engineering, specializing in Photonics, from the University of Southern California. Email ayick@marvell.com.

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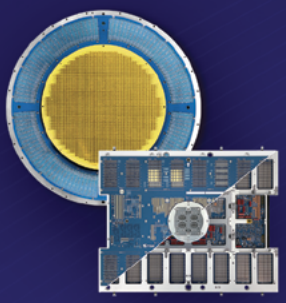
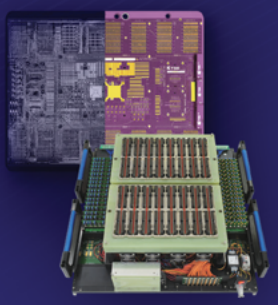


Probe Card



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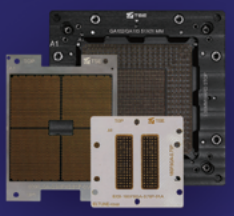

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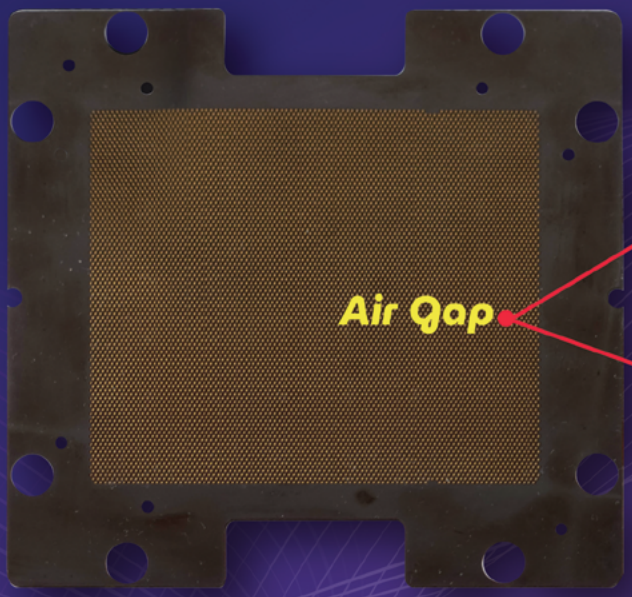

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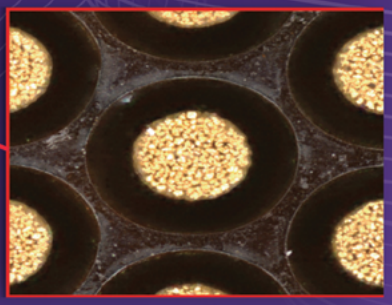

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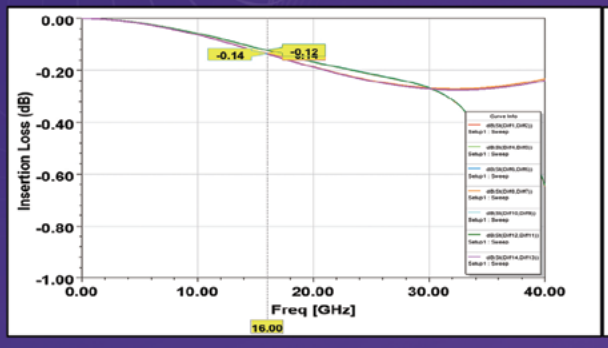
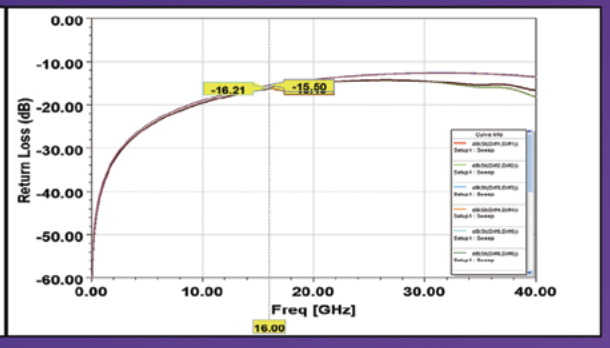


Insertion Loss(dB)



Return Loss(dB)

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AI optimization of a wafer-scale fabric for heterogeneous chiplet integration

By Rabindra N. Das, Albert Reuther, Vitaliy Gleyzer, Ryan Touzjian, Alex Wynn, Ravi Rastogi, Brian Tyrrell, Paul Monticciolo, Paul W. Juodawlkis [MIT Lincoln Laboratory]

This article proposes an artificial-intelligence (AI)-based decision tree concept for fabrication-informed optimization of wafer-scale fabric. The optimization process considers high-resolution deep ultraviolet (DUV) EX4 (22mm × 22mm) reticles, large-field (44mm × 44mm) I-line stitched reticles, and wafer-scale laser direct-write (LDW) lithography. These fabrication techniques are combined to enable a circuit area to include the entire 200mm wafer, enabling a full system-on-wafer (SoW) form factor. To demonstrate the scalability and viability of heterogeneous integration, we fabricated micro-bumps on a 200mm wafer with a bump size down to 1.5µm at a 5µm pitch. We further developed various thermal solutions capable of handling twenty 20mm x 20mm chips uniformly spaced on a 200mm wafer, to address the challenging thermal budget constraints of a SoW approach. Air cooling with heat pipes, traditional liquid cold plates, micro-channel liquid cold plates, and jet impingement on silicon are used to evaluate the thermal performance of SoWs. These thermal analyses indicated that high-power chips can be handled with an appropriate thermal architecture.

AI, machine learning, and the greater embedded computing industry are driving toward miniaturization and accelerator specialization to enable continued gains in computing scale and efficiency in a post-Dennard scaling environment. This demand has led to high-performance computing (HPC) packages to support smaller and more diverse technology nodes with higher integration scales pushed to the packaging level.

With the inherently longer interconnect distances across wafer-scale systems, increasing system-level power consumption continues to be a challenge, and there is a need to improve advanced packaging technologies to support the continued scaling of HPC. In traditional HPC systems, a large portion of power is consumed by the data movement required to support the computation. New packaging architectures need to integrate multiple processors and accelerator chips with minimum chip-to-chip spacing to minimize the interconnect length and support low-dielectric-loss materials. These requirements are driven by the need to reduce communication energy requirements and integrate higher-density on-chip memory. Additionally, packaging architectures must also address the need to efficiently dissipate heat while being pushed into smaller I/O pitches for higher bandwidth connections, and should support a versatile assembly solution to accommodate the complexity associated with size, weight, and power (SWaP) optimization. To achieve this goal, we suggest a SoW solution based on a wafer-scale heterogeneous integration approach. To support these SoW platforms, we developed three functions: 1) An AI-based decision tree concept to realize a complex active SoW fabric; 2) Evaluated feasible thermal management architectures for SoW platforms; and 3) Implemented an interconnect solution for heterogeneous integration down to a 5µm pitch flip-chip package.

An AI-based decision-tree strategy was proposed to fabricate 200mm wafer-scale active-fabric-based substrates. These substrates consist of multi-chip modules (MCMs) that interconnect heterogeneous chiplets (e.g., central processing unit [CPU], graphics processing unit [GPU], and memory). Here, the I-line, EX4, and laser direct-write lithography are used in conjunction, each of which occupies a different point in the trade space between the field size, feature size, throughput, and cost. By decomposing the fabrication process in a manner that employs multiple lithography tools, the benefits of each can be exploited as required for different steps of the process. A typical process uses a DUV reticle to create active elements, an I-line reticle to interconnect multiple DUV reticles, and a wafer-scale direct-write interconnect to distribute a signal to the entire wafer. The decision tree simplifies the partitioning of the fabrication process to create complex structures with relatively high yield.

Decision-tree concept

This section presents various representative experiments to initiate training datasets for the decision-tree concept. This section further proposes machine language development (MLD) and AI algorithm approaches for developing a wafer-scale platform with an optimized assembly approach to create a fully-functional system with minimum yield loss.

Figure 1 shows an example of how the fabrication process can be used to integrate a wafer-scale system. Here, we interconnect 16 high-resolution DUV EX4 (248nm lithography) reticles into a wafer-scale platform. The fabrication optimization process starts by interconnecting four high-resolution DUV EX4 (22mm × 22mm) reticles with a single large-field (44mm × 44mm) I-line (365nm lithography) reticle using EX4 lithography-based sub-micron vias, followed by I-line reticle stitching at the boundaries of 44mm × 44mm fields to fabricate 88mm × 88mm stitched reticles. Wafer-scale direct-write (digital layer) routing interconnects stitched reticles to extend the signal to the entire wafer.

Decomposing a wafer-scale design into a set of chiplets and a system-level interconnection fabric, and implementing that fabric across multiple lithography and hybridization tools, requires optimization across a complex set of many different interrelated parameters. Conventional heuristic-based approaches are not well-

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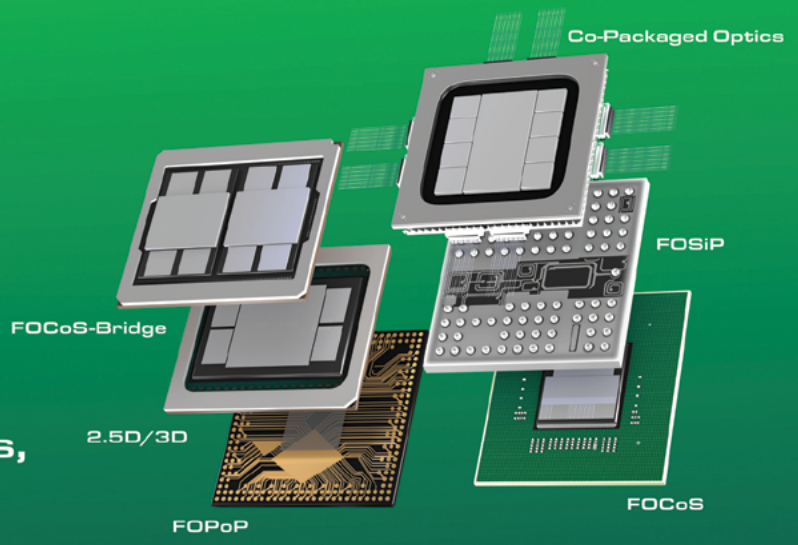

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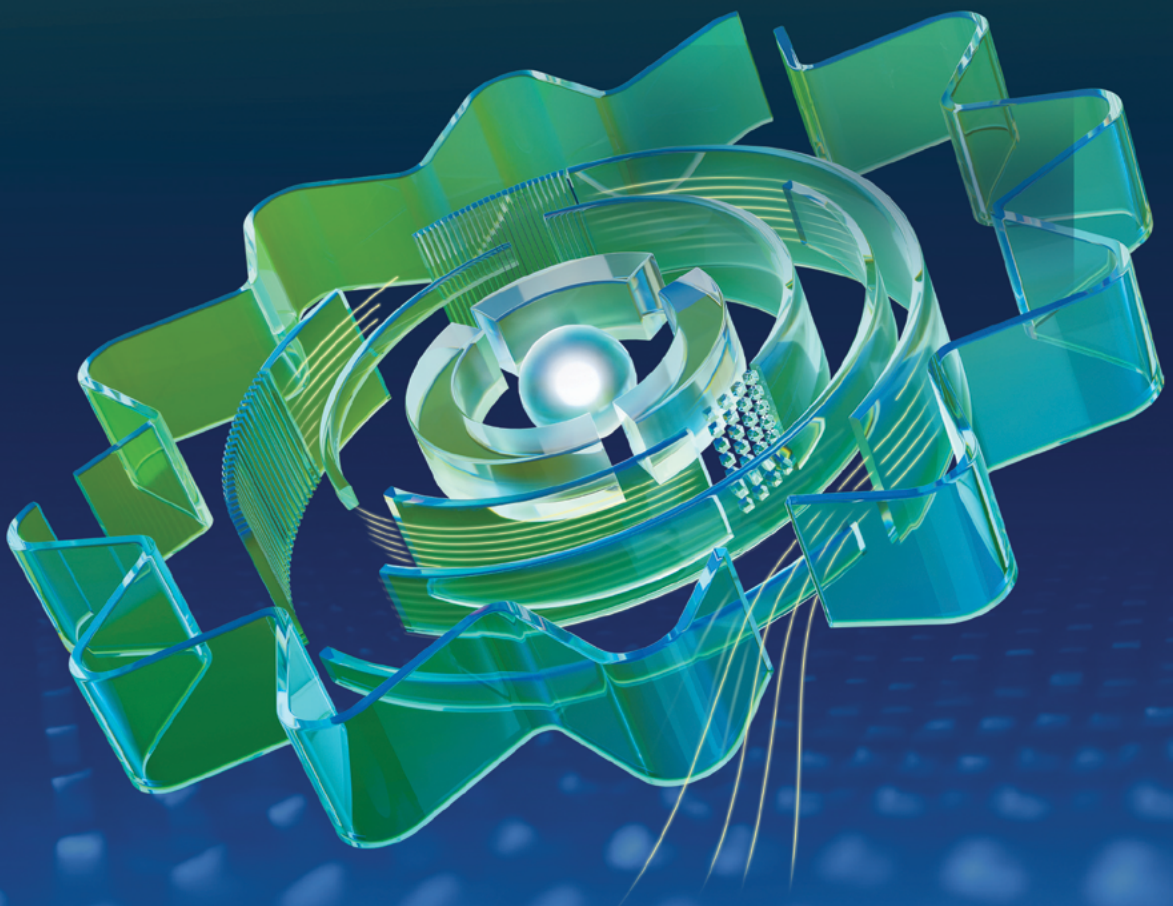

suited for optimization across a design space of this complexity, even in the implementation of monolithic integrated circuits. However, many advancements have been made in the application of AI techniques to monolithic integrated circuit designs [1], and these have been naturally extended to the case of complex heterogeneous circuits. However, unlike the monolithic case, the optimization for a heterogeneous circuit is heavily based on implementation considerations, such as chiplet cost and yield, mask cost, lithography and patterning throughput and yield, and hybridization throughput and yield. It is also necessary to determine routing traces that should be implemented in a reconfigurable manner.

For each sub-circuit block or set of blocks that might map to an available chiplet, selection and mapping must be performed based on considerations such as yield statistics, power and performance estimation, area, and form factor. Although it is sometimes the case that a specific selection of chiplets is known in advance, having multiple candidates provides a degree of freedom that can be exploited at the global design level. Therefore, in the case of multiple chiplet options, it is desirable to include a revisit of the chiplet selection and mapping stage as an optional part of the iterative design flow. With an initial set of identified chiplets, the pin positions and geometric boundaries of each are known, as are the performance information relevant to the higher-level design. Top-level digital constraints on the networks that interconnect these modules are also available. A preliminary floor plan can be derived based on digital design constraints.

For each potential route interconnecting these chiplets, the costs and benefits of static versus reconfigurable routing can be determined. In static routing, global routing is achieved using physical wires. Reconfigurable routing introduces switch-box features that allow for a one-time-programmable or field-programmable selection from a set of routing resources to form the desired routing connection. At this stage, it is necessary to consider not only the chiplet yield, timing, and power performance of the routes being designed, and switch-box resource areas, but also the estimated cost and yield of the overall implementation.

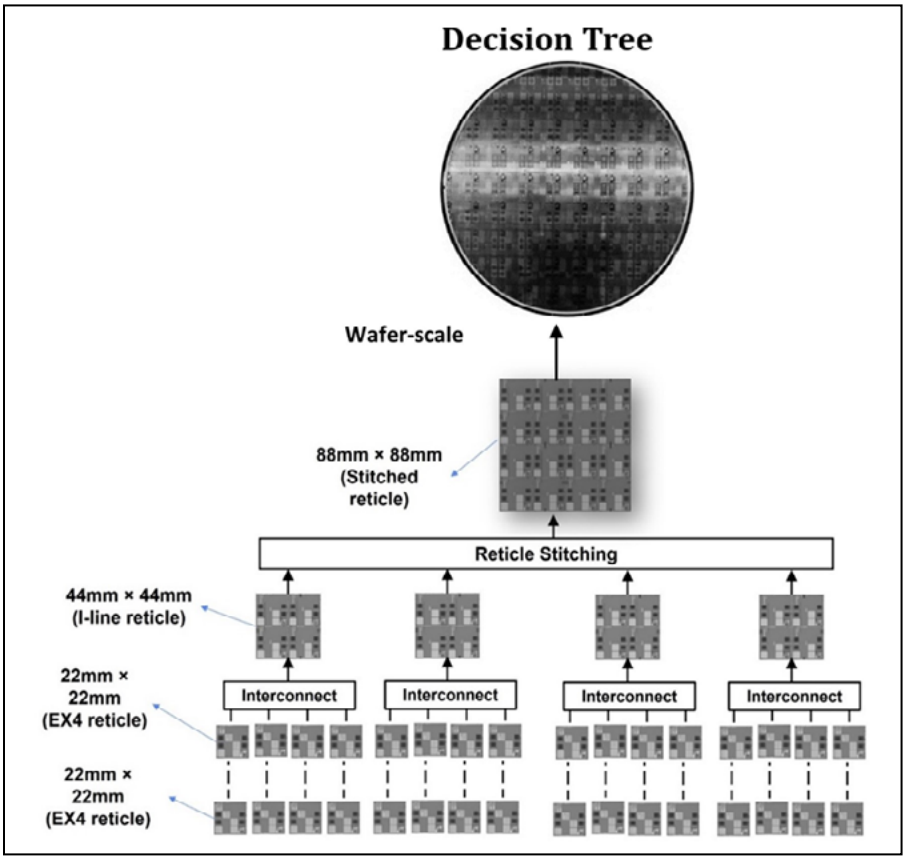

Figure 1: AI-based decision tree concept to fabricate wafer-scale fabric.

Multiple ways of implementing reconfigurable routing paths are possible, each with its own implications for the overall circuit yield, and the optimization needs to be over these routing network design approaches that satisfy circuit redundancy constraints (such as the worst-case available memory or worst-case number of cores). A decision tree can be used to facilitate the identification of redundant and reconfigurable routing insertions. The goal of this step is to provide the information needed to generate a placement of the chiplets and switch boxes so that the placement can be passed to the routing design stage. Placement in this stage is not arbitrary; it must be constrained so that it can be implemented through a combination of stepped reticle exposure and maskless lithography. For the example indicated in **Figure 1**, the placement of the chiplets needs to be constrained to be compatible with repeated use of the same EX4 and I-line reticle patterns. Therefore, the product of this stage needs to provide a set of pins on a common placement corresponding to EX4 reticle-level geometries, a set of pins on a common placement corresponding to I-line reticle-level geometries, additional pins that require wafer-scale connections, and routing track positions compatible with all reticle exposures to be used.

Wafer-scale design routing must be optimized in a manner that considers the yield and performance of reticle-level interconnection, reticle stitching, yield of single and stitched reticles, and wafer-scale-level maskless routing. From a performance perspective, in addition to digital design considerations, it is also necessary to consider the power supply rail droop and thermal behavior in this top-level implementation. As shown in **Figure 1**, this top-level routing is implemented using multiple lithographic methods, each with its advantages and disadvantages, which are described in a subsequent section of this paper. These lithographic design trades drive the optimization in this stage.

Routing implemented using wafer-scale maskless lithography can be performed in two ways. It can be used to complete any connections not made by reticle-level lithography, extend the circuit to cover the entire wafer, or be implemented in a custom manner that is informed by inline testing to modify or re-route a signal to mitigate a defect and provide a fully-functional wafer-scale fabric.

Figure 2 and Figure 3 show representative examples of the digital layer and the interconnection of the digital layer to the stitched reticle to extend the signal to the entire wafer. Figure 2 shows a maskless digital layer (via direct write) printed on a 200mm wafer. Traditional maskless digital layers use direct laser writes to produce micro-scale features. Direct laser writing can produce features of 1µm or larger on the scale of a full wafer, but is much slower than reticle-based I-line lithography.

We propose combining laser direct-write and I-line lithography into a single-process module to reduce the total number of processing steps, with potential benefits in terms of both process yield and cost. One of the lithography challenges is that each tool is optimized to use a different photoresist, which increases the fabrication complexity by introducing additional photolithography steps and complicated etching recipes (because of the dependence of etch selectivity on the photoresist type).

As shown in Figure 3, we used a single photoresist and a double-exposure approach to combine the I-line and direct-write exposures sequentially to define the desired circuits. In this approach, we used I-line lithography with reticle stitching for critical features, whereas laser direct-write lithography provides routing to extend the signal to the entire wafer. Figure 3 shows four 48mm × 48mm I-line reticles stitched together to create a 96mm × 96mm reticle, and subsequent processing with direct-write lithography for fan-out circuits to extend the stitched reticle's connection to the entire wafer [2].

The combined lithography approach for wafer-scale fabrics offers several advantages. The fabric delivers a cost-effective solution for computing systems because it creates chip-like circuits for chip-to-chip communication and eliminates the need for a multi-level assembly process. The combination of EX4, I-line, and direct-write lithography reduced the total number of stitching masks required to create complex architectures. The use of a single photoresist and sequential double-exposure fabrication [3] not only reduces additional processing steps, but also minimizes/eliminates circuit misalignments/defects for the wafer-scale fabric. Furthermore, the digital layer provides fan-out circuits for attaching connectors and cables to connect to the next level of semiconducting electronics.

Figure 4 shows a representative example of a wafer yield map for 32mm × 32mm I-line (365nm) reticles. The wafer map indicates that the single reticle yield prior to the digital layer is over 90%, which is sufficiently high for fabricating single- or stitched-reticle systems.

Figure 4 also shows that the yield of a full-wafer circuit is only 25%, which may vary from one run to another. To improve the effective yield of full-wafer circuits, we propose detecting defects using inline optical defect inspection at the reticle scale, followed by defect avoidance using

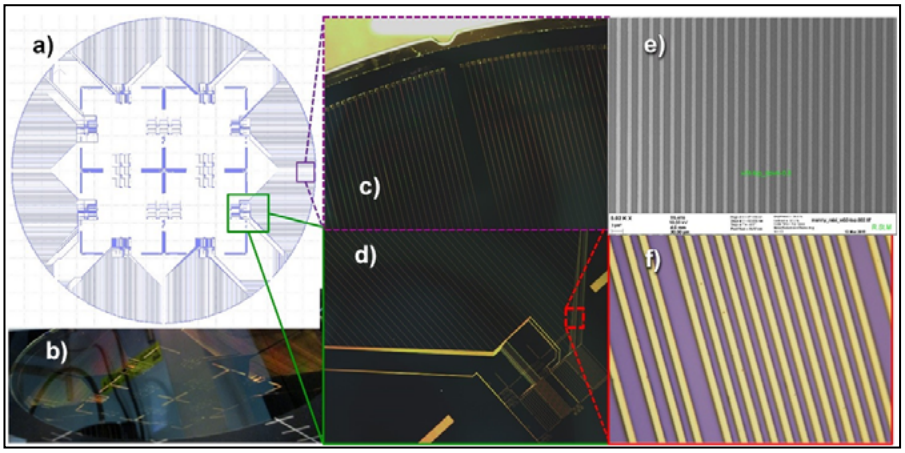

Figure 2: Maskless digital layer: a) Maskless GDS layer; b) Maskless digital layer printed on a 200mm wafer; c-d) Enlarged circuit features printed on a 200mm wafer; and e-f) 0.8-1µm line printed on a 200mm wafer.

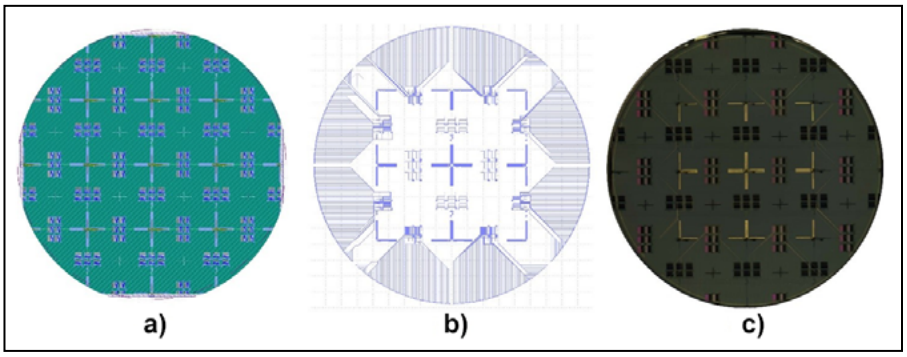

Figure 3: a) Stitched reticles; b) Digital layer to interconnect the stitched reticle; and c) Maskless digital layer interconnected stitched reticle [2].

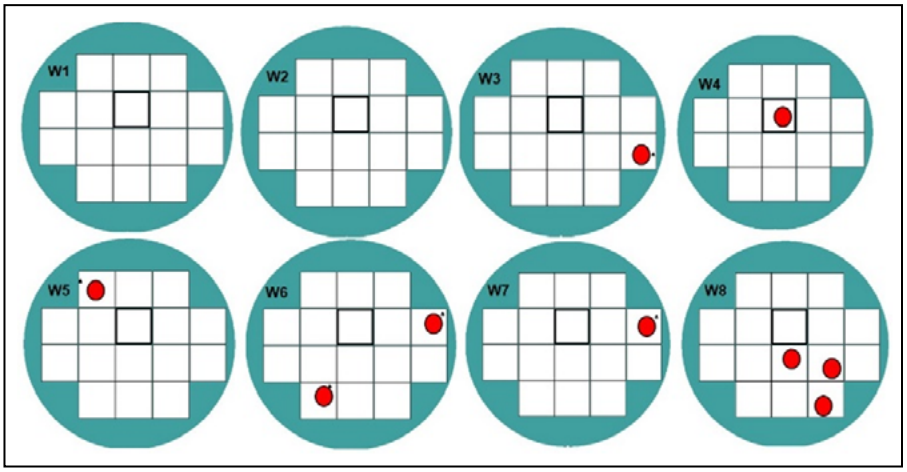

Figure 4: Reticle yield wafer map for MCM prior to the digital layer. Each MCM run produced eight wafers, each consisting of 16 individual 32mm × 32mm reticles. The red dots represent defect-based yield loss of the reticle.

the minimum description length (MDL) principle. Inline optical defect inspection tools can be used to detect defects in nominally-equivalent adjacent reticles; however, MDL does not have repeated identical patterns, which are necessary for typical comparison algorithms. In the absence of the applicability of traditional optical defect inspection methods to MDL, we propose training AI image recognition to identify defects in the MDL. It is also possible to use machine learning to train the design files, assembly net list, bill of materials (BOM), interconnect data, cross section, drawings, assembly sequence, and chiplet list. AI can generate a digital layer specific to an individual wafer to address reticle defects, and possibly re-route the signal to create a fully-functional wafer-scale fabric.

Heterogeneous integration

In this section, we discuss heterogeneous integration and the thermal analysis of a wafer-scale system in the next section. The heterogeneous integration process is based on thermocompression bonding of micro-bumps to combine various integrated circuit (IC) technologies and interconnects in a wafer-scale friendly process flow. Here, we describe heterogeneous integration with chip sizes up to 20mm X 20mm and an interconnect pitch down to 5µm. A series of metal- and metal-solder-based micro-bumps ranging from 1.5µm to 2.5µm diameter were fabricated on a 200mm wafer for 5µm pitch development.

Figure 5 shows micro-bumps on a 200mm wafer to develop interconnects for creating 5µm pitch flip chips. **Figure 5a** shows a representative example of an optical image of a wafer fabricated with tin (Sn) bumps with a minimum bump diameter of 1.5µm for 5µm pitch flip chips. A metal-solder micro-bump-based daisy chain test structure was designed to evaluate 5µm pitch flip-chip devices. The design used DUV lithography to fabricate 1.5-2.5µm diameter bumps of 5µm pitch flip chips. For example, DUV lithography has been used to fabricate under bump metal (UBM) as well as Au, In, and Sn micro-bumps to provide UBM-to-UBM (bumpless), Au-to-Au (i.e., metal-to-metal), Au-to-In (metal-to-solder), Au-to-Sn, In-to-In, and In-to-Sn interconnect combinations for flip-chip bonding. **Figure 5b** shows a representative SEM image of 1.5µm bumps for the daisy-chain test structure prior to bump bonding. The flip-chip daisy-chain devices were attached to the circuit board for the electrical continuity evaluation. The initial flip-chip bonded samples with 1.5-2.5µm gold bumps bonded to 1.5µm tin (gold-to-tin combination) showed low resistance.

Thermal analysis

As a case study, we investigated thermal architectures that could enable high-power-density multi-chip wafer operations while maintaining the low SWaP of the system. This analysis is based on a 200mm wafer bonded with 20 20mm × 20mm chips with total power uniformly split among the chips, as shown in **Figure 6a**. The cooling systems must transfer heat to

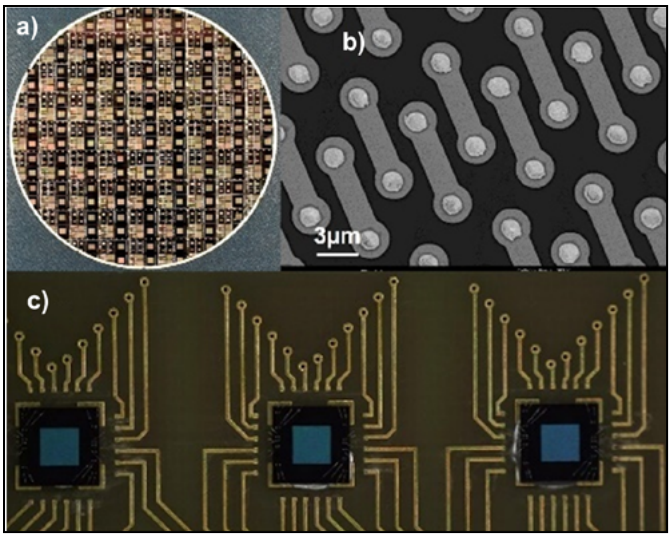

Figure 5: Optical and SEM images before and after completing of the 5µm-pitch flip chip: a) Optical image of a tin-bumped 8-inch wafer; b) SEM of a patterned 1.5µm bump for a 5µm pitch flip-chip daisy chain deposited on the metal pad of the chip/interposer/chip carrier; c) Optical image of a 5µm pitch flip-chip daisy chain attached to a circuit board for resistance testing.

30°C ambient air with a maximum SWaP of $1ft^3$ volume, 70 lb mass, and 350W power consumption. The maximum allowable wafer power was calculated for each cooling type to maintain the chip-junction temperature below 125°C.

The copper heat sink is a high conductivity material, allowing for in-plane spreading of the heat. The through-thickness temperature rise in this component was calculated assuming all the heat transfer occurs through the top surface of each chip, and effective copper cross-sectional area was assumed to be double that of the chips, which is half of the total copper heat sink area. The heat transfer into the wafer was assumed to be negligible.

Each cooling system was evaluated using a common framework as shown in **Figure 6b**. The heat was generated uniformly on the bottom of each chip and flowed up through the chip's 0.7mm thickness of silicon, followed by a 0.05mm thick indium solder joint. Heat transfer to the wafer below each chip was assumed to be negligible. Each chip on the wafer then joined a single common copper heat sink with a thickness of 12.7mm. To account for partial heat spreading, effective cross-sectional area of the copper was assumed to be double that of the chips, and half that of the copper heat sink. The temperature on the top surface of the copper heat sink was assumed to be uniform. Each candidate cooling system then interfaced with the copper plate and rejected the heat to ambient air.

The four candidate cooling systems investigated were heat pipes, traditional liquid cold plates, micro-channel cold plates, and jet impingement. The additional SWaP for the ultimate rejection of heat to ambient air was accounted for using scaling of other known liquid-to-air heat exchange systems and water was chosen as the heat transfer medium.

For each candidate cooling system prediction, the performance was scaled to represent a system that matched the size of our example wafer. The heat pipe air-cooling performance was based on Dynatron U9 [4], an aluminum-finned heat-pipe embedded air cooler, and thermal resistance was scaled to 0.011°C/W. The performance of a traditional cold plate was estimated using performance data from Boyd Corporation round-tube liquid cold plates [5], and thermal resistance was scaled to 0.008°C/W. The performance of the micro-channel liquid cold plates was based on Boyd Corporation's porous metal liquid cold plate specifications [6], and thermal resistance was scaled to 0.003°C/W. The heat transfer of impingement jets was calculated using the Nusselt correlation of Jiji and Dagan (**Eq. 1**) [7], which resulted in a thermal resistance of 0.002°C/W.

$$Nu = 3.84Re^{1/2}Pr^{1/3}\left[0.008\frac{Ln}{d}+1\right] \quad \text{(Eq. 1)}$$

The overall thermal performance is governed by the choice of the candidate cooling system, and significant performance improvements can be realized with more advanced technology, as seen in **Figure 6c**. With air-cooled heat pipes, the maximum wafer power was 3kW, which corresponded to a per-chip power

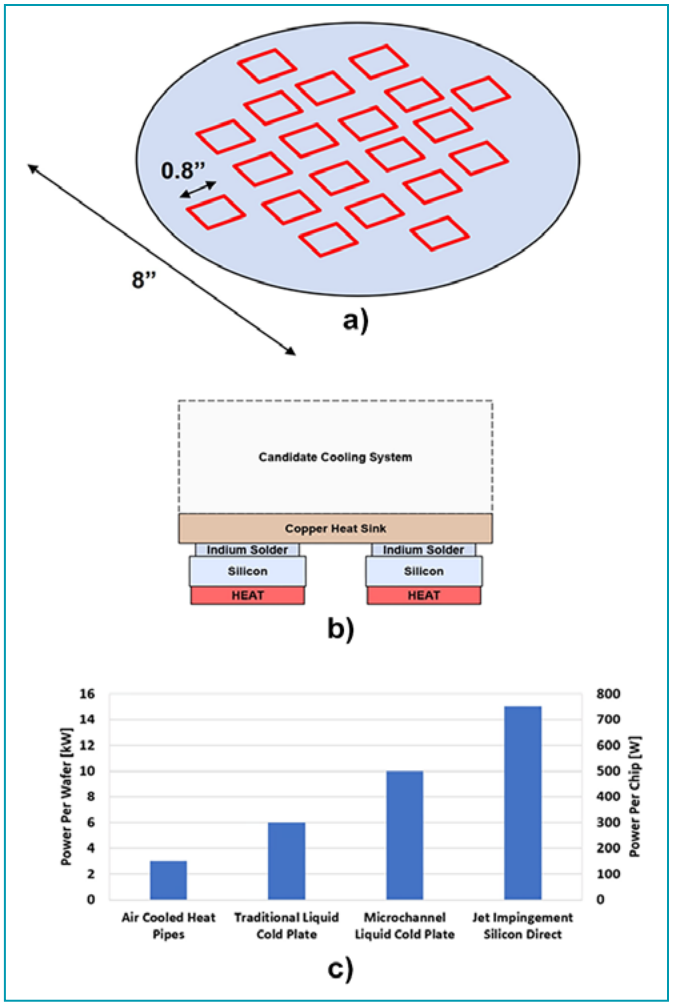

Figure 6: Thermal solutions: a) Schematic of twenty 20mm x 20mm chips uniformly spaced on a 200mm wafer to create a SoW; b) Representative cross-sectional area of a SoW; and c) Thermal performance of SoWs: Air cooling with heat pipes, traditional liquid cold plates, micro-channel liquid cold plates, and jet impingement on silicon.

of 150W. The maximum wafer powers for the traditional liquid cold plate, micro-channel cold plate, and jet impingement on silicon were 6, 10, and 15kW, respectively. It was assumed that the jet impingement bypassed the copper heat sink and impinged directly on the silicon of each chip. Integration may be more challenging for jet impingement; however, this has not been explored further here.

Summary

The goal of high-performance computing scalability, beyond traditional heterogeneous integration, is to drive greater wiring densities and functionality into a single package. One way to address this demand is the use of heterogeneous integration of wafer-scale fabric with micro-bump-based interconnects to produce electrically chip-like interfaces for low-power chip-to-chip communication.

We propose a fabrication-informed optimization of a wafer-scale active fabric for heterogeneous integration. This fabric allows the heterogeneous integration of known-good chiplets to create systems that perform as multi-chip SoWs. Using this approach, wafer-scale systems can be fabricated using advanced node chips. A key focus of this study was to address the scaling and associated thermal challenges faced when building large-scale processors. The initial thermal analysis indicated that wafer-scale systems can support a wide variety of high-power chip designs.

The decision tree used a combination of EX4, I-line, and laser direct-write photolithography to demonstrate a wafer-scale platform. These combined features show the potential to scale the integration platform technology with high-density and low-resistance interconnects to the entire wafer, enabling system integration for next-generation HPC systems.

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References

1. S. L. Murali, "Artificial intelligence in VLSI physical design of circuits to optimize power, performance and area (PPA)," International Research Journal of Engineering and Technology (IRIET), vol. 11, no. 10, pp. 266-270, October 2024.
2. R. N. Das, et al., "Waferscale S-MCM for high performance computing," IEEE 70th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2020, pp. 582-588, doi: 10.1109/ECTC32862.2020.00097.
3. R. N. Das, et al., "Interconnect scheme for die-to-die and die-to-wafer-level heterogeneous integration for high-performance computing," IEEE 69th ECTC, Las Vegas, NV, USA, 2019, pp. 1611-1621, doi: 10.1109/ECTC.2019.00248.
4. https://www.boydcorp.com/thermal/liquid-cooling-systems/liquid-cold-plates.html
5. https://www.dynatron.co/product-page/u9
6. https://info.boydcorp.com/hubfs/Thermal/Liquid-Cooling/Boyd-Thermacube-Datasheet.pdf
7. L. M. Jiji, Z. Dagan, "Experimental nvestigation of single phase multi-jet impingement cooling of an array of microelectronic heat sources," Proc. of the International Symposium on Cooling Technology for Electronic Equipment, Pacific Institute for Thermal Engineering, Hawaii, pp. 265–283, 1987.

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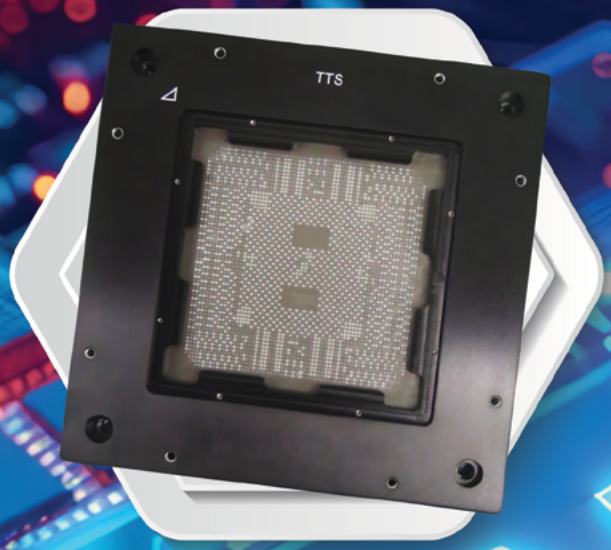

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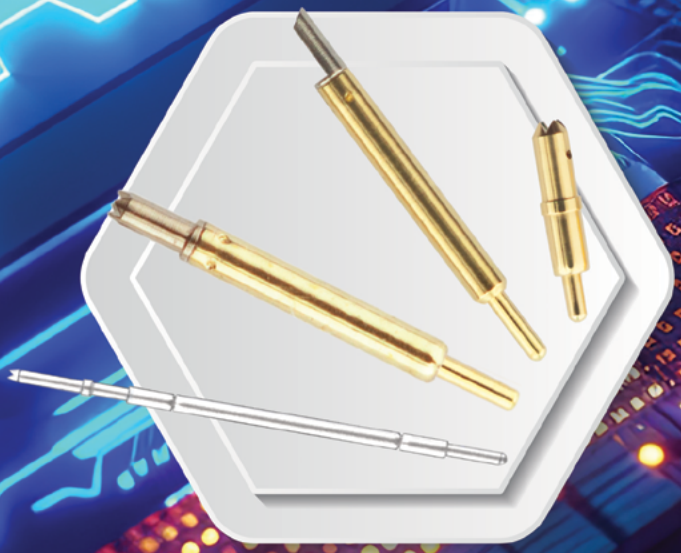

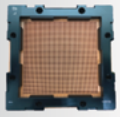

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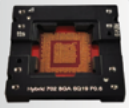

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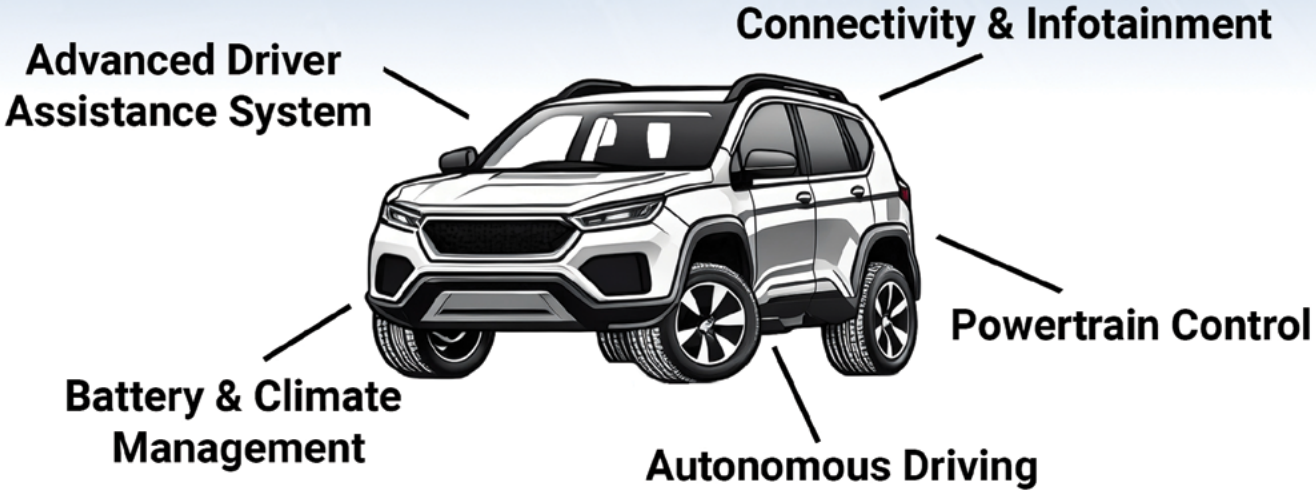

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Integrated stress analysis: A critical capability for next-gen 3D IC design

By Shetha Nolke [Siemens EDA]

The benefits of 3D integrated circuit (IC) assemblies are well-documented: Smaller IC footprints integrated with lower-technology interposers and substrates allow high-performance functions to be designed on leading-edge nodes while relying on established nodes for less complex integrative tasks. Additionally, 3D packaging can enable smaller form factors and potentially reduce power consumption while increasing performance. While the advantages of the heterogeneous design methodology have been proven, there are more benefits yet to be discovered.

Building ICs in 2.5D and 3D introduces many new challenges. Each product and design will require critical tradeoffs, weighing the risks and benefits. The opportunities for failed chips abound. As the semiconductor industry embraces heterogeneous 3D IC designs for applications like high-performance computing (HPC), automotive and Internet of Things (IoT), it will be critical to eliminate systemic sources of failure across all three physical dimensions. One particularly problematic failure mechanism is caused by thermo-mechanical stress: Heat can create stress, and stress can create circuit mobility changes that impact device functionality and reliability.

Challenges of heterogeneous 3D ICs

The move to heterogeneous 3D IC architectures brings a host of new design challenges that must be carefully navigated. As chip designers integrate multiple dies and technologies into a single 3D package, the interactions between the chip and package become increasingly complex and critical to overall device functionality. Compared to traditional 2D ICs, 3D ICs introduce new failure mechanisms that can severely impact reliability. The thinning of dies, use of new interconnect materials, and thermal stresses from the packaging process can all lead to issues like die cracking, solder joint fatigue, warpage and delamination, which are discussed in the sections below.

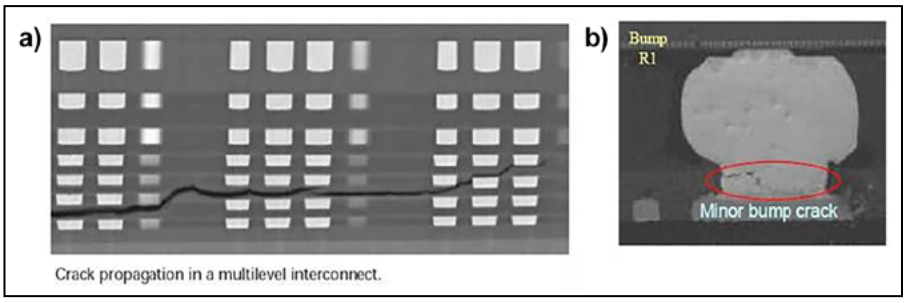


Figure 1: A scanning electron microscopic (SEM) image: a) (left) Of a crack propagating through multiple levels of interconnect; and b) (right) A small crack in a bump.

Die cracking. Die cracking can lead to complete device failure. This is often caused by the thermal mismatch between the thinned silicon die and surrounding package materials. As the package undergoes temperature cycling during assembly and operation, the differential expansion and contraction can induce high stresses that crack the brittle silicon (**Figure 1**). The problem is exacerbated by the use of thinner dies in 3D ICs, which have less structural integrity.

Solder joint fatigue. Solder joint fatigue is another major reliability risk. The repeated thermal and mechanical stresses experienced by solder interconnects during power cycling can cause them to gradually degrade and fail over time. This is a particular challenge for 3D ICs, which often utilize fine-pitch, high-density solder connections to enable the vertical stacking. Improper design of the solder joints and package architecture can accelerate this fatigue process.

Package warpage. Package warpage can lead to interconnect failures and mechanical damage. Warpage is caused by the complex interactions of thermal expansion mismatch, residual stresses, and package asymmetry. As the 3D IC package is subjected to temperature changes, the differential expansion of materials can cause the overall structure to bend and deform. Excessive warpage can lift solder bumps, disrupt electrical connections, and even crack the die (**Figure 2**).

Delamination. Delamination, or the separation of material layers, can occur at interfaces between the die, interconnects, and package substrates due to poor adhesion or thermal-mechanical stresses. Delamination disrupts heat transfer paths and creates localized stress concentrations that further propagate the failure.

The mechanical failures noted above are readily visible, but there are also more insidious device-level stresses that can cause subtle electrical changes and functional failures. For example, piezoresistive effects can alter the electrical characteristics of transistors

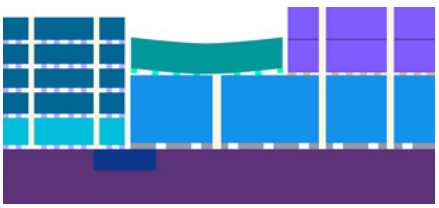


Figure 2: An illustration of die-level warpage.

and other devices when subjected to mechanical stress, impacting overall circuit performance. This is a particular concern for sensing applications that rely on piezoelectric transduction. Failing to properly model and mitigate these chip-package interaction effects can result in 3D ICs that do not meet their intended specifications, even after manufacturing.

Addressing these stress-related challenges is absolutely essential for the successful adoption of 3D IC technology across high-performance computing, automotive, IoT and other markets. Designers must have the tools and methodologies to accurately simulate mechanical stresses throughout the 3D IC assembly, from early feasibility analysis to final design sign-off. Only then can they identify and resolve potential failure modes before committing the design to manufacturing.

Root causes of 3D IC stress

Some risks in 3D ICs have already been identified and addressed, forcing innovation in the way that these packages are designed and assembled. Most risks are still in discovery, as new configurations of assembly and package yield new ways for failures to occur. Probably the best understood concept of connecting devices and ICs in a 3D configuration is validation of design intent (i.e., design rule checking [DRC]) and circuit intent (i.e., layout vs. schematic [LVS]) within and among various components.

Less well defined is the understanding of how the power input may be converted into heat, and how heat may or may not be able to disperse within the devices and package. Another area of thermo-mechanical impact occurs during the chip packaging flow/reflow, where the temperature gaps exceed both typical system-on-a-chip (SoC) processing temperatures and power-induced thermal loads. These unavoidable thermal loads, thinned dies and the nature of the metal/dielectric material properties combine to exacerbate the risk of mechanical failure within the die. As with any failures, mechanical changes in the package don't only imply mechanical impacts, but also imply electrical influences due to well-defined piezoresistive effects [1].

The impact of stress on 3D IC reliability

While all circuits integrated at the die level could be impacted by chip-package stress, certain types of devices that require extra reliability will be most at risk for failures. Specifically, devices that use piezoelectric changes to determine device function will require early modeling and validation that neither packaging process, nor operating temperature ranges (that can range widely for automotive purposes), will put the device out of specification for piezoelectric mobility changes. This level of reliability will also be required for sensors integrated in health monitors, smartphones and even IoT, transportation and infrastructure devices. To ensure reliability it will be key to verify, both in the early design phase and final sign-off mode, that the circuit-level performance will not be negatively impacted by chip/die level stress.

Evaluating stress in 3D IC packages

Evaluating 3D IC package stress seems intuitive in theory—how difficult could it be to calculate a simple physical model of stress? In fact, the physics component of this problem is the easiest part to solve. However, the reality is that there are several crucial steps of due diligence that must be undertaken before any meaningful stress calculations can be performed.

The first and most critical task is to accurately describe the 3D IC package in granular detail, accounting for everything from the millimeter-scale package substrates down to the nanometer-scale features within the chip design layers. As a chip designer, it is essential to collaborate closely with the package design team—both at the foundry and outsourced semiconductor assembly and test (OSAT) levels—to fully understand the package components and assembly process. This shared understanding of the package description is absolutely crucial because designers may need to make initial assumptions about materials and dimensions before the final design is complete. Leveraging standards like 3Dblox can help establish a common language for describing the package assembly.

The complexity of 3D IC packages can vary greatly, ranging from simple single-die stacks (2.5D) to intricate multi-die assemblies (3D). Regardless of the specific architecture, all 3D IC packages will require rigorous analysis to identify potential stress-related reliability impacts. This analysis may need to happen before all the package details are finalized, which calls for a modular, flexible approach. In the early pathfinding stages of design, there may be assumptions made about materials and component sizes that will later need to be updated as the package design matures.

Even if the die-level design is not yet complete, leveraging knowledge of the design technology, such as layer thicknesses, density specifications, and routing directions, can enable the creation of accurate initial estimates of stress profiles across the die. Then, as the package component designs are finalized, the package description can be updated with detailed material and size information to enable more precise stress modeling. This iterative chip-package co-design process can take months or even years, depending on the complexity of the 3D IC assembly. **Figure 3** illustrates the levels of 3D design from chiplet, to SoC, to board.

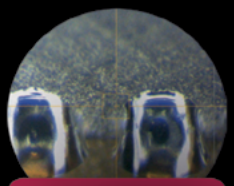
Collaborative stress evaluation across design domains

Another key consideration in evaluating 3D IC package stress is understanding who is responsible for performing this analysis, and how their unique perspectives and priorities may influence the process. Is it the IC designer, the packaging designer, or some combination of the two? Each will have their own context from which to understand the risks for failure in different parts of the product. The solution space for stress evaluation should consider all these cases in a collaborative co-optimization.

The next consideration of evaluating stress is the physical material properties of the components within the assembly. Given the multi-disciplinary nature of 3D IC assemblies, any one individual or team may only have a complete understanding of the materials and dimensions within their specific domain. For unknown components, it may be necessary to make simplified "black box" assumptions, such as treating the IC as a monolithic silicon block. While this can provide initial stress estimates, it will inherently be less accurate than a more detailed physical description of the IC stack.

Another complicating factor is the potential need to obfuscate certain

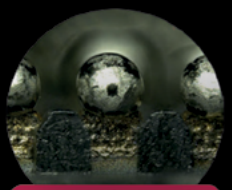
BALL PLACEMENT & LASER SOLDERING

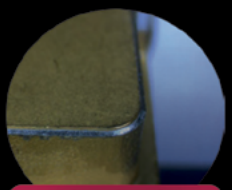

3D-Soldering

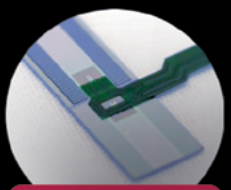

Solder Stacking


Wire Soldering


BGA Soldering


Pre-Soldering of SMD Connector Elements


Lid Sealing for Connectors & IR-Sensors

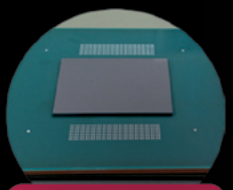

Flex to Chip Soldering

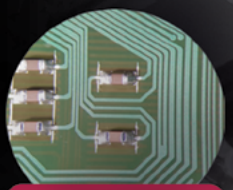

Through Hole Soldering

LASER ASSISTED BONDING (LAB, LCB, LAR)


3D Multi Layer Stacked Packaging


Optoelectronic Device Assembly


CPU on Interposer Assembly

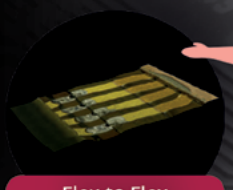

SMD Capacitor Assembly

SOLDER & CHIP REPAIR


BGA Rework


Interconnects of Camera Module


BGA Package Assembly onto Substrate


Flex to Flex Seperation

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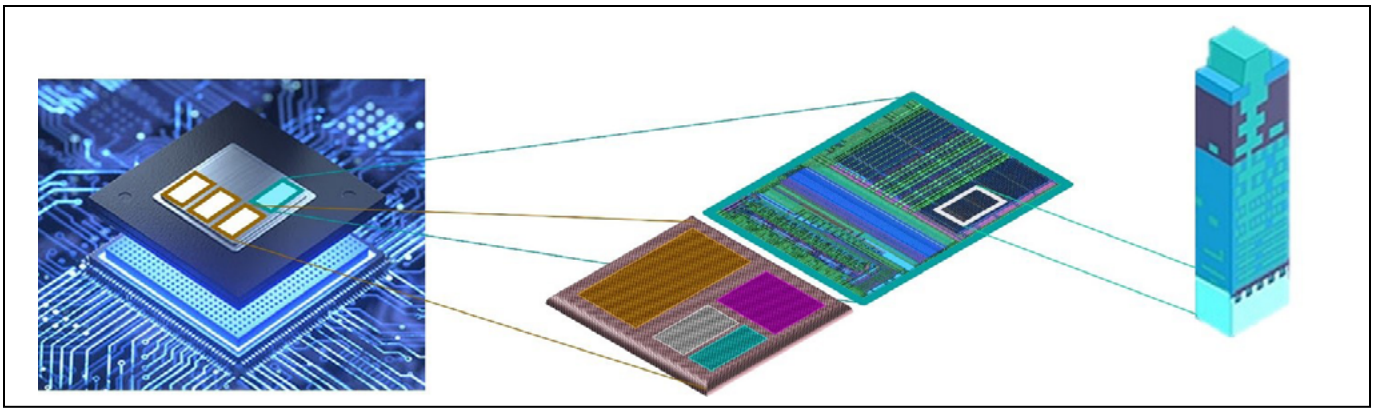

Figure 3: 3D IC assemblies need to be evaluated for stress at multiple levels of integration.

proprietary technology details and material properties, as these may be considered intellectual property by the foundry or packaging team. Navigating these confidentiality concerns while still enabling accurate stress modeling requires careful collaboration and information-sharing protocols.

Finally, it is critical to fully account for the stresses imparted by the packaging process itself, which can vary significantly across different assembly stages and local thermal environments (**Figure 4**). Especially within the IC portions of the package, adjacent materials can, and most likely will, behave very differently as temperatures change. For more accurate stress values, consider nominal temperatures vs. peak or trough values, such as annealing temperatures, or in the area of ball grid array (BGA) soldering. Capturing these process-induced stresses requires a deep understanding of the assembly flow, as well as the use of advanced finite element analysis techniques.

Interpreting 3D IC stress results

After the initial boundaries of the 3D IC package have been defined and the stress analysis has been performed, designers are faced with the critical task of interpreting the resulting stress values. The first and most obvious step is to quickly assess whether the calculated stresses have exceeded any basic material thresholds for the relevant package components. This could be as simple as a binary go/no-go determination, or it may require more complex, iterative re-analysis and design rearrangement to bring the stresses back within acceptable limits.

Early in the design process, when there are still several degrees of freedom available, a full-package stress analysis can be conducted relatively quickly, even if some reasonable assumptions must be made. This can provide valuable, informative results that allow chip-level designers to carefully consider the package composition and its potential impact on the die-level design.

As the package planning and design progress, and the component placements become more locked in, the focus can shift to evaluating the specific interfaces between the package and the integrated chiplets or ICs. By understanding the stress profiles at these critical junctions, designers can identify regions where placement of sensitive devices should be avoided. Additionally, "what-if" analyses may be necessary to determine whether the specific macro placements within the chiplet will exceed mechanical or electrical stress thresholds based on their location within the overall package.

Finally, once the full 3D IC assembly has been defined, a comprehensive sign-off analysis of the chip-package interaction stresses must be performed. This will validate that the circuit performance remains within acceptable tolerances, ensuring the reliability of the completed product. **Figure 5** illustrates some of the visual stress distribution mapping that can be leveraged in this final validation step.

Beyond the initial go/no-go stress assessments, designers may need to consider a variety of other analysis techniques and visualization methods. Detailed, region-specific evaluations can provide insight into localized areas of concern, while more global package-level analyses can reveal broader stress patterns and trends. In addition to normal stress values, factors like shear stress, warpage/offset, and even piezoresistive impacts on device mobility may need to be considered.

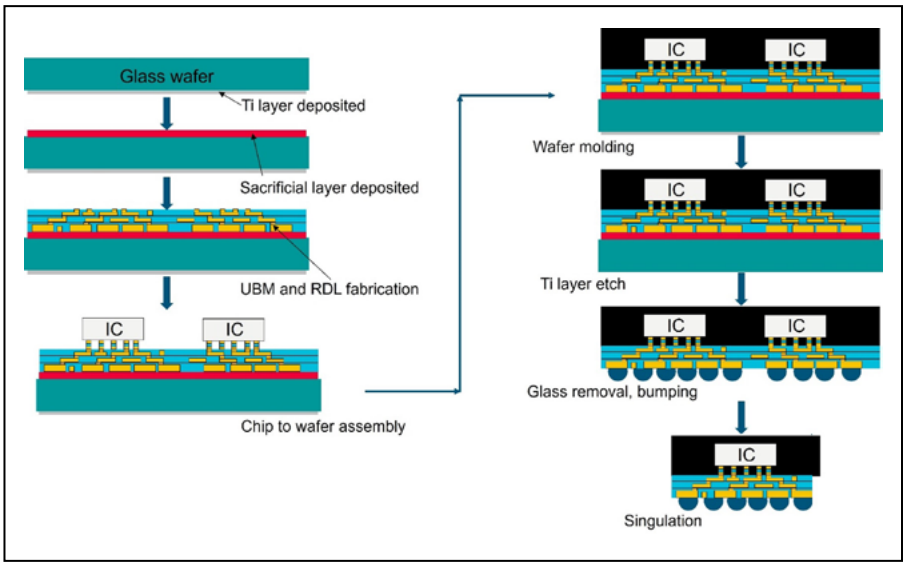

Figure 4: Stresses can be imparted throughout the 3D IC package assembly flow.

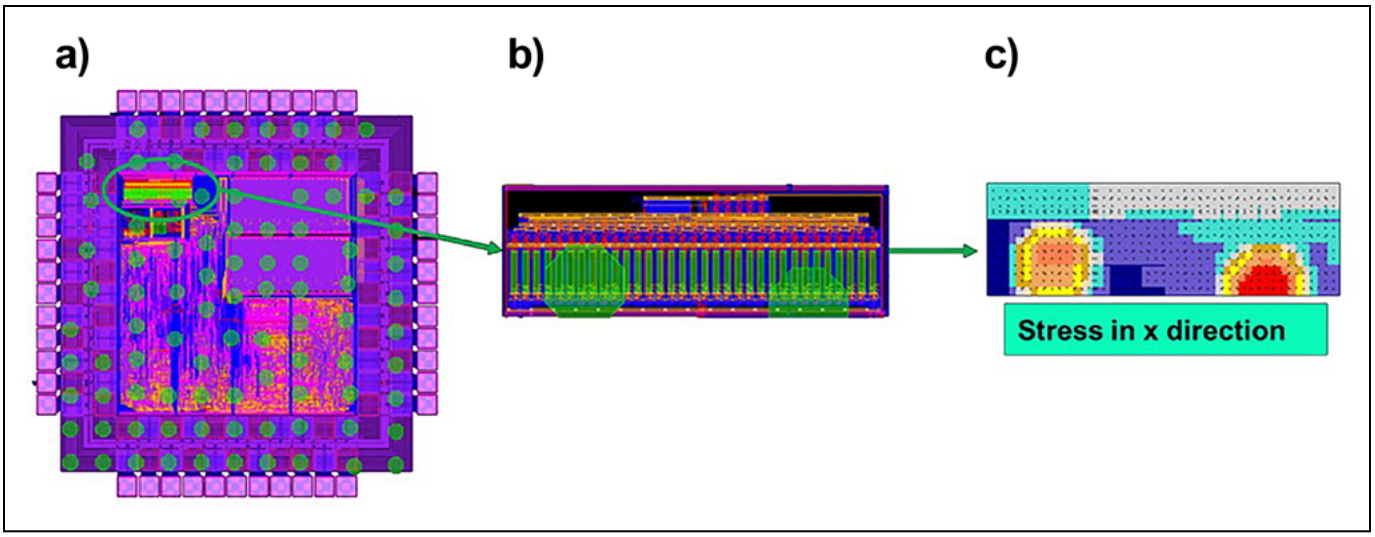

Figure 5: Stress distribution maps: a) (left) Highlighting a device/cell of interest on a chip design with bumps; b) (middle) A close up of the device/cell of interest; and c) (right) A view of stress in the x direction in the device/cell of interest, showing stress resulting from bumps.

Ultimately, these diverse stress analysis approaches all offer unique and valuable information about how the calculated stresses will impact the performance and reliability of the 3D IC design. Some focus more on the overall quality and integrity of the packaged device, while others delve deeper into the implications for individual circuit components and their functionality. Both perspectives are crucial for ensuring the successful development of these complex heterogeneous systems.

The understanding of piezoresistive behavior and its impact on circuit performance has become so critical that some designers are exploring methods to directly model and back-annotate these stress-induced electrical effects into the LVS extraction and verification process. This holistic approach to stress analysis and mitigation is essential for unlocking the full potential of 3D IC technology [2].

The path forward for 3D IC stress management

Clearly the shift to heterogeneous design and advanced packaging has introduced a whole new level of complexity. But, the same is true of all new technologies since the introduction of the point contact transistor over a century ago. Physics has been in the driver's seat for the entire journey and it's not soon likely to give up the wheel. As we navigate this new terrain in 3D, the complexity of physical verification will require the ingenuity of many to converge on stable, reliable and consistent results, for both inspection and manufacturing of 3D IC products. For mechanical and electrical reasons, physical stress will become a major player in the game of successful design at die and package levels.

Summary

The simulation tools that can perform the type of 3D IC thermo-mechanical stress evaluation discussed in this article have mostly been custom in-house software, but commercially-available tools are coming to market that can provide a more comprehensive and integrated approach to this challenge. Commercial electronic design automation (EDA) tools can provide a tighter integration with the design data and tools that IC and package engineers already use, streamlining the overall workflow. Perhaps most importantly, commercial solutions enable a more collaborative, co-optimization approach between the IC and package design teams—an important capability given the intricate interplay between the two domains. As the complexity of 3D ICs continues to escalate, access to such automated, integrated stress analysis tools will be essential for ensuring reliable, high-performance designs.

References

1. P. W. Bridgman, "Some properties of single metal crystals," Proc Natl Acad Sci U S A. 1924 Oct;10(10):411-5. doi: 10.1073/pnas.10.10.411. PMID: 16576849; PMCID: PMC1085739.
2. A. Kteyan, et al., "Novel methodology for assessing chip-package interaction effects on chip performance," ISPD '22: Proc. of the 2022 International Symp. on Physical Design:83-89. doi: https://doi.org/10.1145/3505170.3511798

Biography

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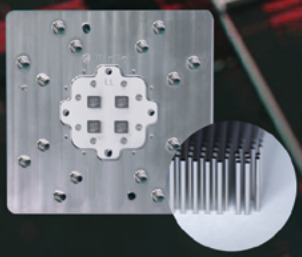
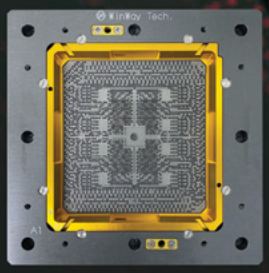


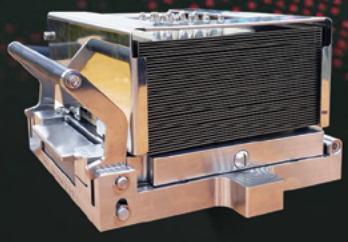
Vertical Probe Card

Minimum pitch : 75 um
High pin count ≤ 35,000pins



Coaxial Socket

SerDes 224Gbps PAM4
Supports up to 30,000 pins

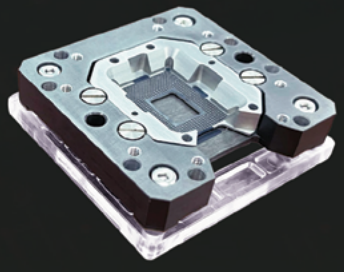


Functional Burn-in

High Power 1000W
High Speed PCIE Gen5 32Gbps

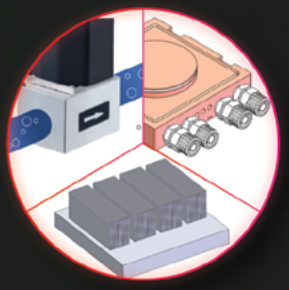
Spring Probe

In-house manufacturing



Optical Socket

SerDes 224Gbps PAM4
Optical alignment



Thermal Product

2000W cooling capacity
Temperature : 20 to 150°C

Glass-based 3DHI transmit and receive system-in-package

By Jeb H. Flemming, Rob Hulsman, Ed Horne, Kyle McWethy, Craig Willis [3D Glass Solutions, Inc.]

A manufacturing platform for the production of vertically-stacked glass substrates with heterogeneously-integrated surface mount devices for advanced radio-frequency (RF) systems-in-package (SiP) is presented. This work includes the design, fabrication and assembly of a true 3D heterogeneously-integrated vertically-assembled half-duplex 6-12GHz Tx/Rx module using four stacked-glass layers with 14 embedded components that have excellent simulation vs. measurement agreement. Furthermore, we present early work on thermocycling environmental reliability test data and key design components (e.g., low-loss 50Ω vertical interconnects) that produce low-loss RF SiPs. In this article, we present design, production, and assembly considerations that impact size, weight, and performance (SWAP) metrics for a variety of product definitions.

Introduction

The push for higher communications frequencies, greater system integration, and smaller space requires many unique challenges on RF and packaging engineers in the development of next-generation cellular products for 5G, WiFi 6, military, and other applications. Furthermore, RF systems are utilized in a variety of systems including radar, communications, electronic warfare, and navigation. Reductions in size and weight of these next-generation wireless devices allow for lower payload costs for airborne applications and longer battery life for wearable applications. Traditional materials, such as low-temperature co-fired ceramics (LTCC), organic laminates, and silicon, face major limitations to dramatically improve system SWAP. For better or worse, decades of innovation have brought these materials to the latter half of their innovation cycle.

Photosensitive glass-ceramics (PSGs) have gained a lot of attention as a next-generation RF packaging substrate for a variety of reasons. Glassy materials provide a smooth, strong, and transparent backbone for the formation of electrical redistribution networks, solder resist, and chip-on-board assembly. Glassy materials also have ideal properties for RF, mmWave, and terahertz applications.

The innovation challenge is to change the paradigm from: 1) Wafer fabrication, followed by 2) Packaging, to this sequence: 1) Wafer fabrication, followed by 2) "Scale-in" (glass layer fabrication), and finally, 3) "Scale-out" (stacking glass layers vertically to produce true 3D heterogeneously-integrated SiPs). This work employs photosensitive glass (PSG) as the interconnect fabric. PSGs are materials that can exist in both a glassy and ceramic phase, where micro-patterns of ceramic are selectively created through a simple three-step process (expose, bake, and etch), whereby the ceramic phase is selectively etched (60:1) to form complex anisotropic 3D structures (e.g., through-glass vias (TGVs), cavities, and conductor undercuts) and the resultant product is typically 100% glass. PSG benefits include:

- Use of an inexpensive, high-throughput batch manufacturing process to selectively-create precise (3σ=2.5µm) 3D structures, including: Densely packed copper-filled TGVs with thick multi-layer copper redistribution layers (RDLs) on the top and bottom sides to minimize interconnects' distances (and therefore, parasitics) and electrical/thermal resistance.
- In-glass microfluidic heat exchangers that use high-density TGV arrays for: 1) Thermal transfer through very large surface area via arrays and conductive heat transfer, and 2) Vertical I/O interconnects capable of integrating multiple RDL layers per side with direct die integration.
- Cavities (extending through the full glass layer or partial depth cavities) to embed active and passive components and to construct high-gain antennas, air/magnetic core inductors, and air-filled substrate integrated waveguides for mmWave applications up to 500GHz.
- Micro-Faraday cages using TGVs to provide >60dB shielding (isolation) enabling tighter embedded component integration.
- 8.5ppm/ºC coefficient of thermal expansion (CTE) from -77°C to 350°C, which improves reliability by bridging the CTE mismatch between disparate materials such as silicon, copper, and printed circuit boards (PCBs).
- Smooth surface (<10nm rms) and excellent balance of hardness and ductility, enabling fabricating thick multi-level RDL interconnects on both sides and embedding many diverse components.
- High radiation capability: Rad-hard for defense applications (>400K Rads).
- Unique composition enables stronger polymer and metal adhesion compared to other glasses.

In this article, we present our work using PSG for 3D heterogeneous packaging solutions. We will share the advantages of using PSG for advanced RF packages and our work towards building vertically-stacked glass packages for advanced RF SiPs.

Design, assembly, and testing

The next sections discuss various aspects of design, assembly and testing of 3DHI SiPs.

50Ω vertical interconnects. An important design feature in 3DHI SiPs is the ability to transmit RF signals vertically through a glass stack with low loss. We have designed a broadband, low-loss, 50Ω vertical interconnect. **Figure 1** shows the use of a vertical signal path, surrounded by ground vias—all interconnected using solder glass-to-glass interconnects.

The simulated performance of the designed 4-layer vertical stack demonstrates 0.21dB of insertion loss at 20GHz with broadband performance out to 100GHz, with 0.85dB of insertion loss at 80GHz.

6-12GHz half-duplex TxRx SiP. To demonstrate the benefits outlined above, we designed, simulated, produced, assembled, and tested a 6-12GHz half-duplex transmit and receive (TxRx) SiP that consists of two RF switches, power amplifier, low-noise amplifier, and 10 passive surface mount components (e.g., capacitors).

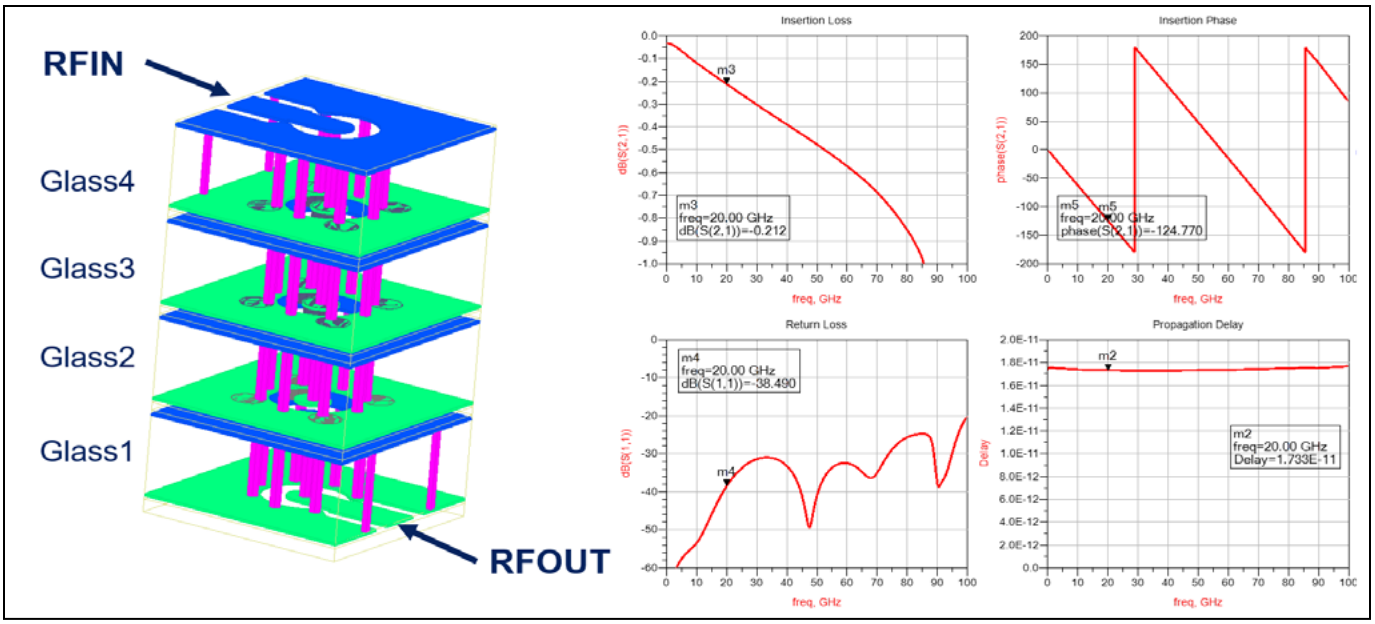


Figure 1: The layout and simulation of a broadband 50Ω vertical interconnect designed to efficiently transmit RF signals across four different glass layers with very low loss.

The designed TxRx module leverages the following:

- Heterogeneous material integration of GaAs, GaN, and silicon;
- Heterogeneous integration of wire bond, ribbon bond, solder-based surface-mount technology (SMT) and flip-chip assembly techniques;
- Cavities and tightly-spaced TGVs to create micro-Faraday cages around active devices enabling them to be packaged closely together;
- High-density TGV arrays for effective signal and ground routing and efficient thermal removal;
- High-density solder ball interconnects for effective signal and ground routing and efficient thermal removal; and
- Use of a land grid array assembly structure for PCB assembly.

The designed system incorporates a total of four glass layers, 9 integrated cavities, 14 embedded components packaged within a 7mm x 8mm x 1.2mm (height) system footprint representing an approximately 60% reduction in footprint and a 25% reduction in weight over a PCB with an equivalent build of materials (Figure 2).

SiP production included: 1) The production of the four different glass layers; 2) The assembly of the active and passive components onto individual glass layers; 3) The assembly of populated glass layers together, and then finally, 4) The solder attachment of the SiP to a PCB test board. Glass layer-to-layer assembly was performed using solder balls and great care was taken to keep the bond line thickness consistently between 30-50µm. Using this process, vertical RF transmission lines were measured to be 50Ω +/-1Ω. Figure 3a shows a top-down X-Ray showing the various building blocks of the fully-assembled device.

After assembly to the test board, the RF performance of the system was tested. The measured results were compared against simulated performance in Figure 4.

Thermocycling reliability studies. To investigate the long-term reliability of such multi-glass layer SiPs, we designed, built, and assembled a 4-glass layer 2-15GHz Wilkinson power divider. This system consisted of similar design features to the above discussed TxRx SiP, including: 1) Cavities; 2) Vertical 50Ω interconnects and surface-mounted devices (resistors); 3) High-density TGV usage for signal, ground, and thermal management; and 4) High-density glass-to-glass solder interconnects for signal, ground, and thermal management.

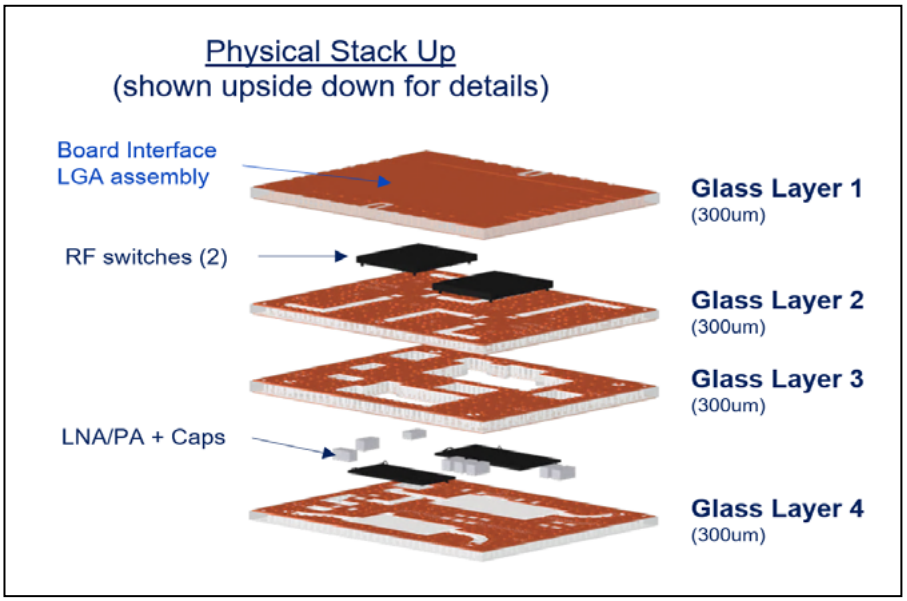


Figure 2: An exploded view of the designed TxRx SiP shown upside down. The illustration shows the land grid array SiP interconnect pads for PCB assembly and the location of the LNA, PA, RF switches, and SMT capacitors.

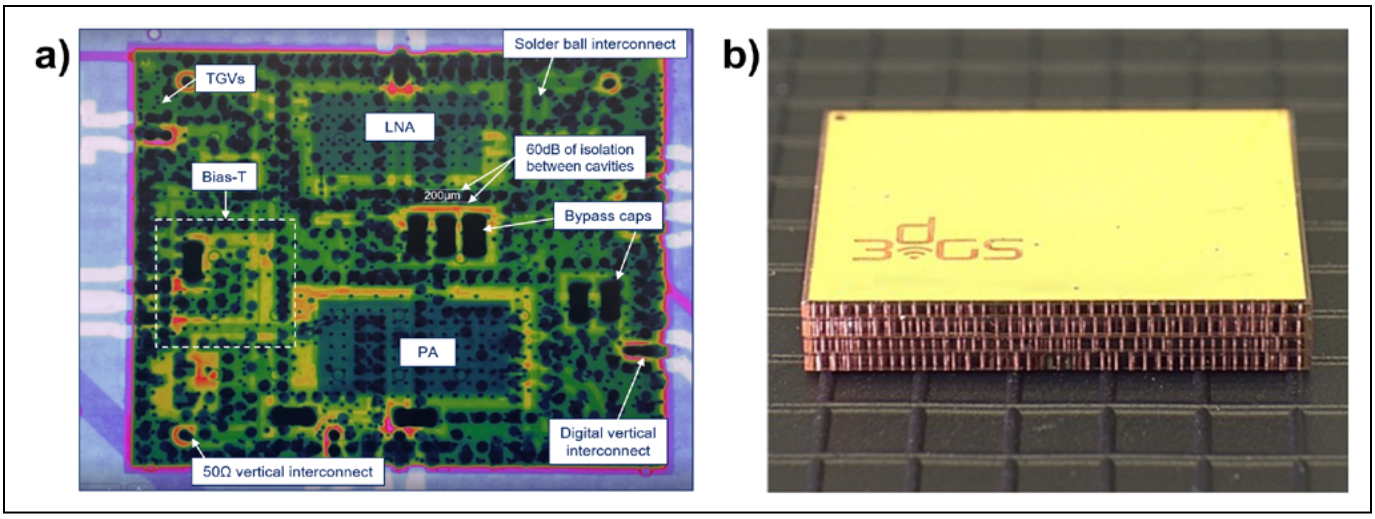


Figure 3: a) (left) A top-down X-ray showing the LNA, PA, bypass capacitors, as well as RF and digital interconnects; b) (right) Side view of the SiP showing the four glass layers and TGVs.

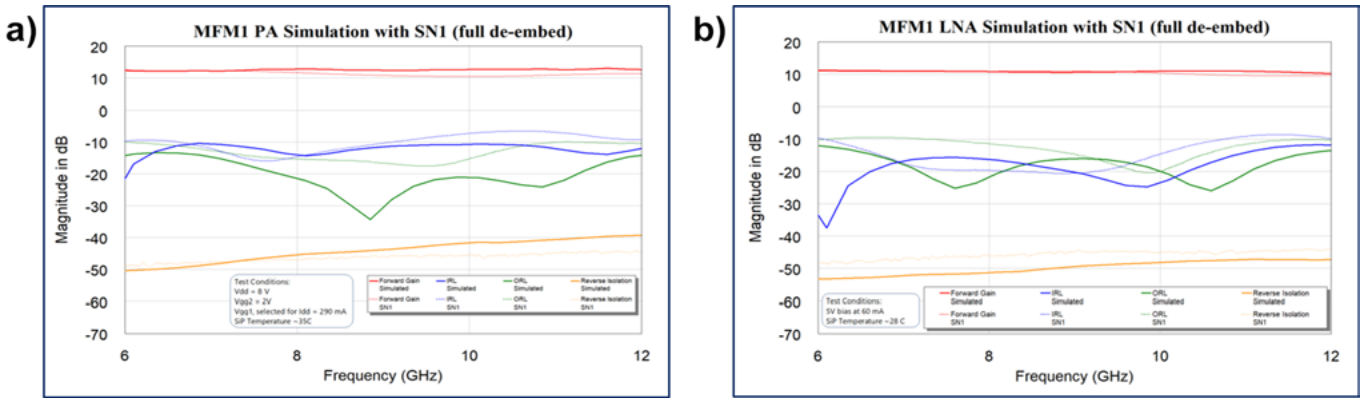


Figure 4: The simulation and measured performance of the designed TxRx SiP for both the: a) (left) Power amplifier signal path; and the b) (right) Low-noise amplifier signal path.

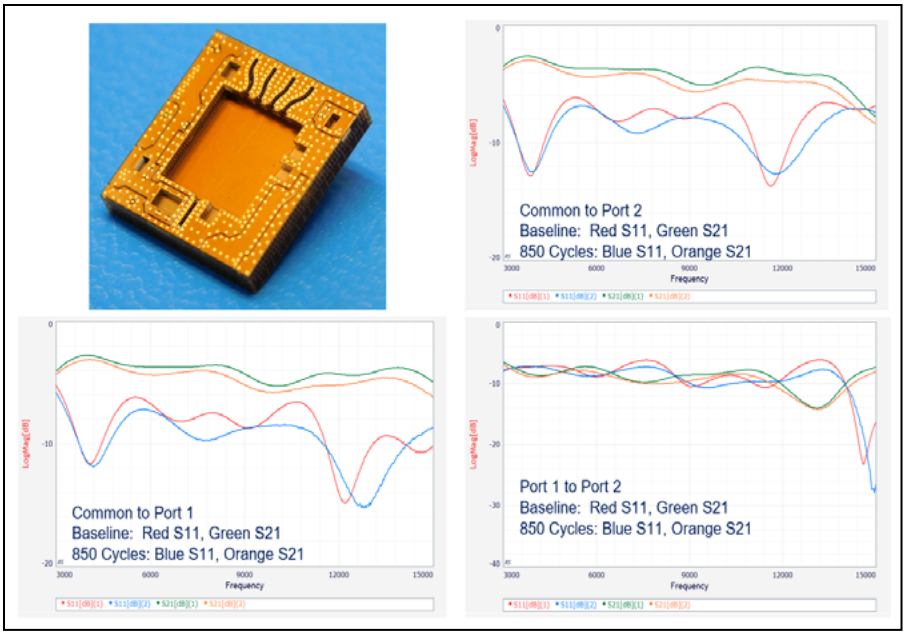


Figure 5: Measured performance of a 2-15GHz four glass-layer Wilkinson power divider (see the inset photo) before and after 850 thermocycles (-40°C to 125°C). The plots measure each pair of the three-port system.

The data presented in Figure 5 shows the data collected pre- and post-850 cycles of JEDEC A104, condition G (-40°C to 125°C). As can be seen in the data, overall there is a high degree of correlation in pre- vs. post-thermocycling measurements, without any significant degradation in performance. Slight mismatches noticed in measured performance can be attributed to variation in RF probe contact to the electrical pads because unoccupied solder pads were used for RF measurements vs. probing on designed ground-signal RF launches.

Summary

In this work, we have demonstrated a holistic approach to 3D stacking of glass layers for the formation of systems-level devices requiring 3DHI. The initial design ecosystem was validated through device testing with high correlation. Furthermore, assembly techniques have been instituted that validate long-term reliability based upon JEDEC standards.

Acknowledgments

The authors would like to thank the entire 3DGS design, production, assembly, and test team for their assistance in producing the above components. Portions of this article were presented at IMAPS/DPC 2025.

References

1. X. Mi, O. Toyoda, S. Ueda, F. Nakazawa, "A 3D heterogeneous integration method using LTCC wafer for RF applications," IEEE International 3D Systems Integration Conf. (3DIC), Osaka, Japan, 2011, pp. 1-5.
2. M. Manley, A. Kaul, M. S. Bakir, "Design space exploration for power delivery network in next generation 3D heterogeneous integration architectures," IEEE 74th Electronic Components and Technology Conf. (ECTC), Denver, CO, USA, 2024.
3. T. M. Hancock, J. C. Demmin, "Heterogeneous and 3D integration at DARPA," 3DIC, Sendai, Japan, 2019, pp. 1-4.
4. R. Tummala, et. al., "Heterogeneous and homogeneous package integration technologies at device and system levels," 2018 Pan Pacific Microelectronics Symp. (Pan Pacific), Big Island, HI, USA, 2018.
5. C. Li, F. Zhang, M. Di, Z. Pan, A. Wang, "Advances in 3D heterogeneous structures and integration for future ICs (Invited)," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conf. (S3S), San Jose, CA, USA, 2019, pp. 1-3.
6. J. -M. Yook, D. Kim, J. C. Kim, "High performance IPDs (integrated passive devices) and TGV (through-glass via) interposer technology using the photosensitive glass," ECTC, Orlando, FL, USA, 2014.
7. 3D Glass Solution Inc, https://www.3dgsinc.com/, Albuquerque, US.

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Metallization of glass-core substrates and high-aspect ratio TGVs using liquid metal ink

By Simon McElrea [LQDX Inc.]

The practice of applying metal to glass dates back to ancient times, with evidence of gold being applied to Roman and Byzantine objects as early as 600AD, when it was used to create decorative items such as gilded glassware and mosaics (**see inset** of a 1st century Roman glass and gold flask). The first manufacturing application of metal on glass dates to the 19th century, with the development of silvering techniques for mirrors in the 1830s, but it took a further 100 years before the process began to become more industrialized to produce decorative tableware, glassware, and scientific instruments.

When I joined Johnson Matthey in the mid 1990s, I was astonished to learn that the bulk of the scientists in the extremely large Cookson Matthey Colors & Ceramics business were dedicated to deciphering these ancient "Witches Brew" recipes and attempting to translate them into synthetic industrial chemical processes. My lessons learned: 1) Metallizing glass isn't easy, and 2) Pay attention to the wisdom of the ancients!

Modern day advances

Jumping to the present, in the past few years there has been a substantial acceleration in the field of glass technology for advanced semiconductor packaging, spurred by companies such as Intel and Samsung, and led by global experts like Prof. Rao Tummala, whose Georgia Tech research focuses on integrating glass as a substrate material in advanced packaging, and highlighting its advantages in terms of electrical performance, thermo-mechanical stability, and large-panel-form processing.

As "chiplet" artificial intelligence (AI) computing now dominates the semiconductor roadmap, glass has gained considerable interest as a substrate for advanced semiconductor packaging and interposer applications because of its exceptional properties, including high dimensional stability, low coefficient of thermal expansion (CTE), low dielectric loss, and excellent surface smoothness. These features make it extremely well suited to ultra-high-density routing and redistribution, high-speed chip-to-chip interconnect, and optoelectronic integration. According to Yole's "Status of the Advanced Packaging Industry, 2024" report (**Figure 1**), "glass's resilience allows for a 50% increase in the number of chiplets within the same package area," however, "its disadvantage is still cost effectiveness and manufacturability."

The problem

Despite the inherent advantages, metallizing glass remains a significantly difficult and costly challenge. Why? Glass is chemically inert and lacks surface functional groups for bonding—which is why we store drinks and medicines in glass vessels—but this makes direct metal adhesion extremely difficult to achieve without clever (and sometimes ancient-wisdom driven) surface modification.

Several methods have been explored in the literature to address the problem of direct metal adhesion. One widely-explored approach uses physical vapor deposition (PVD), typically sputtering a titanium/copper seed layer followed by electrochemical deposition (ECD). These methods have demonstrated some promise for low-aspect ratio through-glass vias (TGVs), but they require expensive vacuum deposition equipment, involve multiple complex process steps, involve

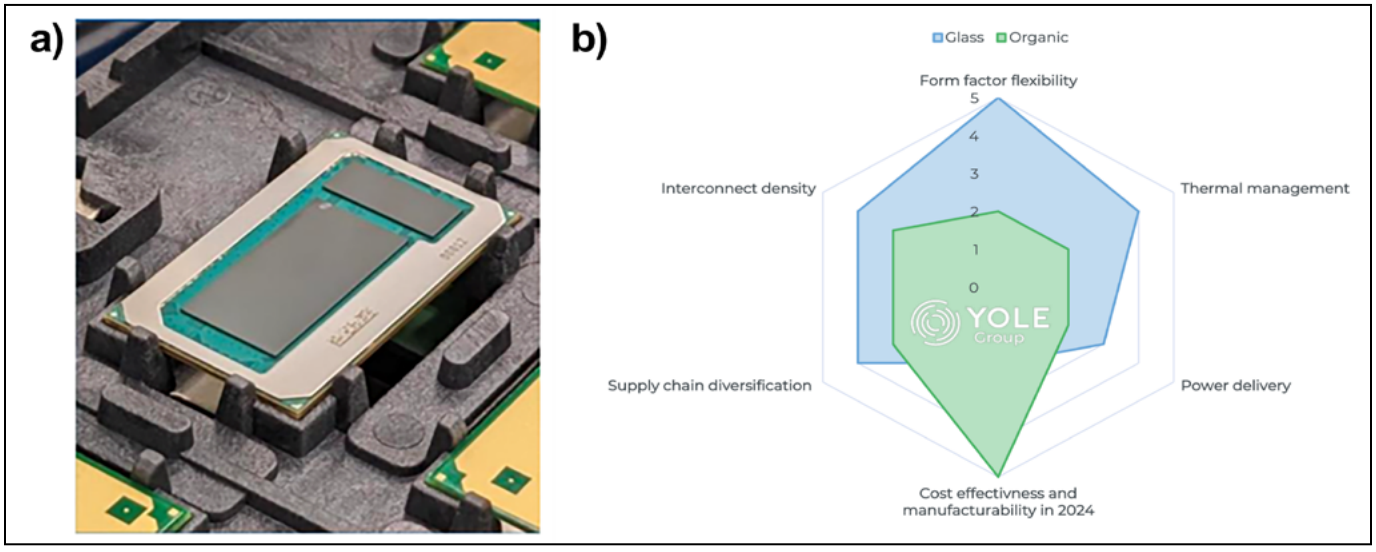

Figure 1: a) (left) Intel's fully-assembled glass-core test chip; and b) (right) Yole's 2024 Pro/Con Matrix. SOURCE: Yole [1]

high-temperature glass preparation techniques, and are limited in their ability to conformally-coat high-aspect ratio TGVs due to line-of-sight limitations. More recent work has focused on laser-assisted surface modification, particularly through techniques like selective surface activation induced by laser (SSAIL). This method uses short-pulse lasers to locally modify the surface of glass or transparent polymers, thereby enabling site-selective electroless copper deposition. SSAIL is attractive for producing narrow metal traces with reasonable adhesion, but it typically requires separate chemical activation steps (e.g., silver nitrate baths) and does not scale easily to large-area or 3D structures such as TGVs. Nanoparticle-based catalysts, especially those using silver or palladium colloids, have also been studied to initiate electroless copper deposition. One recent example demonstrated the use of silver nanoparticles stabilized by polyethyleneimine and glutaraldehyde on grit-blasted glass. However, nanoparticle systems tend to suffer from agglomeration, limited dispersion stability, and relatively low catalytic efficiency per unit mass. They also generally require costly high-temperature surface-roughening techniques and additional chemical primers, such as silanes, to improve adhesion to glass.

In contrast to the approaches noted above, our approach is based on atomic-scale palladium deposition from molecular precursor inks, not nanoparticles. The palladium ink—referred to as LMI®, or Liquid Metal Ink—is applied over a proprietary adhesion-promoting organic coating, LiqueCoat™. The latter introduces polarity onto the glass surface, improving interaction with the palladium/copper and enabling significantly better adhesion of the subsequent plated copper. Upon mild thermal treatment (≤200°C in air), the ink decomposes cleanly to form atomically-dispersed palladium that serves as an efficient catalyst for electroless copper plating (**Figure 2**). This method does not require plasma activation, surface roughening pre-treatment, high-temperature processing, or vacuum deposition. In short, it is low cost and old school!

Our atomic ink methodology has its origins in earlier patents from Dr. Sunity Sharma, formerly of the Stanford Research Institute, and currently Chief Scientist at LQDX. For example, US Patent 5,894,038 describes the use of palladium carboxylates and related compounds that decompose at low temperatures to generate catalytic surfaces, and US Patent 5,980,998 outlines selective patterning techniques using such inks to produce metal features on insulating substrates. Unlike alternative colloidal, aqueous, or nanoparticle chemistries, these inks allow for nano-level control over thin film and fine-pattern formation, are applicable without complex surface treatment or high-temperature processes, are highly tailorable (using organic modifiers and solvents incompatible with alternative water-based solutions), and are particle free and shelf stable.

The LMI® process is particularly effective for metallizing smooth glass surfaces and for achieving conformal coverage in high-aspect ratio TGVs. This article does not aim to provide a comprehensive survey of all alternative methods under investigation, but focuses on establishing the viability of this

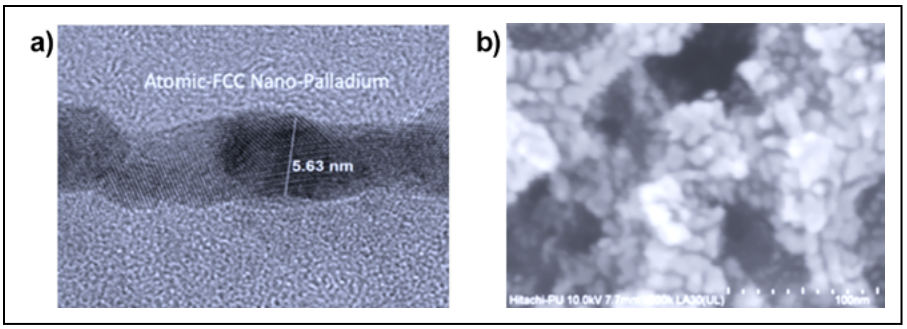

Figure 2: a) (left) TEM Image of the Pd-Ink deposition layer; and b) (right) FESEM of a laser-cured Pd-ink film.

alternative ink-based approach. The method and process integration has been studied at LQDX, San Jose State University (under Prof. Roger Terrill), and Arizona State University (under Prof. Hongbin Yu), using a range of analytical techniques—thermogravimetric analysis/differential scanning calorimetry (TG/DSC) for thermal behavior, atomic force microscopy (AFM) and field emission scanning electron microscopy (FESEM) for surface morphology, and X-ray photoelectron spectroscopy (XPS) for chemical characterization of the resulting atomic palladium film from LMI®. Electrical conductivity has been assessed using a 4-point probe method, and adhesion performance has been evaluated using nano-scratch and other more traditional scratch/pull test methods. The process (Figure 3) is at the state of being implemented and tested at large-scale semiconductor

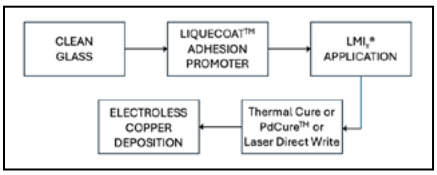

Figure 3: High-level process flow-chart for LMI® copper deposition on glass.

equipment manufacturers.

The glass metallization process using LMI® and LiqueCoat™ is typically assessed and monitored using a broad range of spectroscopic and physical characterization tools. LiqueCoat™—an organic polar "buffer coating"— enhances copper adhesion on glass by modifying its inherently non-polar surface. Following thermal maturation of LiqueCoat™ at temperatures below 200°C, palladium deposited via LMI® is then applied and activated thermally or chemically to produce atomic palladium, which in turn catalyzes subsequent electroless copper deposition. The metal ink is applied as a room-temperature liquid formulation, by panel dipping, spraying, or wafer spin coating, and it immediately generates atomic palladium upon thermal or chemical decomposition (**Eq. 1**). The generation of atomic palladium is independent of the nature of the substrate, provided it is solid, not chemically reactive, and tolerates the <200°C activation temperature.

Figure 4a presents the differential scanning calorimetry values (DSCs) of LMI® in quartz sample holders and in LiqueCoat™-coated quartz sample holders. The thermal collapse temperatures of the LMI® in quartz sample holders and in similar LiqueCoat™-coated holders are within ±5-7°C. Also, the overall profile of the two DSC curves are nearly duplicates of each other lending support to the premise that atomic palladium generated by LMI® is independent of the nature of the substrate. **Figure 4b** shows the thermogravimetric analysis (TGA) of LMI® in air: The weight loss cut-off is close to 192°C and matches with the thermal profiles exhibited by DSC. Transverse electromagnetic (TEM) cross-section analysis of the Pd film (**Figure 2**) shows the crystal planes of the quasi-2D palladium film. FESEM analysis of the thermally-matured Pd film on glass illustrates nano-domains of palladium reflecting the diffusion of atomic palladium. The films

Eq.1

$$\text{LMI} \xrightarrow{Thermal/Chemical/Photothermal} Pd_{atomic} + \text{Binding Inert Organic Products}$$

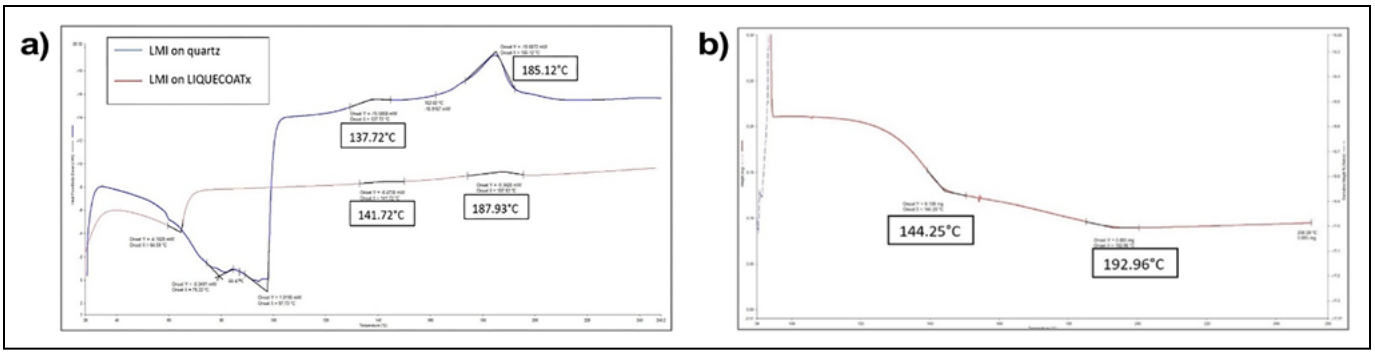

Figure 4: a) (left) DSC of LMI® in a quartz sample holder; and b) (right) TGA of the LMI® in air.

formed are modestly textured, in contrast with the precipitated aggregates that result from Pd nanoparticle precursors. Comparing the FESEMs of LMI® by laser and the thermal curing process, it is concluded that atomic palladium is easily generated by both methods.

A unique feature of cured LMI® vs. alternative palladium catalysts is that a sub-nanometer oligomeric organic polar coating forms on the substrate surface adjacent to the atomic palladium film. This "buffer layer" is critical for: 1) Enhancing substrate bonding/adhesion; 2) Improving its compatibility for subsequent copper metallization; and 3) For essentially normalizing all substrates—including glass—to a universal state, thereby allowing standard low-cost low-temperature downstream processing without the need to introduce exotic and expensive etch, laser, or high-temp firing techniques. XPS analysis reveals the presence of these multiple polar organic functionalities, and Pd^0 in addition to PdO_m ("m" representing non-stoichiometric composition). The atomic palladium generated through thermal or chemical treatment conforms to the nanoscale contours of the substrate enabled by the sub-nanometer organic oligomeric layer thereby replicating the topography with high fidelity. This effect is corroborated by AFM imaging of the substrate at various stages, confirming nanoscale replication prior to copper metallization. The surface profile of Schott BOROFLOAT® 33 glass was obtained using AFM before and after LiqueCoat™ as shown in **Figure 5**.

The glass substrates are then subjected to electroless copper deposition, typically using MKS Atotech's Printoganth MV-TP2, however alternative Okuno and Uyemura chemistries are also viable, with the deposition of copper monitored by sheet resistance measurements made at different intervals of time. The drop in sheet resistance to the specification of <0.2 Ohm/square is achieved within 5 minutes of residence time in the bath. Subsequently, the adhesion of the electroless copper film is qualitatively assessed by crosshatch testing, which demonstrates adhesion at the highest achievable level, Category 5B. Parallel nano-scratch quantitative testing typically demonstrates peel values of >16mN—a highly acceptable value for subsequent processing and reliability.

A critical feature of the LMI®/Cu metallization process is its ability to fully and evenly coat high-aspect ratio TGVs at the same time as the planar top and bottom surfaces of the glass-core substrates due to its extremely high wettability (low contact angle on glass), and with the same uniform thickness and topography throughout. This has been substantiated by plating TGV glass core samples with LMI®/Cu and examining multiple focused ion beam SEM (FIB-SEM) images of the vias from top to bottom on a multi-sample basis. **Figure 6** shows typical SEM energy dispersive X-ray (SEM-EDS) images of the via terminations (entry

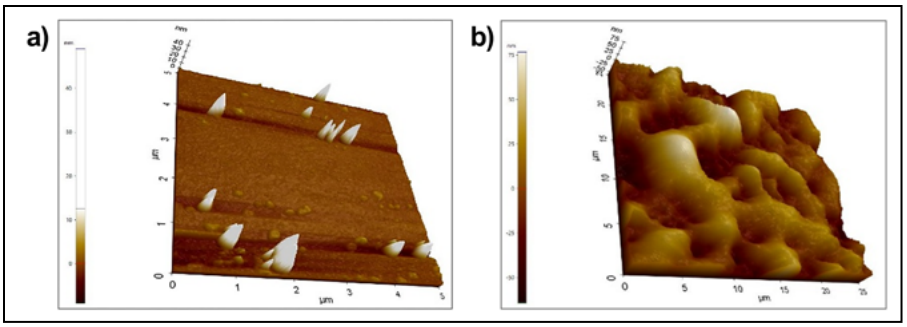

Figure 5: (left) AFM after LiqueCoat™ (Sa: 1.1nm); and b) (right) AFM after electroless copper (Sa: 16.8nm).

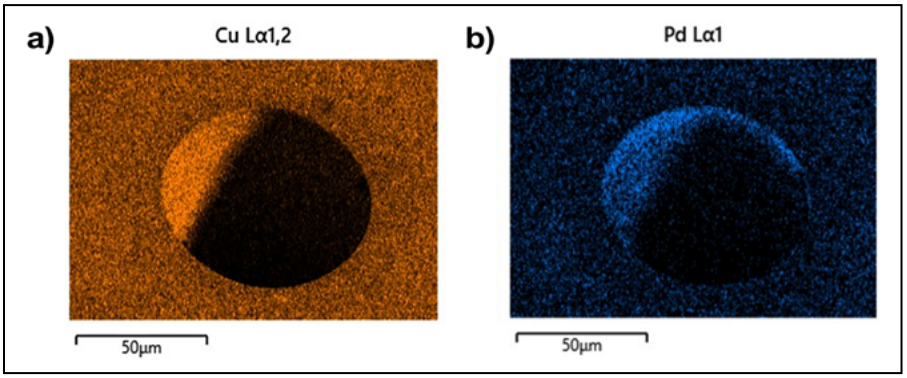

Figure 6: SEM-EDS images of: a) (left) Copper; and b) (right) Palladium (LMI®) at via entry points.

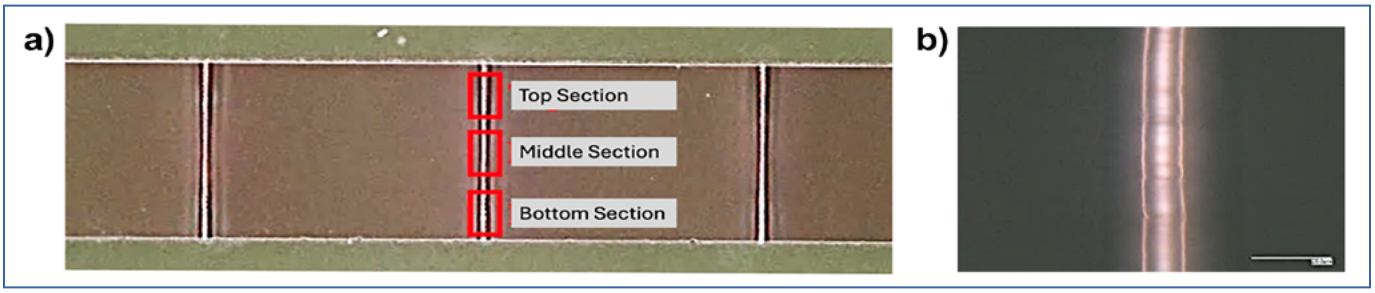

Figure 7: a) (left) Cross section of 20:1 TGV electroless copper on Schott Borofloat® 33Glass (100x); and b) (right) Cross section of 20:1 TGV electroless copper on Schott Borofloat® 33Glass (2500x).

points), highlighting excellent conformality and coverage of both copper and palladium (LMI®), as well as a lack of the typical dog-boning or corner abnormalities seen with other methods that can easily initiate downstream reliability failures.

Figure 7a shows a typical cross section of TGV electroless copper on Schott Borofloat® 33 Glass with 100x magnification; Figure 7b presents a further close-up with a magnification of 2500x. Further FIB techniques followed by dual-beam plasma-focused ion beam (PFIB) analysis at 50,000x on the via sidewalls at the top, middle and bottom sections conclude that the metal coverage on all samples tested (so far up to 20:1 aspect ratio) have uniform coverage, adhesion, and conductivity.

Summary

Glass-core substrates with high-aspect ratio TGVs provide a superior platform for the next node of advanced semiconductor packaging because of their exceptional dimensional stability (facilitating large-panel format processing and minimal CTE-driven warpage compared to organic materials), their improved electrical performance (due to the low-loss properties of the dielectric), and tailorable smoothness (facilitating a 2x fine-pitch density improvement in chiplet architecture). A critical bottleneck for mass adoption is the need for simple, non-exotic, low-cost and low-temperature glass metallization that can easily integrate into standard, and next-generation panel-based, equipment. We have developed a simple metal ink-based solution to this problem that delivers conformal, adherent, and reliable copper metal on all glass surfaces, including the deepest TGVs. Sometimes the simplest, ancient-wisdom-derived solutions are the best.

Reference

1. "Status of the Advanced Packaging Industry, 2024," report, Yole; https://www.yolegroup.com/product/report/status-of-the-advancedpackaging-industry-2024/

Biography

Simon McElrea is Chairman and CEO of LQDX Inc., Santa Clara, CA. McElrea has a track record of founding or restarting tech companies and leading them to exits, such as: Semblant Inc. (sold to HZO Inc. in 2018), Invensas Corp. (now Adeia), SonicEnergy, COO of FreePower (a SharkTank seeded wireless charging innovator adopted by Tesla in 2023), Interim CEO of Vertical Circuits Inc. and Energous Corporation (whose IPO concluded in 2014). He has held various senior positions at Johnson Matthey, Honeywell and Amkor Technology and authored 35 US patents. He has BS and MS degrees in Engineering Science from Oxford University. Email simon@lqdx.com

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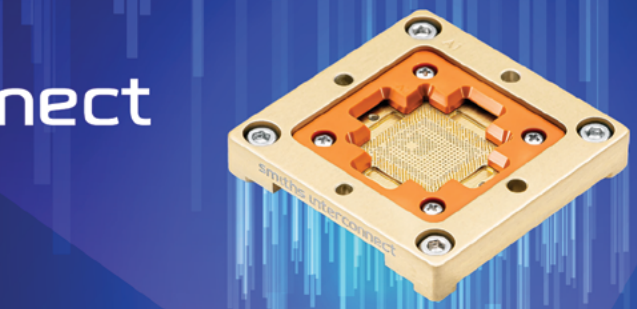

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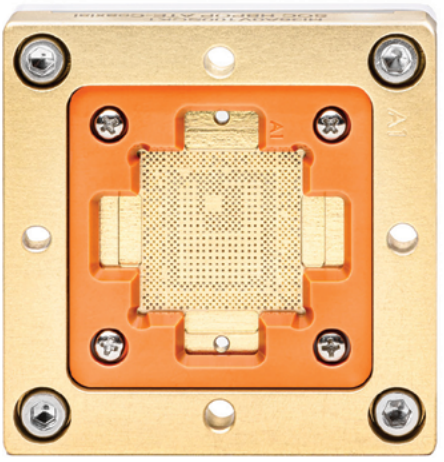

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Highlights of the 21st IMAPS Device Packaging Conference (DPC)

By Amy Lujan. General Chair Device Packaging 2025

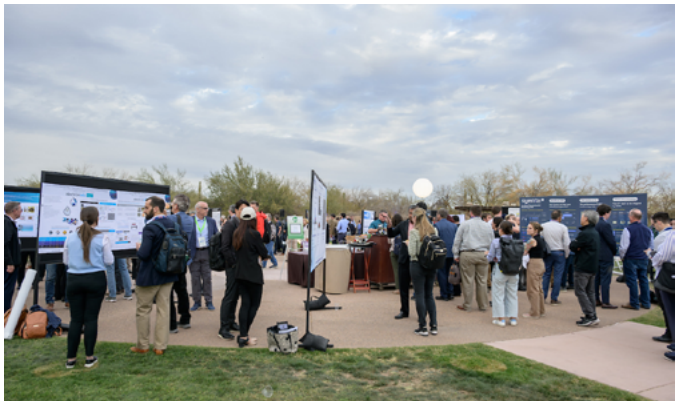
The 21st IMAPS Device Packaging Conference (DPC 2025) set a new attendance record of more than 1,050 attendees. This beat the previous year's record by almost 40%. IMAPS leadership and conference attendees alike had many positive things to say about the new venue, which was a key part of enabling the growth of the conference.

The conference brought together industry pioneers and researchers who provided valuable insights into cutting-edge packaging solutions that drive AI acceleration, automotive electronics, high-performance computing, and much more.

This year brought a major focus on AI, covered by an evening panel and our Global Business Council (GBC) plenary session.

The popular GBC focused this year on "Scaling AI from Datacenter to Consumer," with industry thought leaders from Marvell, PDF Solutions, Qualcomm, TechSearch International and YOLE Group. The evening panel's lively discussion covered the topic of "Preparing for the Coming AI Winter?" and it concluded that there is no worry about Winter! The panel consisted of participants from ASE, Intel, STATS ChipPAC, IBM and Amkor.

Our keynote sessions were full to capacity with engaging presentations from IBM, Absolics, ScaleFlux, and Arizona State University/SHIELD. The program ran four concurrent technical tracks, up from three tracks in previous years. This year featured two full tracks on emerging technologies, including automotive, photonics, glass, additive manufacturing, and MEMS/sensors. Of particular interest to attendees were the photonics and glass-based substrates sessions, with standing room only. The other two tracks focused on the tried-and-true topics of 2D/3D heterogeneous integration, flip-chip, and wafer-level packaging, all of which continue to be integral to our industry.



The busy international exhibit hall drew in the entire industry supply chain and is always a critical complement to the conference's global technical program. This year we were able to accommodate more booths than ever, and there was still a waitlist for exhibitors.

Many exhibitors commented on the meaningful conversations they had with visitors and the ability to expand their connections. IMAPS leadership is already reviewing the 2026 meeting space allocations to potentially add booths to expand to an even larger exhibit hall in March 2026 when we return to The Sheraton at Wild Horse Pass.

Our evening interactive poster session was a hit with 25 posters presented in a beautiful outdoor setting overlooking the reservation and desert backdrop.

Attendees were very engaged with the poster presenters, asking the type of detailed questions that are more difficult to accommodate in oral sessions.

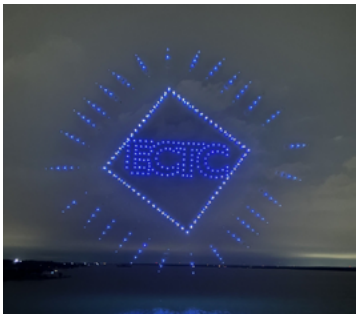
The posters were followed by the 3D InCites Back Yard Olympics—a fun team competition with six games and a lot of laughs. Congratulations to NAMICs, the gold winning team.

Each year, attendees provide feedback that this event is unique with its multitude of networking opportunities and the opportunity to directly converse with industry leaders, researchers, new talent and suppliers.

We were thrilled with the significant student participation this year from Arizona State University and the University of Arizona. One-hundred plus students participated in our professional development courses and had the ability to speak directly with our subject matter industry experts. ASU, University of Arizona, and the Chandler Unified School District participated with tabletop exhibits.

This summer, Chandler Arizona's Hamilton High School (in partnership with University of Arizona) is kicking off the nation's first Career and Technical Education Program in Semiconductor Manufacturing. We are excited about this level of student activity and the chance to help develop the industry's future workforce.

We look forward to DPC 2026 at the same venue on March 2-5, 2026.



ECTC 2025 celebrated its 75th anniversary with a spectacular drone show.

2025 IEEE ECTC: Record attendance shows growing importance of advanced packaging

By Florian Herrault [CEO, PseudolithIC, Inc., and General Chair, 2025 IEEE Electronic Components and Technology Conference]

By any measure, the 75th anniversary edition of the IEEE Electronic Components and Technology Conference (ECTC: www.ectc.net), held May 27-30 in Dallas, TX, was the most impactful and successful one in the conference's long and storied history. Advances in hybrid bonding, heterogeneous integration, co-packaged optics, power delivery and other vital microelectronics technologies were unveiled at this premier conference.

On a quantitative basis, for the second year in a row, ECTC had record attendance, a record number of paper submissions and presentations, record international and student participation, and a record number of exhibitors in a sold-out exhibition hall. Here are some key ECTC 2025 statistics:

- 2,518 attendees, the highest in the conference's 75-year history and a significant increase over the 2,008 who attended last year, which itself was a record.
- The number of abstracts submitted was the highest ever (775), as were the 390 technical papers presented in 36 oral and 5 interactive presentation sessions, including one dedicated to students. See https://www.ectc.net/press/index.cfm for highlights of some of the noteworthy technical papers that were presented.
- Several paper presentations attracted more than 600 attendees. Sessions on topics of intense industry interest—such as hybrid bonding and glass core interposers vs. redistribution layers (RDLs)—were standing-room only.
- 16 professional development courses were attended by 596 participants.
- There were speakers from over 20 countries.
- There was a record level of industry support, with 51 corporate sponsors and 138 booths in the exhibit hall.

A place to collaborate

On a more qualitative basis, the hallways and the meeting rooms buzzed with conversation and activity (IEEE Electronic Components & Technology Conference's albums | Flickr: www.flickr.com/photos/38916807@N07) as the world's major industry players and top university researchers in semiconductor packaging and component technology came together to collaborate, as conference committee members, panelists, presenters and/or attendees.

A key focus of many of these collaborations and discussions were the myriad technology advancements needed to realize the promise of artificial intelligence (AI) and high-performance computing (HPC), not just for the evolution of the electronics industry, but for the betterment of humanity as well.

Another area of focus was the industry's workforce challenges, which led ECTC to offer a number of new opportunities for student engagement this year, to inspire students in their studies, to give them the opportunity to showcase their work, and to provide them with networking opportunities.

Finally, a celebration of ECTC's 75th anniversary was held during this year's IEEE EPS (Electronics Packaging Society) President's Panel, to acknowledge the skills, accomplishments, and contributions of the thousands of people who have participated over the years. The work of these participants has helped to make electronics one of the most important, vibrant and exciting industries in the world. A timeline was presented, showing how the significant developments announced at ECTC, and its predecessor event, through many decades, have contributed to the growth and development of the semiconductor industry since before the invention of the transistor.

Program highlights of ECTC 2025 are summarized below.

Plenary keynote talk by AMD

The ECTC 2025 keynote address, "Achieving Efficient Zettascale Compute in the AI Era," was given by Sam Naffziger, Sr. Vice President and Corporate Fellow at AMD. He described the applications driving the growing demand for compute, and how the

Sam Naffziger, Sr. Vice President and Corporate Fellow at AMD, gives the ECTC 2025 keynote address, "Achieving Efficient Zettascale Compute in the AI Era."

energy needed to power it is increasing faster than ever before. He noted that meeting the challenge of delivering this processing power in the AI era requires holistic innovation from the device to the datacenter level, and detailed the fundamental processing, memory and power challenges, calling the efforts to meet them, "The grand challenge of our day," for the industry.

Special sessions

In addition to the keynote talk, ECTC 2025 held a series of Special Sessions, where panels of industry experts discussed technology status and roadmaps in these key areas:

- Ultra High-Density Interconnect Technologies and Supply Chain Readiness for AI & HPC;
- Hybrid Bonding (HB): to B, or not to B? Needs and Challenges for the Next Decade;
- Quantum Photonic Advanced Packaging;
- Glass Core vs. RDL Interposers: Ready for Prime-Time?
- Advanced Materials for Enabling Co-Packaged Optics Integration;
- Advances in Chiplets: Tackling Fault Isolation and Failure Analysis in Heterogeneous Integration;
- Advancements in mmWave and Sub-THz Packaging for Communication and Radar Applications;
- Thermal Management Solutions for Next-Generation Backside Power Delivery;
- IEEE EPS Seminar: User Perspective of Chiplet Technology;
- ECTC 2025 Plenary Session: Emerging Advanced Power Delivery for the AI Computing Era; and
- IEEE EPS President's Panel: ECTC at 75 – Celebrating the Past, Innovating for the Future.

Student engagement

One of the new opportunities for student engagement at ECTC 2025 was a Local Student Engagement Program, which brought approximately 30 students and their teachers/professors from local high schools/community colleges to ECTC so the young students could interact with industry professionals and gain insights into the electronics packaging and semiconductor manufacturing industries.

Another new initiative was a Student Volunteer Service Program, where student attendees who have already chosen the electronic packaging industry as their career path could build and expand their professional network by working with ECTC Technical Committee members on various session-related duties.

ECTC 2025 also featured a Student Competition, offering groups of students the opportunity to describe

their proposed solutions to enhance the thermal performance/reliability of high-temperature microelectronic components and systems in certain technical areas.

From left: Karlheinz Bock (TU Dresden), ECTC Jr. Past General Chair; Bora Baloglu (Intel), Asst. Program Chair; Michael Mayer (Univ. Waterloo), Vice-General Chair; Florian Herrault (PseudolithIC Inc.), ECTC 2025 Chair; Przemyslaw Gromala (Robert Bosch GmbH), Program Chair; Tanja Braun (Fraunhofer IZM), IT Coordinator.

Students also had the opportunity to participate in an Innovation Challenge competition that also included start-up companies, where their ideas were pitched to a jury panel. Patrick Heissler, from Scrona, won the startup competition, and the team from Georgia Tech won the student project competition.

Other engagement opportunities were a student reception hosted by Texas Instruments; a Student Interactive Presentation (IP) session, giving them the opportunity to receive direct feedback from industry and academic leaders on their work; Best/Outstanding Student Paper Awards, sponsored by Intel and TI; and an ECTC Student Travel Award to encourage student participation, providing 15 students with a certificate and reimbursement for travel expenses (up to a specified limit).

Heterogeneous Integration Roadmap (HIR) Workshop

ECTC 2025 also featured a Heterogeneous Integration Roadmap (HIR) workshop with four focused discussions:

- IoT & AI at the Edge;
- Advancing Heterogeneous Integration through Metrology & AI;
- Integrating Photonics in HPC & Network Systems; and
- Advances in Panels, Substrates, and Printed Circuit Boards.

Professional Development Courses

In addition to the technical program, ECTC 2025 offered 16 Professional Development Courses (PDCs) in conjunction with the co-located IEEE ITherm Conference (www.ieee-itherm.net) that focused on thermal/thermomechanical issues in electronic systems. These four-hour courses were taught by world-class experts, enabling participants to broaden their technical knowledge base. Attendees were awarded either continuing education units (CEU) or professional development hours (PDH) credits.

Looking ahead

ECTC 2025 had a record-setting year, and the variety and technical depth of the work presented is evidence of the tremendous amount of innovation taking place in advanced chip packaging. It's an exciting time to be in this industry, and we can't wait to see what's in store for next year, when ECTC 2026 takes place in Orlando, FL from May 26-29, 2026. See you there!

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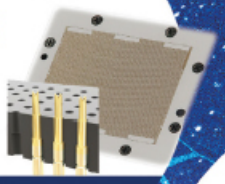

Probe Head

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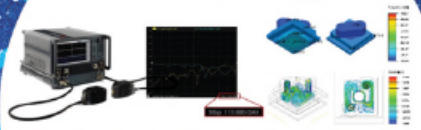

RF/Thermal Simulation

Actual Measurement

2-Port: 110GHz
4-Port: 43GHz

10 Sockets in 7 Days!

Logic & SLT Socket

AI

Specification

Frequency : 80GHz(BGA), 100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%

1K Pins in 7 Days!

Coaxial Probe 100GHz

5 Sockets in 10 Days!

100GHz Coaxial Socket

Excellent RF & Electrical Performance!

MP Socket

Pin Counts 5K~

Device Power ~1,200W

10 Sockets in 10 Days!

Large Device Socket/Lid

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Measuring the Invisible

XM8000™

Automated X-ray Metrology

Advance your Semiconductor X-ray Metrology with XM8000™

Nordson's XM8000™ AXM system provides industry-leading measurement of micron-scale features in wafer and panel level advanced packaging applications.

- Using proprietary imaging chain including Nordson's own design X-ray tube and CMOS detectors to generate ultra-high resolution images capable of detecting and measuring hidden defects within complex semiconductor packages.
- Successfully being used to enhance packaging quality in a variety of applications including bump voiding, TSV/TGV measurement, fill analysis and chip gap height measurement.

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