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The Future of Semiconductor Packaging

Volume 29, Number 1

January • February 2025

AI driving demand for advanced packaging solutions

AI

- Benefits and challenges of sensors that utilize chips and MEMS
- Early detection of C-RES degradation on high-current power planes
- Next-generation high-density RDL packaging for a 2.5D large silicon interposer
- Ultra low-loss ion-exchange waveguides in optimized alkali glass for co-packaged optics
- Vertical fan-out (VFO) package with enhanced form factor and performance for mobile applications

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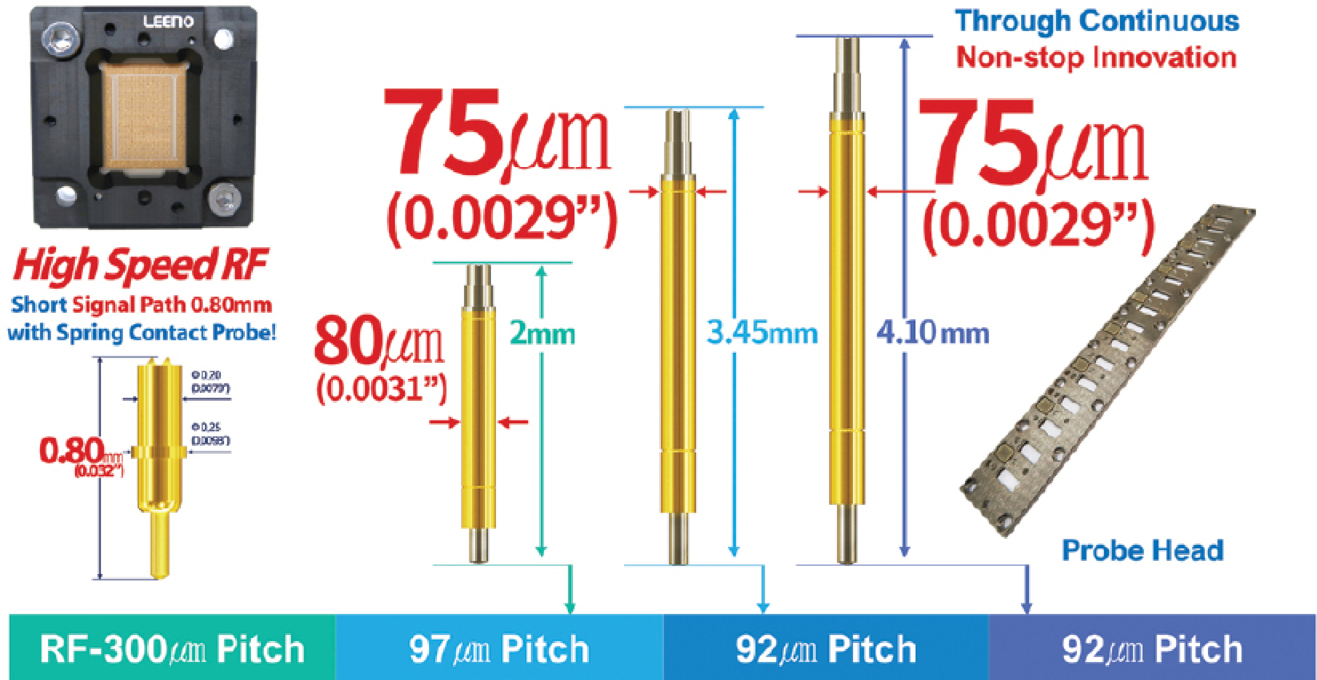

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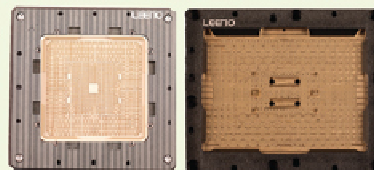

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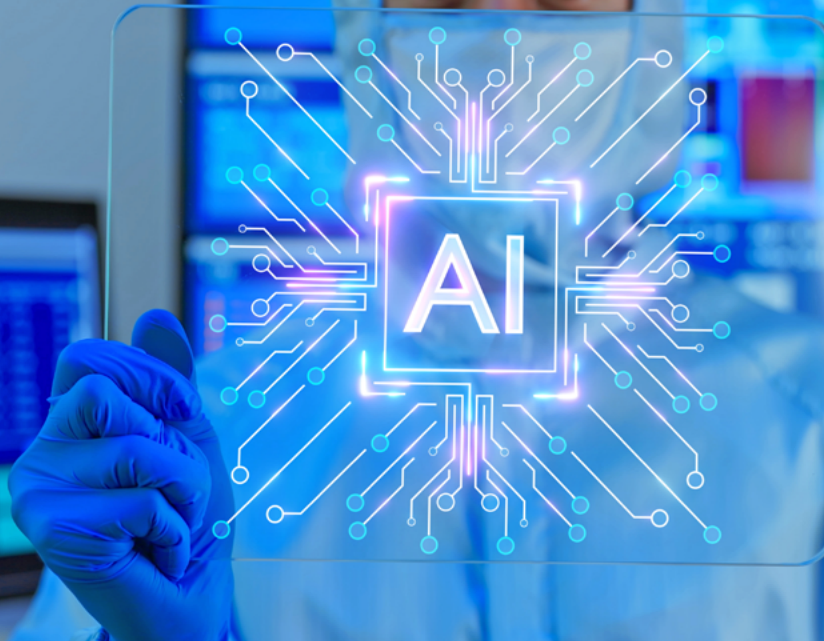

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There have been any number of market drivers for advanced semiconductor packaging over the years, including improved form factor, power, and operational temperature requirements to accommodate the demand for ever-smaller consumer electronics. Automotive applications have also been a significant driver for packaging. More recently, the semiconductor industry is embracing the process improvements needed to implement artificial intelligence in a broad swath of military and commercial applications. The cover article discusses an integrated wet processing platform that meets the needs of chips for AI applications, and that also has a low cost of ownership.

Cover image courtesy of iStock/Pony Wang

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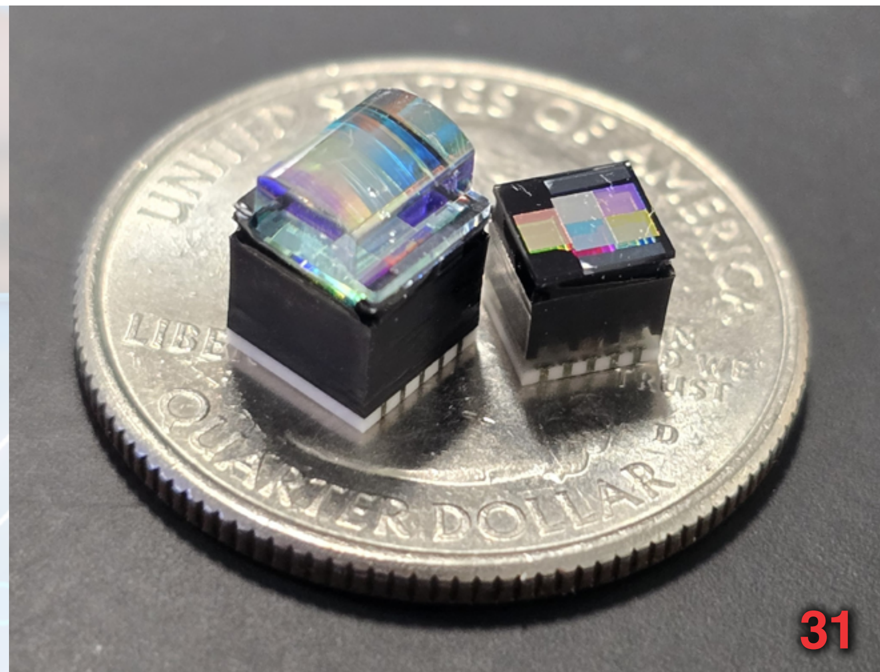

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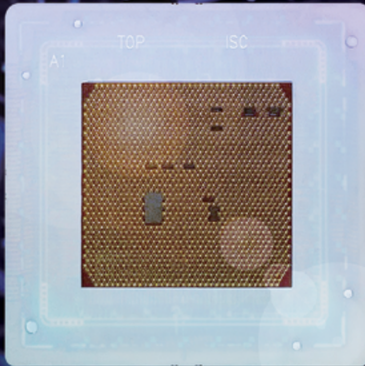

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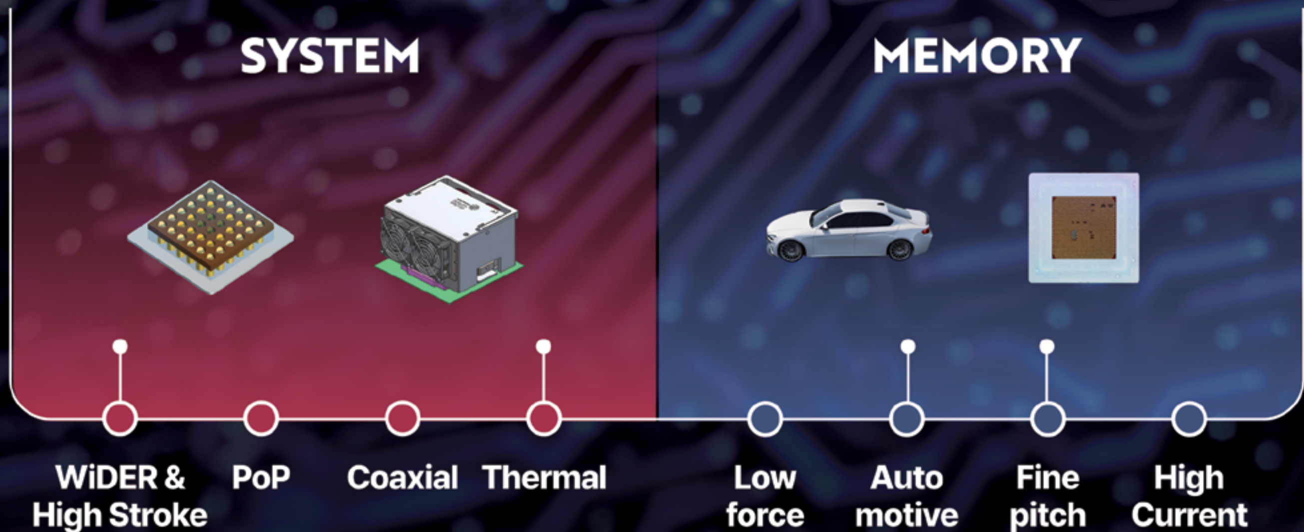

AI driving demand for advanced packaging solutions

By John Taddei [Veeco]

Advanced packaging is experiencing rapid growth due to the demand for high-performance computing in artificial intelligence (AI) applications and the automotive industry. Given the high demand for AI systems, foundry leader TSMC has reported that it aims to balance supply and demand by 2025-2026 and expects to have the capability for 60,000 wafer starts per month in 2025 for its chip-on-wafer-on-substrate (CoWoS®) technology [1].

Advancements in 3D technologies in recent years include die-to-die, die-to-wafer, wafer-on-wafer, and die-on-substrate architectures. These advancements required new process technology and process equipment to produce 3D features with high yields. These backend devices were manufactured on 300mm wafers and required low defectivity levels that were previously restricted to front-end processes. As a result, the new toolsets needed to have low defectivity to obtain high yields, while delivering a low cost of ownership.

This strong need for 3D has pushed capital expenditures for advanced packaging over the $5 billion mark for 2024, and this figure should continue to grow in 2025 as the demand for AI drives advanced packaging forward. When stacking chips in a 2.5/3D package, as shown in **Figure 1**, several techniques can be employed to connect the devices, including bumps, micro bumps, pillars, through-silicon vias (TSVs), and hybrid bonding. These can connect to the die directly, on the substrate (3D), or use an interposer (2.5D) such as glass, silicon, printed circuit board (PCB), or organic. Supporting processes include photolithography and deposition (plasma, sputtering, electrochemical). Wet processes implemented to create the devices and then connect them in 3D architectures include spin coating, develop, etch, photoresist strip, temporary bonding material removal, and cleans.

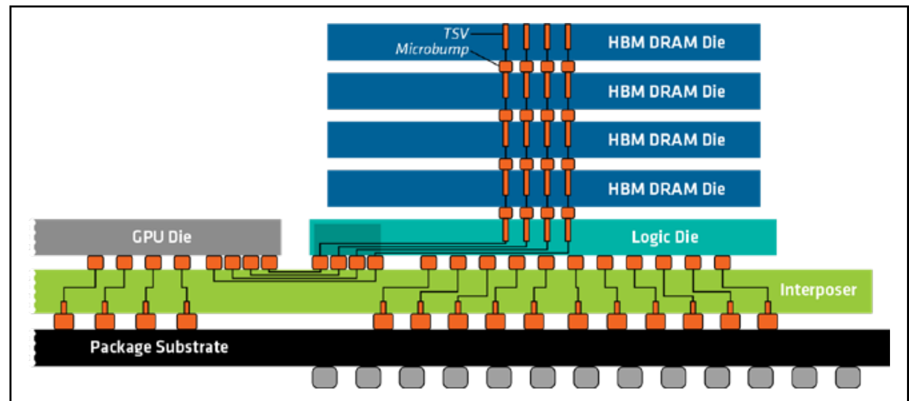

Figure 1: Techniques can be employed to connect devices within a 2.5/3D package, including bumps, micro bumps, pillars, TSVs, and hybrid bonding. SOURCE: Veeco

Cleaning technologies for advanced packaging

Advanced packaging creates unique challenges for the cleaning process. As device dimensions shrink, the backend cleaning process needs to create clean surfaces both for the deposition of materials and to facilitate material bonding. Any contamination can impact the electrical quality of the film being deposited, as well as material adhesion. A versatile multi-chamber cleaning system capable of multiple immersion chemistries, utilizing surface cleaning techniques such as high-pressure spray, high-velocity spray, and megasonics can help address advanced packaging cleaning requirements. We explore how a versatile cleaning system can benefit the cleaning processes for advanced packaging in the sections below.

TSVs are a staple of the front end of the line (FEOL) and advanced packaging. The via is first etched in silicon or the packaging substrate—the aspect ratio can vary depending on the end application. When etching the via, the deep reactive-ion etch (DRIE) process leaves behind a polymer residue that can lead to defects and voids in the barrier, seed, and fill steps that follow. Effective cleaning of the polymer is performed by using an immersion chemistry that effectively dissolves the plasma-exposed photoresist mask and the sidewall polymer residue. Once the polymer is dissolved, the wafer is transferred while wet into a high-pressure spray chamber, where the spray pressure can be ramped and controlled up to 3,000psi. In the chamber, any remaining residues are removed, leaving clean sidewalls before the deposition process.

In cases where the residual debris is particularly stubborn, a megasonic wand can be used first to loosen stubborn residues using the base cleaning chemistry, and then the high-pressure spray used as a final step before the wafer drying process. This process sequence has proven effective in removing residues in the TSVs used for AI technology and other advanced packaging applications.

TSVs connect wafers or die, using either hybrid bonding or metal bumps. Each of these processes has its own cleaning challenges. In hybrid bonding, the surfaces of both copper pads and dielectric sections need to be contaminant-free. Particles, polymers, and surface residues will prevent the wafer surfaces from fully contacting each other and can prevent proper bonding of the surfaces. Contaminants can impact

the contact resistance between chips, as can polymers, causing surfaces to have poor contact and introducing impurities into the copper.

A versatile cleaning tool enables multiple methods of eliminating contamination. Plasma cleaning of the surface can remove polymers and metal oxides that may be present before bonding or the next process in the sequence. Immersion cleaning removes polymers, contaminants, particles, and oxides. High-pressure spray—and the ability to scrub both the sides and walls of the features before bonding—can ensure contaminant-free surfaces for the bumping process. Immersion cleaning with a subsequent high-pressure spray can also be used to remove adhesives that bond the wafer or die to the carriers used in the advanced packaging process.

While the future of bonding high-bandwidth memory (HBM) and 3D packaging is hybrid bonding, bumping technology is the current process of choice. Bumping for HBMs poses significant challenges for the cleaning process. The memory die are stacked on top of each other with the spacing between the wafers at about 15µm. It is extremely challenging to remove the flux residue after the bump bonding process.

Flux cleaning is critical to wafer bumping and joint formation processes because it removes oxide layers and other impurities left by solder materials, which will impact bonding and electrical characteristics. To ensure a clean metallic interface for the next assembly step, a liquid fluxing agent is delivered to the bumped surface. The immersion soak is used to dissolve the remaining flux residue.

Additional cleaning steps remove any other residues left behind. Soak-and-spray technology enables the cleaning platform to remove flux residues from even the tightest spacing. The wafers are first immersed in the appropriate chemistry to dissolve the flux material and are then transferred wet to the high-pressure spray chamber, where the spray angle and spray pressure remove any remaining flux and exchange the chemistry in and around the bumps. After undergoing the solvent high-pressure spray, the wafers are transferred again into an immersion/spin chamber sequence to displace any solvent or flux residues to prepare the wafer for spin dry.

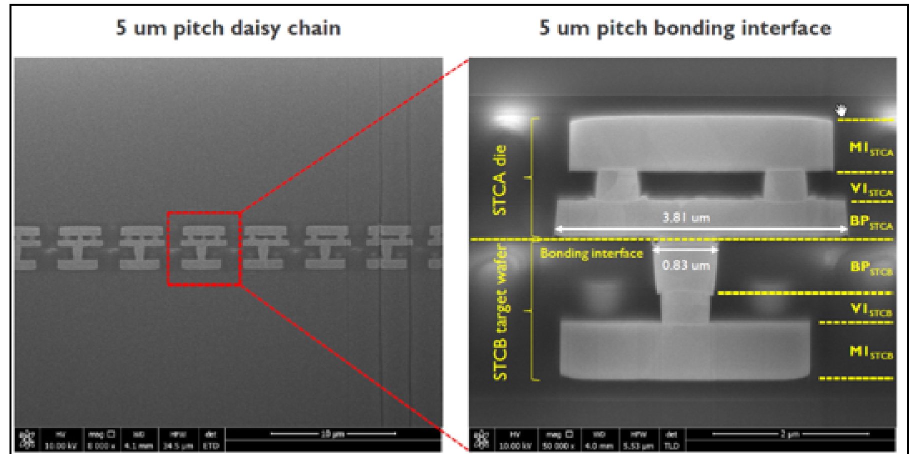

Figure 2: Using a strip and clean process for removing temporary bonding material prior to hybrid bonding resulted in up to a 97% yield for features as small as 5µm. SOURCE: Veeco

As this approach has been demonstrated to be repeatable, it is currently used in the manufacturing line at HBM vendor sites.

For larger geometries, a spin-only process is possible. Flux cleaning at the interposer level or for chip-on-wafer (CoW) applications can be accomplished with spin-only processing that employs high-pressure spray and low-surface tension fluids.

As 2.5D and 3D packaging continue to evolve, dimensions will shrink below 10µm pitch, necessitating a transition to hybrid bonding from ball bump bonding for improved packaging efficiencies. Critical cleaning processes for hybrid bonding start with the need to clean the photoresist. In a modern flexible cleaning system, the resist can first be removed via immersing the wafers in solvent followed by a high-pressure spray with solvent and then a spin rinse dry. Before bonding the wafer or die together, surfaces need to be particulate-free, and an activation process ensures the bonding process is successful. In the process tool, a plasma process is used to activate the bonding surfaces and ensure there is no particulate contamination. Figure 2 shows excellent hybrid bonding with features as small as 5µm pitch for such a process.

Summary

Advanced packaging cleaning requirements are diverse. The required combination of processes and cleans necessitates a cleaning tool with significant process versatility that can ensure high yields for a multitude of processes on geometries requiring more than immersion or low-pressure dispenses alone. These processes, which include resist strip (spin-on or dry film), temporary bonding materials strip (adhesive, mechanical and/or laser release), pre-bond cleaning, TSV cleaning, and CoW/HBM die stack flux removal, can be combined on a wet processing platform to provide state-of-the-art cleaning for advanced packaging with a low cost of ownership. Implementing such an integrated platform optimizes the advanced 3D packages needed for high-performance computing essential to burgeoning AI and other microelectronic applications.

References

1. https://www.digitimes.com/news/a20240815PD228.html

Biography

John Taddei is the Director of Process Engineering Development for Veeco's wet processing product line, Horsham, PA. Before his current position, he was the Process Lab Director where he developed advanced packaging toolsets and processes to assist Precision Surface Processing (PSP) customers. Before joining Veeco, he was a project manager in the industrial gas industry working in cryogenics and specialty gas applications, mainly related to the semiconductor industry. Email jtaddei@veeco.com

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Next-generation high-density RDL packaging for a 2.5D large silicon interposer

By Douglas Shelton, Masaki Mizutani, Yusuke Tokuyama, Noriyuki Shiozawa, Mizuma Murakami, Hiromi Suda, Ken-Ichiro Shinoda, Ken-Ichiro Mori [Canon, Inc.; Canon USA]

In recent years, demand for graphics processing units (GPU), field-programmable gate arrays (FPGA), and artificial intelligence (AI) chips has continued to grow as applications including AI system processing and deep learning require higher computing capability. In order to produce higher-performance computing systems, 2.5D interposer technology has been developed and matured as a technology for high-speed communication between different chips such as processors and high-bandwidth memory (HBM). Recently, in order to realize even higher-performance devices, technology for mounting and integrating many chips on large interposers has been developed to help enable heterogeneous integration and chiplet technology. As the interposer size increases, improved resolution and increased density of interposer interconnections is necessary for high-speed interconnection.

To meet sub-micron resolution interposer requirements, it is necessary to use a stepper to realize patterning of fine through-silicon via (TSV) and redistribution layer (RDL) patterns. However, because the size of the exposure region of a stepper is limited by the size of the reticle and reduction ratio of the projection lens, it is sometimes not possible to expose the entire area of the interposer in a single exposure. To increase the device size to greater than one reticle, a stitching exposure technique in which multiple, adjacent exposure areas are exposed can be used. In stitching exposure, a RDL used for interconnection between chips will not yield if each exposure field is not aligned accurately with respect to the adjacent exposure fields. A key performance factor of the large-field stepper is stitching accuracy.

Figures 1 and **2** show images of a chiplet device with two processors and eight HBMs in a large device. The interposer used to connect the chips is made by performing a 4-shot (Shot A, B, C, D) stitching exposure. **Figure 1** is a top view of the large device, and **Figure 2** is a cross-sectional view of Region A of the large device. In this image, the RDL layer used for the connection between the two processors in Region A straddles the boundary of the exposure area of the stepper and is connected by a stitching exposure. If the adjacent positions of Shot A and Shot C are out of alignment, the RDL between the processors will be misaligned and the connection between the processors will be broken. Stitching accuracy must be maintained for high-resolution and large-device manufacturing using a stepper.

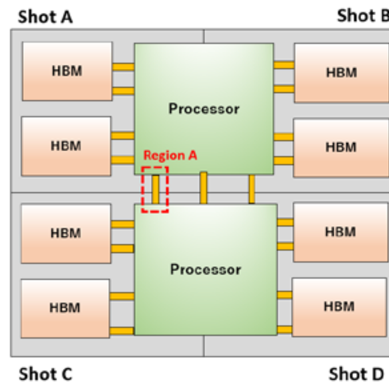


Figure 1: The top view of a large device.

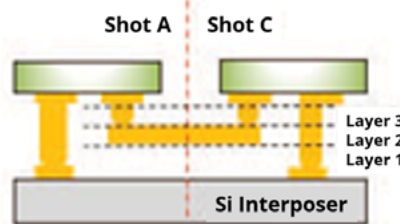


Figure 2: Cross-sectional view of a RDL.

Alternative technologies that embed smaller local Si interconnects (LSIs) in mold substrate have been developed to complement or replace large Si interposers for large-device production. LSIs are advantageous in terms of cost because they can help minimize the area of Si utilized in the interposer while providing high-resolution TSV and RDL patterning.

Figure 3 shows a top view of a device using LSI. The device has a Region B area using an LSI for connection between two processors, or between a processor and an HBM. The RDL layer between the chip of the processor or HBM and the input/output (IO) terminals is used for connection with the outside of the package. **Figure 4** shows a cross section of Region B. As can be seen from this figure, the processors and LSI are

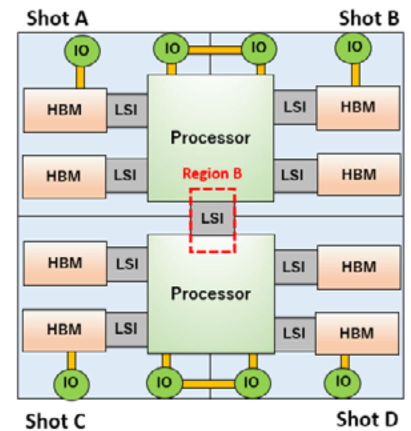


Figure 3: The top view of an LSI package.

Figure 4: Cross-sectional view of an LSI structure.

connected through the pad and RDL layers, and communication between the processors is carried out using fine-resolution LSI. On the other hand, because the LSI is embedded in the mold material of the package substrate, position errors (bonding errors, process errors, etc.) can occur during the embedding process. Therefore, die shift of the LSI with respect to the mold substrate must be considered.

Figure 5 shows a top view and a cross-sectional view when the LSI is shifted relative to the mold substrate. The processor connection pad is indicated by a black circle, and the LSI connection pad is indicated by a red circle. As can be seen from **Figure 5**, when the LSI has a large position error with respect to the mold substrate, and when the intermediate

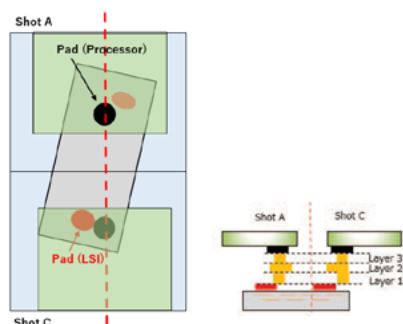


Figure 5: Influence of the LSI shift error.

layer for connecting the processor and the LSI is formed, the via of the RDL layer formed in the intermediate layer may not accurately overlay with the connection pad of the LSI and may become electrically shorted. Therefore, when an LSI interposer is exposed by using a stepper—in addition to the stitching accuracy—the overlap accuracy (i.e., the mix and match overlay [MMO] accuracy) with the interposer becomes important.

In general, when position error or distortion is generated in a lower layer (interposer), exposure can be performed with good overlay accuracy with respect to the lower layer. Lower-layer position error between adjacent shots can cause stitching accuracy to deteriorate. For a substrate with a large position error, it is difficult to balance stitching accuracy and the MMO accuracy and it may be necessary to sacrifice the accuracy of one parameter to maximize yield.

During the 72nd ECTC in 2022, Canon provided a stitching accuracy report and introduced the optimum exposure equipment for large interposers [1-5]. In order to realize even greater stitching accuracy, a new lithography system was developed to provide reduced optical and stage grid distortion and improved in-plane critical dimension (CD) uniformity. However, the issues of balancing stitching accuracy and MMO accuracy remain when overlaying distorted substrates for large-device production. In this study, we investigated the feasibility of high-density interconnection for large interposers and the possibility of improving MMO accuracy for LSI-embedded interposers.

Stepper for high-precision stitching: specs and improvements

In order to realize stitching accuracy and MMO accuracy with high precision, the performance of a high-resolution stepper with a large image field was evaluated. The specifications of the large-field stepper are shown in **Table 1**. The new machine is designed to provide improved distortion, stage grid accuracy, and CD uniformity over the previous model steppers.

Optical distortion was reduced from

	Current	New Stepper
NA	0.24 - 0.15	
Image field	52 x 68mm	52 x 68mm 55 x 65mm
Distortion	48nm	12nm
Grid-accuracy	120nm	40nm
CD uniformity (Target: 0.8μm L/S)	67nm	36nm
Depth of Focus (Target: 0.8μm L/S)	5.8μm	8.0μm

Table 1: Specification and performance comparison of large-field steppers.

48nm to 12nm across the large image field by employing highly accurate aspherical processing of the lens glass elements. The stage grid accuracy was also improved from 120nm to 40nm by adopting a new stage-drive algorithm.

Regarding CD uniformity, the homogenizer in the illumination system was upgraded to improve CD uniformity in the exposed image field. As a result, the CD uniformity can be improved from 67nm to 36nm, and the depth-of-focus (DOF) can be improved from 5.8μm to 8.0μm.

Stitching accuracy and MMO accuracy results

The following sections discuss the scope of the study, experimental conditions and results.

Outline of the study. In this study, we confirmed the stitching accuracy and MMO accuracy performance of the new stepper. The possibility of improving MMO accuracy for substrates with bonding errors was also examined. As mentioned earlier, when performing stitching exposure on a substrate containing large position error or distortion, if the exposure pattern is aligned to the distorted substrate, stitching accuracy will deteriorate. Conversely, if stitching accuracy is improved, the overlay accuracy with the distorted layer will deteriorate. To solve this issue, we examined the possibility of expanding the process window in which the required MMO and stitching accuracy are both within specification by optimizing the alignment sequence. MMO and stitching accuracy were compared when overlaying multiple distorted layers. Overlay was performed using multiple alignment sequences to confirm the optimum condition. The study comprised the following elements: 1) Verification of stitching and MMO accuracy; 2) Confirmation of distorted layer position error on stitching and MMO accuracy; and 3) Confirmation of MMO accuracy improvement by changing the alignment sequence.

Experimental conditions. Figure 6 shows the wafer layout for the large-field exposure of a 110 x 110mm device on a 300mm wafer. Because the maximum exposure area of the stepper is 55 × 65mm, four 55 × 55mm fields are exposed

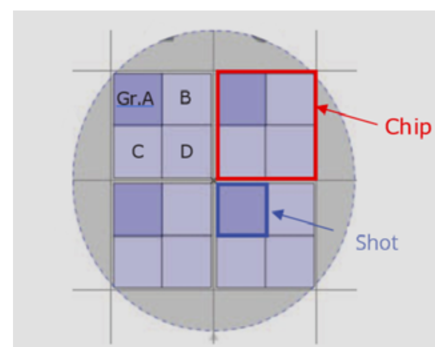
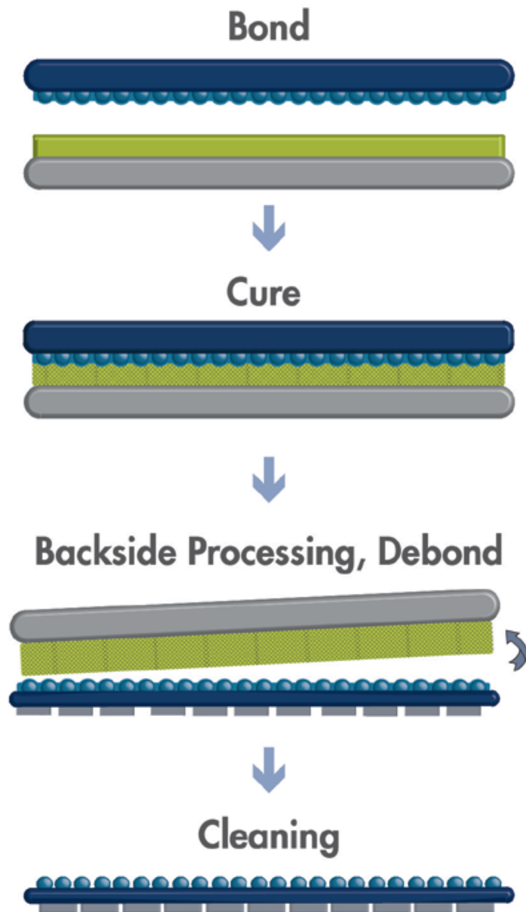


Figure 6: Stitching and MMO accuracy study layout.

adjacent to each other and stitched together to achieve a 110mm square chip. **Figure 6** shows that four 110 x 110mm devices can be fabricated on a single 300mm wafer. Four exposure fields are stitched together to pattern each of the large-field devices.



In order to confirm MMO accuracy and stitching accuracy when aligning to distorted lower layers, the position of shot in the distorted layer was randomly shifted and overlay exposure was performed. The shift position errors given in the distorted layer were randomly selected from seven normal distributions having sample distribution 3-sigma (3σ) values as shown in **Table 2**.

	3σ
Bottom Layer Random Variation	0nm, 50nm, 100nm, 150nm, 200nm, 300nm, 400nm

Table 2: Lower-layer shift-error condition.

Three kinds of alignment sequences were evaluated. The first (Seq.1) is global alignment, which is commonly used in steppers. In Seq.1, the alignment marks of the four shots on a wafer are measured, wafer shift, wafer magnification, and wafer rotation are calculated and all shots are exposed using common overlay correction values. In global alignment, because all shots are exposed with the same correction values, stitching accuracy is expected to be within the range of the stage grid and distortion accuracy of the stepper. MMO accuracy is assumed to deteriorate when overlay global alignment is performed to correct for lower-layer position error.

The second alignment sequence (Seq.2) is every shot alignment, which measures alignment position for each shot and corrects the overlay compensation by optimizing the exposure position of each shot. In this case, even if the position error of the lower layer is large, the MMO result with the lower layer can be expected to be good because the measurement and correction are applied to each shot. However, stitching accuracy with adjacent shots is assumed to deteriorate with each shot alignment because overlay compensation is not based on the position error of the distorted lower layer.

The third alignment sequence (Seq.3) is a newly developed function, called every shot (chip-common) (**Table 3**). In Seq.3, the measurement values obtained by the alignment measurement of each shot are averaged within each large-field device, and all shots in each device are exposed using the common correction value. In this method, because all shots in each device are exposed with the common correction value, it is expected that the accuracy of MMO can be improved even for substrates that have large lower-layer position errors while maintaining the stitching accuracy.

Seq.		Alignment	Compensation
1	Global	4 shots in the wafer	All Shot Common Correction
2	Each Shot	Every shots	Every shots
3 (New)	Each Shot (Chip Common)	↑	The same correction to the in-chip average value.

Seq.1
Seq.2
Seq.3
Chip
In-Chip Common Ofs. Compensation

Table 3: Alignment sequence conditions.

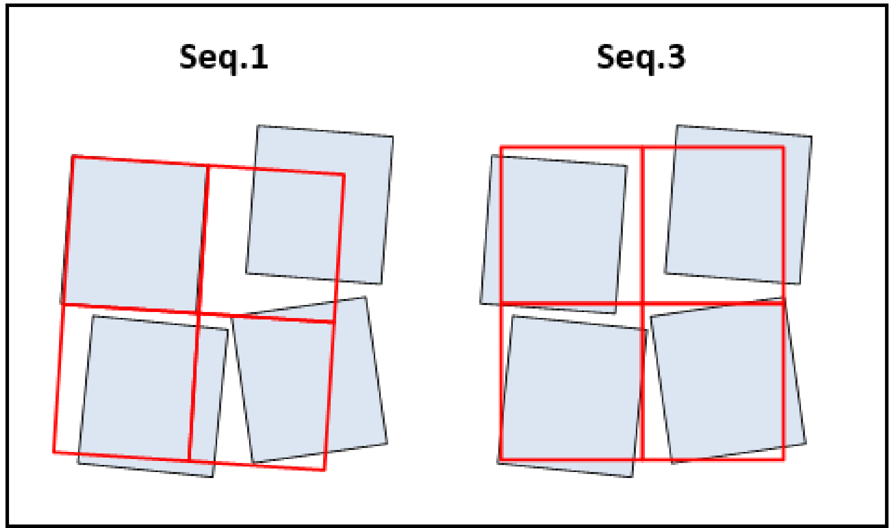


Figure 7: Overlay error of Seq.1 and Seq.3.

Figure 7 shows an image of a 4-shot exposures sequence when overlay exposure is performed with Seq.1 and Seq.3, for a substrate with position error in the lower layer. Each picture shows the overlapping result of a 4-shot overlay that integrates the 4-shots into one large device using a stitching exposure. Seq.1 performs the alignment measurement at a specific shot for each chip (upper left shot in Figure 7) and performs overlay exposure using the single-shot data. Overlay error does not occur with respect to the shot for which the alignment measurement is performed, but for the other shots in the device, overlay error can be large because overlay exposure is performed without directly measuring the positional error of all the lower shots. On the other hand, Seq.3 averages and applies overlay compensation based on the positional error of the four shots of the lower layer. Stitching accuracy for the single large device can be improved while minimizing overlay error across the field.

Experimental results

The following sections discuss various aspects of the experimental results.

Verification of stitching and MMO accuracy. Figure 8 shows the results of MMO and stitching with no position error in the lower layer. This distortion-free exposure condition commonly uses global alignment (Seq.1) and the MMO accuracy results reflect the stitching accuracy of 4 shots that are stitched into one large array and overlaid over the lower layer using the stitching exposure.

The results of MMO are 3σX: 58nm and 3σY: 49nm, which is less than the process target of 100nm. Overlay exposure to the lower layer is achieved with high accuracy. Stitching accuracy with adjacent shots was also confirmed to be 3σX: 61nm and 3σY: 33nm, which also achieved the target accuracy of 100nm. By using the new stepper, we were able to confirm the results of a high-precision exposure in both MMO and stitching accuracy for non-distorted substrates.

Confirmation of distorted layer position error on stitching and MMO accuracy. The results of performing overlay exposure on the substrates with position errors shown in Table 2 are discussed in this section. Figure 9 shows the results of the stitching accuracy under the three alignment conditions. The horizontal axis is the lower-layer random shift amount and the vertical axis is the 3σ value of the stitching accuracy.

In the case of global alignment (Seq.1), the correction value calculated from the position error of the lower layer is commonly corrected for all shots in the wafer during exposure. Adjacent shot overlay error in the 4-shot device can be controlled within the range of stage-grid accuracy and distortion accuracy of the exposure system and is not affected by the position error of the lower layer.

Similarly, in the case of every shot (chip-common) (Seq.3), the alignment measurement is performed on all shots, but the measurement values of four shots in each

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chip are averaged, and the overlay exposure is performed by applying a common correction to four shots in each chip. Therefore, it was confirmed that the stitching accuracy was the same as that of Seq.1 and was also not affected by the position error of the lower layer.

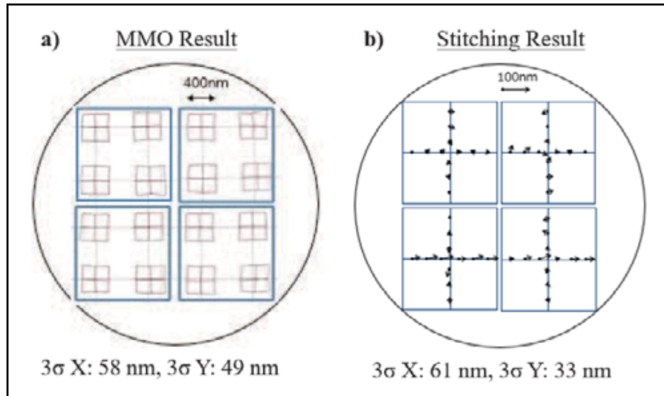

Figure 8: a) Wide-field stepper MMO, and b) stitching results.

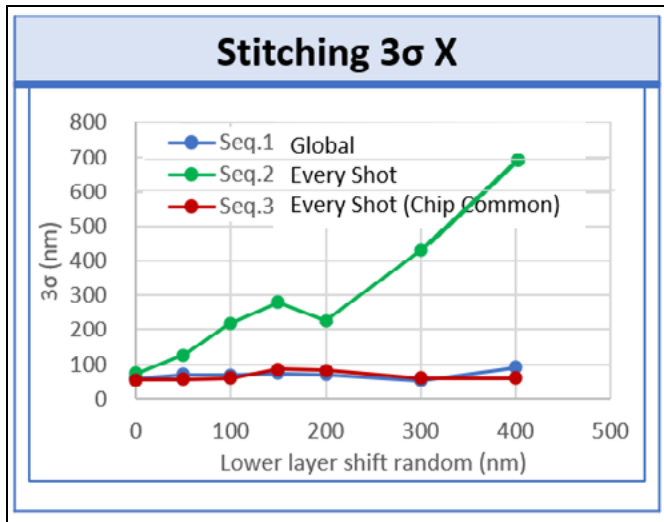

Figure 9: Stitching results.

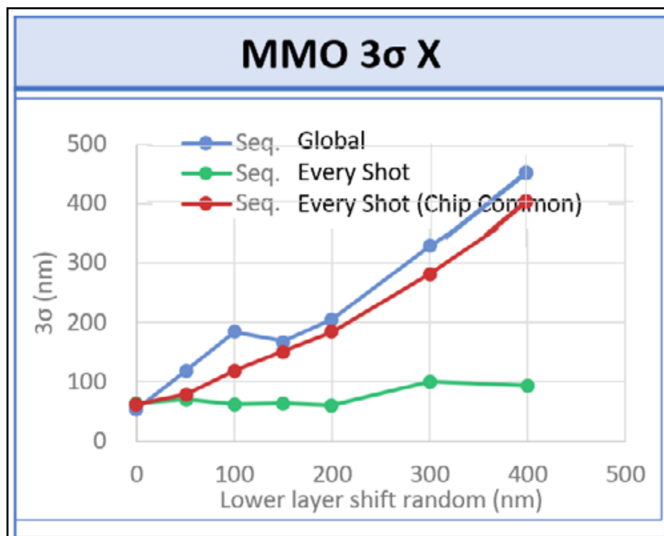

Figure 10: MMO result.

It was confirmed that when using Seq.1 and Seq.3, an adjacent shot overlay exposure could be performed without being affected by the position error of the lower layer and good stitching accuracy could be maintained. On the other hand, in the case of every shot alignment (Seq.2), the overlay exposure is performed with the goal of correcting position error with respect to the lower layer. Exposure position for each shot is determined according to the position error of the lower layer, therefore, the position error between shots in the stitching exposure depends on the position error in the lower layer, and stitching accuracy deteriorates.

Next, MMO results are shown in Figure 10. The horizontal axis is the random amount of shift in the lower layer, and the vertical axis is the MMO 3σ value. In the case of every shot alignment (Seq.2), the overlay exposure is performed to correct the position error of the lower layer. It was confirmed that the Seq.2 MMO accuracy is not affected by the position error of the lower layer and MMO accuracy can be maintained. On the other hand, when exposure was performed using the global alignment (Seq.1) and every shot (chip-common) (Seq.3) sequences, the position errors of the four shots of the lower layer are averaged to calculate the exposure correction value. MMO accuracy deteriorates with respect to the lower layer. It should be noted, however, that the MMO accuracy was improved relative to global alignment (Seq.1) when applying exposure with every shot (chip-common) (Seq.3). MMO accuracy improvement was confirmed by correcting the position error of the average of four shots that are combined into one large device using a stitching exposure.

Data also shows that Seq.3 processes can tolerate greater substrate distortion while maintaining MMO within specifications. Table 4 shows the maximum position errors that can be tolerated on a substrate for each alignment sequence, while still maintaining MMO. The maximum lower layer shift random values required to achieve MMO 3σ 100nm and 300nm when exposed in the global alignment (Seq.1) and every shot (chip-common) (Seq.3) sequences are shown. By selecting Seq.3, the position error required for the lower layer can be reduced by 30nm.

MMO3σ	Seq.1 Target	Seq.3 Target	**Seq.3 Improvement amount**
100nm	36nm	76nm	**40nm**
300nm	280nm	316nm	**36nm**

Table 4: Position error of the lower-layer and MMO achievement condition.

The effect of each alignment sequence on overlay accuracy is shown in Table 5. By selecting the optimal alignment sequence for each device process, high-accuracy overlay exposure with accurate stitching required for large device fabrication can be realized.

	Sequence	Stitching	MMO
1	Global	○	×
2	Every Shot	×	○
3	Every Shot (Chip Common)	○	Δ (Superior vs. Seq.1)

Table 5: The effect of each sequence on accuracy.

Confirmation of MMO accuracy improvement by changing the alignment sequence. To investigate the effect of different alignment sequences on MMO improvement in more detail, we estimated the effect of the lower-layer position error, and the residual overlay correction error for each sequence. In this study, the relationship between the position error of the lower layer and the correction residual (MMO) when the overlay exposure is performed for each sequence was confirmed by simulation. In fact, it is known that the position error of the LSI is on the order of a few microns to a dozen microns, and is affected by the bonding error, die shift during molding, and other factors. Here we confirmed the effect of different alignment sequences to overcome lower-layer errors in the range of magnitude common in LSI applications. In this simulation, as in the experiment, the correction results of overlay exposure are shown. Alignment measurement and correction were performed for each sequence and the position error of the lower layer is random according to the normal distribution.

Figure 11 shows the relationship between the position error of the lower layer and the maximum MMO error. The horizontal axis is the lower-layer random shift amount, and the vertical axis

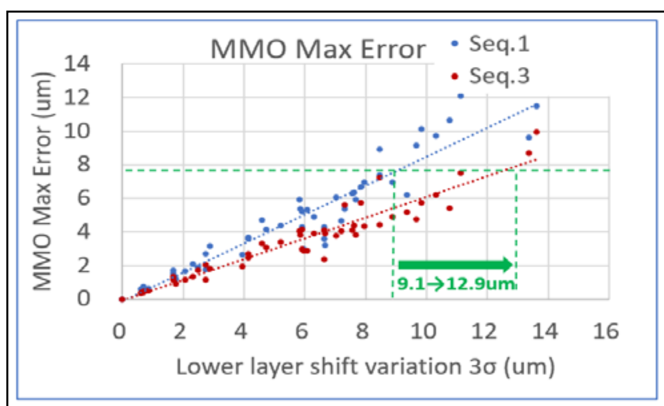

Figure 11: MMO simulation result.

is the maximum residual MMO error value. As can be seen from Figure 11, the slope of Seq.3 (red line) is smaller than that of Seq.1 (blue line). Even when evaluating position errors within the range of LSI, the result shows that MMO improves using Seq.3. The improvement rate is shown in Table 6.

The linearity of Seq.3 is 0.62 and that of Seq.1 is 0.88, indicating that the MMO error is less affected by the random shift amount of the lower layer. For example, if the MMO error is allowed to be 8µm, the shift error of the bottom layer can be

	Seq.1	Seq.3	Improving rate (Seq.1 / Seq.3)
Error Linearity	0.88	0.62	1.42

Table 6: MMO improvement result.

relaxed from 9.1µm to 12.9µm. By selecting a new every shot (chip-common) alignment sequence, it was confirmed that the tolerance of the LSI bonding error can be increased by 1.4 times compared with the conventional global alignment sequences.

Summary

In this study, we investigated the feasibility of high-density patterning for large interposers and the possibility of improving MMO accuracy for LSI interposers. As a result, it was possible to show that by selecting the optimal alignment sequence with the latest stepper, the overlay accuracy can be improved for large interposer production, as well as for fabrication of substrates with embedded local Si interconnect chips. Alignment sequence optimization allows processing substrates containing large position errors while maintaining the stitching accuracy required for RDL connection. These results show that challenges presented by stitching and substrate position errors can be mitigated, which is expected to help enable development of future silicon and high-density Si bridge interposers.

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Biographies

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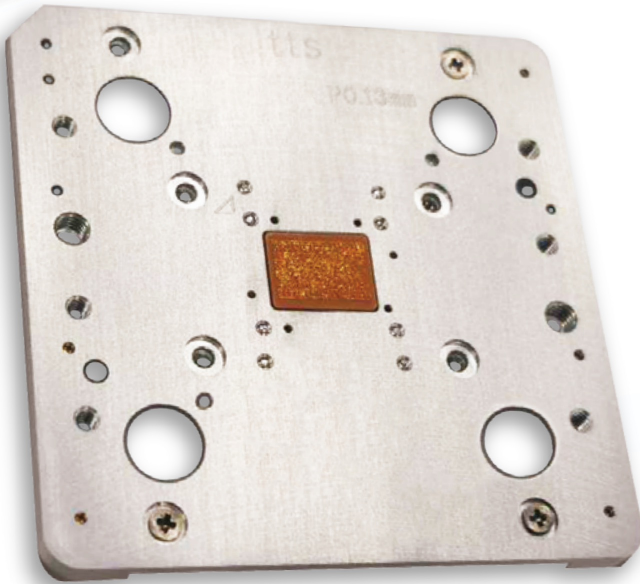

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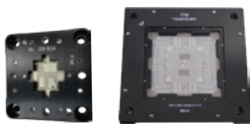

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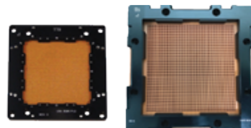

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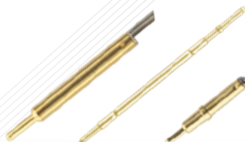

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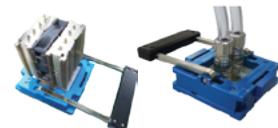

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Vertical fan-out (VFO) package with enhanced form factor and performance for mobile applications

By Ho-Young Son, Ki-Jun Sung, Kyoungtae Eun, Seowon Lee, Sungwon Yoon, Kangwook Lee [SK hynix Inc.]

Heterogeneous and homogeneous integration schemes with advanced packaging have recently been the subject of extensive discussion and development in order to pursue optimum electronic system performance. The concept of miniaturized systems is particularly important for mobile applications that demand more integrated functionality, better electrical performance, and smaller form factors. The fan-out wafer-level package (FOWLP)—one of a number of advanced packaging technologies—is one of the latest to meet the requirements of smaller form factor and higher performance for mobile applications.

In this paper, a vertical fan-out (VFO) package has been introduced as the next-generation platform based on FOWLP. VFO has better thermal, mechanical, and electrical performance than current memory packages in fine-pitch ball grid array (FBGA) applications. VFO has features including vertical wires on reconstructed stacked dies and multiple redistribution layers (RDLs) with a simple manufacturing process. It has a thinner z-height that is 27% less than the height of an FBGA that is achieved by eliminating organic substrates. Mechanical, electrical and electromagnetic interference (EMI) characteristics of a package were also evaluated. In addition, board-level reliability (BLR) drop, temperature cycling (TC), and package reliability were evaluated.

Introduction

Microelectronic devices for mobile, networking, and high-performance computing (HPC) applications have grown the semiconductor market. These applications have driven improvement in semiconductor device performance—and they continue to be driven by front-end scaling technology. However, fab nodes have reached limits due to manufacturing costs associated with the designs and processing of chips. To overcome this restriction, advanced packaging technology currently plays a critical role in lowering fab costs and delivering the required form factor and improved electrical and power consumption requirements.

FOWLP is extensively being adopted as an advanced packaging solution because it allows for more design flexibility, a smaller form factor and better electrical performance [1]. Therefore, FOWLP is readily implemented in mobile applications where package profile thickness in package-on-package (PoP) is a key consideration for the final product. Recently, application processors (APs) with FOWLP have been studied using either Cu pillar, gold vertical wire, or an organic interposer [2-6]. Contrary to a thinner AP height in a mobile system, memory packages on fine-pitch ball grid arrays (FBGAs) are also faced with consistent challenges to reduce their z height by scaling up of capacity and density. There are several ways to reduce thickness—it can be done by decreasing the thickness of components such as memory dies and die attached films. However, everything has been approaching its physical limitation even though it is minimized up to its critical point. Therefore, a more effective way to lower the package z-height is to use FOWLP technologies that could eliminate organic substrates in package circuits. For this reason, various candidates of FOWLP for memory applications have been studied [7-8].

In a previous study [9], we developed an ultra-thin memory fan-out package that utilizes multiple die reconstructions with two landing and 4-high stacks using vertical wires and multiple RDLs. This package was named "vertical fan-out" (VFO) and is shown in **Figure 1**. In this paper, we investigate the fabrication process and integration of a VFO package and discuss results of studies regarding its mechanical and electrical performance, as well as EMI and reliability characteristics for mobile applications.

VFO process flow

The overall process flow for the manufacture of a VFO package is described in **Figure 2**. The VFO package is processed using an RDL-last process based on FOWLP to further reduce the memory package height and simplify the process steps. At first, a release layer for a temporary process is coated over a 300mm glass wafer that is used as the carrier; then a flexible mold material

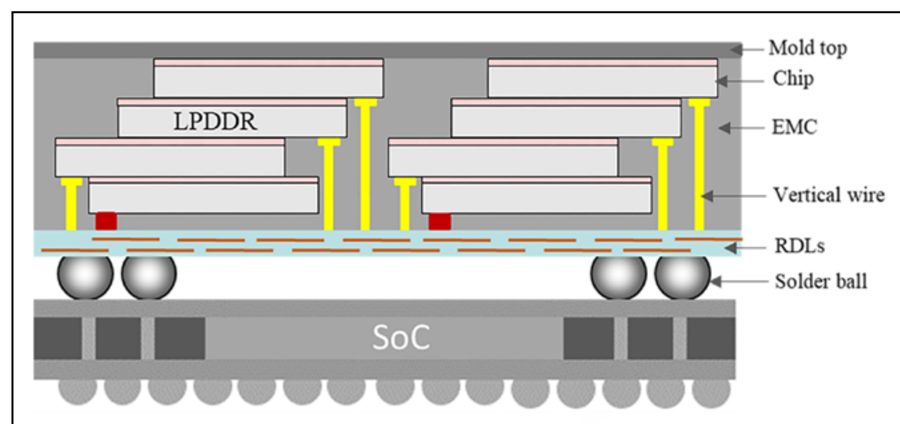

Figure 1: Schematic illustration of a VFO on an SoC package.

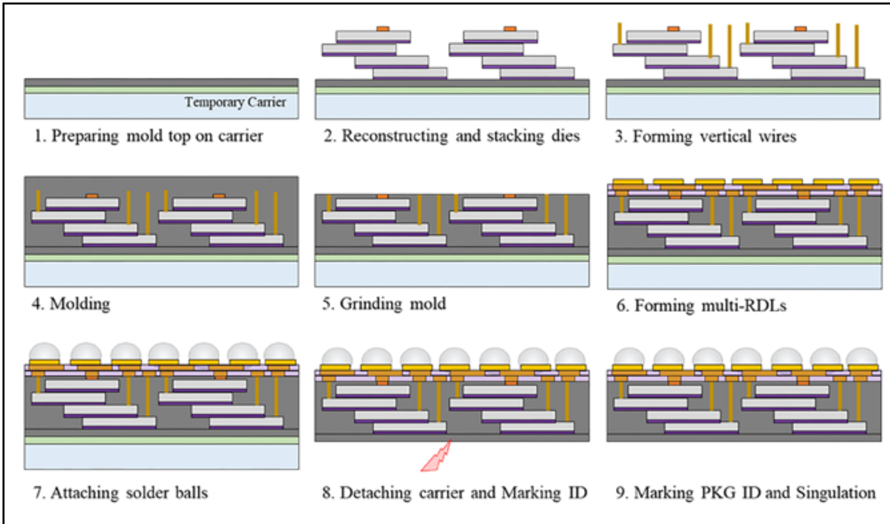

Figure 2: VFO packaging process flow.

is laminated for the mold top on the carrier. Second, after memory dies in a chip-to-chip (C2C) arrangement are reconstructed and stacked on the mold top in sequence, the vertical wires that directly interconnect with the RDLs are formed along the peripheral pad on a fine-pitch array containing dies. Third, the entire assembly units containing the dies and vertical wires are encapsulated with epoxy mold compound (EMC) using a wafer molding process. Then the overmold is reduced with a normal wafer backgrind process. Fourth, RDLs that replace the substrate are processed on the top of the grinded mold surface. The grinded mold surface consists of copper (Cu) for the RDL, and photosensitive dielectric insulation (DI) that is used as the interlayer passivation. After the RDLs are fabricated, solder balls are placed using a reflow process. Finally, the glass carrier is debonded and the package singulation is performed on the molded wafer.

Package integration

As shown in **Figure 3**, it is evident that vertical wires and RDLs in the package were well connected and integrated with each other. VFO thickness was decreased by 27% from 0.69mm to 0.50mm as a 20µm mold top and three thin RDL layers were applied. **Table 1** presents the comparison of VFO and normal FBGA thicknesses.

Forming vertical wires and encapsulating them with epoxy mold compound (EMC) are very important processes with respect to joint interconnection yields. In other words, vertical wires inside the EMC could be moved by high pressure and temperature during the mold process. Shifted wires

	VFO	*FBGA*
Substrate(RDL)	40µm	100µm
Package body	240µm	280µm
Mold Top	20µm	110µm
Solder ball	200µm	200µm
Overall PKG THK	500µm	690µm

Table 1: Comparisons of overall package thickness and other package constituents.

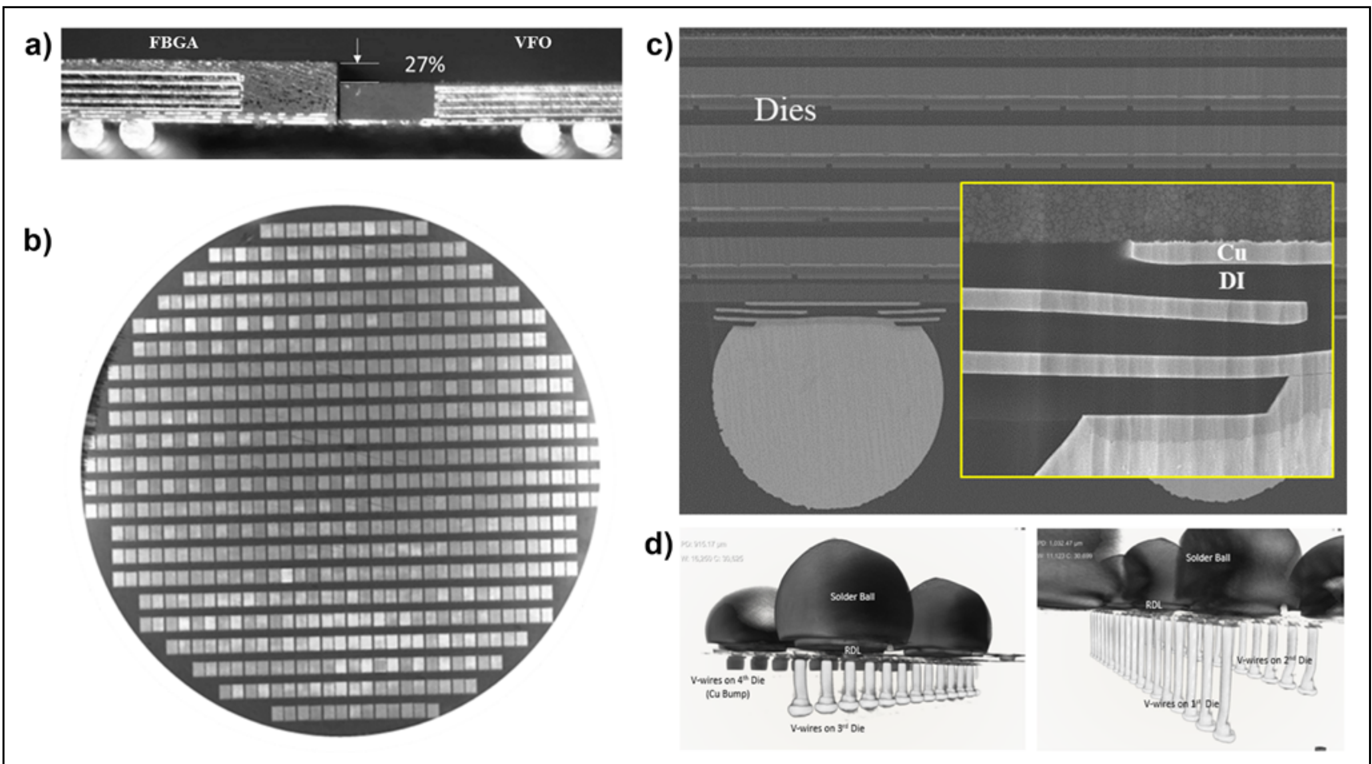

Figure 3: a) Comparison of package thickness of FBGA and VFO structures; b) Wafer SAT image; and c) Cross-sectional view and d) images of a VFO package.

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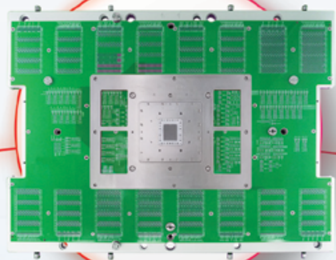

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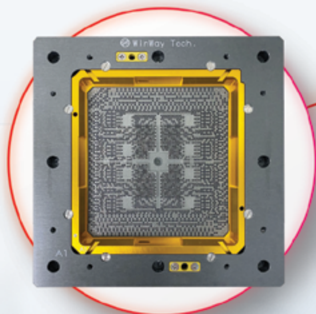

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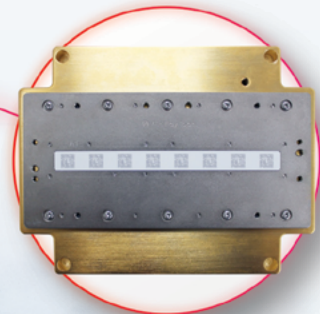

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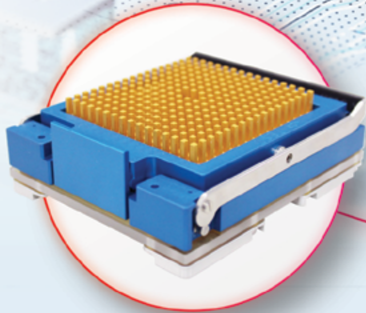

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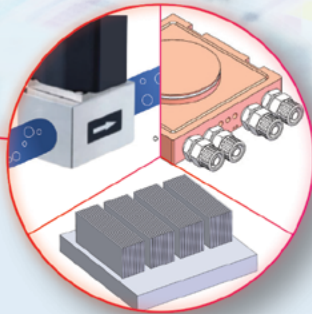

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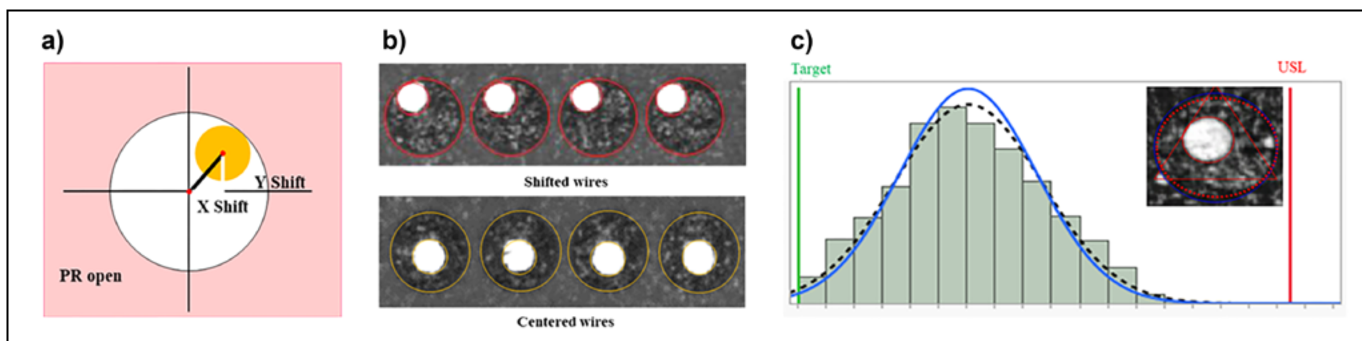

Figure 4: a) PR-wire center-to-center distance; b) AVI image; and c) Whole inspection data for a wafer.

could be induced with an electrical short problem. Therefore, the accuracy of the photoresist (PR)-wire center-to-center distance is crucial for the joint yield on vertical wires and RDLs. Auto visual inspection (AVI) was conducted after the initial RDL process. As shown in **Figures 4a** and **b**, vertical wires were located within the PR opening area. The distance of shifted wires was calculated using the equation as presented in **Eq. 1**.

$$\text{Distance} = (X^2 + Y^2)^{1/2} \quad \textbf{Eq. 1}$$

After the process optimization for forming and molding vertical wires, the maximum wire offset with a Cpk>1.67 was measured through AVI during whole-wafer inspection. This result indicates minimal shifts in wire position across the entire wafer.

Wafer and package warpage

The wafer warpage performance of VFO—influenced by the coefficient of thermal expansion (CTE) of the EMC—was assessed using three types of EMC to minimize warpage during the fabrication process. This is crucial because it can impact the electrical pattern of RDLs depending on the quality of the fine lines and spaces. In this study, to understand the behavior of molded wafer warpage, we considered A, B, and C type EMC materials on a 0.8mm thickness glass carrier. The material properties of the EMCs are detailed in **Table 2**. Following the optimization of EMC dispensing and compression molding—which included the process steps of molding and the entire RDL process—wafer warpages were measured using shadow moiré interferometry.

The maximum allowable warpage of a 300mm reconstituted wafer after molding and grinding is recommended to be 3mm; however, around 1.0mm is preferred for a high fabrication yield. As shown in **Figure 5**, the warpage of wafers with A and B types of EMC after the molding process has been found to be all in a "smiling" wafer configuration, and the warpage values rapidly increased during the RDL process as the layer of RDLs increased while stacking Cu and the DI materials. The maximum warpage using A and B EMCs is 2.8mm, and 1.7mm, respectively. It means that the tensile residual stress due to CTE mismatches of the RDL's material and the EMC on the glass carrier results in the molded wafer having the "smiling" type of warpage. However, the C type EMC, which has a smaller CTE gap compared to the glass carrier used in the process, has a lower CTE than the A and B types.

Again, referring to **Figure 5**—before proceeding to the second step in the RDL process flow—there was minimal change in the warpage. However, substantial changes occurred when transitioning from the second layer to the third layer of photodielectrics in step 3 of the RDL process flow. This result implies that thick dielectric material induces more tensile stress even though the glass carrier is a low CTE material. To mitigate the wafer warpage, the CTE values of the EMC and glass carrier should be as close as possible. After the fabrication process, the C-type VFO package warpage was over 54µm in a "crying" shape at 30°C, and -59µm in a "smiling" shape at 260°C. As shown in **Figure 6**, the warpage trend of the C-type VFO package closely matched the warpage trend of the FBGA package with only a slight difference.

	A Type	B Type	C Type
CTE1(α1)	25ppm/°C	23ppm/°C	9ppm/°C
CTE2(α2)	41ppm/°C	37ppm/°C	19ppm/°C

Table 2: Comparison of the CTEs of various EMC materials.

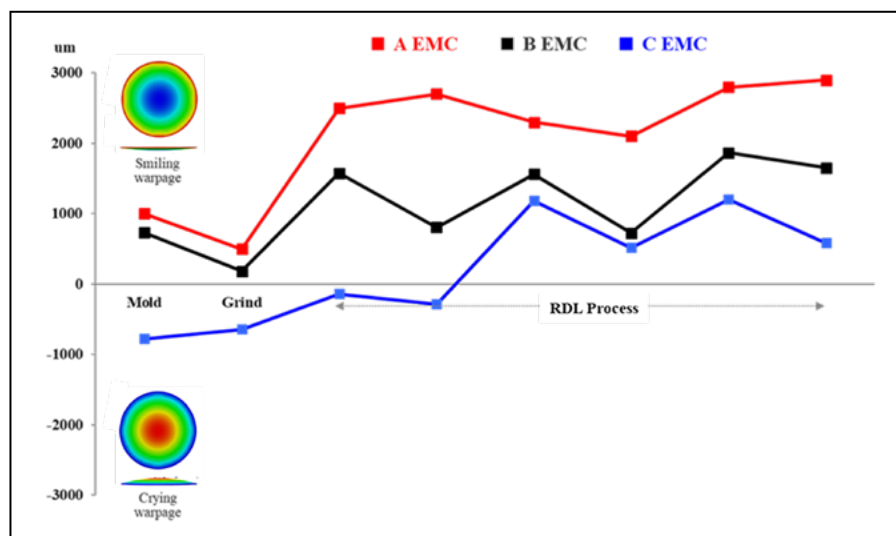

Figure 5: Wafer warpage values for three types of EMCs used in VFO manufacturing processes.

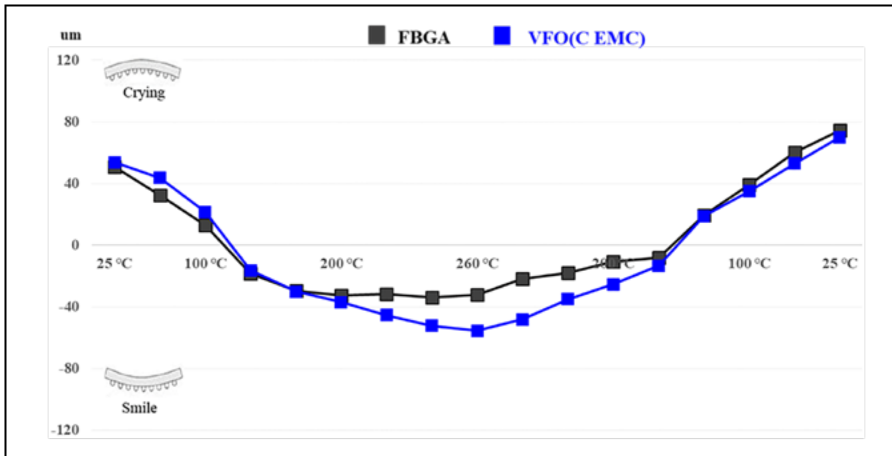

Figure 6: Package warpage values for FBGA and VFO packages with a C-type EMC.

The reason for the improvement in electrical characteristics of the VFO package was that power integrity (PI) characteristics were improved by adopting fan-out technologies [8-9]. The end result of optimizing the reduction in capacitance and increasing the inductance in the VFO package was to match the impedance of the AP package within the characteristic margin.

After conducting simulations to optimize the DI and Cu thicknesses in the RDL, the electrical characteristics of the VFO package were validated and a comparison was made with those of the FBGA package. As shown in **Figure 8**, the verification results of Rx valid windows for the VFO package showed a notable 5.4% improvement over those for the FBGA package. Furthermore, measurements of package characteristics confirmed enhancements of 5.5% for tDS (data setup time), and over 20.0% for tDH (data hold time).

RDL design optimization for electrical performance

To investigate the electrical characteristics of the VFO package, electrical simulations of a PoP structure with a memory package at the PoP-t (top) and an AP package at the PoP-b (bottom) were conducted using RDLs with DIs and Cu layers of varying thicknesses. The driver model was based on the 12Gb LPDDR4x SPICE model. The experimental conditions included various RDL thicknesses from 2.0µm to 8.0µm in 2µm increments, and Cu thicknesses from 2.5µm to 3.5µm in 0.5µm increments. As shown in **Figure 7**, the results indicated that with increasing DI thickness and decreasing Cu thickness, the DATA eye windows were narrowed. Optimization experiments for DI and Cu thickness revealed that the highest performance was achieved with a DI thickness of 4.0µm and a Cu thickness of 3.0µm. In the RDL thickness variation simulation, all VFO eye windows were notably wider than those for the FBGA package.

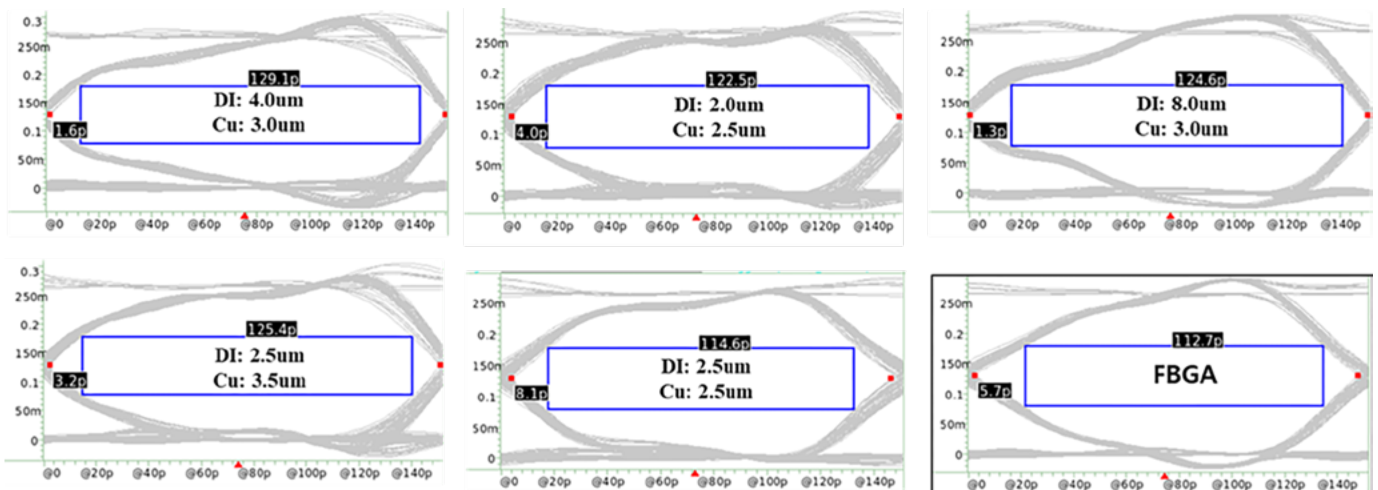

Figure 7: Simulation eye diagrams for various DI thickness values of RDLs and Cu in VFO and FBGA packages at 6400Mbps.

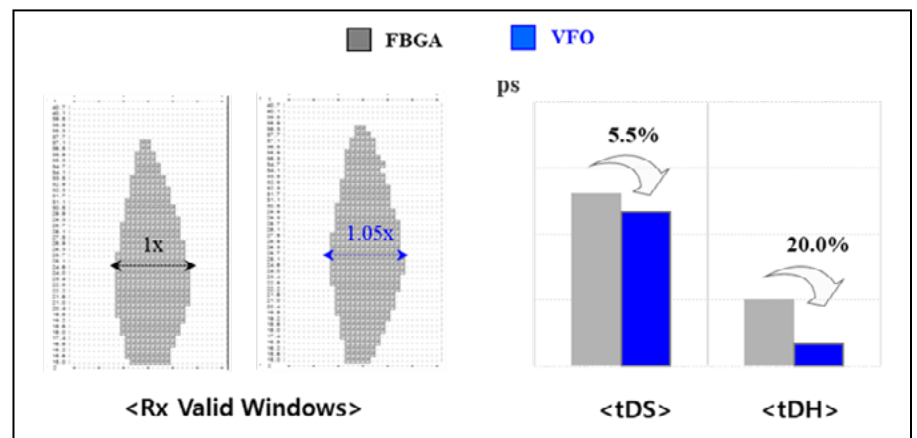

Figure 8: Eye diagrams of various DI thickness values of RDLs and Cu in VFO and FBGA packages at 6400Mbps.

EMI performance of the VFO package

Near-field electromagnetic radiation was measured at frequencies from 100MHz to 8GHz by using a scanning system to evaluate EMI performance of the VFO package. A magnetic field probe with a diameter of 1mm was employed to separately measure the Hx and Hy near-field components. The scanning area was 18mm x 16mm—including a package structure with a 1mm interval—and the distance between the probe head and the top surface of the package was maintained at 1mm. Measurements of the Hx and Hy near-field components were conducted under the operating conditions of a 4224MHz DRAM.

We demonstrated EMI performance focusing on the Hx near-field component because the magnetic level of Hx was found to be higher than Hy. **Figure 9** compares the area-averaged Hx near-field magnitude for FBGA and VFO packages across various frequencies. The magnetic field strength of the VFO package demonstrated a decrease in value ranging from a minimum of 0.5dB to a maximum of 2dB compared to the magnetic field strength of the FBGA package across the entire frequency spectrum. **Figure 10** shows Hx near-field maps for FBGA and VFO packages, respectively. The highest magnetic field was measured around the wire bonding areas of the FBGA package. In contrast, the magnetic field for the VFO package was consistently reduced across all measured frequency ranges.

Board-level and package-level reliability

We conducted a board-level reliability (BLR) drop evaluation on the VFO daisy chain—following JESD22-B111—and compared it with results for the FBGA package. The results of the BLR drop test are presented in **Figure 11**. It was observed that the first failure of the BGA occurred at around 20 cycles, while the VFO structure exhibited failure at around 50 cycles, thereby showing an improvement of more than 2.5X. The superior performance of the VFO package in the drop test can be attributed to a lower Young's Modulus—approximately 10% less than for the FBGA—in the EMC and in the DI materials used in the VFO package.

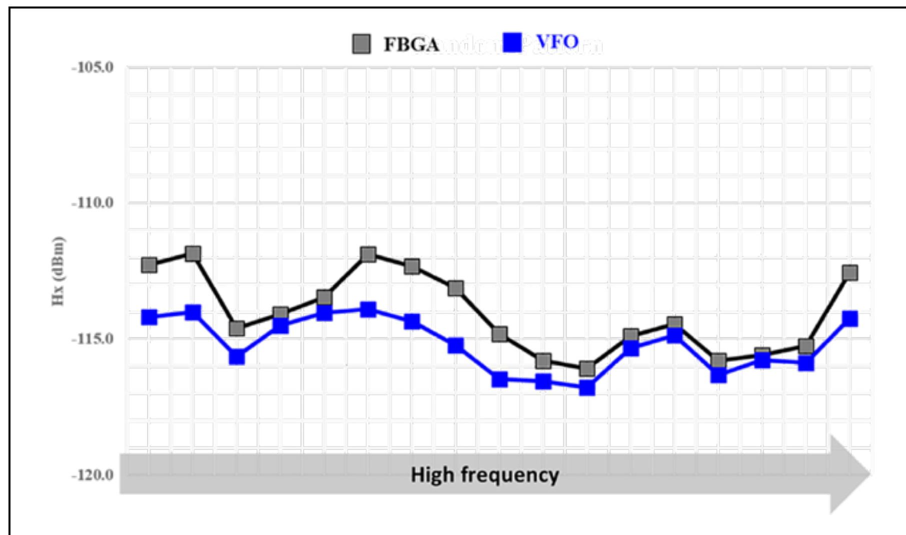

Figure 9: Magnetic field strength data at various frequencies for VFO and FBGA packages.

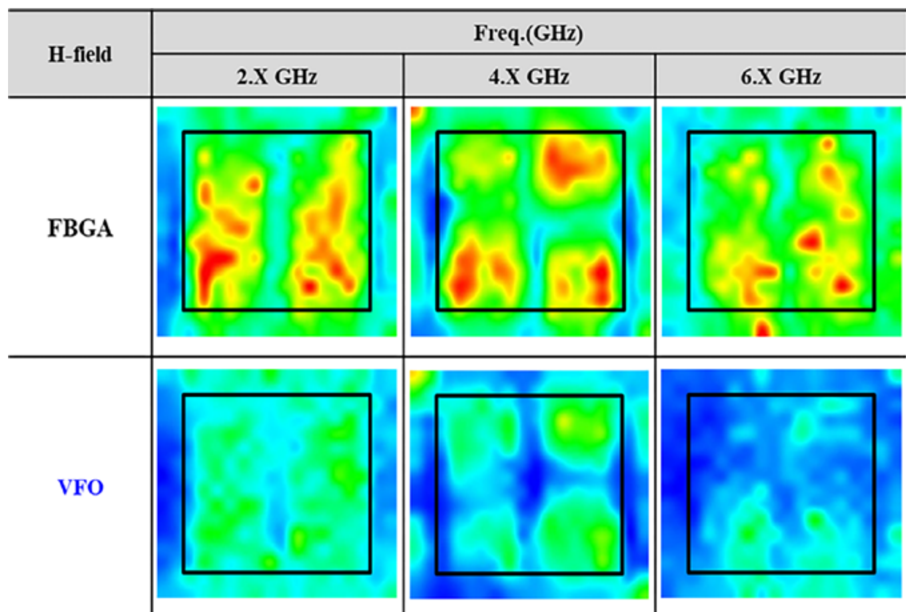

Figure 10: Near-field plot of 2.x, 4.x and 6.x GHz for VFO and FBGA packages.

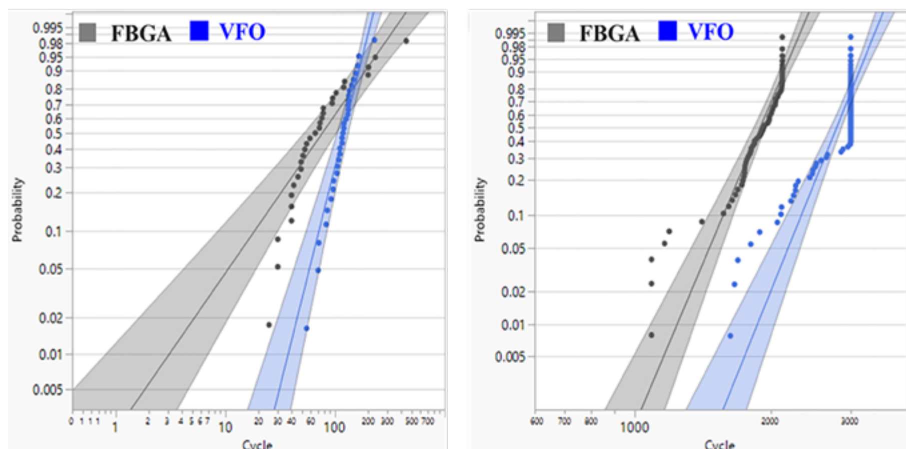

Figure 11: Results of the BLR-drop and TC tests for both VFO and FBGA packages.

These Young's Modulus values were believed to enhance the BLR drop characteristics. Furthermore, BLR thermal cycle (TC) tests—in accordance with JESD22-A104—were conducted. The test progressed from initial failure time to total failure time, while simultaneously checking for electrical shorts. The first failure for the FBGA and VFO packages occurred at approximately 1000 cycles and 1800 cycles, respectively. These results indicate an exceptionally higher thermal cycle value for the VFO package compared to the value achieved for the FBGA package. This result is attributed to the thinner VFO construction and the lower Young's Modulus for both EMC and DI materials.

Additional reliability testing of the VFO package was conducted in accordance with JEDEC standards and included the following: 1) Temperature cycling at test condition B (TCB); 2) Unbiased highly accelerated stress test (uHAST); 3) And HAST and high-temperature storage (HTS) testing as outlined in **Table 3**. The test vehicle successfully passed these tests without any delamination and with no joint cracks in the RDLs, which was confirmed using scanning acoustic tomography (SAT) and external crack analysis. The reliability test results for the VFO package demonstrated a performance consistent with the results obtained from BLR-TC tests.

	Condition	VFO
TC-B	-55~125°C/1000Cyl.	Pass
uHAST	110°C/85%, 168hrs.	Pass
HAST	130°C/85%, 168hrs. Applied Max. Voltage	Pass
HTS	150°C/1008hrs.	Pass

Table 3: Reliability test results for a VFO package.

Summary

In this study, we introduced the application of FOWLP technology in mobile products focusing on the VFO structure, which features vertical wires and a RDL. The effectiveness of the VFO package was comprehensively investigated in terms of form factor, mechanical/electrical/EMI characteristics, and package reliability. The VFO package demonstrated a 27% reduction in z-height, and exhibited wafer warpage under 1mm, as well as a package warpage trend that is consistent with that of a FBGA package. This thinner package profile aligns well with the ongoing demand for reduced package z-height in PoP applications. Furthermore, the electrical characteristics were also improved by 5.5% for tDS, and 20.0% for tDH, respectively. EMI performance at high frequencies was reduced by 2.0dB. Collectively, these findings underscore the distinctive benefits of a VFO package, making it a promising solution for advanced packaging for mobile devices. BLR-drop and TC tests exhibited improved characteristics with an increase of 50 cycles, and 1800 cycles, at the first failure point, respectively. The reliability evaluation indicated no critical failures.

VFO technology has the potential to be applied in a number of applications—not only for mobile memory packages, but also for wide I/O solutions. Currently, 3D memory stacking technology, such as high-bandwidth memory, is the best solution to support the requirements on the bandwidth and memory capacity. Its high manufacturing cost, however, would be a critical hurdle for wider applications. Individual and vertical interconnection from each die to fan-out RDL is effective for widening the memory bandwidth and capacity. Additionally, it is very compatible with heterogeneous integration of memory devices and other logic dies that use fan-out RDL. Therefore, VFO technology can be one of the potential solutions to overcome the current limitations in terms of memory bandwidth and capacity.

Acknowledgment

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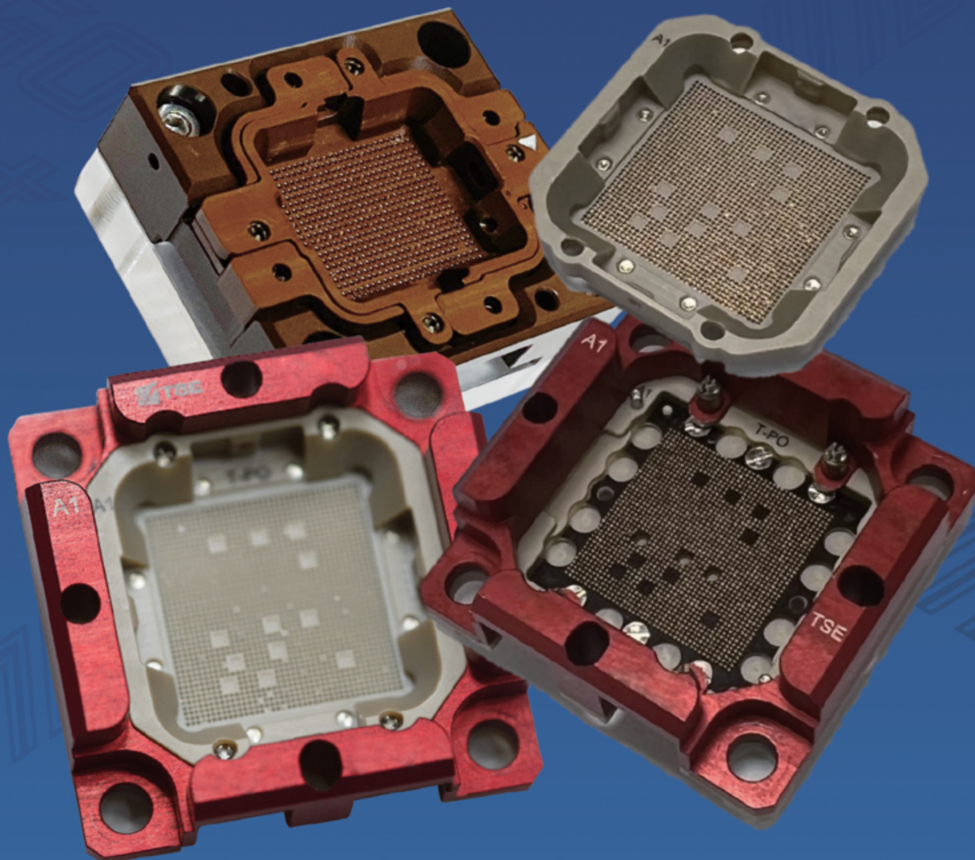

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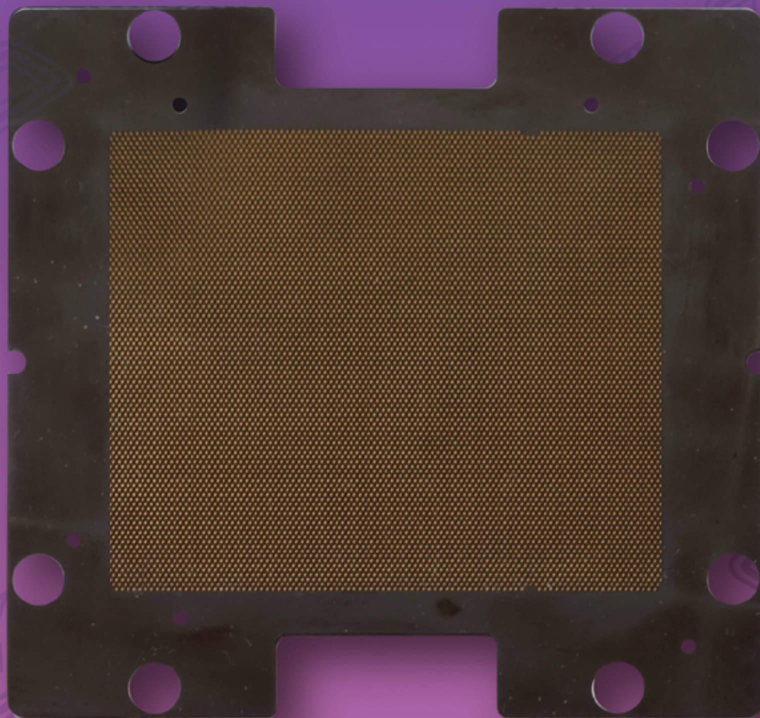

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Ultra low-loss ion-exchange waveguides in optimized alkali glass for co-packaged optics

By Lars Brusberg, Matthew J. Dejneka, Aramais R. Zakharian, Chukwudi A. Okoro, Chad C. Terwilliger, David J. McEnroe
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Co-packaged optics (CPO) with silicon photonic transceivers require novel packaging concepts and materials for significant improvements in power efficiency and manufacturing [1]. Glass substrates with integrated optical interconnects made by silver ion-exchange offer low-loss and high-density fiber-to-chip coupling. Additionally, they provide a path for high-throughput manufacturing by panel-scale processing and photonic flip-chip assembly.

One of the key applications driving CPO are switch integrated circuit (IC) packages with data throughput capacity of tens to hundreds of terabits. Corning developed a design for a 102.4Tbps glass package [2]. Both optical and electrical interconnects are integrated into a glass substrate to enable fan outs and optical fiber connectivity of multiple Tbps/mm shoreline density. The process integration includes ion exchange (IOX), through-glass via (TGV), electrical redistribution layer (RDL), and optical interface [3].

For optical interconnects in glass, the following key attributes are required for the packaging substrate or photonic interposer: 1) Low-loss (<0.05dB/cm) integrated waveguides for optical routing and fan-out; 2) Fiber connector for detachable optical fiber cable; 3) Mode-matching between integrated waveguides and optical fiber; 4) Broadband, dense, and low-loss coupling of glass waveguide to attached photonic integrated circuit (PIC); 5) Low-cost batch process scalable to panel level for larger optical circuits; 6) Supporting thermal requirements of heterogeneous packages with a service lifetime of 5 years at a temperature of 85°C; and 7) Compatibility with processes including laser processing for singulation, and modification. **Figure 1** shows two concepts of glass panel-level processing for fabrication of multi-chip modules with an area of 75mm x 75mm and a large optical circuit with IOX waveguides for optical routing with an area of 255mm x 420mm.

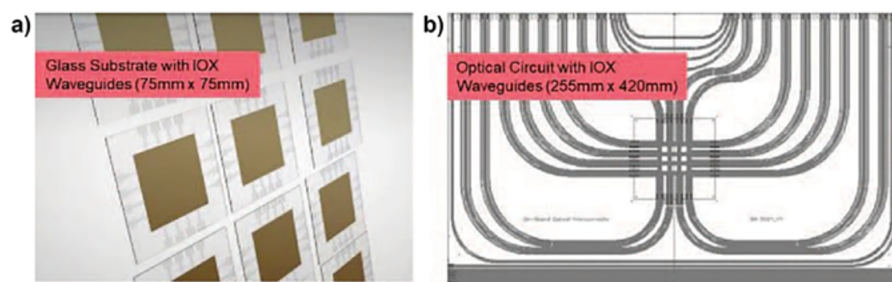

Figure 1: Schematic of glass waveguide panels for fabrication of: a) (left) Co-packaged optical packaging substrates, or b) (right) optical circuit boards.

Low-loss IOX waveguides with a loss of 0.043dB/cm [4] and alkali glass composition for longevity [5] were reported. An optimized glass meeting both requirements is needed to enable high-performance and reliable glass-based photonic packages for datacenter, artificial intelligence (AI) computing clusters, high-performance computers, or 6G applications.

Ion-exchange waveguide modeling

The following sections discuss the ion-exchange waveguide process and longevity modeling.

Ion-exchange waveguide process. A thermal ion-exchange process was selected for waveguide fabrication because of the benefit of batch processing of multiple glass substrates and the scalability for panel-level processing. The waveguide process consists of the four main process steps as shown in **Figure 2**. First, a thin-

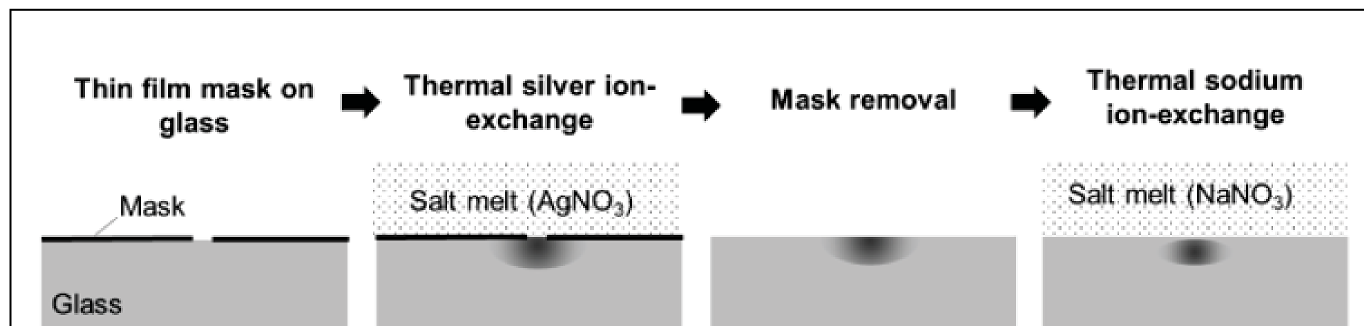

Figure 2: Process for fabrication of thermal ion-exchange glass waveguides, comprised of thin-film mask processing and two step ion-exchange.

film mask layer is made by deposition, lithography, and etching. Then, the masked glass is immersed in a molten salt bath solution containing a mixture of silver and sodium ions. Next, fiducials defined in the mask layer are protected when the mask is etched off. The last step is a sodium ion exchange to bury the waveguide core below the glass surface. The diffusion time required for the ion exchange is dependent on the glass diffusivity, which is temperature dependent.

Glass compositions with ion-exchange times of up to several hours were investigated for waveguide longevity. The optical circuit layout is defined by the diffusion mask on the glass surface during the primary ion exchange. The waveguides are formed close to the glass surface. The waveguide index contrast is controlled by the ion-exchange process parameters and the glass composition. Waveguides with a peak refractive index increase of 4.7×1E-3 were previously designed for close matching to single-mode fiber and the measured waveguide loss was reported to be 0.048dB/cm [6] at a wavelength of 1310nm.

The ion-exchange waveguide glass compositions require alkali ions to exchange with silver ions to create the higher index waveguides. These waveguides are fabricated by thermal diffusion at temperatures around 350°C. For a co-packaged optics application, the optical waveguides will be as close as a few millimeters away from the heat dissipating electrical computing chips that can dissipate hundreds of Watts of thermal power with operating temperatures significantly below the IOX process temperature, but still high enough for waveguide degradation over a period of weeks.

Waveguide longevity modeling. We developed a model to predict the service lifetime and performance of waveguide profiles and optical mode analysis dependent on operation temperature and service lifetime. A finite element method (FEM) modeling of the glass waveguides' index profile was applied to study the change in refractive index dependent on silver ion diffusivity in the glass and time. The starting condition was defined

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to be a single-mode gradient index 2D profile with an index change of Δn=0.005. Considering an air cladding at the planar waveguide glass surface, the single-mode fiber coupling loss was calculated by the mode overlap integral of fiber and waveguide mode to be 0.3dB at a wavelength of 1310nm.

Over its lifetime the waveguide core index can drop due to bulk diffusion in the glass, which increases the total area of the gradient index and reduces the index contrast that leads to less-confined optical modes. For example, a 5% index contrast reduction does not significantly change the optical waveguide mode and fiber coupling loss increases by only 0.04dB. However, a 50% index drop of the core leads to an additional fiber coupling loss of 1.12dB. A drop in optical loss of 0.04dB may be acceptable as long as it is considered in the overall maximum power budget of the total link loss (transmitter to receiver), which is 4dB for 400G-FR4 datacenter interconnects [7]. Significantly higher losses, however, may cause degradation of the signal recovered by the receiver, leading to a failed optical link before the end-of-service lifetime. For this study, we assumed a service lifetime of 5 years at a constant temperature of 85°C. It should be considered that the operation temperature can be even higher if the waveguide is directly exposed to the dissipated heat of an electrical computing chip. The computing load cycles can be variable during the day, which should also be considered for a full thermal analysis of a package.

We modeled the core index change of the waveguide dependent on the glass diffusivity for 5, 10, and 15 years. The relative decrease in core index change is shown in **Table 1**. We computed the waveguide mode in the degraded waveguide and calculated the change in coupling to a single-mode fiber. The relative increase in the coupling loss is shown in **Table 2**. For a minimum five-year threshold in service lifetime, the glass would need a diffusivity of 1E-21m/s² or less at the desired (static) maximum operation temperature to keep the index change at 5% or below and the change of fiber coupling loss is negligibly low with only an increase of 0.02dB. For a maximum temperature of 85°C, the silver ion diffusivity for the glass needs to be 1E-21m/s² or lower

D(T) [m/s²]	Decrease in Core Index Change [%]		
	5 years	*10 years*	*15 years*
1E-23	0	0	0
1E-22	1	1	1
1E-21	4	8	12
5E-21	19	30	37
1E-20	30	41	46

Table 1: Modeled change in waveguide core index contrast.

D(T) [m/s²]	Increase in Single-mode Fiber Coupling Loss [dB]		
	5 years	*10 years*	*15 years*
1E-23	0	0	0
1E-22	0	0	0.01
1E-21	0.02	0.04	0.06
5E-21	0.1	0.25	0.4
1E-20	0.25	0.57	0.87

Table 2: Modeled change in single-mode fiber coupling loss.

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to meet the service lifetime of 5 years. Currently-available glasses for ion exchange waveguides have silver ion diffusivities orders of magnitude too high to meet this longevity requirement.

Novel glass for CPO

We tailored a glass composition for CPO applications that was made and experimentally evaluated by characterization of temperature-dependent diffusion. The key objectives were to make glass that has a diffusivity of 1E-21m/s² or lower to support a temperature of at least 85°C for 5 years. We focused on a glass with low bulk absorption for fabrication of low-loss IOX waveguides, process compatibility with post-process steps like laser singulation, and compatibility with panel-scale fabrication techniques.

Corning demonstrated that the glass meets the longevity requirements for CPO. For intrinsic loss, we optimized the fabrication process and batched with high-purity raw materials to reduce tramp transition metal ions in the glass that would increase optical losses. The impact of β-OH on optical waveguide loss was studied for multiple glass compositions. **Figure 3** shows the dependency between β-OH content for seven different compositions and the optical absorption in the glass measured in dB/cm. We made a dry glass and measured 0.008dB/cm bulk absorption at a wavelength of 1310nm<0.1.

Glass was melted, refined, and then cast into 154mm diameter boules 50mm thick that were annealed and then sliced and finished to 150mm wafers for waveguide fabrication as shown in **Figure 4**. Large glass substrates for panel-level processing could be made with a different forming technology.

Low-loss waveguide demonstration

IOX waveguides were fabricated with the process shown in **Figure 2** at a temperature of 350°C for silver and silver-free IOX diffusion steps. After wafer processing, the wafer was cut into samples of different lengths. Multiple waveguides for each sample were measured with single-mode fiber probing on both sides by active alignment using high-precision hexapods. As a light source, a superluminescent diode (SLD) at a center wavelength of 1310nm was coupled into the launch fiber and index matching oil was applied between

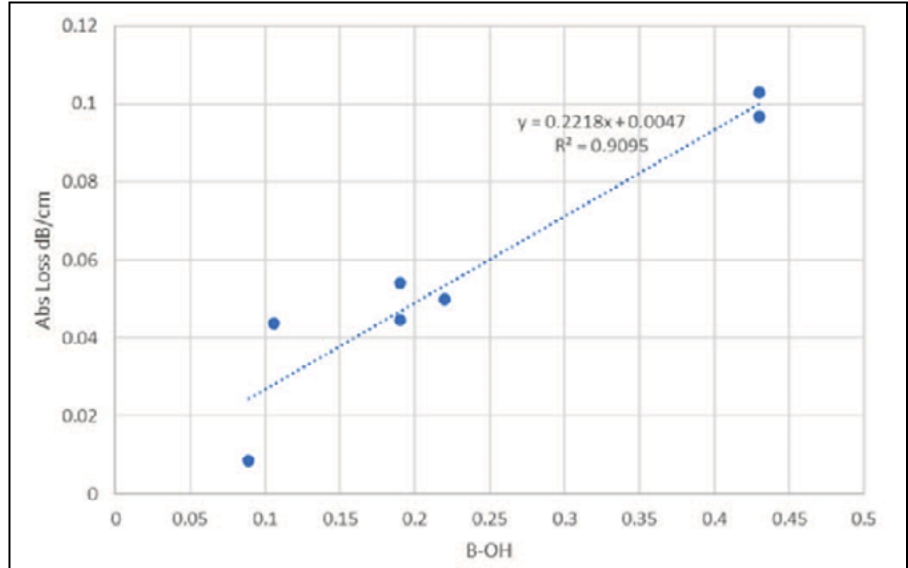

Figure 3: Dependency between β-OH concentration in seven different glass compositions and bulk glass absorption loss.

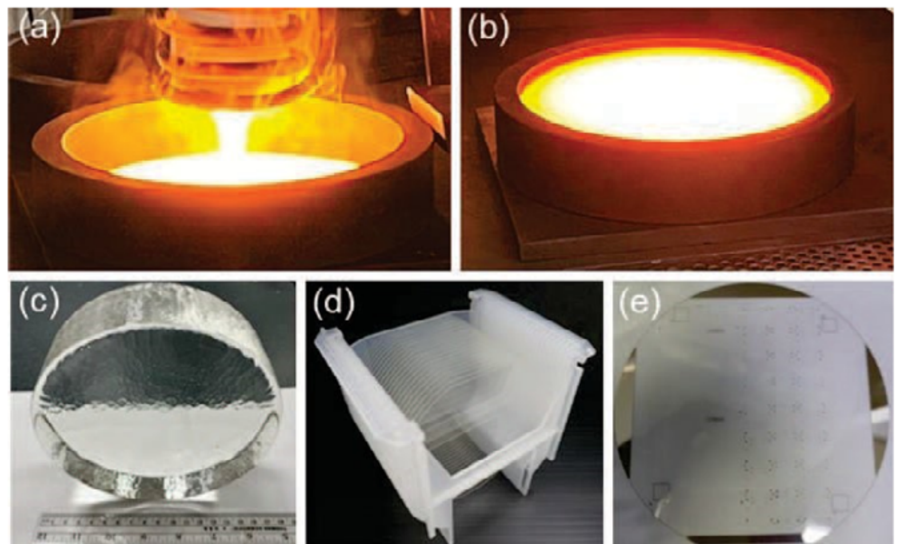

Figure 4: a) Molten glass was cast into b) boules; c) Once the boule was cooled down, d) 150mm wafers were made and e) waveguides integrated by the IOX process.

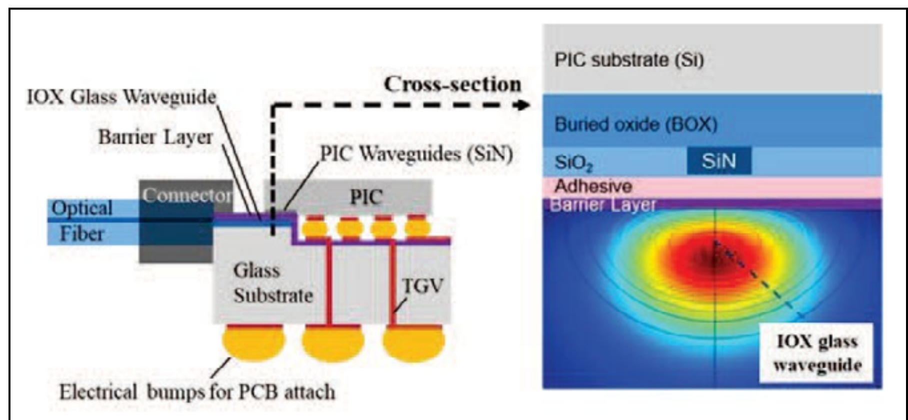

Figure 5: Glass substrate with optical barrier layer for flip-chip assembly of a PIC.

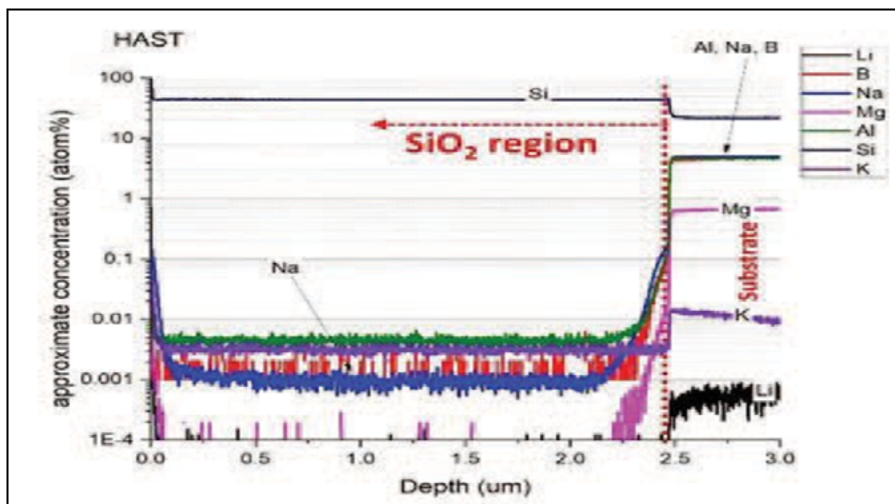

Figure 6: ToF-SIMS-based depth profile elemental analysis of test structure having SiO_2 on alkali glass. Depth profiling started from the top of the SiO_2 film into the glass.

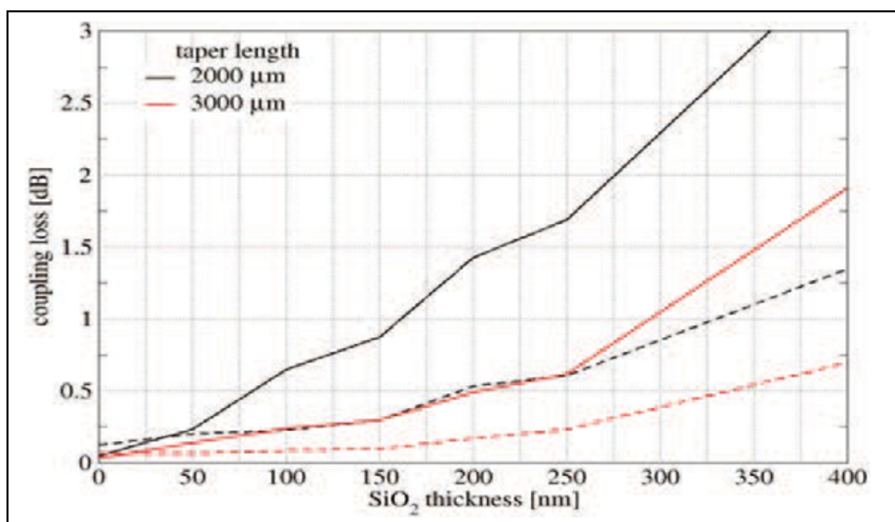

Figure 7: IOX glass waveguide to SiN waveguide coupling loss dependence on the SiO_2 barrier layer thickness. Solid lines refer to the TE mode, and dashed lines refer to the TM mode.

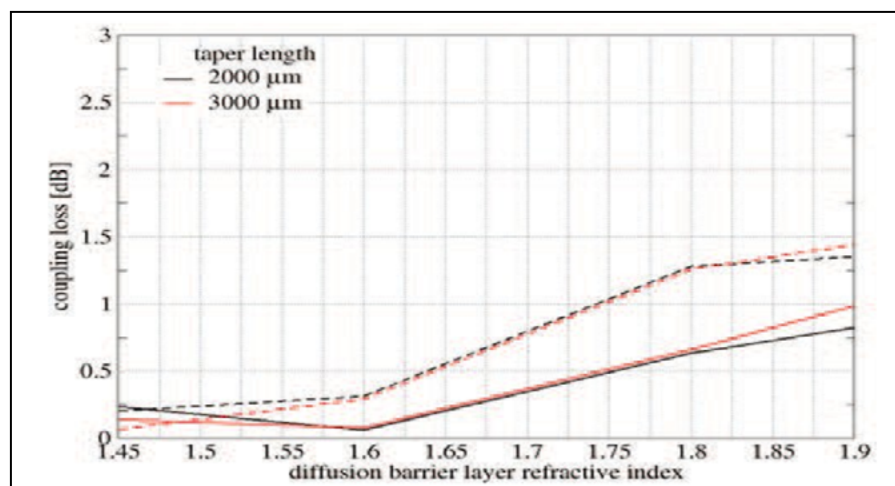

Figure 8: Coupling loss vs. the 50nm barrier layer refractive index. Solid lines refer to the TE mode, and dashed lines refer to the TM mode.

the laser cut end-faces of the glass waveguide and the single-mode fiber end faces. The collected insertion loss data of four samples at different lengths was analyzed and the propagation loss was calculated to be 0.034dB/cm. The measured fiber coupling loss for each fiber waveguide interface is 0.31dB, which aligns very well with the modeling results. The measured waveguide loss is four times larger than the bulk material loss because any imperfections in the waveguide add on top of the bulk material losses.

Alkali migration reliability

The following sections describe challenges and solutions with respect to alkali migration reliability.

Inorganic diffusion barrier layer on glass. Considering the high alkali ion content (e.g., Na^+) of the glass substrate required for the integration of optical waveguides by ion exchange, mobile ions like Na^+ can also migrate into interface materials (e.g., optical adhesive) and assembled integrated circuits and lead to changes in optical performance for the optical interface or to transistor function degradation of the IC. The addition of a barrier layer to the glass surface stops ion migration but needs to be optically transparent to maintain low-loss evanescent coupling. Additionally, the barrier layer needs to support waveguide confinement in the glass waveguides. **Figure 5** shows the packaging concept introduced in [3] with the addition of a thin barrier layer shown in purple.

A study was completed by deposition of SiO_2 on the glass by Corning. Two environmental tests were performed to evaluate sodium migration for elevated temperature operation and solder reflow assembly by highly-accelerated stress testing (HAST) at 130°C/85%RH and high-temperature storage at 300°C. We demonstrated that the deposition of an inorganic barrier layer successfully prevents the migration as shown in **Figure 6**.

Evanescent coupling with barrier layer. The impact of the thin SiO_2 layer on the IOX-to-SiN waveguide coupler performance was evaluated using designs optimized for coupling at 1310nm with a 0.5µm-

thick adhesive. The lower (than IOX glass) refractive index of the SiO_2 layer reduces the overlap between the IOX and SiN waveguide mode fields, which results in longer coupler lengths compared to the case without the SiO_2 layer. The dependence of the coupling loss on the barrier layer thickness for IOX waveguide design is summarized in **Figure 7**. The impact is most pronounced for barrier layer thickness values >200nm. For smaller thicknesses the coupling loss of <0.5dB can still be achieved with coupler lengths of 2.5-3mm.

Figure 8 shows coupling loss dependence on the barrier layer refractive index, n_b (where $n_b \approx 1.45$ corresponds to SiO_2 at 1310nm). For a thin layer, a small increase in the refractive index of the diffusion barrier layer may provide some benefit to optical coupling, as the higher index contributes to increasing the IOX and SiN waveguide mode overlap. Barrier layers with refractive index values >1.6 and/or a larger thickness can support guided modes that interfere with the direct coupling from IOX to SiN, thereby increasing the coupling loss. The layer thickness can, therefore, be optimized to enable optical evanescent coupling between ion-exchange waveguides and surface-mounted PICs with a loss <1dB, while stopping alkali migration out of the glass.

Summary

An FEM modeling approach was chosen to calculate the required diffusivity of 1E-21m/s² or less at operation temperature was required for a five-year service life. A new alkali-containing glass composition suitable for fabrication of IOX waveguides was designed that meets the longevity requirements for five years at 85°C and demonstrated a record low loss of 0.034dB/cm. To minimize the risk of alkali migration out of the glass into the attached components, an optical barrier layer made of SiO_2 is deposited on the surface and was highly-accelerated stress tested (HAST) at 130°C/85%RH and high temperature at 300°C for 1000h, thereby successfully stopping alkali migration. Keeping the barrier layer thickness below 200nm enables efficient evanescent coupling between IOX waveguides and attached Si_3N_4 waveguide components, with a simulated coupling loss of <0.5dB. The presented glass composition and the deposition of barrier layer on alkali glass increases the reliability of glass-based photonic packages for CPO at elevated temperatures.

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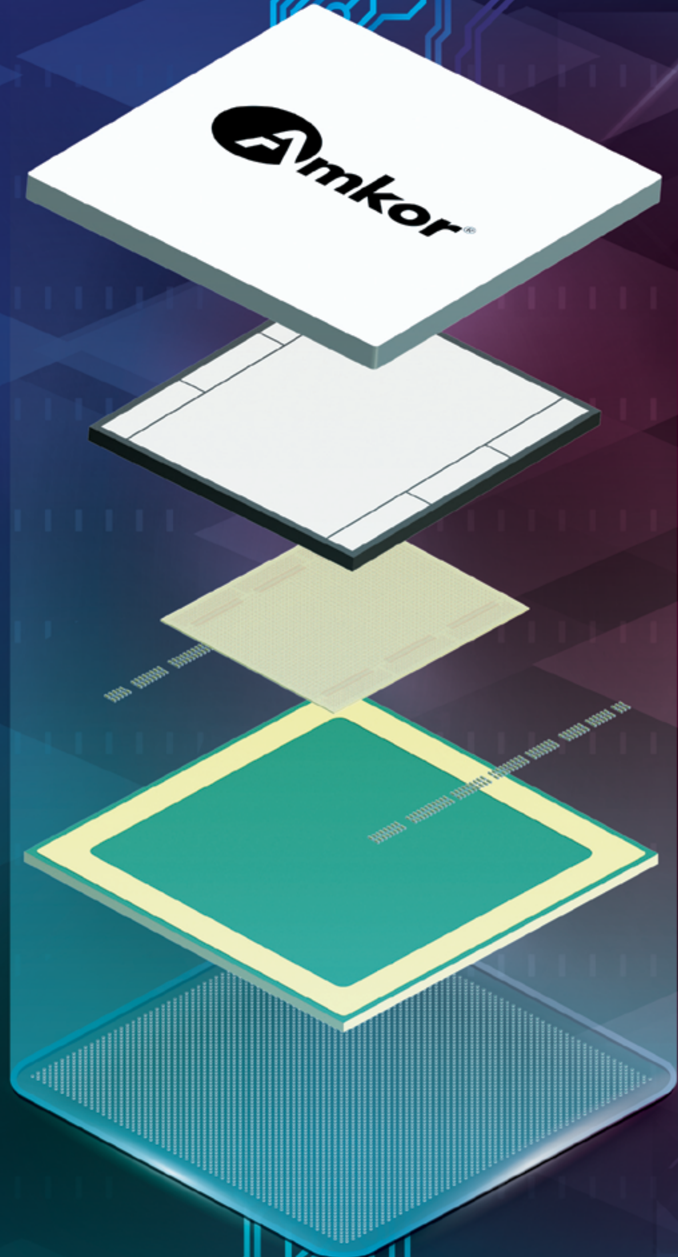

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Benefits and challenges of sensors that utilize chips and MEMS

By Richard F. Otte [Promex Industries, Inc.]

Semiconductor chips, including microelectromechanical systems (MEMS), have revolutionized sensors in recent times. The inclusion in sensors of these miniature semiconductor and mechanical devices enables detection, analysis, communication and physical motion functions. These capabilities are of use in many applications, from consumer electronics, to automotive, healthcare, and aerospace. These devices are usually small, require minimal amounts of power and enable precise measurement and control of physical parameters. However, the successful integration of chips and MEMS into sensors and other functional devices requires overcoming significant packaging and assembly challenges. This article will explore some of these multifaceted challenges, highlighting the impact of heterogeneous integration (HI) on enhancing device performance, reliability, and functionality. HI implemented with wafer-level packaging (WLP), flip-chip bonding, and 3D integration facilitates the seamless integration of sensors and MEMS with complementary components such as integrated circuit (IC) microfluidic systems, optical and ultrasonic components and others, thereby ensuring optimal functionality, reliability, and manufacturability.

To illustrate the points noted above, we will describe real-world examples of projects that have successfully addressed these sensor and MEMS assembly challenges through close coordination between engineers, material scientists, and manufacturing experts. Implementing the optimal assembly process plays an important role in optimizing sensor performance and minimizing production costs.

Sensor challenges

All sensors to be discussed contain one or more semiconductor chips. These are primarily "standalone" sensors but can be integrated into systems. Many applications require non-electronic components and therefore need HI technology—with all that implies about tradeoffs among functionality, manufacturing processes and cost.

A result is that a variety of assembly processes beyond those typically utilized for electronic devices are required. These processes must accommodate the unique characteristics of all of the parts—meaning, they cannot damage the device or cause its performance to deteriorate. Standard electronic assembly processes often incorporate reflow temperatures of 250°C, deionized water wash, automated pick-and-place tools, plasma cleaning, ultraviolet (UV) exposure, and other processes that are detrimental to MEMS and other sensing devices.

Semiconductor evolution's impact on sensors

The evolution of semiconductors has significantly impacted sensor technology by enabling smaller physical sizes, increased computing power, and virtually unlimited information storage. This evolution also facilitates low power consumption, mass production at low costs, and the ability to communicate through electromagnetic, light, radio-frequency (RF), and microwave technologies. MEMS, in particular, have benefited from this evolution, allowing for easy integration with other functions.

MEMS as sensors

MEMS technology adds a key capability to sensors; the addition of motion and the ability to move something—such as opening a valve, moving a mirror, rotating a shaft, bending a beam, etc. In a sensor, the phenomena to be sensed (e.g., pressure, velocity, distance moved) act on the MEMS device in a manner that is usually converted to an electronic measure by capacitance, the piezoelectric effect, and other methods. In addition to enhancing sensing phenomena, MEMS devices add further functionality that goes beyond sensing to add further capabilities to devices. **Table 1** offers some examples.

Sensing phenomena and components

Let's begin looking at details. Sensors and MEMS devices are designed to detect a variety of physical phenomena, including:

- Presence or concentration of a substance: These sensors can detect gases, liquids, solids, molecules, DNA sequences, and proteins, with each requiring specific technical approaches to achieve accurate readings.
- Location and position: Sensors can measure velocity, pressure, temperature, electric or magnetic fields, voltage, current flow, charge, power levels, and frequency. They

Motion	Purpose
Open a valve	Enable fluid movement or flow
Perform a repetitive linear motion	Move one part with respect to another a known amount at a known rate.
Generate circular motion with a gear train	Run a pump, Generate higher force thru mechanical advantage
Tile a mirror or antenna element	Steer a beam of RF or light
Move under pressure	Sense and measure pressure

Table 1: Typical MEMS functions enabled with micro-movements.

can also assess mass, images (including photos, videos, and light detection and ranging [LiDAR]), and time-based parameters like delay and latency.

The addition and/or combination of electronic devices with sensing components enables the electronics to collect, store/remember, analyze, and communicate data. Some key components include:

- Optical components
  - o Light emitters: Such as light-emitting diodes (LEDs), vertical-cavity surface-emitting lasers (VCSELs), and lasers that can emit single-wavelength or broadband light, sometimes with modulation.
  - o Light detectors: Including image sensors with arrays as small as 1-micron pixels, and detectors designed for specific wavelengths using bandpass filters.
  - o Light manipulation and transmission: Through lenses, prisms, fibers, and free space, ensuring accurate and efficient data transmission.
- Fluids and ultrasonic technologies
  - o Fluids: Sensors detect specific chemicals in liquids and gases.
  - o Ultrasonic technologies: Spanning kilohertz to megahertz, including point devices and arrays for source detection.
- MEMS devices
  - o Motion generation and sensing: MEMS technology enables precision in motion generation, including valves and sensors for motion detection.
- Piezoelectric materials
  - o Motion and force applied to piezoelectric materials generate high impedance voltage as an analog signal that is easily detected or amplified. These materials are reciprocal, meaning that the application of voltage to a piezoelectric material generates small amounts of motion with high forces.
  - o Piezoelectrics complement MEMS devices and are frequently used together, which includes making the MEMS device itself out of a piezoelectric material.

The above components are combined with electronics to make sensors that enable information to be gathered, analyzed, stored, consolidated/summarized, and finally, communicated in a timely manner. Many sensors communicate with a system; others an individual or multiple individuals. Some of the difficulties inherent in designing sensors are shown in **Table 2**.

Characteristics of sensors vs. other chips

Sensors differ from other semiconductor chips in their fundamental purpose and function. While traditional chips primarily focus on data processing, sensors are designed to detect and measure physical phenomena. This distinction influences their design, packaging, and assembly requirements.

Sensors often incorporate components that interact directly with the environment, necessitating protection from contamination, mechanical stress, and temperature fluctuations. These factors make the assembly of sensors more complex than that of standard semiconductor devices.

Sensors and MEMS devices detect a wide range of physical and chemical phenomena using a range of sensing mechanisms. Some of the most common include the following:

Presence and concentration. 1) Measure mass: Sensors can detect changes in mass, which may indicate the presence or concentration of a substance; 2) Interact with light: Some sensors rely on the interaction between light and materials to detect the presence of specific substances; and 3) Sense physical presence: This includes sensors that detect objects based on their physical presence, such as proximity sensors.

Measure chemical makeup. 1) Chemical reactions: Sensors can detect specific chemical reactions, providing information about the chemical composition of a sample; 2) Spectroscopy: This technique is used to analyze the interaction of light with matter, providing detailed information about a substance's chemical makeup; and 3) Electronic phenomena: Sensors that measure electronic properties like charge, current flow, and voltage are crucial in applications requiring precise electronic monitoring.

Phenomena to sense	Sensing element	Manufacturing Issues to address
Image	Photodetector array with a source of illumination An emitter or sensor array	Particle control Many parts Tolerances
Presence of a chemicals or molecule	Spectroscopy/fluorescence Chemical interaction	Contamination Fluid leakage Laminar flow needed
Contaminant in a fluid	Chemistry sensitive to contaminant Electrical conductivity	Fluid leakage Some hazardous Corrosion resistant materials
DNA Sequencing	Chemistry & fluorescence/charge sensing	Preserving chemistry functionality Create watertight fluid seals Non-standard materials
Protein, bacteria, virus	Chemistry	Contamination Some hazardous Corrosion resistant materials
Voltage, current, power	Electronic components and displays	Thermal issues from temperature rise Potential EMI shielding
Pressure	Deformable member that can be measured Pressure sensitive compound	Calibration needed Wide range of pressures; inches of water to thousands of PSI Robustness of sensor Environmental robustness
Harmful radiation; UV, X-Ray, gamma rays	Crystals Solid state detectors Spectroscopy Optical filters	Particles Scratches EMI
Position of a part	Electrical contact Capacitance Photodetectors	Sensitivity Latency

Table 2: Sensing elements and resultant manufacturing issues.

Powering sensors and MEMS devices

Powering sensors and MEMS devices is a critical consideration, especially for portable or remote applications. A number of different methods are used to supply power as listed below.

- Connect to power source: In fixed installations, sensors may be directly connected to a power supply.
- Operate from a battery: Portable sensors often rely on batteries that can be rechargeable for extended and repetitive use.
- Electromagnetic induction: Some sensors harvest energy from electromagnetic fields, reducing the need for a direct connection to a power source.
- Harvest energy from the environment: Innovative sensors can harness energy from environmental sources. Examples include solar cells or photocells that convert light into electrical energy; temperature gradient sensors that generate power from temperature differences; and pressure change sensors that can convert pressure variations into usable energy.

Sensor development costs

The development costs for sensors and MEMS devices are highly dependent on the complexity of the sensor and the anticipated production volume. High-volume production helps to amortize the development costs, making major development cost financially viable. However, demand for many sensors is relatively low, meaning margins become critical.

Custom-designed sensors, particularly MEMS, can be expensive to develop due to the complexity of design, wafer fabrication cycles, and the need for multiple fab runs to achieve the desired performance. In addition, developing sensors with unique functions is challenging and may require extensive testing. The stringency of testing depends on the application, with medical sensors demanding the highest levels of reliability.

Lifetime and shelf life

Sensor longevity varies based on the type of sensor and its application. Generally, electronic components within sensors have a long shelf life. However, some sensors, especially those with sensitive components requiring >1.0 or 0.1% accuracy, may degrade over time, require periodic calibration or even replacement.

Environmental sensitivity is also an issue. Sensors that operate in harsh environments, or those with liquid components, may have a limited lifetime due to issues like drying out, leakage, or sensitivity to temperature and light. Temperature changes may also slow the sensor's reaction time.

Examples of sensors

Several innovative sensors exemplify the range of applications and challenges in sensor design as follows:

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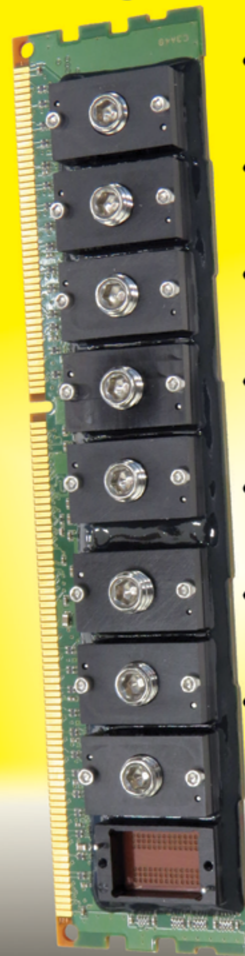

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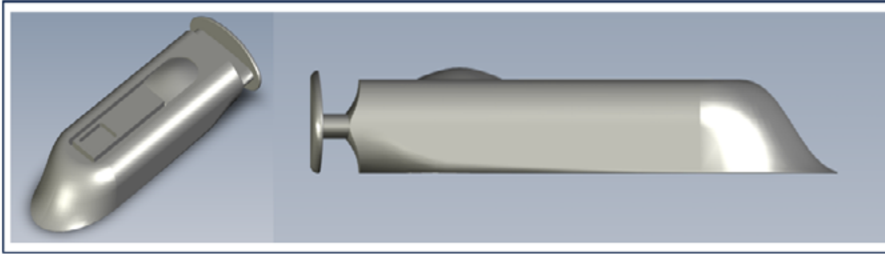

Figure 1: Glaucoma detection device designed for implantation in the eye, developed by Injectsense.

- Endoscopic cameras: These high-resolution (1024 lines, stereoscopic, full color) cameras are used in medical applications. They require minimal power (<1.0W) and are physically small (<1cm in diameter).
- Pathogen detection utilizing fluorescence: A 10-channel optical spectrometer is used to detect pathogens with high precision, demonstrating the complexity of integrating optics with sensor technology.
- Injectable pressure sensors: Used in medical applications such as monitoring glaucoma or encephalitis, these sensors must be highly reliable and operate in harsh physiological environments.
- Self-propelled pill cams: These innovative devices navigate the gastrointestinal tract, capturing images and transmitting data wirelessly.

Specific device examples

The following sections discuss two specific examples of sensors.

Glaucoma detector. The glaucoma detection device shown in **Figure 1** contains a MEMS pressure sensor, a custom application-specific integrated circuit (ASIC) that communicates the pressure to a detection device electromagnetically. This device measures 8mm x 2mm x 0.9mm, slightly larger than a grain of rice. It is implanted in the eyeball with a specific insertion tool. Once in the eye, it measures pressure and communicates that information on demand. The primary issue with this device is that it must not interfere with the patient's vision or result in harm to the eye. The primary issues in building this device result from the need to be physically small and compatible over the long run with the fluid in the eyeball.

Lab-on-a-chip instrument. A customer wanted to create a small, ruggedized optical system within a 5mm x 5mm x 5mm mechanical envelope (**Figure 2**). HI was needed to transform a system that traditionally consists of discrete optical elements carefully assembled within mechanical structures and characterized on the centimeter length scale into a device of the requisite size.

The resulting ultra-sensitive optical detection system was used to sense multiple targets from within a single sample volume. In this case, various targets were labelled with chemistries such that they would fluoresce—or light up—with specific colors corresponding to particular targets.

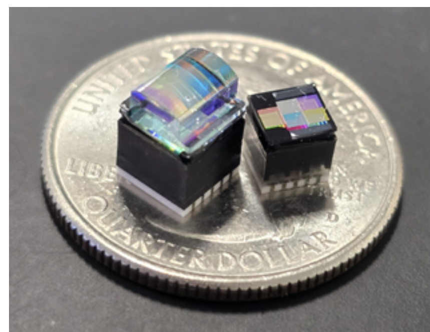

Figure 2: These complementary optoelectronic chips measure <5x5x5mm^3 and serve as the foundation of a multi-wavelength fluorescence detection system within a diagnostic medical device.

In this optoelectronic chip, optical elements were adjoined, using special materials, to mechanical structures created within the chip itself. Fabricating these chips was performed by employing traditional semiconductor packaging equipment in a different way, as is often the case with HI.

Major challenges to overcome in this optoelectronic chip included: 1) Selecting materials that offered appropriate mechanical stability and optical performance that were readily available and could be handled by automated equipment; 2) Incorporating tiny optical components into the assembly process flow—these components are easily scratched/damaged and are difficult to see with traditional vision systems; 3) Developing a three-dimensional assembly process where proper alignment and flatness is maintained throughout many assembly steps; and 4) Developing a workflow such that materials were not damaged by excessive temperature exposure.

Summary

The integration of sensors and MEMS devices into functional systems requires overcoming significant challenges in packaging, assembly, and power management. Advances in heterogeneous integration and semiconductor technology continue to push the boundaries of what is possible, enabling the development of smaller, more powerful, and more reliable sensors. MEMS devices offer unique micro-motion functions to sensors. The variety of motions and their uses are many and continue to be a challenge to designers and innovators.

As the demand for these sensing devices grows, particularly in specialized and high-demand applications, the importance of optimizing development costs and ensuring long-term performance will remain critical. The future of sensor technology lies in the continued collaboration between engineers, material scientists, and manufacturing experts to meet the evolving needs of various industries.

Biography

Richard F. Otte is CEO of Promex Industries, Inc., Santa Clara, CA. After starting his career as an electronics engineer, he joined Raychem, where he developed interconnect products. He then ran Advanced Packaging Systems, a joint venture with Corning. Otte joined manufacturing services provider Promex in 1995. He has BSEE and MSEE degrees from MIT and a Harvard MBA. Email dotte@promex-ind.com

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Early detection of C-RES degradation on high-current power planes

By Brent Bullock [Advantest America Inc.]

Probe-card or device contactor damage can be dramatic and catastrophic, with yield dropping drastically very quickly. What is not dramatic is the hypothesized slow probe needle or contactor degradation process that might precede catastrophic failure. Such degradation is difficult to detect in the early stages, when probe cards, die, and packages continue to yield normally. A key goal is to detect this degradation as soon as possible to avoid catastrophic damage without incurring yield loss or unnecessary equipment downtime. A related goal is to determine the root-cause scenarios that cause damage to probe needles or contactors.

Measuring contact resistance

One possibility for detecting the onset of probe or contactor degradation is to measure contact resistance (C-RES). This measurement can be accomplished by taking equipment offline, which also allows visual inspection of probe tips. This approach, however, thwarts the goal of minimizing downtime, and it provides limited insight into the root causes of failures—for example, it cannot determine what test sequences were running when a failure occurred.

Low-current C-RES measurements are valuable; given uniform planarity with clean probe needles, for example, uniform C-RES changes will correlate between I/O pins and large VDD power planes, regardless of pin type (**Figure 1a**). However, C-RES can be nonuniform because of particles, needle warpage, device contact defects, or other anomalies affecting a few pins. Unfortunately, low-current measurements cannot detect subtle changes in C-RES for a small percentage of pins isolated within large power planes, rendering nonuniform C-RES issues within large VDD planes unobservable on I/O pins (**Figure 1b**). This limitation can be overcome by improving measurement granularity, taking measurements at higher current levels, or combinations of the two.

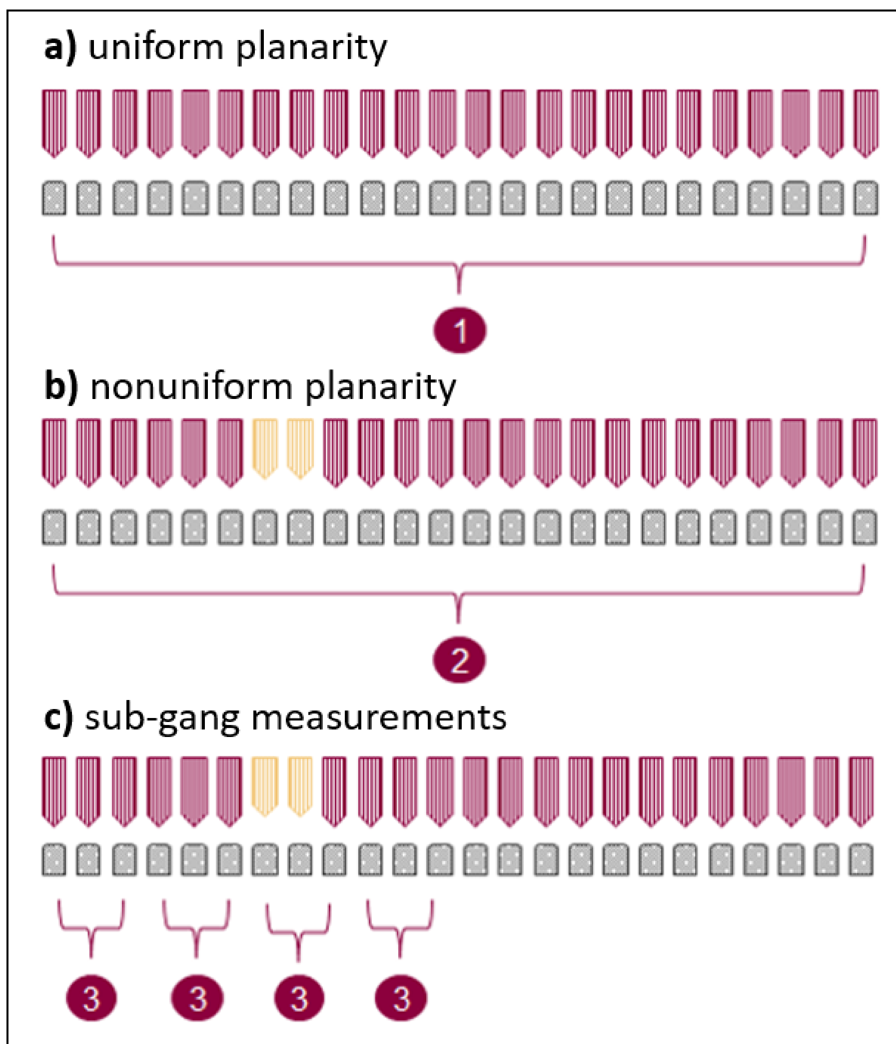

Figure 1: Probes can exhibit a) (top) uniform or b) (center) nonuniform planarity, and c) (bottom) sub-gang measurements can provide adequate resolution to detect anomalies in the latter.

Sub-gang measurements

One approach to improving C-RES measurements despite nonuniform contact problems is to take advantage of the fact that a VDD power plane is likely to be powered by multiple power supply channels. The multiple channels allow sub-gang per-channel measurements that can provide sufficient granularity to detect C-RES variances with adequate resolution (**Figure 1c**). For example, Advantest's EXA Scale generation of instruments for the V93000 platform include power supplies, digital comparators, and data converters (**Table 1**) that can discern C-RES variations between channels.

EXA Scale instruments can determine C-RES by measuring the voltage drop

Capability	Instruments	Accuracy, Resolution, Sample Rate (BW)
Primary vDrop Profile	XPS256 XHC32 UHC4T	±150µV, 10µV (12 bit), 200ksps (500kHz) ±150µV, 10µV (12 bit), 200ksps (500kHz) ±2mV, 200µV (12 bit), 200ksps (25kHz) – shared ADC
Extended vDrop Profile	XHC32	±150µV, 10µV (18 bit), 2Msps
High Speed Differential Sampler	UHC4T	2mV, 400µV, 10Msps – shared ADC
Digital Comparator	PS5000	±5mV, 1mV, 5GHz
Board ADC	PS5000	±500µV, 10uV (20 bit) 1Msps (130 kHz)

Table 1: Exascale instrument capabilities and specifications.

(vDrop) across the probe head for a given measurement current. vDrop can be measured and recorded at a specific point in time or averaged over multiple points in time. This approach may require additional test time, and similar to off-line measurements, it provides limited insight into the root causes of failures.

Monitoring vDrop

A better approach involves the monitoring of vDrop using continuous analog digital convertor (ADC) sampling and the triggering of an alarm when significant C-RES anomalies occur. This approach has the added advantage of pinpointing what test sequences were executing during significant C-RES changes, thereby facilitating root-cause analysis. **Figure 2** shows the XHC32 ultra-high-current power supply configured to provide such continuous monitoring of the C-RES values on both the VDD and VSS sides of the die. This approach requires an extended sense line, which must be added during the device under test (DUT) board design, in addition to the primary sense line.

Advantest's SmarTest automatic test equipment (ATE) software includes a feature that facilitates the programming of the extended monitoring and alarm functions in either interactive or application programming interface (API) modes. **Figure 3** shows results with per-channel ganging granularity, initiated by checking the perPogo box in the instrument view (**Figure 3a**). Data for each channel is shown (**Figure 3b**) with the highlighted channel showing a significant anomaly in measured current. To further control the ganging granularity, we offer a capability called Ganged on the Fly dynamic master-channel switching, which is useful for changing the master sense line when the IR drop across a power plane varies with test content. The capability supports unique signal names for desired master-channel scenarios.

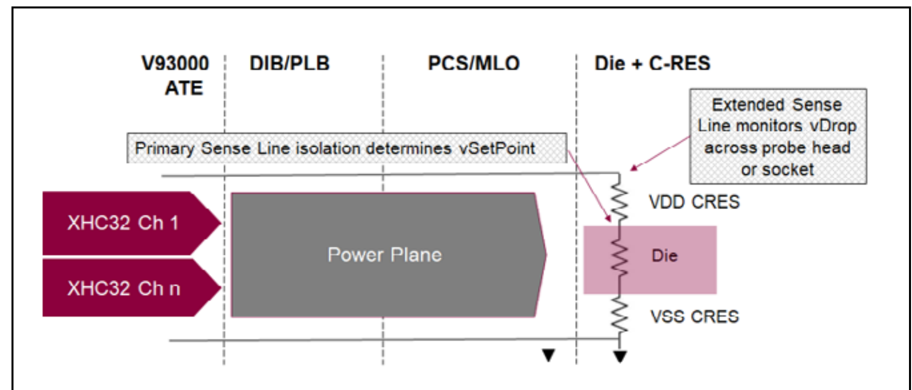

Figure 2: An XHC32 extended sense line monitors the delta value relative to the primary sense line.

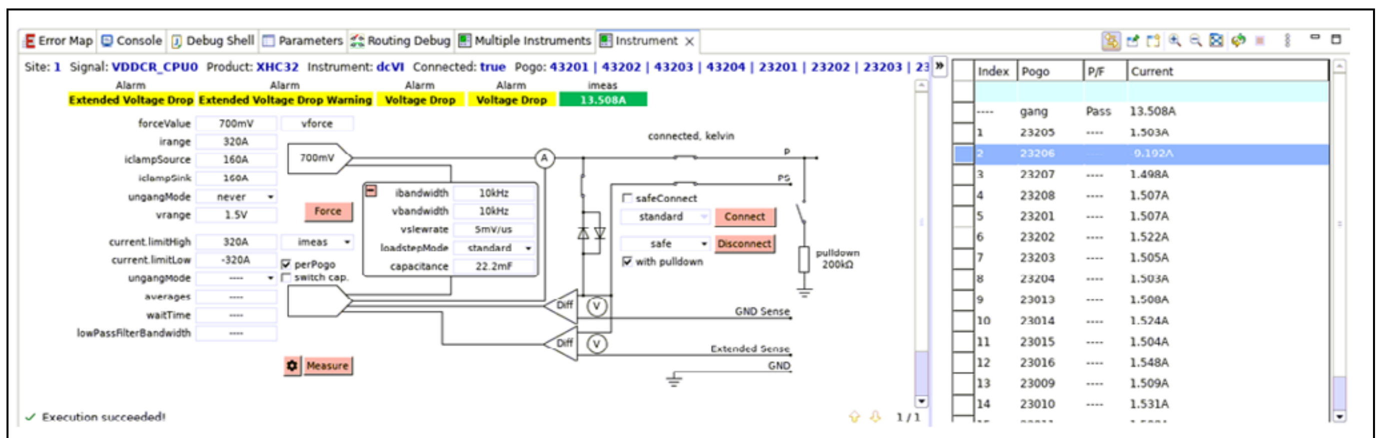

Figure 3: a) (left) Checking the perPogo box in the instrument view enables the b) (right) display of per-channel results.

Measurement results and comparisons

Figure 4 shows actual waveform results, with the extended vDrop profile shown in blue and the current shown in yellow. Extended vDrop scales with the current flow, with capacitor charge/discharge cycles inducing transient variations. **Figure 5** shows the extended vDrop and current values shown in **Figure 4** converted to power (brown) and C-RES (blue) values, with C-RES impacted by device contacts as well as the probes. The conversion is part of our new Contact Rating feature, which eliminates the issue of having to adjust for power, thereby reducing engineering workload.

Figure 6 shows vDrop measurement trial data for two equipment setups A and B, each of which have induced variations in the equipment and known variances in DUT contact quality. Measurements

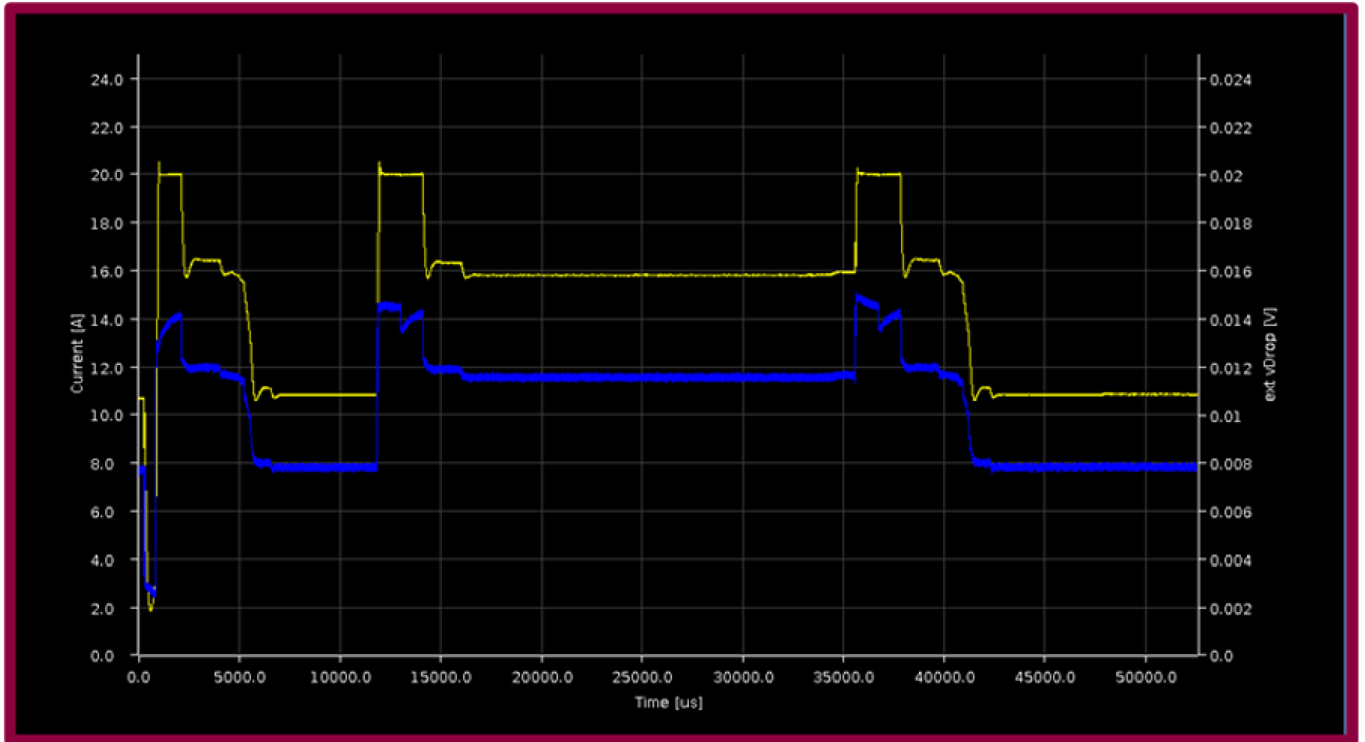

Figure 4: The extended vDrop value (blue) scales with current (yellow), with capacitor charge/discharge cycles inducing transients.

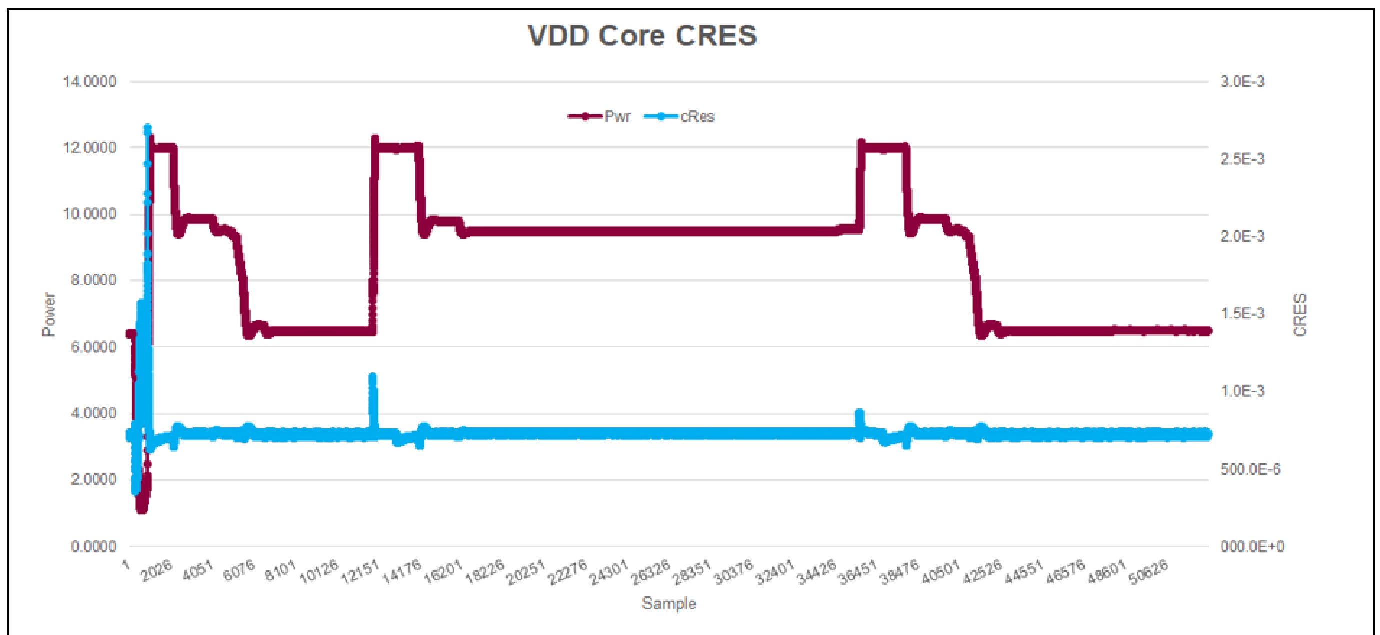

Figure 5: The brown and blue traces represent power and C-RES, respectively, derived from the voltage and current traces in **Figure 4**.

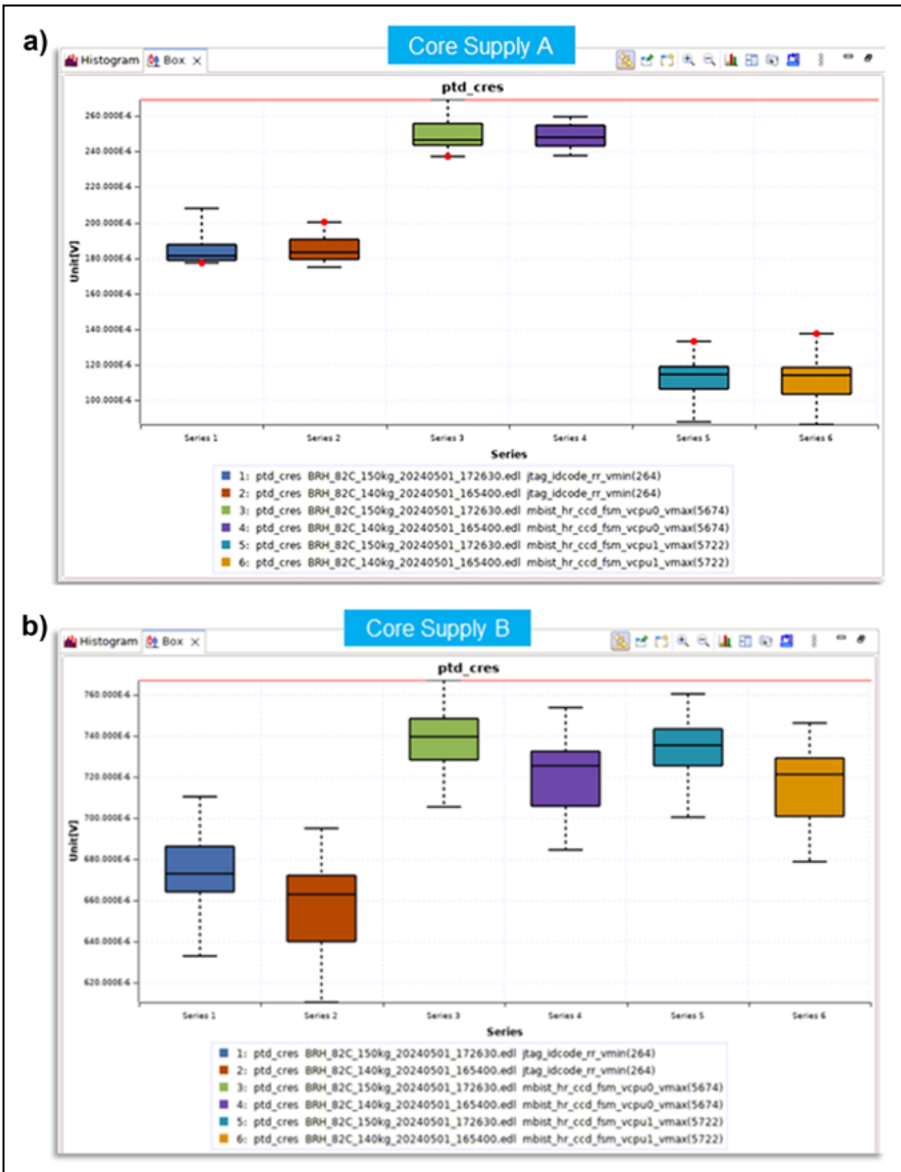

Figure 6: Measurements taken with the a) (top) lower power Core Supply A and the b) (bottom) higher power Core Supply B show that the higher power supply provides improved capability for distinguishing C-RES variations.

were taken for three separate tests, with each test performed four times, once for each of the two setups using the lower power Core Supply A, and once for each of the two setups using the higher power Core Supply B.

As shown in **Figure 6**, tests run on each setup using the low-power Core Supply A yield very similar results. For example, the measurements at the left of the Core Supply A (**Figure 6a**) results show that test 264 run on Equipment Setup A (Series 1) and the same test run on Equipment Setup B (Series 2) (**Figure 6b**) yield nearly identical measurements, making it difficult to draw inferences about C-RES variations. In contrast, the results for the same test run on the same two setups using the higher power Core Supply B are clearly distinguishable, demonstrating improved capability for vDrop measurements, and therefore, C-RES measurements, when utilizing currents that represent a higher percentage of total CCC.

Summary

Extended vDrop measurements can detect test cell variations but have limited potential for isolating root causes of probe failures. In contrast, extended vDrop monitoring with alarm functionality is effective at detecting C-RES degradation, and because the monitoring is continuous, it is also effective in determining the root causes of the degradation—for example, test program sequences that may inadvertently apply too much current.

The implementation of vDrop monitoring requires planning because C-RES measurement or monitoring is not possible without proper routing, and the required extended sense lines must be designed into the DUT board. For the best results, retain the primary sense lines in the same location used for previous designs and add the extended sense lines on the opposite side of the die or contactor. We offer the instruments and software necessary to implement extended vDrop monitoring and we are performing additional work to automate the process of setting adaptive current clamp and vDrop alarm limit values.

Biography

Brent Bullock is a Sr. Technical Consultant at Advantest America, Inc., Austin, Texas. He is a 40-year veteran of the ATE industry working for semiconductor, PC, and ATE manufacturers. His roles have included QA, failure analysis, component test engineering and ATE field applications for leading-edge high-performance digital semiconductors. He has ET & AASE degrees from DeVry Institute of Technology, Phoenix, AZ. Email brent.bullock@advantest.com

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The 5th SWTest Asia Conference and EXPO was a resounding success!

By Jerry Broz [General Chair, SWTest US and SWTest Asia Conferences, and Delphon Industries]

The Semiconductor Wafer Test (SWTest) Asia Conference and EXPO is the premier Asia technical event exclusively focused on the complex challenges of wafer-level test and probe technologies. Preparations for SWTest Asia 2024 in Japan began back in 2019 and were built on the success of the prior four conferences held in Taiwan. The 5th SWTest Asia convened for the first time in Fukuoka, Japan (October 24-25, 2024) and was a resounding sold-out success.

SWTest Asia 2024 was a two-day event that welcomed 768 attendees from 18 countries—75% of the attendees were from the Asia test communities—and brought together probe and test professionals to share knowledge, learn from colleagues, and informally network with other experts in a relaxed, friendly setting. The diverse two-day technical program included a Visionary Keynote, two Industry Vision Keynotes, 6 podium sessions with 22 outstanding peer-reviewed presentations, two poster sessions (**Figure 1**) that included 20 industry and academic posters, five Platinum Sponsor Tech Showcase sessions, and a sold-out EXPO for 60 global suppliers (including 10 local suppliers from the Fukuoka prefecture) (**Figure 2**).

At the standing-room-only Thursday morning plenary session, Prefecture Vice-Governor, Masaru Eguchi, joined Nobuhiro Kawamata, SWTest Japan Program Chair, and Dr. Jerry Broz, SWTest General Chair, to welcome attendees to Fukuoka and the conference. Afterwards, an insightful Visionary Keynote (**Figure 3**) was delivered by Professor Hiroto Yasuura, PhD, who serves as Vice Director General & Chief Cyber Science Infrastructure Director for the National Institute of Informatics. Dr. Yasuura made a thought-provoking

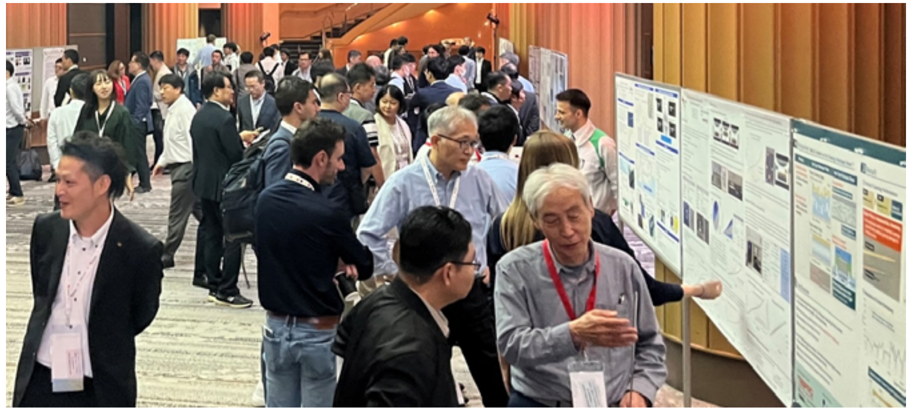

Figure 1: SWTest Asia 2024 Poster Sessions were a constant buzz of networking, socializing, and connecting among technologists, colleagues, and key suppliers.

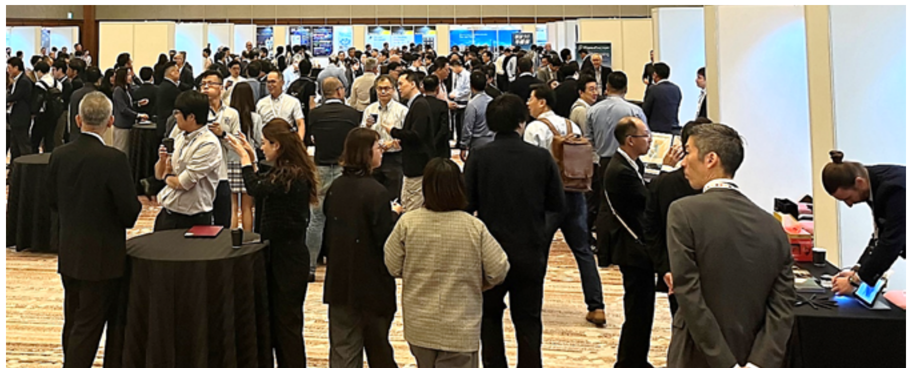

Figure 2: SWTest Asia 2024 Conference and EXPO.

Figure 3: On Thursday, Professor Hiroto Yasuura, PhD (Vice Director General & Chief Cyber Science Infrastructure Director for the National Institute of Informatics) discussed the critical needs of a re-energized Japan semiconductor industry. On Friday, Shinya Akata (Deputy Senior General Manager at SONY) and Tetsu Ozawa (General Manager at SOCIONEXT) focused their industry visions on testing processes for the next generation and challenges for advanced wafer process nodes.

Figure 4: During the opening Kagami-Wari Ceremony, Fukuoka Prefecture Governor, Seitaro Hattori, joined Nobuhiro Kawamata (Japan Program Chair) and Jerry Broz (SWTest General Chair), the SWTest Asia Executive Committee, Keynote Speakers, and a representative from each Platinum Sponsor. The meaning behind this time-honored traditional Japanese ceremony is that breaking the sake barrel lid releases prosperity and good fortune.

presentation that discussed the "Silicon Seabelt 2.0: Challenges of Kyushu for Reproduction of Silicon Island." He outlined and delved into the major challenges of infrastructure, resources, and manpower being faced by Kyushu Island with the technical and commercial resurgence of the semiconductor industry there, and in the rest of Asia. After the Visionary Keynote, the technical program consisted of sessions focused on Practical Solutions and Innovations for meeting Wafer-Level Test requirements.

On Thursday evening—to kick-off the SWTest Asia EXPO—Prefecture Governor, Seitaro Hattori, welcomed attendees and spoke about the excitement for semiconductor industry growth in the Fukuoka prefecture. After his opening comments, Governor Hattori joined the SWTest Asia Committee and Platinum Sponsors for a Kagami-Wari Opening Ceremony (**Figure 4**). Because SWTest Asia EXPO brings together international suppliers that play integral roles within the wafer probe industry and support infrastructure, Governor Hattori took extra time in the EXPO area to meet some of the international suppliers.

The Friday opening session was again fully attended, and two forward-looking Industry Vision Keynote presentations were delivered. The first was made by Shinya Akata (**Figure 3**), Deputy Senior General Manager at SONY, and the second by Tetsu Ozawa, General Manager at SOCIONEXT. Akata-san discussed the "Critical Role of Test for Image Sensor Development" and highlighted the essential, rigorous, and thorough testing processes that allow the next generation of optical devices to shine through their strengths and eliminate their weaknesses. In Ozawa-san's presentation, entitled "New Wafer Testing Challenges in Leading-Edge SoC Products," he detailed critical demands faced by the industry for advanced wafer

Figure 5: Andrew Yick (Marvell Technology) received the Best Overall Presentation Award from Nobuhiro Kawamata (SWTest Japan Program Chair) and Jerry Broz (SWTest General Chair) for his team's innovative work entitled, "From Lab to Line: Enabling Efficient PIC Testing for Mass Production."

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Figure 6: Two outstanding presentations received the Best Data Presentation Award, presented by Nobuhiro Kawamata (SWTest Japan Program Chair) and Jerry Broz (SWTest General Chair) to: 1) Yuki Hirose and Kosuke Yamanishi (Tokyo Electron, Ltd.-Japan); and 2) Vicky Tran (Gel-Pak-US) and Tomonao Nakashima (JEM-Japan).

Figure 7: Shen Jiayi (Tohoku University) received the Best Poster Presentation Award from Nobuhiro Kawamata (SWTest Japan Program Chair) and Jerry Broz (SWTest General Chair).

process nodes, enlargement of the devices, and the increasing high-current and high-speed requirements that increase the value added to chips and assemblies. After the Industry Vision Keynote, the technical program consisted of topics ranging from Improved Probing Efficiency to Known Good Die (KGD) Testing. The second day of the conference wrapped up with a terrific networking event for all attendees that featured a local Yatai (屋 台) Street Food Festival and traditional entertainment.

From all the excellent presentations delivered during the conference, the Technical Program Committee was pleased to award the Best Overall Presentation to Andrew Yick, PhD, Calvin Yang, Supreet Khanapet, Andy Chang (Marvell, USA) and Christian Karras and Tobias Gnausch (Jenoptik, Germany) for their innovative work entitled, "From Lab to Line: Enabling Efficient PIC Testing for Mass Production" (**Figure 5**). From the session focused on High-Speed KGD and Power Module Test, Yuki Hirose and Kosuke Yamanashi (Tokyo Electron Ltd., Japan) received one of the Best Data Presentation awards for their work on "Accomplishing True Known Good Die Verification Testing in Wafer Test," (**Figure 6**). The other Best Data Presentation award went to the collaborative work by Victoria Tran, PhD (Gel-Pak, USA) and Tomonao Nakashima (Japan Electronic Materials Corp., Japan), entitled, "Cleaning Innovations to Maximize OEE for High Volume Memory Test," which was presented during the session on Advancing Wafer Probing Efficiency (**Figure 6**). The Best Poster Presentation was awarded to Jiayi Shen and Tak Fukushima (Tohoku University - Japan) for their work on "3D-IC Fabrication with TSV at the Die Level from 2D-IC," (**Figure 7**). Each year, SWTest Conferences support the attendance of students through the generosity of key industry sponsors, as well as the William Mann Student Travel Grant Program. We are also proud to announce that *Chip Scale Review*, the SWTest Media Partner, has selected the Best Overall Presentation for publication as a full article in an upcoming issue.

The feedback from SWTest Asia 2024 has been overwhelmingly positive and, as the General Chair of this event, I am pleased that our conference and EXPO provide a variety of exciting technical and professional opportunities. Throughout the schedule, our attendees always have ample time and numerous opportunities for visiting with the key exhibitors, and networking during the long breaks, daily meals, and nightly social and hospitality events.

I would also like to take this opportunity to thank the sponsors, exhibitors, authors, speakers, session chairs, committee, and the SWTest Asia Team members whose deep commitment made this year a fantastic record-setting conference and EXPO (**Figure 8**). Finally, the SWTest Asia organizing team wants to thank Prefecture Governor, Seitaro Hattori, Vice-Governor, Masaru Eguchi, and the Fukuoka Prefecture Team for their participation and kind support during the planning process.

Looking ahead to 2025, mark your calendars for the upcoming 34th SWTest Conference and EXPO that will be held at the Omni La Costa in Carlsbad, California from June 2-4, 2025. Plan to attend this probe technology forum where attendees come to learn and network with colleagues about the recent developments and meet with key suppliers for the probe and wafer test industry. The Call for Papers is already open at https://www.swtest.org/ and will close on February 21, 2025. Whether you are an end user, supplier, engineer, sales and marketing professional, SWTest San Diego or SWTest Asia offer something unique for everyone in the wafer-level test industry.

Figure 8: SWTest Asia Committee Members and Platinum Sponsors were honored for their participation by the Fukuoka Prefecture Governor, Seitaro Hattori, during the Kagami-Wari Ceremony and the EXPO, as well as the support of the Fukuoka Prefecture Government throughout the planning process.

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