Heterogeneous chiplet integration to make megachips

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This paper describes a new, extremely large area integrated circuit (ELAIC) solution—we are calling a "megachip"—suitable for combining multiple chiplets of varying type (e.g., memory, application-specific integrated circuits [ASICs], central processing units [CPUs], graphics processing units [GPUs], power conditioning) into a single package on a common interconnect platform.

The megachip approach helps to rearchitect heterogeneous chip tiling for developing highly complex systems having desired circuit density and performance. Recent work on large-area superconducting integrated circuits to join multiple individual die is highlighted in this article, with particular attention paid to the processing of the high-density electrical interconnects formed between the individual die. A variety of megachip assemblies were fabricated and characterized using several techniques (i.e., scanning-electron microscopy (SEM), optical microscopy, confocal microscopy, X-ray) to investigate the integration quality, minimum feature size, silicon content, die-to-die spacing, and gap filling. Silicon dioxide, benzocyclobutene (BCB), epoxy, polyimide, and silicone-based dielectrics were used for gap fill, via formation and redistribution layers (RDLs).

For the megachip approach, the thermal stability is improved by reducing the die-to-die (D2D) gap and increasing the silicon content, allowing assemblers to mitigate the problem of mismatch in coefficient of thermal expansion (CTE) for different substrates/modules integration schemes, which is important for allowing the broad temperature range stability from reflow to operation at room or even cryogenic temperatures. Megachip technology facilitates more space-efficient designs and can accommodate most heterogeneous dies without compromising stability or introducing CTE mismatch or warpage. A variety of heterogeneous chips were used to fabricate megachip modules. The present process allows fabrication of megachip buildup layers having thicknesses in the range of 1-10µm, which allows packaging structures having both finer pitch and higher density. The processes and materials used to achieve smaller feature dimensions, satisfy stringent registration requirements, and achieve robust electrical interconnections are discussed.

Introduction

The increasing demand for digital computing, mobility, and connectivity is driving the microelectronics industry toward cost-driven, highly-integrated, miniaturized technology with increased performance and lower power consumption to bring next-generation devices into more and more applications [1-2]. Over the last decade, high-performance computing (HPC) has evolved to adapt smaller and more diverse technology nodes suitable for artificial intelligence (AI), machine learning, and embedded computing platforms—these applications consistently involve trade-offs between enabling more compute capability versus constraints in volume, weight, power, and thermal management.

Most of the power consumption for the above applications is due to moving data between chips in a system rather than the actual computing [3]. Furthermore, traditional Moore's Law scaling for developing next-generation devices faces various challenges including fabrication of larger chip sizes and associated yield improvement, development time, and cost scaling. This has forced the microelectronics industry to develop a number of alternative advanced packaging architectures and heterogeneous integration technologies [4]. A modern packaging architecture needs to integrate multiple processor and accelerator chips with minimum chip-to-chip spacing to minimize the interconnect length, on-chip memory, higher bandwidth connections, and management for greater heat densities, while being pushed into higher I/O counts, smaller pitches, and larger footprints [5-6]. This necessarily drives a requirement for improving the power efficiency of the chip-to-chip I/Os. In addition, new advanced packaging requires low-loss, mixed material, and versatile construction to accommodate the complexity associated with size, weight, and power (SWaP) optimization.

Conventionally, better wiring densities have been achieved by using filled dielectric to reduce via dimensions, lines, and spaces—thereby increasing the number of circuit layers—and utilizing microvias for interconnection. However, each of these methods has inherent limitations. For example, there are limitations related to laser drilling and electroplating of high aspect ratio blind- and through-vias, increased resistance of narrow (and) long circuit lines, and increased cost of fabrication related to additional wiring layers [7]. As a result, microelectronics packaging is moving toward alternative, innovative, low-cost approaches as solutions for miniaturization [8-10]. Fabrication, assembly, and heterogeneous integration are bridging the gap by enabling economic use of the third dimension (2.5D and 3D packaging). System-level integration is also emerging. These approaches include multi-die system-on-chip (SoC), system-in-package (SiP), stacked die, or package-stacking solutions.

In addition to the trend toward miniaturization, new materials and structures are required to keep pace with more demanding packaging performance requirements. Wafer-level packages (WLP), panel-level packages (PLP), silicon/organic interposers with redistribution

layers (RDLs), active interposers, and bridge die have become the preferred methods for lower-cost integration to meet the demands of higher functionality in ever-smaller packages, especially when coupled with the use of different technology node die [11-13]. The size of WLP increases with smaller technology nodes and causes more reliability and chip package mismatches. Today, various WLP technologies including WLPs with and without through-silicon vias (TSVs), WLPs with embedded-integrated passive devices, and use of low CTE, low-loss, high-glass transition temperature (Tg) material-based wafer-level substrates featuring fine traces and embedded/integrated passives, are used to reduce WLP chip package mismatch. Similarly, flip-chip integration with the bridge die embedded within the package substrate allows for shorter interconnect lengths for chip-to-chip communication. Active interposers with active-to-active bonding [14] are preferred for high-bandwidth, low-latency communication.

Although there are many packaging approaches available today for chiplet integration, the authors believe that there is room for further improvement. Tiling hundreds of known-good chips in proximity to one another and creating chip-like wiring and silicon content are highly desirable for creating next-generation chiplet-based computing architectures, but has yet to be demonstrated. Here, we present the implementation of such a chiplet-based tiling approach.

This paper discusses a heterogeneous chip tiling that enables the realization of extremely large-area integrated circuits (ELAICs)—or megachips—containing hundreds of closely spaced small chiplets that are interconnected using RDLs fabricated via a lithographic process. The ELAIC platform allows the tiling of known-good chiplets to make systems that perform as a single-chip monolithic device, despite being composed of many smaller heterogeneous chiplets. With this approach, one can fabricate a large-format single-chip-like SoC from advanced-node chiplets, screening for known-good die in order to increase the yield and performance of advanced-node technology beyond what is possible in a single-chip format.

A key focus of this paper is to address the scaling challenges faced when building large-scale processors. For example, the ELAIC solution is suitable for combining multiple types of chips (e.g., memory, ASICs, CPUs, GPUs, power conditioning) into a single system. This approach extends the number of chip tiles within a given space by enabling sufficiently high chip-to-chip connectivity to allow multiple chiplets to perform as a single-chip monolithic device. Connecting chiplets through our approach will enable a path to increase the format size of heterogeneous processors. The ELAIC structure, having 5-20µm chip-to-chip spacing, creates short (i.e., 50-500µm) electrical links for high-bandwidth, low-latency communication. An ELAIC has a chip-like silicon content (about 99%), allowing thermally-stable and inexpensive fabrication of a heterogeneous SoC with chip-like wiring densities. For HPC, power consumption comes primarily from moving data between chips in a system rather than from the on-chip computing operations. The ELAIC approach reduces data movement constraints by integrating multiple chiplets with minimum chip-to-chip spacing, thereby reducing the loading of these I/O paths by at least an order of magnitude. By integrating multiple chiplets into one large-area chip (2D array), the ELAIC approach can help solve many scalability challenges for high-end electronics.

The megachip approach

The following sections discuss the megachip (or ELAIC) approach with respect to tiling, physical characterization, and demonstration of the electrical interconnect.

ELAIC chip-tiling approach. The approach to ELAICs involves developing an integration process that can address the scaling challenges faced by many multi-chip systems. Integration of multiple chips that were produced using different (heterogeneous) fabrication technologies has been a persistent challenge. Typically, individually-packaged chips use a board-level assembly approach, and the associated "parasitic" electrical overhead and latency often become the limiting factors to a system's performance.

The ELAIC integration process will allow the tiling of known-good chips to make systems that perform as a single-chip monolithic device, despite being composed of several smaller heterogeneous chips. The primary goal of this effort is to develop a chip packaging interconnected with a RDL that is capable of integrating hundreds of chips in proximity to one another in a single system as shown in **Figure 1**. The RDL typically has multiple metal layers, each separated by a plasma-enhanced chemical vapor deposition

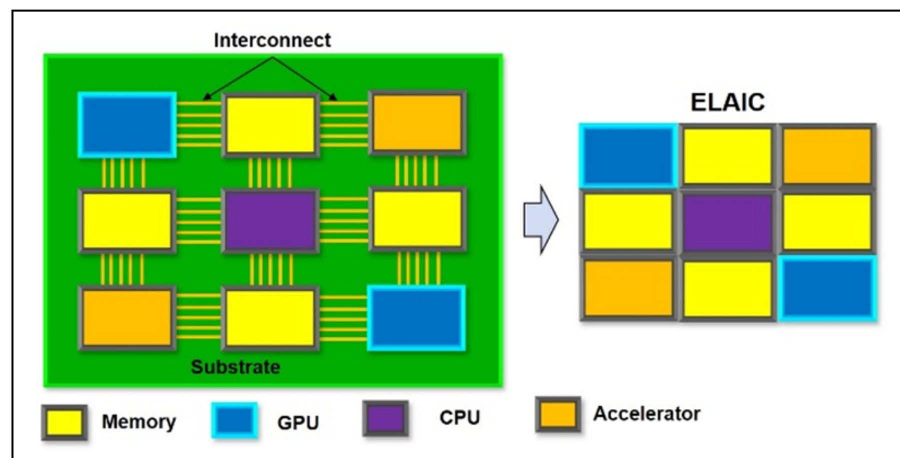

Figure 1: Extremely large-area integrated circuit (ELAIC), or megachip, concept: a) (left) Regular package where individual chips are attached to the substrate (organic or Si) and interconnected through the substrate; b) The megachip combines all the chips in a single plane where each individual chip will have at least two nearest neighbor chips for interconnection. The megachip enables chip-like wiring and eliminates the need for a substrate containing interconnects.

(PECVD) silicon dioxide layer, polyimide, or BCB dielectric, and uses micro-vias for interconnection. For our demonstration, the metal wiring layers were patterned using non-contact direct-write photolithography, which supports minimum wiring layer dimensions of 1µm and field sizes exceeding the largest relevant reticle size (50 x 50mm^2).

We evaluated various chip-like dielectric, wiring, and interconnection options. An ELAIC process flow is illustrated in **Figure 2**. The illustration displays the process flow for a double-layer RDL with a micro-bump layer on top of the RDL. The primary advantage of the ELAIC assembly is to produce a narrow (5-20µm) gap between the chips. This kind of gap is suitable for short (50 to 500µm) chip-to-chip interconnect lengths as shown in **Figure 2c**. Today, many high-performance electronic integrated circuits (e.g., field-programmable gate arrays [FPGAs]) use parallel interfaces for chip-to-chip communication. This approach requires small electrical length and more individual physical wires for data transmission. ELAIC enables narrow chip-to-chip spacing (10-20x smaller than the traditional approach) for smaller interconnect lengths and finer feature circuits, thereby enabling more physical wires for I/O connections with lower-latency, lower-power, higher-bandwidth chip-to-chip communication.

As a first step for chip tiling, we developed an assembly process for maintaining narrow gaps between the chips while maintaining top chip surface planarity in a larger scale ELAIC format. The top chip surface planarity enables thin dielectric deposition to make a finer pitch interconnection with chip-like RDL circuits. We assembled various ELAIC configurations using 5mm x 5mm to 20mm x 20mm chips in order to test chip surface planarity and chip-to-chip spacing/gap for the ELAIC structure. **Figure 3** shows various ELAIC

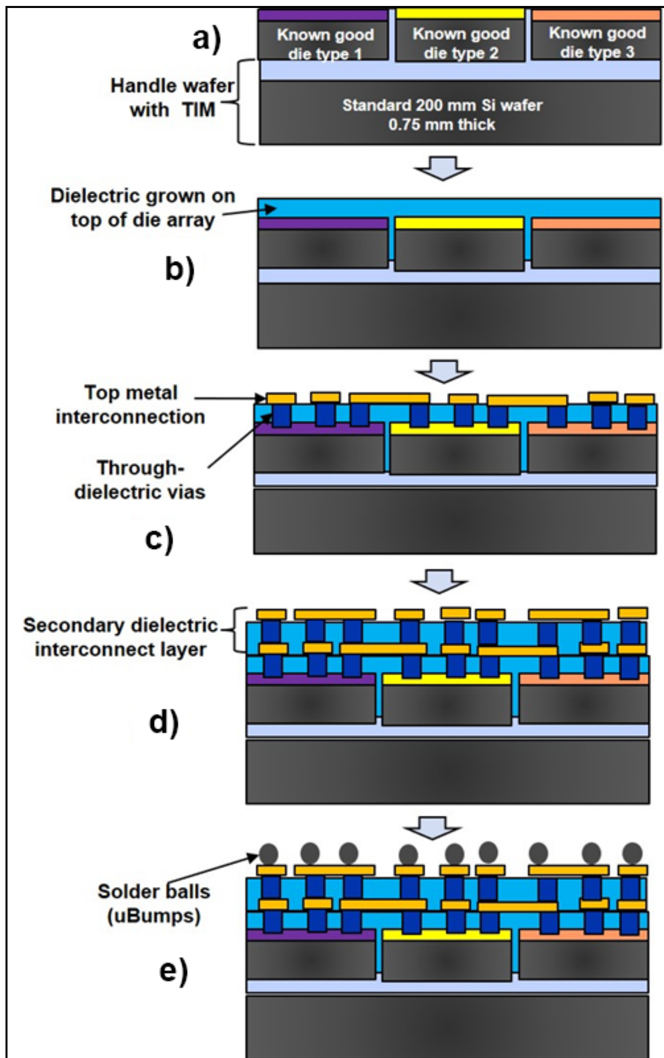

Figure 2: Process flow for an ELAIC construction. The chips are assembled on a handle wafer: a) Known-good die are placed face-to-face using a microscope. In general, the die use thermal interface materials (TIM) or related materials for die attachments; b) The dielectric layer is deposited; c) The first RDL is formed; vias are etched and top metal is deposited on the dielectric layer; d) The second RDL and additional dielectric layers for more complex interconnectivity are formed (target up to 4 RDLs); and e) Micro-bump fabrication—the bumps are deposited for flip-chip connection.

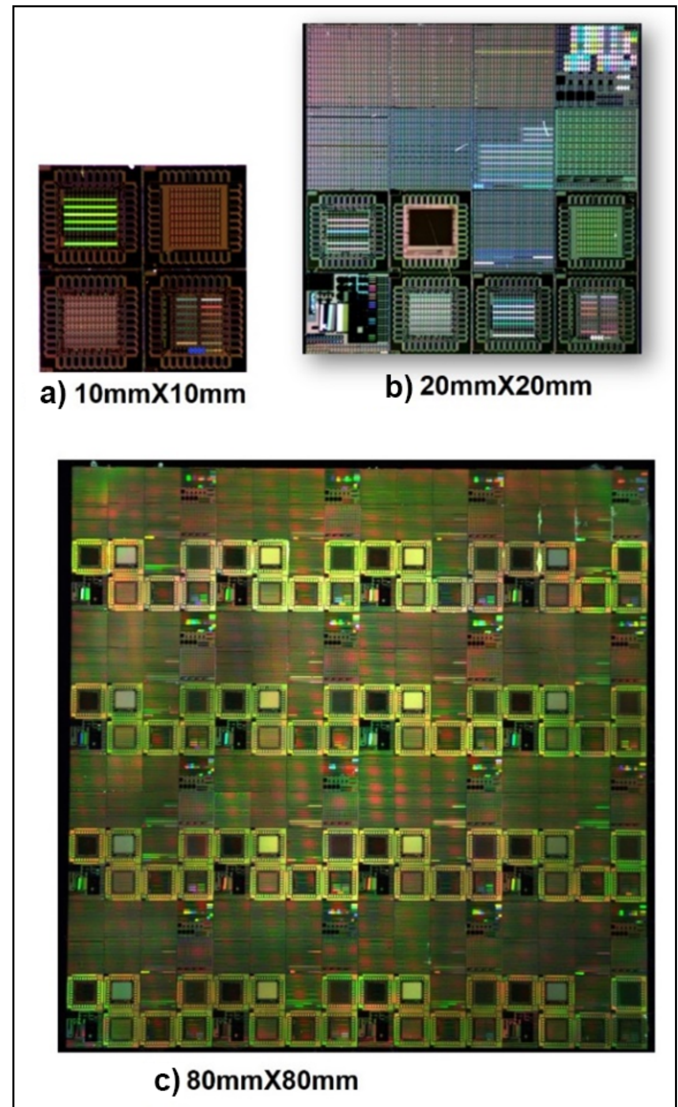

Figure 3: The ELAIC combines known-good die together to make systems that perform like an extremely large single chip. The scalability of the ELAIC fabrication process is shown—with assembly sizes ranging from 4 chips to 16 chips to 256 chips: a) Four 5mm x 5mm chip assembly; b) 16 5mm x 5mm chip assembly; and c) 256 5mm x 5mm chip assembly.

configurations using 5mm by 5mm chips ranging from 4 chips up to 256 chips as a representative example. The extremely large area (**Figure 3c**, 80mm by 80mm) circuits can be useful for advancing many systems, including those for HPC with diverse technology nodes for AI and deep learning, superconducting classical and quantum computing, large-format digital-pixel focal plane arrays [15-17] with minimum seam loss, photonic-chip tiling, millimeter-wave phased-array radar tiles, etc. The process involves the tiling of known-good chips to make systems that perform like a single-chip monolithic device, despite actually being composed of several smaller heterogeneous chips. Integration of multiple chips with different (heterogeneous) fabrication technologies has been a persistent challenge. The ELAIC (or megachip) platforms in many ways support chiplet-based system requirements by:

- Combining known-good chips together to make systems that perform like an extremely large single heterogeneous chip with very narrow inter-chip spacing for compact assembly. And for phased arrays, allowing the tightening of the lattice spacing (area is less) for better beam-steering.
- Providing aggressive interconnect pitch scaling for true process node interchangeability. And for RF, achieving lower interconnect parasitics that support more broadband connections.
- Enabling chip-like circuit content with good inter-chip planarity.
- Providing a built-in heatsink, thereby allowing for a better thermal solution for large chips.
- Supporting mixed-material construction with more Si/mm^3 (chip-like Si density), minimizing CTE mismatch, and supporting reliable operation ranging from room temperature to high (fabrication) and low (cryogenic) temperatures.
- Offering a path for introducing heterogeneous integration of non-silicon chips (not explored in this present work).
- Allowing active-to-active bonding (mix-and-match chiplets),

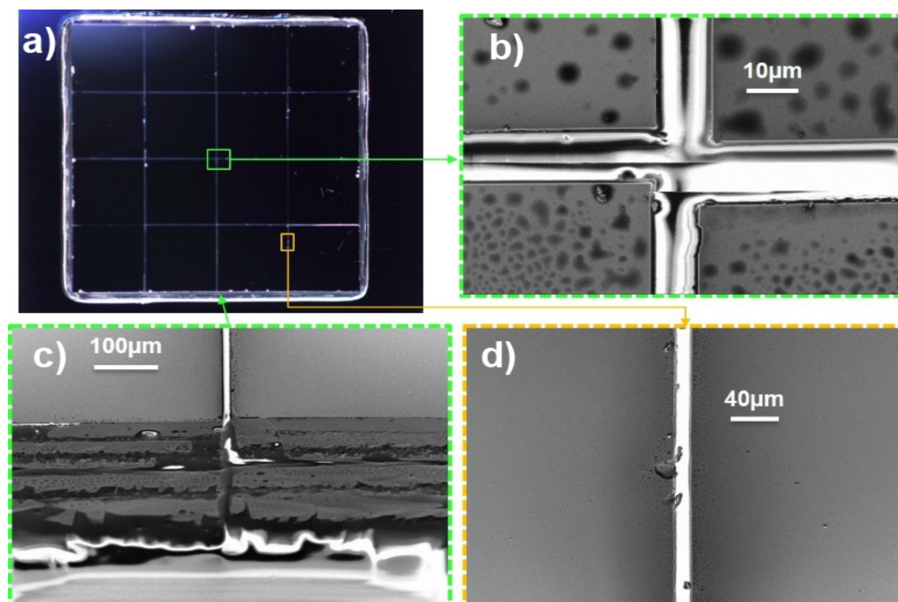

Figure 4: A 16-chip ELAIC assembly with very small 5-20µm chip-to-chip (C2C) spacing filled with dielectric. a) (top left): optical image of a 16-chip (each 5mm x 5mm) ELAIC assembly and b-d) (top right, bottom left, bottom right) corresponding enlarged SEM images that indicate a narrow C2C spacing filled (white area in SEM) with dielectric.

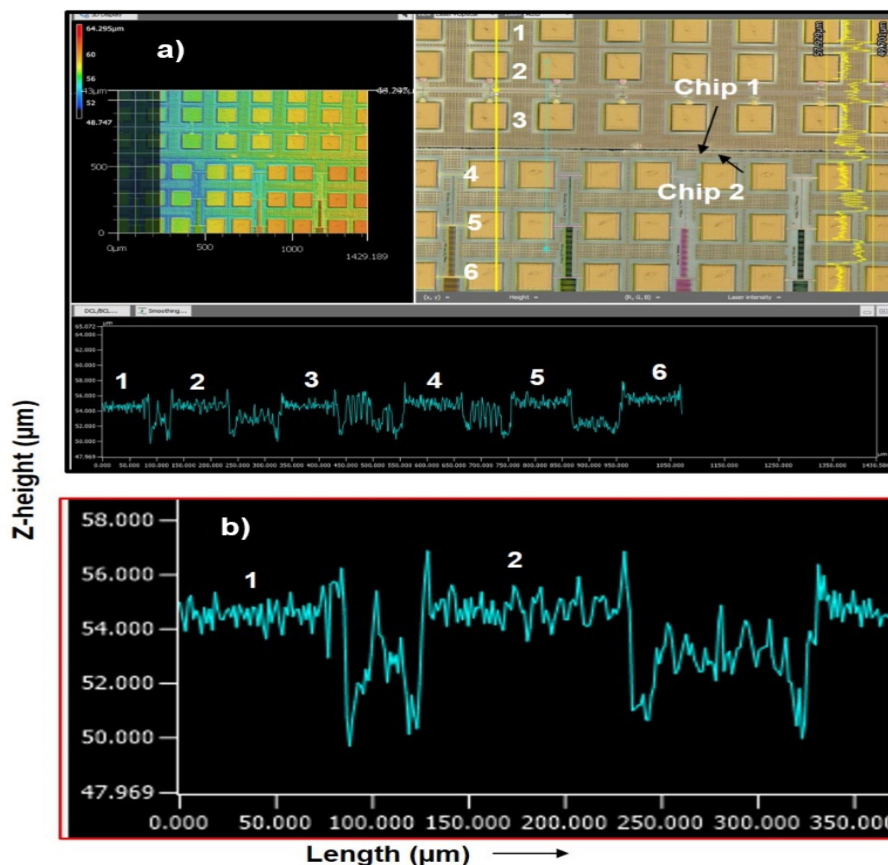

Figure 5: Selective-area confocal scan for a 4-chip ELAIC assembly. The figure shows confocal images and corresponding line scan between the chips to measure inter-chip planarity: a) Confocal micrograph and corresponding line scan. Confocal line scan from chip 1 metal pads (1,2,3) to chip 2 metal pads (4,5,6); and b) An enlarged confocal line scan; the confocal line scan shows metal pad height variation along the line as it scans from one edge to the other.

both side efficient metallic thermal interface materials (TIM), reduced die-die thermal resistance, and thermal cross-talk between neighboring die.
- Handling higher power density with a thermally-efficient Si floor plan.

ELAIC physical characterization. We used a variety of nondestructive analysis techniques for ELAIC physical device characterization. **Figures 4-5** show representative examples of ELAIC characterization. SEM, confocal scan, X-ray, and optical images are used to characterize key fabrication steps, which include chip-to-chip spacing, inter-chip planarity, dielectric deposition, via formation, feature size, and micro-bumping. **Figure 4** shows spacing between the stealth-diced chips in a 16-chip ELAIC assembly. The SEM data indicates that the ELAIC fabrication process maintains a narrow gap of 5-20µm between the chips and gap filling between the chips. Appropriate cleaning to remove dicing debris and give a smooth chip edge with minimal chipping is critical for minimizing chip-to-chip spacing.

Confocal microscopy was used to evaluate inter-chip planarity. **Figure 5** shows representative confocal images of a 4-chip ELAIC module measured using 100nm resolution in the z-axis. The confocal line scans show z-height variation along the line as it scans from one chip to the other. Metal pad height variation (pad 1-6) within and between the chip is negligible (less than 1µm). It is clear from confocal line scan data that the fabrication process maintains chip-like inter-chip planarity. We have developed a variety of ELAIC assembly approaches to optimize critical alignments between the chips. For example, the ELAIC devices used optical microscope for chip-to-chip alignment, and the post-process alignment accuracy was ±3µm. The gap fill and chip surface planarity allow us to select from a variety of dielectric material (PECVD oxide, benzocyclobutene [BCB], silicone, polyimide, etc.) to deposit on top of the ELAIC surface.

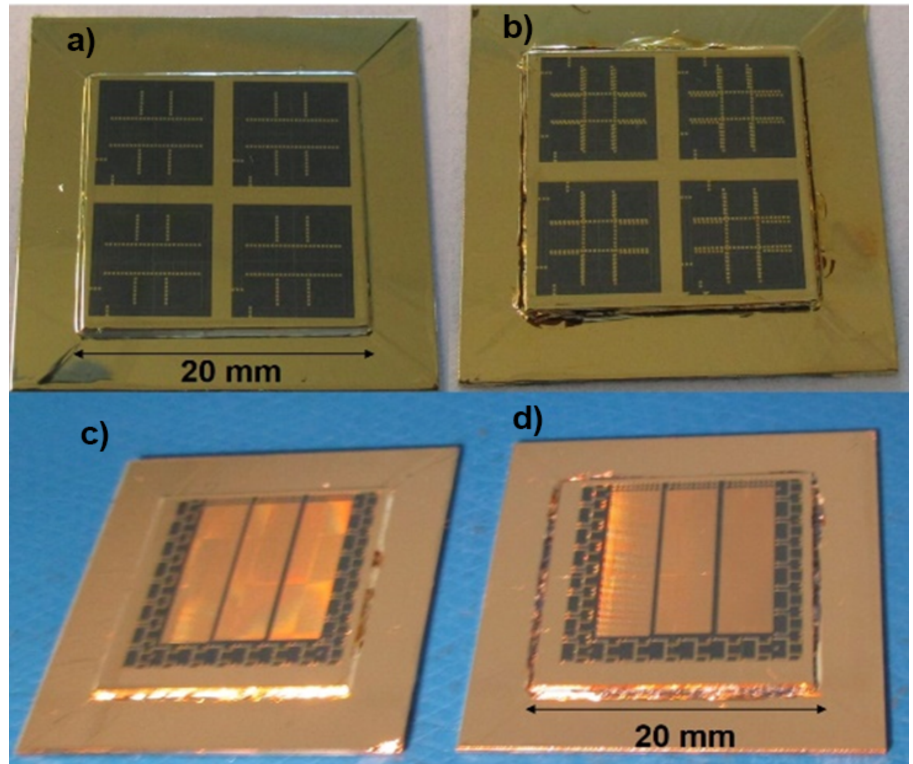

Figure 6: Passive circuit demonstration on top of a 16-chip ELAIC assembly: a) A single metal layer RDL; b) A double metal layer RDL deposited on BCB; c-d) A daisy chain circuit created on top of a 16-chip ELAIC assembly using multi-layer BCB dielectric.

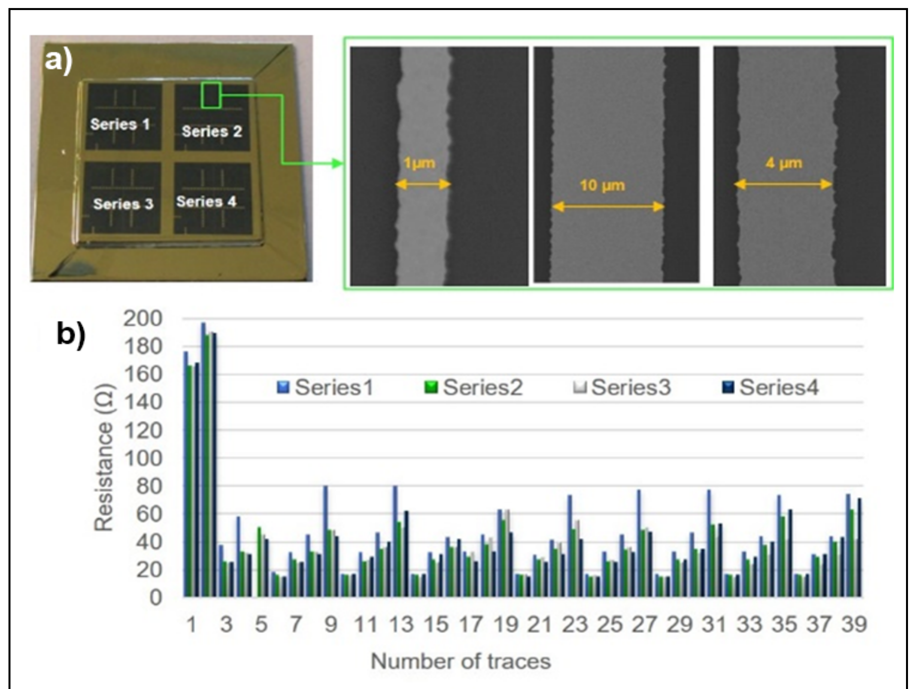

Figure 7: A passive interconnection circuit demonstration on top of a 16-chip assembly. The figure represents single-metal-layer passive circuits with four sections. Each 4-chip section has 1-10µm wide, 5-20mm long circuit traces going between the chips. a) Optical image of ELAIC and corresponding selective area SEM images of the circuit connecting the chips; b) Measured room temperature (RT) passive circuit resistance for four different sections. Resistance variation is due to the different widths and lengths of the electrical interconnect lines.

ELAIC electrical interconnect demonstration. As a next step for chip tiling, we selected PECVD oxide and BCB for RDLs. We have used single- and double-metal layers for implementing a passive electrical-interconnect demonstration. **Figure 6** shows a variety of passive interconnects deposited on a 16-chip (each 5mm x 5mm) ELAIC assembly. For example, it shows a variety of passive interconnects ranging from having 1-10µm wide and 5-20mm long circuit traces going between the chips. We also used a daisy chain circuit to access interconnections between metal layers. **Figure 7** shows a representative single-layer passive circuit example. **Figure 7a** shows an optical image and corresponding enlarged SEM images of a passive circuit lithographically-fabricated using BCB dielectric on a 16-chip ELAIC assembly. The SEM shows finer line circuits down to 1µm connecting multiple chips. These kind of fine-line circuits support chip-like wiring. **Figure 7b** shows room-temperature resistance of the passive circuits. It consists of four sections and each section has 1-10µm wide (trace width:1-10µm) and 5-20mm long traces going between the chips. Linewidth and linelength dictate the total resistance for individual passive circuits.

In addition to passive circuits, we also investigated interconnection between active superconducting chips containing tri-layer Josephson junctions (JJs) for larger system applications, such as quantum processors, readouts, control, and amplifier chips. Active chips can be connected together to create a multi-die SoC. These JJs and other active components may be on the same chip, or separate chips assembled into the ELAIC platform. In either case, a first step toward assessing the suitability of the ELAIC structure with Nb/Al-AlOx/Nb tri-layer junctions is to determine the impact of fabrication on the tri-layer junction performance. The addition of the RDL fabrication to the JJ chip may change the critical current, sub-gap voltage and other junction properties. In addition, multiple chip assembly, gap filling, and planarization may affect the stability and junction performance at 4K. To quantify the effects of fabrication on the tri-layer junction, we fabricated an ELAIC assembly where multiple superconducting chips with tri-layer junctions are attached to a single large ELAIC. This allowed us to determine the impact of ELAIC fabrication and to demonstrate basic desirable functionalities for multi-die SoC.

To assess the electrical performance of the chip assembly, multiple 4-chip ELAIC devices (**Figure 8**) were attached to a circuit card and wire bonded to measure I-V characteristics of tri-layer-based JJs at 4.2K. ELAIC-assembled superconducting chips had multiple sizes of junctions ranging in size from 700nm to 1000nm. Each measurement showed a typical

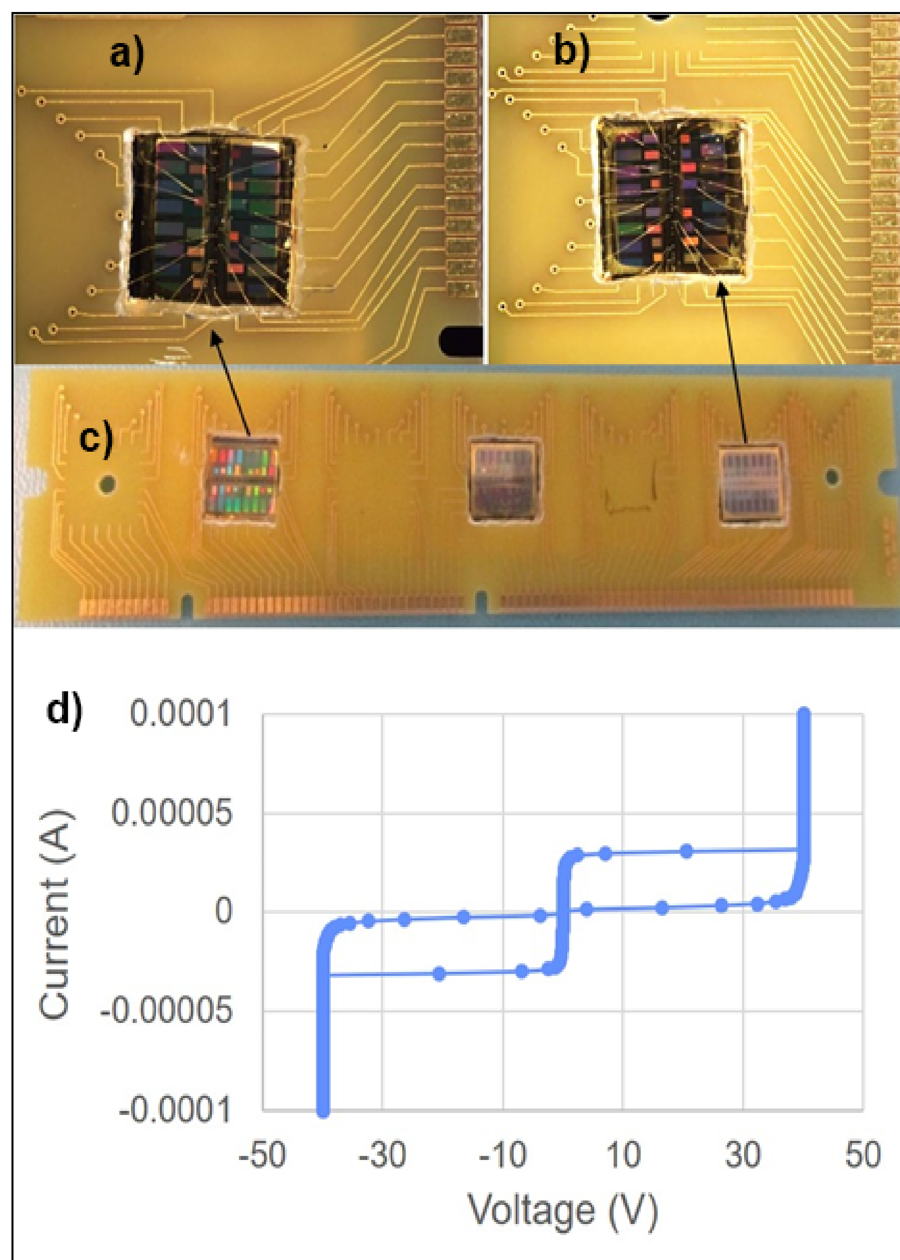

Figure 8: An active circuit demonstration. The figure shows three 10mm x 10mm ELAIC samples attached to a circuit card. Each ELAIC module consists of four active device chips containing superconducting junctions. These ELAIC devices used PECVD silicon dioxide as the dielectric and Ti-Au chip-to-chip interconnections. a-b) Optical image of 10mm x 10mm ELAIC attached to a circuit card for cold testing; c) Three 10mm x 10mm ELAIC samples attached to a circuit card for cold testing; d) The I-V characteristics of JJ series arrays connected between the chips through Nb and gold lines with a drawn JJ diameter of 0.7µm and 1µm.

I-V characteristic of Nb/Al-AlOx/Nb unshunted tunnel junctions (i.e., with respect to the Josephson critical current, sub-gap voltage, normal resistance at 4.2K). A variety of active superconducting chips with tri-layer junctions have been assembled to implement the ELAIC. The I–V characteristics and switching current of various tri-layer flip-chip JJ arrays were measured. We measured many ELAIC JJ arrays ranging from 40 to 20,000 JJs in series, with JJ drawn diameters ranging between 1.0µm and 0.7µm. I-V characteristics were measured for ELAIC JJ arrays connected across multiple chips through the RDL. **Figure 8d** shows a representative example of the typical I-V curve obtained from these multi-chip JJ series arrays connected through Nb and gold lines between the chips. This confirms connectivity between the chips through RDL and the preservation of JJ characteristics after RDL fabrication.

Single chip vs. the megachip concept

Figure 9 compares the ELAIC assembly with an equivalent single chip fabricated using a standard integrated circuits process. A 20mm x 20mm unsingulated chip was diced into 16 5mm x 5mm chips and reassembled to create a 20mm x 20mm ELAIC. We used X-ray imaging to inspect the single chip before dicing as well as the subsequent ELAIC. The X-ray image of the single chip and ELAIC looks similar. Dicing of the single chip removes Si from the dicing lane causing a smaller metal-to-metal gap between the chips as shown in **Figure 9d**. Overall, the ELAIC fabrication process produces a highly compact (>99% Si content) chip assembly with 5-20µm spacing between the chips, and maintains inter-chip planarity that is required for the finer line and smaller interconnect length needed to form parallel interfaces with wide I/O, high-bandwidth, and low latency for chip-to-chip communication. **Table 1** compares the single-chip SoC option with ELAIC multi-die SoC.

ELAIC can be used for flip-chip bonding to simplify fabrication and enhance connectivity and functionality in 3D for various applications. Flip-chip ELAIC (see **Figures 10-11**) offers a number of advantages over conventional

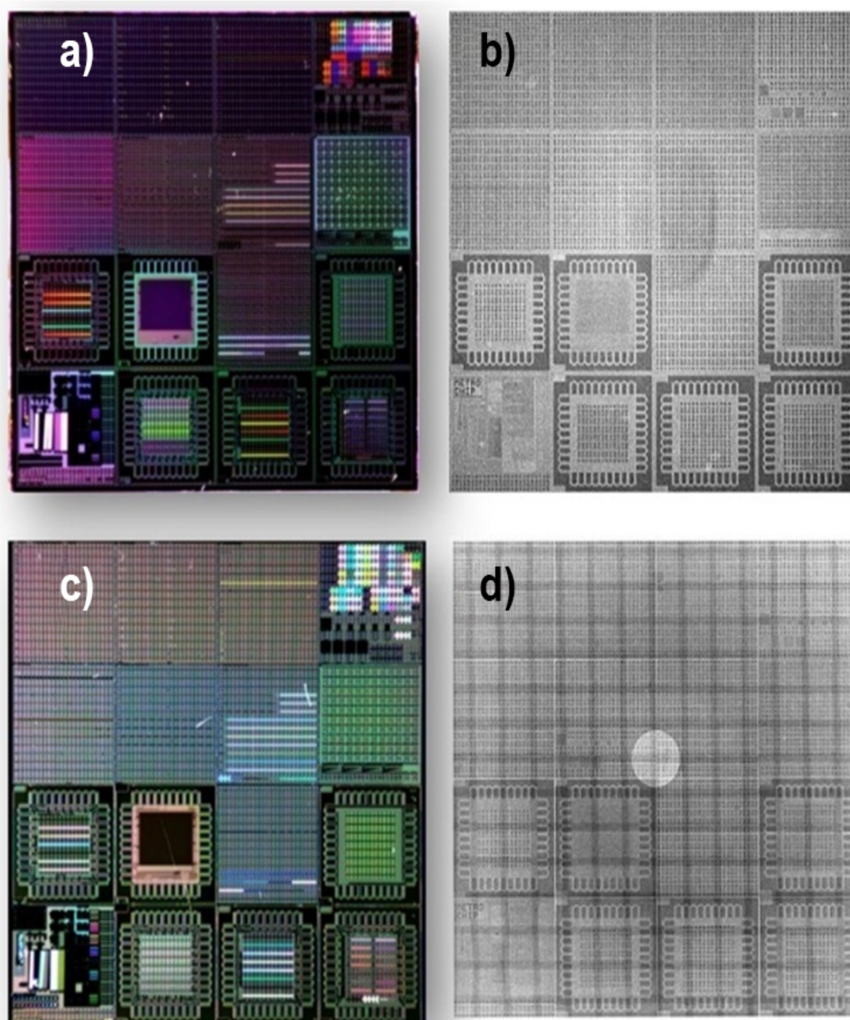

Figure 9: A single-chip vs. an ELAIC assembly: a) Optical image of a 20mm x 20mm unsingulated chip; and b) corresponding X-ray image of that unsingulated chip. This 20mm x 20mm single chip was subsequently diced into 16 5mm x 5mm chiplets. c) Optical image of a 20mm x 20mm ELAIC formed by recombining the 16 5mm x 5mm chiplets into single chip-like structures; and d) corresponding X-ray image of the ELAIC in c).

System	Single Chip/SoC	ELAIC
Si content	All (100%) Si	>99% Si
Interconnection	Through the wafer process	Through RDL
System-on-chip	Monolithic SoC	Multi-die SoC
Technology node	Single-node homogeneous system	Multi-node heterogeneous system

Table 1: A megachip vs. a single chip.

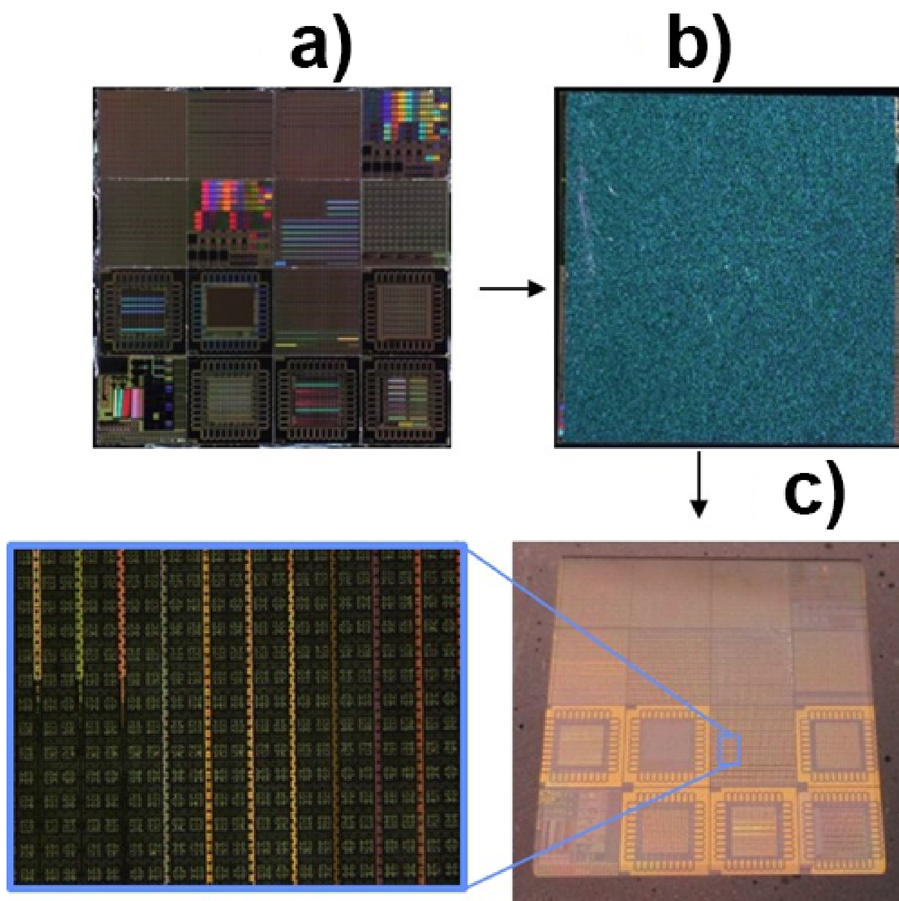

Figure 10: A flip-chip ELAIC: a) A 20mm x 20mm 16-chip ELAIC; b) An ELAIC flip-chip bonded to Si-die and underfilled to make a flip-chip ELAIC; and c) Si etched from flip-chip die and stopped at the oxide surface of the flip-chip die—this view shows a Si-less flip-chip ELAIC and the corresponding enlarged image looking through the oxide surface.

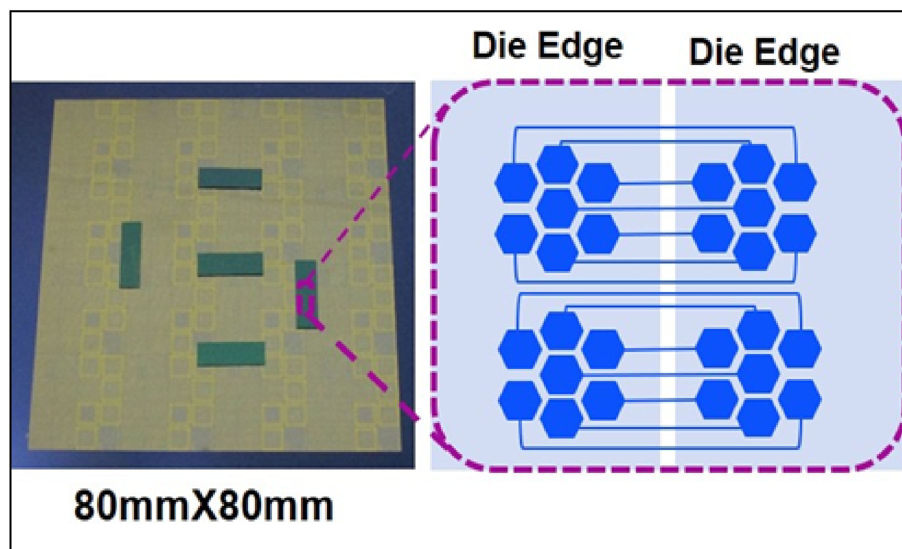

Figure 11: An 80mm x 80mm ELAIC (or megachip). It has sixteen 20mm x 20mm chips assembled to create the 80mm x 80mm megachip. The figure also shows a flip-chip bonded megachip and the corresponding enlarged schematic to show a chip-to-chip connection option through the flip-chip die. The next step is to remove Si from the flip-chip die (similar to **Figure 10c**) and stop at the oxide layer. Adding a Si-less interconnect layer adds 2-6µm thickness—necessary for creating the finer pitch megachip assembly.

monolithic SoC approaches:

- Provides various low-cost multi-chip read-out IC (ROIC) assembly for silicon avalanche photodiodes (Si-APDs) and other imagers [15-17].
- Introduces flip-chip Si-less active/passive bridge for chip-to-chip connection.
- Enables a thermally-optimized Si floorplan.
- Provides a cost benefit for yield and node optimization.

Summary

An integrated approach to develop ELAICs, or "megachips," using various heterogeneous die configurations has been demonstrated. This approach is suitable for high-end, expensive electronics where an SoC can be divided into chiplets with desired functionality and an ELAIC multi-die SoC can be created. The ELAIC can incorporate chips/chiplets from different foundry processes, and different technology nodes to improve mix and match capability, which further improves package performance. It also provides scalability to place a large number of chips onto the ELAIC platform, and enables a design that packages many different functionalities together, making it a viable approach to build larger systems.

The ELAIC solution is suitable for making the right choices in terms of cost and partitioning–for each of the targeted applications, and to provide a heterogeneous path for large-scale fabrication. The ELAIC integration supports the capability to integrate hundreds of chips (also known as chiplets) in proximity to one another in a single system. This integration technology enables small (50-100µm) interconnects required for parallel interfaces for chip-to-chip communications. The extremely large area integrated circuit allows for connections between bare chips, and the wiring between chips to be as small as the wiring within a chip. The approach increases the circuit complexity that can be integrated within a given space by enabling sufficiently high chip-to-chip connectivity to allow multi-chip systems to perform as a single-chip monolithic device.

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