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Volume 28, Number 2

March • April 2024

High precision wafer thinning using ultra-low TTV glass carrier and temporary bonding

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- A package solution for an optical engine in silicon photonics
- 3D integration of photonic and electronic chips on a glass substrate
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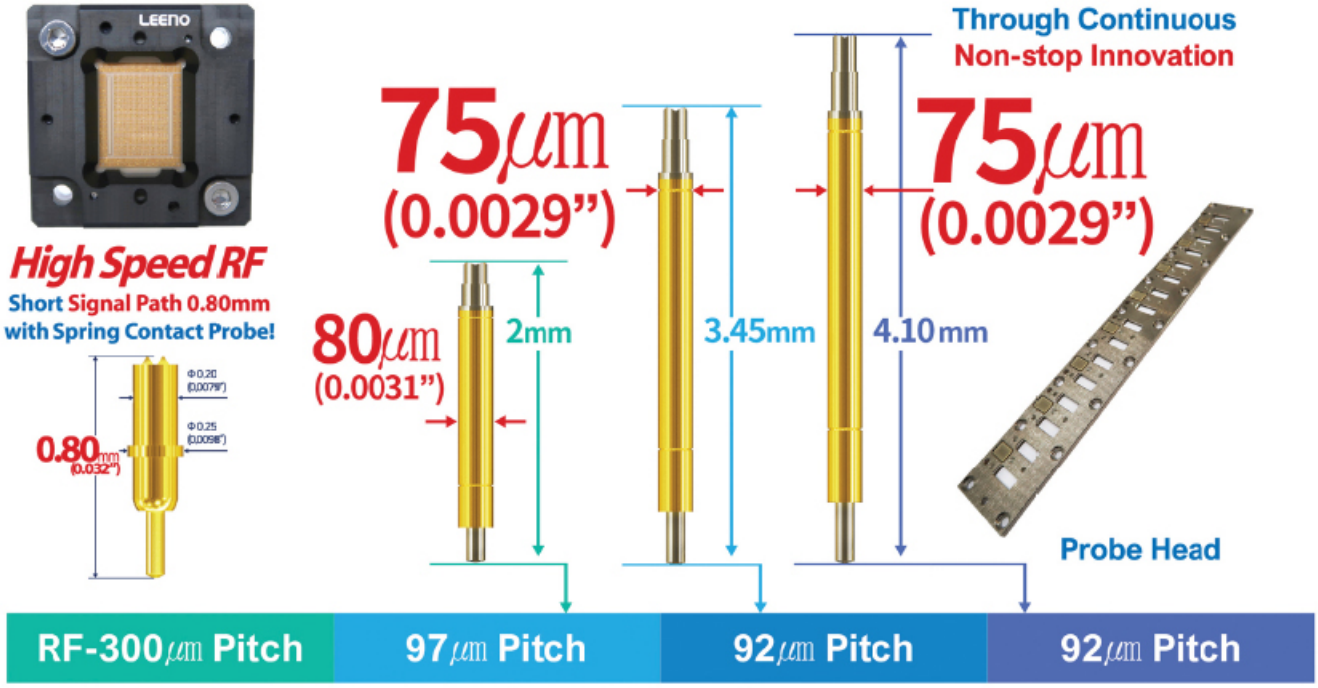

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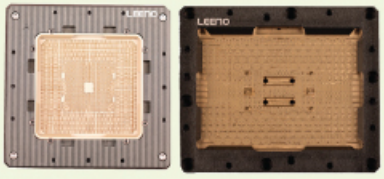

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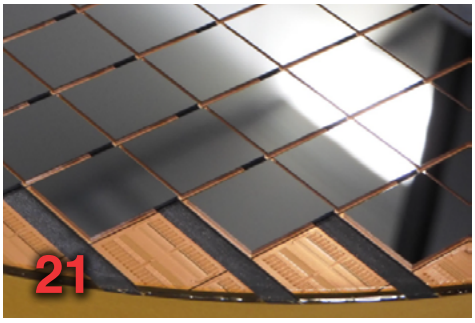

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Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry.
Chip Scale Review is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December.

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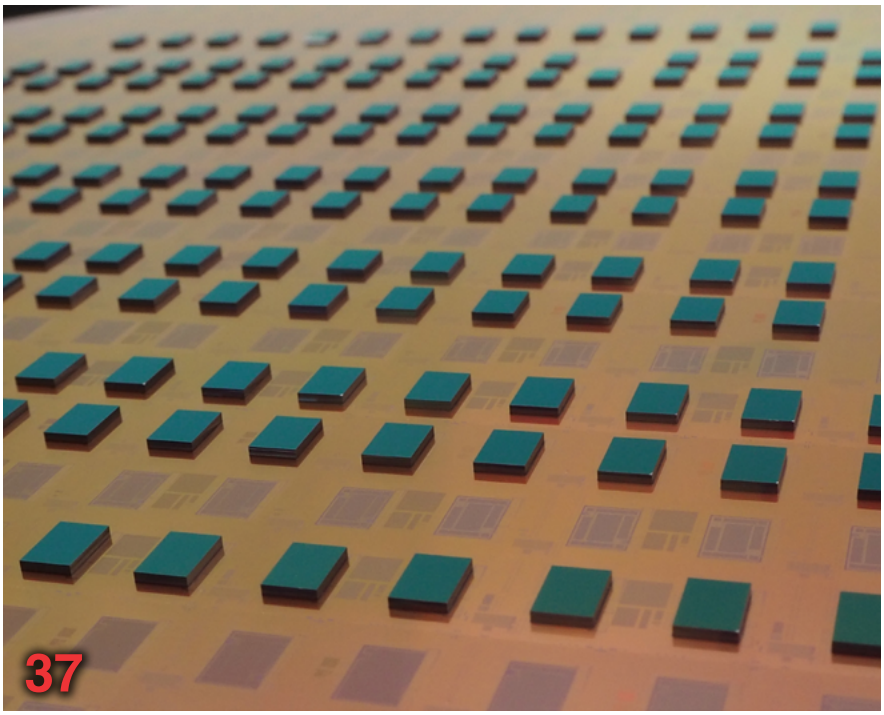
Printed in the United States



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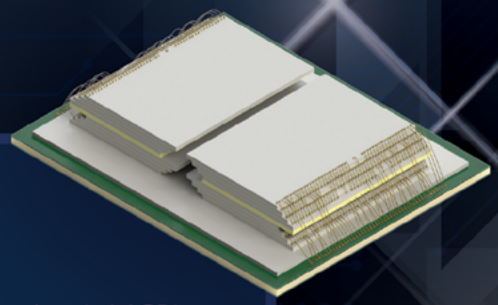

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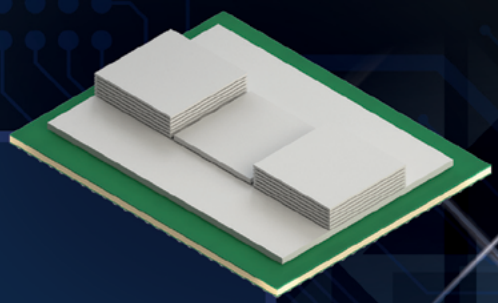

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High-precision wafer thinning using ultra-low-TTV glass carrier and temporary bonding

By Jay Zhang [Corning Incorporated]

Wafer thinning is a critical part of device making and advanced packaging in semiconductor manufacturing. Carrier-supported wafer thinning becomes attractive when the final wafer thickness becomes very thin, say <100µm, due to handling difficulties. Post-thinning processing (deposition, chemical mechanical polishing [CMP], bonding, etc.) also benefits from having a rigid and thermomechanically stable support structure. In order to achieve very low total thickness variation (TTV) of the final wafer, both the carrier wafer and the temporary bonding material—typically an adhesive layer—must deliver sufficiently low TTV. The carrier wafer also must have a suitable coefficient of thermal expansion (CTE). In this paper, we describe a glass carrier solution and a temporary bonding method that combine to enable low TTV wafer thinning. Feasibility demonstration is done using a 150mm diameter single crystal lithium tantalate wafer, and thinning reaches 5µm with wafer grinding alone.

Introduction

Glass wafers are being adopted by more and more companies in advanced packaging as a carrier. Attractive attributes of glass include: tailorable CTE, ability to deliver high-precision features such as excellent flatness and very low TTV, stability over a wide range of processing temperatures, chemical durability, and compatibility with mechanical, thermal or light-based debonding methods. Glass is also highly manufacturable, delivering cost efficiency.

In a typical use scenario, the glass carrier wafer is bonded to the wafer to be thinned using a temporary adhesive layer that is designed to be releasable after processing. Both the adhesive layer and the carrier wafer have thickness variations that will limit the uniformity of the thinned wafer. This is illustrated in **Figure 1**. We use stack TTV to describe the combined TTV of the carrier wafer and the adhesive. For emerging applications that either demand <10µm final wafer thickness, or wafer thickness tolerances <1µm, total thickness variation of the support structure, namely the stack TTV, must be <1µm, ideally <<1µm. This requires innovation in both carrier wafer manufacturing as well as in the temporary bonding method.

Ultra-low-TTV (ULTTV) glass carrier wafers

Glass wafers are typically made using one of two methods. Wafer blanks can either be extracted out of a flat glass sheet, or sliced out of a glass block using what is called a ganged wiresaw. While high-precision sheet forming technology, such as our fusion method, can deliver excellent flatness and TTV without additional polishing, it is not capable of delivering a TTV smaller than 1µm with reasonable yields, let alone a fraction of 1µm. This challenge is tougher the larger the wafer size. Sliced wafer blanks have a rough surface that must go through lapping and polishing to be usable as a carrier wafer.

Although double-sided polishing techniques have existed for decades, achieving TTV<1µm on a 300mm diameter wafer takes fundamental understanding of the entire finishing process and optimization of the equipment as well as the consumables. Recent work at Corning has produced 200mm and 300mm glass wafers with TTVs as low as 0.2µm. **Figure 2** shows TTV performance of a 300mm glass wafer. As of May 2022, ultra-low-TTV (ULTTV) wafers are commercially available: 200mm or smaller wafers promise TTV<0.2µm; 300mm wafers promise TTV<0.4µm.

Critical glass wafer attributes for carrier applications

Wafer shape distortion during bonding and post-bonding processing can be understood from thermomechanical modeling. We introduced a simplified formula for cases where the carrier wafer supports another much thinner wafer to relate magnitude of shape distortion to carrier properties [1]:

$$\approx 0.75L^2\Delta\alpha\,\Delta T\,\frac{E_s\left(1-\nu_g\right)t_s}{E_g\left(1-\nu_s\right)t_g^2}$$

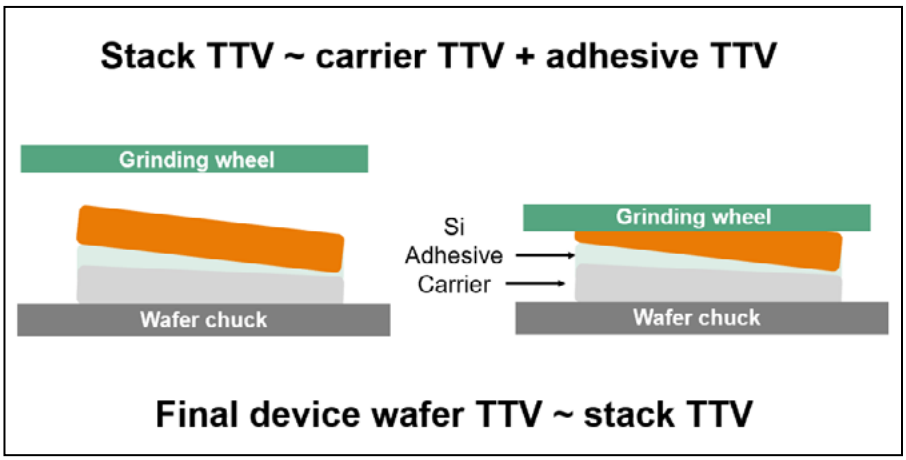

Figure 1: Both carrier TTV and adhesive TTV impact thinned wafer TTV.

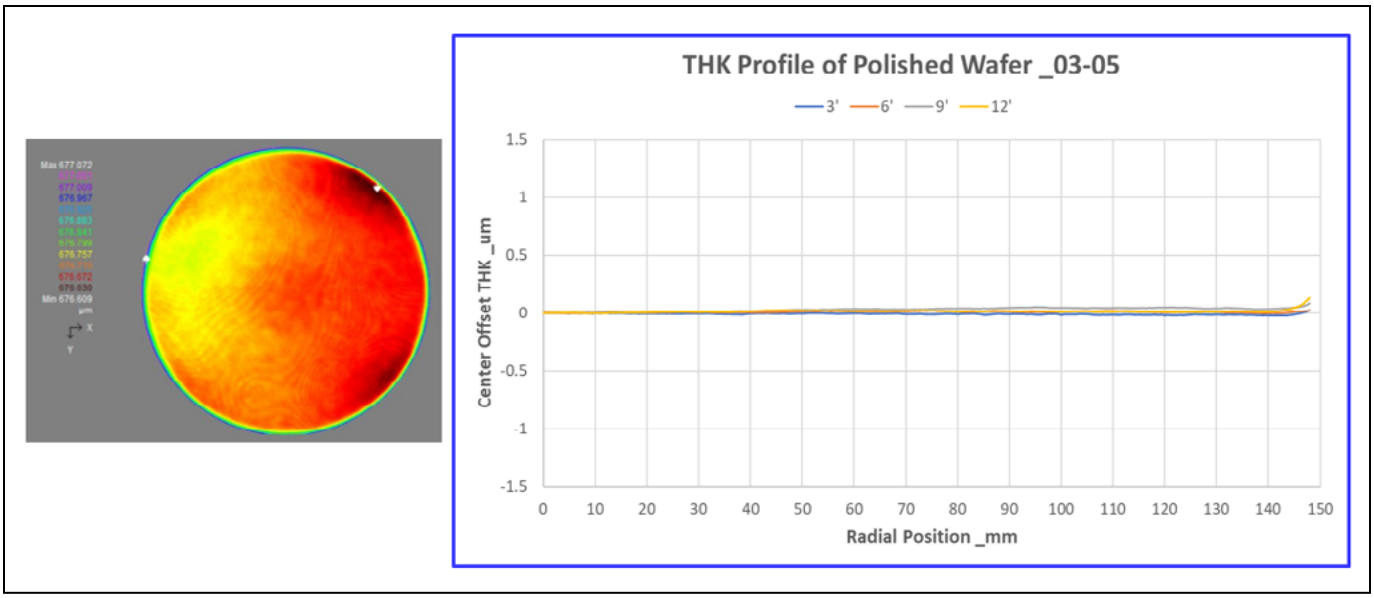

Figure 2: Wafers that have gone through high-precision polishing could achieve a TTV well below 1µm. This example shows a 300mm diameter wafer with thickness variations on the order of 0.2µm in the 3, 6, 9 and 12 o'clock directions, respectively.

Here, we use subscript "s" to designate the material properties of the semiconductor wafer on the carrier: E_s for Young's modulus, t_s for the wafer thickness, υ_s for Poisson's ratio, and α_s for the thermal expansion coefficient. For the carrier glass, we use subscript "g" for the same parameters accordingly. L is the size of the carrier.

From this simplified relationship, one clearly sees that for the bonded wafer pair, CTE matching between the semiconductor wafer and the carrier is the most direct and impactful factor in minimizing distortion. In Si wafer thinning applications, a typical device wafer often has metallization and dielectric materials in the wafer makeup. In the case of through-silicon vias (TSVs), Cu-filled vias may occupy a significant volume fraction of the entire wafer, making the effective CTE higher than that of pure Si. If the device wafer is made of a non-Si material, such as GaAs or sapphire or SiC, the carrier wafer also needs to deliver a matching CTE to these materials, respectively. In the same formula, one also realizes two other high-impact parameters: the shape distortion is inversely proportional to the glass's Young's modulus; it is also inversely proportional to the square of the carrier wafer thickness.

As a result of understanding the relationships noted above, we now offer glass wafers that cover a wide range of CTEs with fine granularity. **Figure 3** shows availability between CTE values ranging from 3-12.5ppm/°C. For products in the red box, the carrier glass wafers also deliver a high Young's modulus and flexibility in wafer thickness. Wafers can be made all the way to 5mm in thickness. The light blue diamonds indicate products that typically do not exceed 1mm in thickness with a somewhat lower Young's modulus. Because mechanical polishing techniques that produce the ultra-low-TTV characteristics are independent of the glass's thermomechanical properties, all the available glass types in **Figure 3** can be manufactured to have ultra-low-TTV.

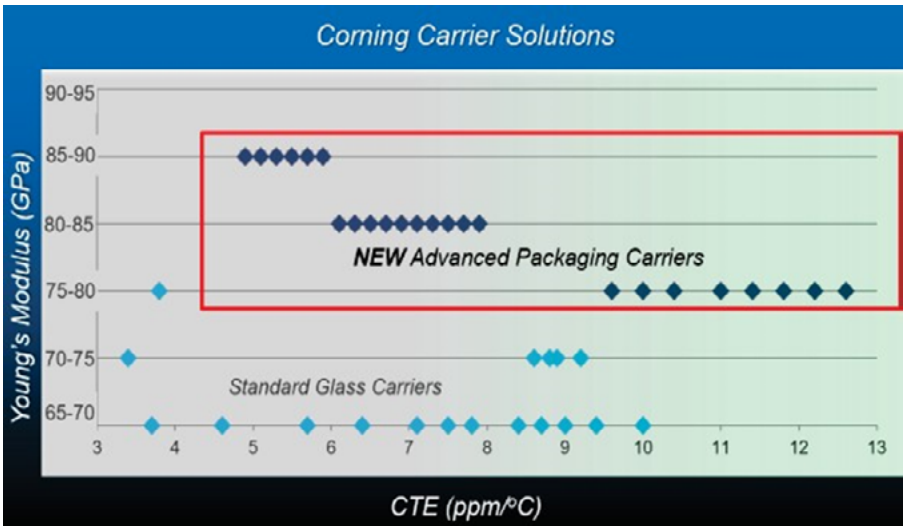

Figure 3: Corning's carrier wafer offering covers the entire 3-12.6ppm/°C range with fine granularity. Products in the red box have high Young's modulus by design as well as thickness flexibility all the way to 5mm.

ALoT: Advanced Liftoff Technologies

ALoT is an acronym for Advanced Lift-off Technologies—a broad term that describes our portfolio of temporary bonding technologies. The original motivation behind developing ALoT was to support the use of Corning's ultrathin Willow® glass [2] in making thinner, lighter, more flexible and durable displays by leveraging existing display panel infrastructure.

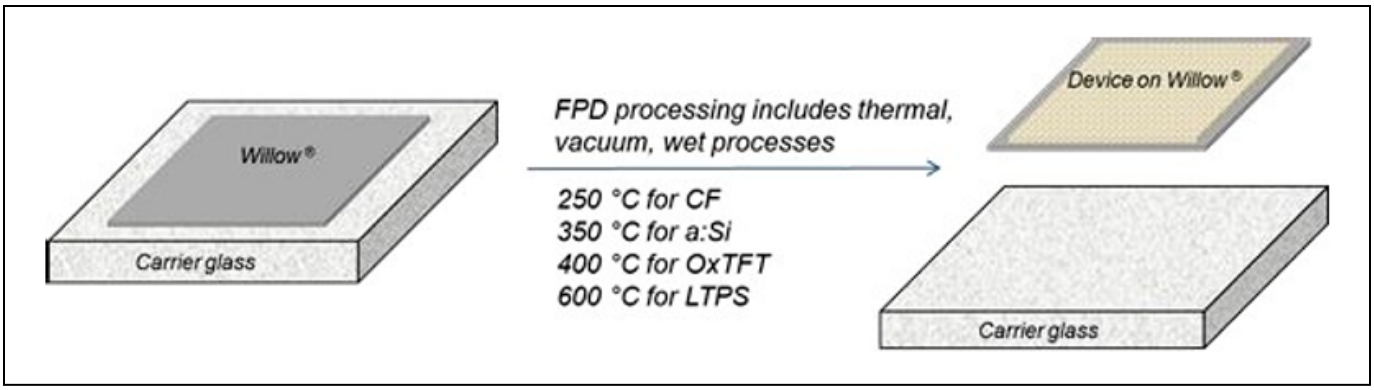

Figure 4: Schematic of ALoT-based approach to flat panel display (FPD) processing.

Incumbent methods used either mechanical or chemical thinning with significant environmental and cost challenges. **Figure 4** illustrates the concept. ALoT details are covered elsewhere [3].

A common feature of the ALoT family is the extremely thin bond layer, ranging in thickness from sub-nanometer to tens of nanometers. Such a thin layer would add essentially no TTV to the stack TTV, which is composed of carrier TTV and bond layer TTV. Most ALoT recipes use room-temperature pre-bonding followed by annealing at temperatures <150°C to achieve sufficient bond strength to support wafer thinning and remain mechanically debondable using standard debonding equipment. Low annealing temperature allows materials of different CTEs to be bondable without delamination or breakage due to stress. In the demonstration to be described next, ALoT bonding is done between a piezoelectric single crystal wafer with a CTE of ~14ppm/°C and a glass carrier with a CTE of 3.4ppm/°C.

ALoT bonding requires both the carrier and the wafer to be thinned to have flat and smooth bonding surfaces. If thinning is performed before device making, such as the example below, wafer surface characteristics can be guaranteed through wafer specifications such as roughness (e.g., Ra) and local flatness (e.g., LTV). When a device wafer to be thinned already has surface topography from prior device making steps, planarization must first be performed to achieve the required surface flatness and smoothness. The latter constraints may limit the ALoT application to only certain device wafer categories.

Wafer thinning demonstration

Single crystal wafers of piezoelectric materials such as lithium tantalate ($LiTaO_3$, LT for short) and lithium niobate ($LiNbO_3$, LN for short) are used widely in acoustic filter radio-frequency (RF) applications. Modern wireless systems (4G/5G) use GHz frequencies that benefit from very thin layers (e.g., <1µm) of these single crystals [4]. If thinning of LT or LN is supported with a high TTV substrate, achieving uniform layer thickness through wafer thinning would be difficult to impossible. Current practice is to follow mechanical thinning with a point-by-point technique such as ion beam trimming to fix the nonuniformity [5]. Ion beam trimming is slow and expensive. One alternative we set out to demonstrate is to use an ultra-low-TTV glass carrier with ALoT bonding. We chose LT for its broad adoption in surface acoustic wave (SAW) devices as well as availability up to 150mm diameter size. The concept is shown in **Figure 5**.

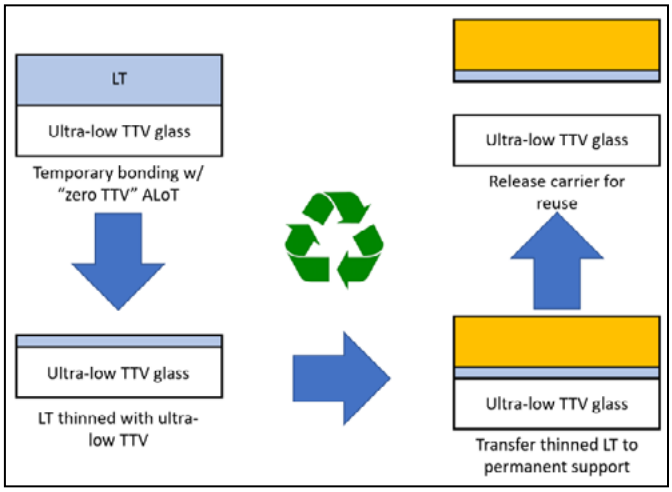

Figure 5: Thinning of LT using ALoT bonding and ultra-low-TTV glass carrier. After thinning, LT is then transferred to a permanent support substrate, and the carrier can be reused.

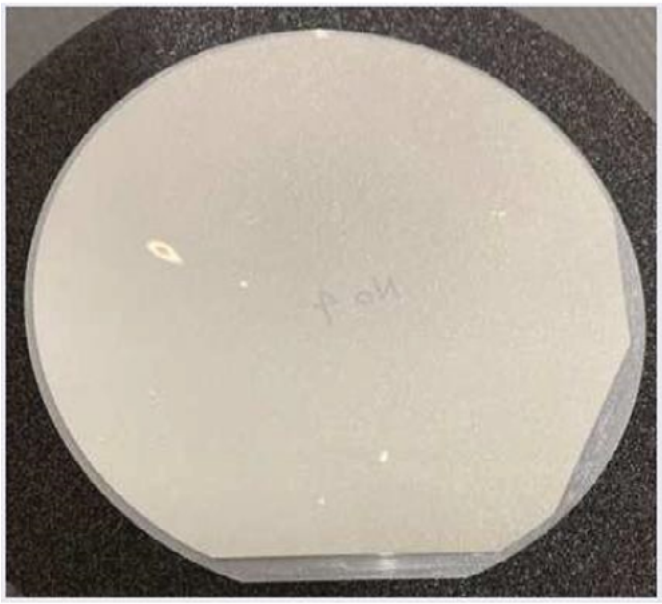

Figure 6: 150mm diameter, ALoT-bonded LT/glass wafer with a small number of remaining bonding defects. Edge trimming was performed to remove bonding defectivity near the edge. LT thickness before grinding is 350µm.

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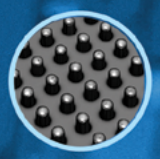

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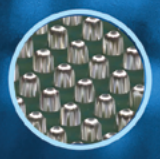

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We report here results from the first two steps, namely ALoT bonding and LT wafer thinning.

Figure 6 shows an ALoT-bonded LT-glass wafer. Due to imperfect cleaning, voids are seen inside the wafer as well as near the edge. The edge voids would cause delamination during thinning, so careful trimming was applied to make sure these are removed. When necessary, the trimming wheel performed linear, "surgical" actions to ensure the edge voids were removed.

Disco model DFG8640 was used to grind the LT. The equipment configuration schematic is shown in **Figure 7**. The equipment has multiple stages that can be configured to do coarse grinding, fine grinding and CMP, all on the same tool. Our experiment only used two grinding steps (Z1 and Z2 in the picture).

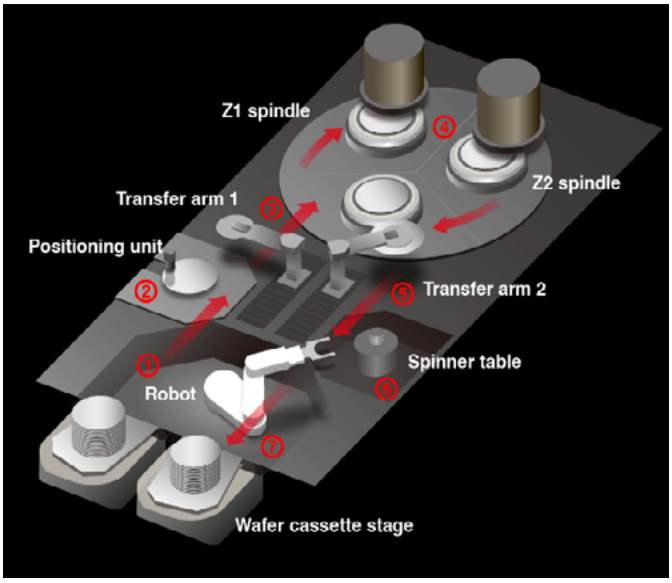

Figure 7: DISCO wafer grinding/polishing tool configured to perform coarse grinding, fine grinding and CMP, all on the same tool. SOURCE: DISCO website.

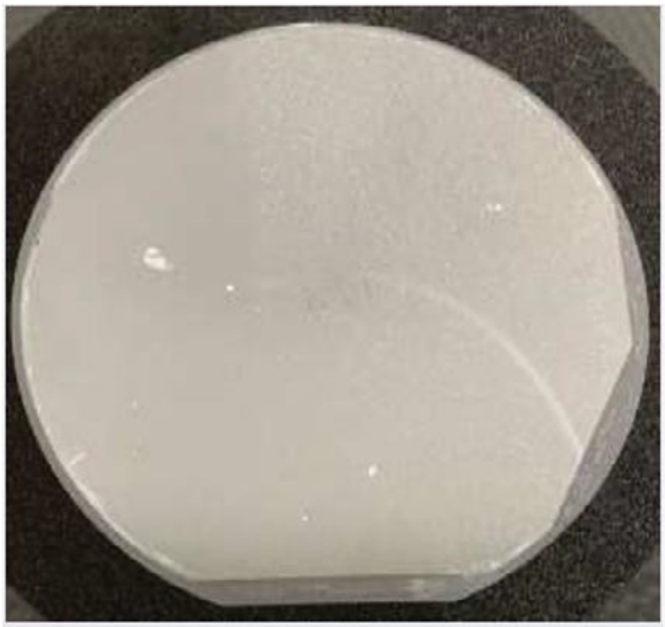

Figure 8: After grinding LT to a thickness of 15µm, the LT wafer is largely intact, with minor chipping at the 9:30 position near the edge.

Figure 9: After grinding LT to a thickness of 5µm, the LT wafer shows more severe chipping all around the wafer.

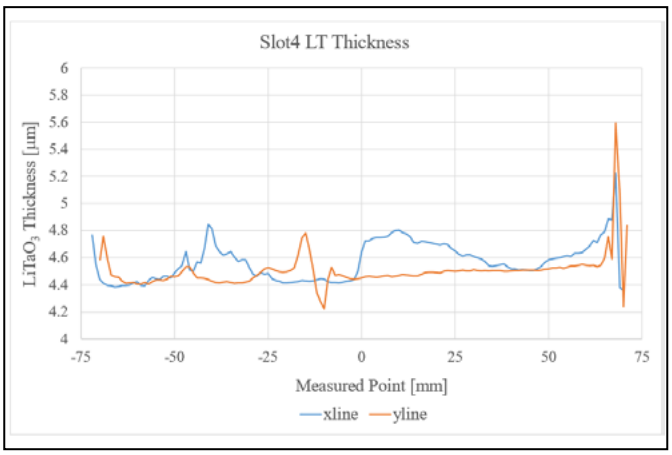

Figure 10: Thickness measurement in the X and Y directions indicate total TTV ~0.4µm. Because the stack TTV is ~0.2µm, other factors such as debris shedding, and equipment vibration during grinding and measurement may have contributed to the LT TTV.

Figure 8 shows the wafer after grinding LT to a thickness of 15µm. Only minor chipping is evident at the 9:30 position. **Figure 9** shows the same wafer when fine grinding further thinned the LT layer to a thickness of 5µm. Much more chipping can be seen all around the wafer. This indicates the ALoT bonding strength may be insufficient. It is well known in the semiconductor industry that bonding is usually weaker around the wafer edge even if voids and other defectivities are not observed visually or by confocal scanning acoustic microscopy (CSAM). The standard mitigation method is to introduce edge trimming around the entire wafer before bonding.

Post-grinding thickness measurement in two perpendicular directions, shown in **Figure 10**, indicated total thickness variation from wafer center to wafer edge. Discounting the wafer edges, TTV seems to be around 0.4µm. We believe stack TTV (~0.2µm), debris shedding from edge delamination, equipment vibration during grinding and the measurement technique itself all contributed to this result.

Work is continuing to further optimize ALoT bonding quality and bonding strength. Grinding conditions such as down pressure, wheel RPM, and feed speed/direction are also under study.

Summary

Precision wafer thinning supported by a carrier wafer can take advantage of two enabling capabilities reported in this work: ultra-low-TTV glass carrier, and near-zero-TTV temporary bonding. The resulting stack TTV can be as low as 0.2µm for wafer size <200mm; for a 300mm wafer, stack TTV can be as low as 0.4µm. While ultra-low-TTV glass carrier wafers are now commercially available, the ALoT bonding method as well as the thinning processes are still under further development.

Future work includes optimizing the ALoT bonding strength and quality to reach even thinner target thicknesses, as well as applying CMP to the ground surface before attempting to bond the thin LT to a permanent substrate such as Si.

Acknowledgments

The following Corning employees made significant contributions to the reported work: Erica Chang, Chris Kuo, Andy Kuo, Julie Tseng, Gwako Liang, Robert Manley, Han-hee Jo, Prantik Mazumder, Julia Brueckner and Kuniaki Yamazaki. The author also wishes to acknowledge DISCO Corporation in Japan for performing LT wafer thinning down to a thickness of 5µm, and Dr. Frank Wei of DISCO Hi-Tec America for insightful technical discussions. This paper was originally presented at the 25th Electronics Packaging Technology Conference (EPTC 2023) and was edited for publication in *Chip Scale Review*.

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Biography

Dr. Jay Zhang is Business Development Director with Corning's Advanced Optics division, Corning, NY. He has been with Corning over 20 years in various business development and program management roles. His recent focus is leading innovation efforts at creating differentiated glass wafer products and solutions that meet challenging applications requirements. He is also active in collaborating with ecosystem partners to demonstrate new product value propositions. He obtained his PhD in Applied Physics from Yale U. and his MBA from Cornell U. Email zhangjj@corning.com

3D integration of photonic and electronic chips on a glass substrate

By Saif Wakeel, Peter O'Brien [Tyndall National Institute, University College Cork, Ireland]
Luigi Ranno, Anuradha Agarwal, Lionel Kimerling [Massachusetts Institute of Technology]

3D printed free-form couplers and inverse tapers are two different vertical integration strategies for coupling light between a photonic integrated circuit (PIC) and glass interposer. For the free-form coupling scheme, 5×5×0.5mm^3 dummy silicon dies are bonded to a glass substrate using solder bumps via flip-chip bonding. The gap distance between the bonded chips is controlled by the solder height based on various bond pad sizes. An array of 14×14 square gold bond pads on the silicon chip is used with the bond pad length varying from 50µm to 105µm in order to maintain a required height. SAC305 solder is jetted onto the bond pads and an optimization of the reflow profile is performed to achieve defect-free, and high-wetting solder bumps. For the inverse taper coupling approach, the PIC is bonded to glass using an ultraviolet (UV)-curable optical epoxy (n=1.5). The measured vertical distance falls within the 2.8µm required Z-tolerance for evanescent coupling according to simulation.

Introduction

The move towards all optical I/Os on a switch package presents a viable solution for enabling low energy consumption (<2pJ/bit per transmitter (Tx)/receiver (Rx)) in devices operating at >100Gbps [1]. In these Tx/Rx packages, the PICs are co-packaged with the electronic integrated circuits (EICs) on a single interposer to minimize radio frequency (RF) track length [2]. This presents a unique opportunity for using the interposer material as a unified electrical-optical interface. Glass can be used for this purpose due to its low dielectric constant, low-loss tangent and low-loss optical wave guiding properties [3]. New optical coupling strategies such as free-form couplers and inverse tapers are promising interfaces for this platform [1,4]. The 3D-printed free-form couplers allow for relatively large alignment tolerances and a high bandwidth density between the PICs and interposer waveguides by collimating and redirecting the light from the waveguides in the PIC to the waveguides in the glass interposer [4,5]. Similarly, the overlapping inverse taper design allows for high optical bandwidth (300nm/1dB) and high-density of out-of-plane optical interconnections between PIC waveguides and glass waveguides [1]. Both integration strategies require different packaging approaches because of the varying vertical spacing requirements between PIC and interposer. The 3D-printed free-form coupling scheme shown in **Figure 1a** requires ≤14µm vertical distance, whereas the inverse taper coupling method requires ≤3µm vertical distance to facilitate evanescent coupling as shown in **Figure 1b**.

The tapered waveguide approach using evanescent coupling requires a smaller Z-tolerance than the free-form coupler approach. A UV-cured optical epoxy can fill such a gap while maintaining a relatively strong bond after curing. Optically transparent epoxies are useful for packaging as they form a layer that is both a strong adhesive and refractive index-matching. During curing, the layer thickness is reduced due to shrinkage. When this effect is accounted for and occurs in the same direction as the optical path, the coupling efficiency can see improvement as the optical path length is shortened after curing [6].

The free-from coupler Z-tolerance is not as strict as the tapered waveguides, so we demonstrated a different packaging method combining flip-chip bonding with solder and an epoxy underfill as bonding materials. This technique is widely used in electronic packaging industries as this method provides both strong mechanical and electrical connections to a package [7,8]. Recently, a group demonstrated flip-chip attachment of a vertical cavity surface emitting laser (VCSEL) onto a Si PIC using solder bonds [9]. Solder was

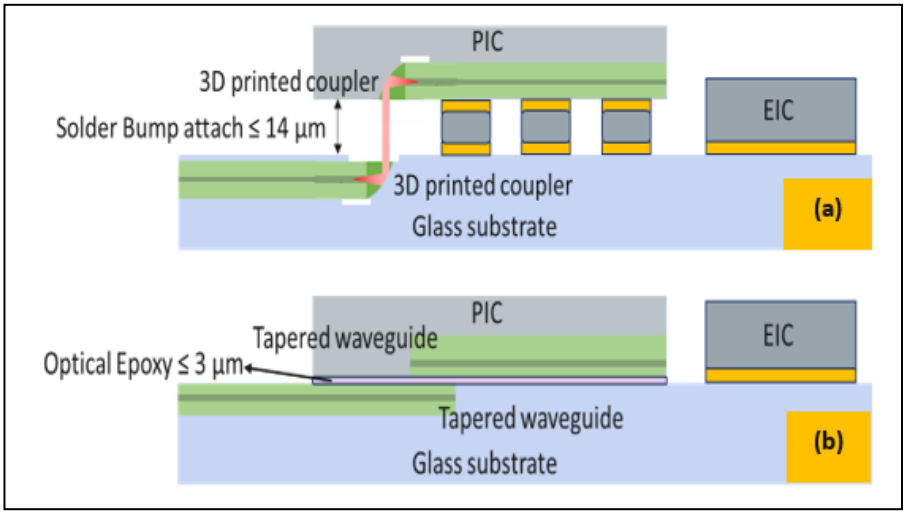

Figure 1: Packaging of PIC and EIC on a glass substrate: a) using solder bump flip-chip attachment between the PIC and glass substrate to enable optical coupling by 3D printed coupler, and b) by epoxy bonding PIC and glass substrate to enable evanescent coupling between PIC and glass waveguides.

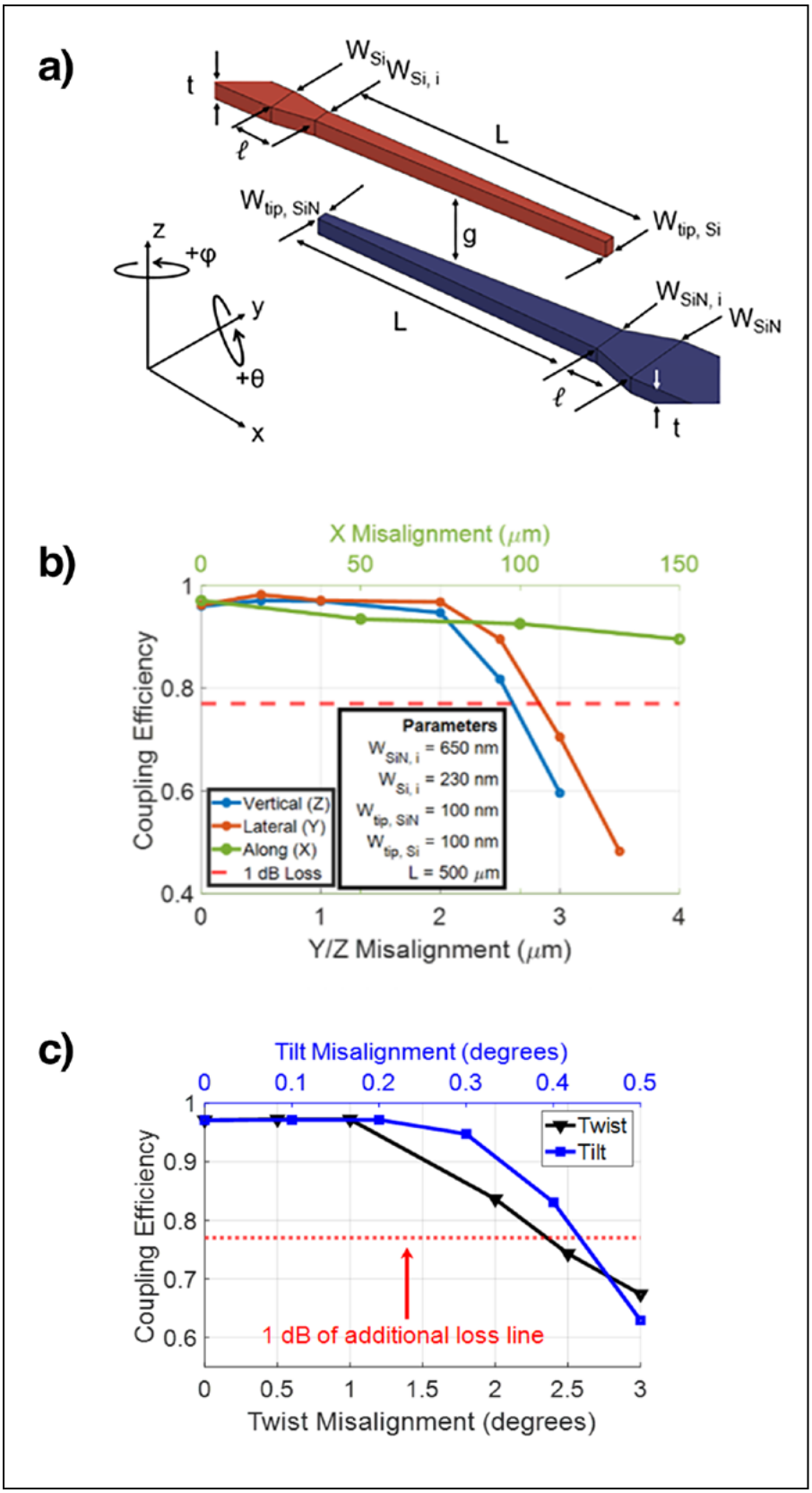

Figure 2: 3D FDTD simulation results showing: a) coupler parameter definitions where the red is Si and the blue is Si_3N_4, b) the translational alignment tolerance in X/Y/Z, and c) the rotational alignment tolerance where tilt indicates rotation about the Y-axis and twist indicates rotation about the Z-axis. Reprinted with permission from [1] © The Optical Society

deposited onto various bond pad sizes to determine and maintain a consistent height for efficient optical coupling to grating couplers. The translational and angular tolerances for both the free-form couplers and tapered waveguides were determined via simulation.

Simulation

3D finite difference time domain (FDTD) simulations were performed to determine the coupling efficiency (CE) for both presented approaches. The alignment tolerances of the structure as a function of translation between the two chips were calculated. For the evanescent coupling approach, simulation results using Ansys-Lumerical's 3D FDTD solver are shown in **Figure 2**. The gap length in the Z direction was input to be 0µm for the X/Y tolerance results and 500nm for both tilt and twist tolerance simulations.

The results from the data in **Figure 2** show this design has a lateral (Y) tolerance of ±2.7µm, vertical (Z) tolerance of 2.8µm, longitudinal (X) tolerance of over ±150µm, twist rotation tolerance of ±2.3°, and tilt rotation tolerance of ±0.4°. For this simulation, the underfill epoxy refractive index is assumed to be 1.457 to match the refractive index of silica being used [10]. Further simulations indicated the Z-tolerance can be extended to near 3.75µm if an epoxy with refractive index closer to 1.5 is used. However, as the epoxy refractive index increases, the light becomes less confined in the waveguides and will require longer tapers to compensate for the scattering loss. This simulation data demonstrates this design has comparable lateral and angular tolerances to those achievable using high-speed pick-and-place die bonders (approximately ±3-10µm) and has a vertical tolerance comparable to back-end-of-line (BEOL) thicknesses typical of active PICs. This indicates there is potential use for this evanescent coupler design in flip-chip bonded packages.

In the case of chip-to-chip freeform reflectors, possible misalignments or tilts that may be introduced during assembly are necessary to determine as they are important metrics to evaluate the practicality of the device. FDTD simulations indicate that the reflectors are very tolerant to both translation and

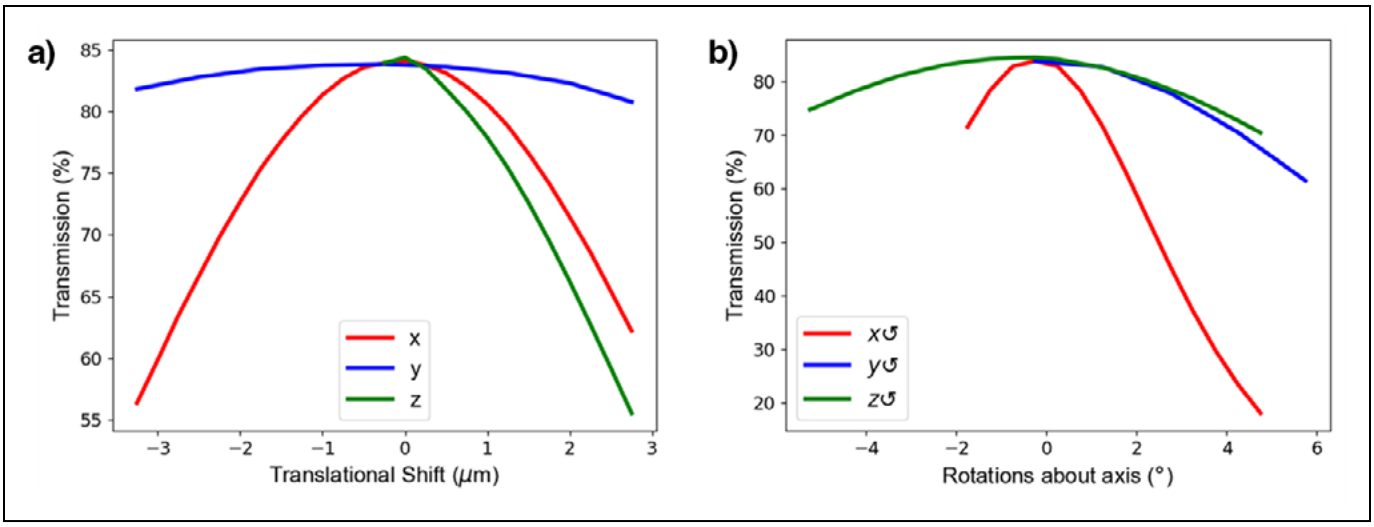

Figure 3: Tolerances of the freeform couplers with respect to: a) linear translation, and b) rotation about each axis. X represents the direction of light propagation, Y the vertical direction separating the two chips, and Z the in-plane direction perpendicular to light propagation.

rotation as seen in **Figure 3**. The tighter tolerances with respect to the rotations about X, the light propagation direction, is due to the tilt about X redirecting the light beam produced by the reflectors causing it to miss the output waveguide facet. The coupling efficiency (CE) of the free-form coupler was simulated to be 84% at 1550nm, corresponding to an insertion loss of 0.76dB.

Methodology

The packaging method used for the 3D-printed free-form coupler approach is based on the variable solder bump height, which can be controlled by varying the bond pad sizes [9]. Additionally, these solder bumps can also act as an electrical interconnection between the PIC and the glass interposer. The vertical distance between the PIC and glass interposer is tested by using 5×5×0.5mm^3 dummy Si and glass chips. The Si chips have a 3µm layer of oxide deposited on the surface of the silicon to better mimic a PIC. In the first case, where the solder bump height is varied, arrays of 14×14 square gold bond pads are deposited on the dummy Si and glass chips with the bond pad sizes varying from 50µm to 105µm. The variations are in steps of 5µm and the pitch between the bond pads remains constant at 100µm in all cases. SAC305 solder bumps are jetted on the gold bond pads of the silicon chip that is followed by reflow in an LPKF Protoflow S oven using the profile shown in **Figure 4**.

For the evanescent coupling approach, the PIC and the glass interposer were bonded together via UV-curable optically transparent epoxy Dymax OP-29. This epoxy is selected due to its fast curing time (~2min), matching refractive index (n=1.5), and balanced viscosity (2500cP). The packaging process starts with six-axis alignment of the glass sample relative to the dummy Si chip that is fixed in position. After alignment, epoxy is deposited onto the surface of the dummy PIC. The glass sample is then slowly brought towards the Si chip allowing capillary action to spread the epoxy evenly across the surfaces of the

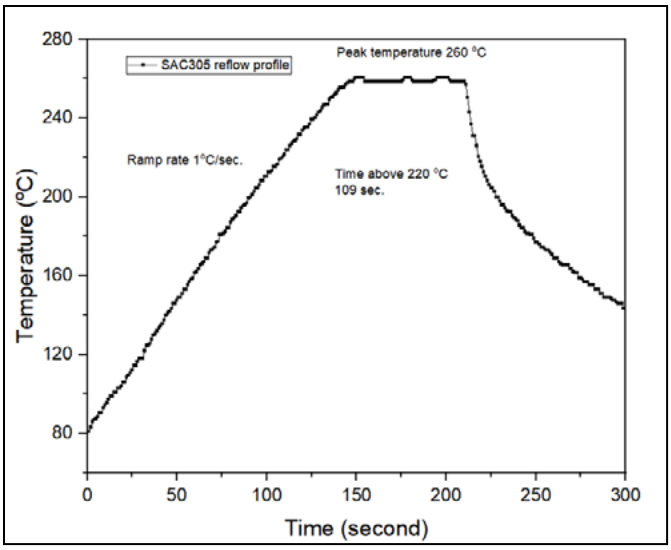

Figure 4: Reflow profile used for solder bump height variation.

samples. When the desired distance between the glass and Si samples has been reached, the epoxy is cured using a UV lamp.

An FEI Quanta scanning electron microscope (SEM) is used to measure the height of the solder bumps and the gap between the chip and substrate in bonded samples. Jetted solder bumps on bond pads after reflow, flip-chip samples bonded using solder, and epoxy-bonded samples are each put into an epoxy mold with a hardener ratio of 2:15 for 10 hours. After this time, grinding of molded samples is performed using 400, 800, 1200, 2500 grit SiC abrasive paper. Polishing is then performed via 1µm alumina suspension. Finally, images of these samples are recorded in the SEM and used to carry out the necessary measurements.

Result and discussion

Solder bump height variation with respect to different bond pad sizes is presented in **Figure 5**. There is a clear trend that increasing the bond pad size reduces the height of solder bump due to the spreading of the solder over a larger surface area. For example, a 50µm diameter solder ball jetted onto a 50µm bond pad results in height of 26.8µm, while a 100µm bond pad results in a bump height of 12.14µm.

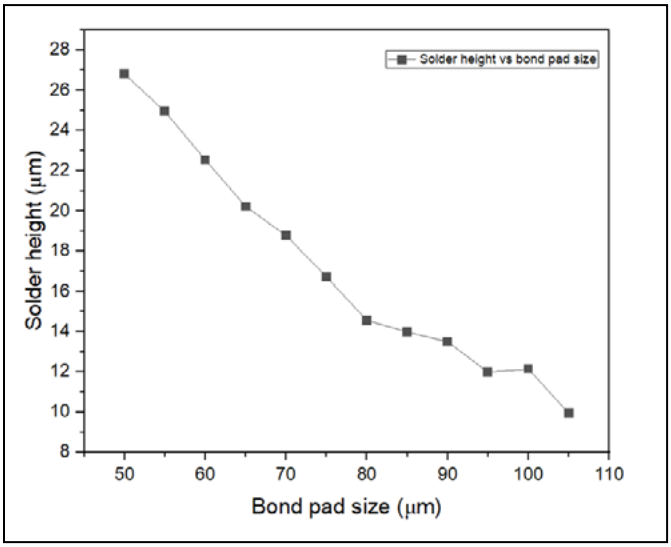

Figure 5: Solder bump height after reflow vs. bond pad size.

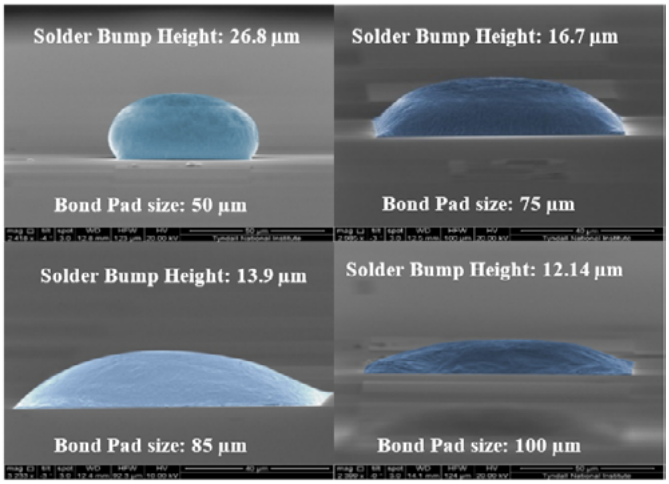

Figure 6: SEM images of the solder bump with different bond pad sizes on the dummy silicon chip.

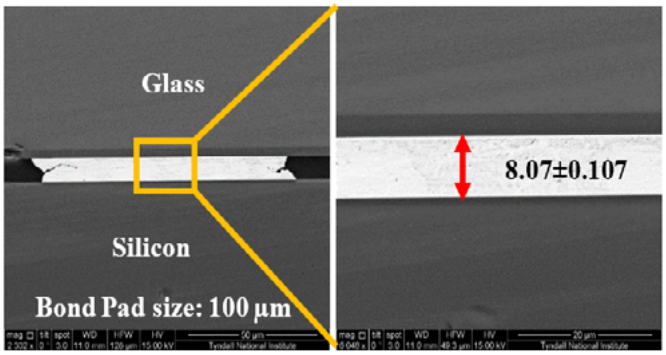

Figure 7: Flip-chip attached silicon and glass chips with the measured vertical distance of approximately 8µm between the two chips when the bond size on both chips is 100µm.

The measurements for the solder bump height on a single silicon chip after reflow can be seen in **Figure 6**. These are used to determine the optimal bond pad size for an application depending on the vertical distance separation requirements for the flip-chip bonding of silicon and glass samples. Solder wettability for smaller and larger size bond pads is clearly depicted with no apparent defects on the surface of the solder.

As the 100µm bond pad size consistently produced samples with a vertical spacing around 12.14µm, this pad size was chosen for the application. In **Figure 7**, the glass and silicon samples were bonded together using 100µm bond pads. The final vertical distance between the two samples was measured to be 8.07±0.177µm, well within the required 14µm tolerance for the free-form couplers.

To enable the tapered waveguide approach, silicon and glass dummy samples are bonded using optical epoxy. Using SEM, the average height between the two chips is measured to be 1.618µm as shown in **Figure 8**, with a variation across the length of the chip interface of ±0.177µm. This measured distance falls within the 2.8µm vertical tolerance for evanescent coupling according to simulation.

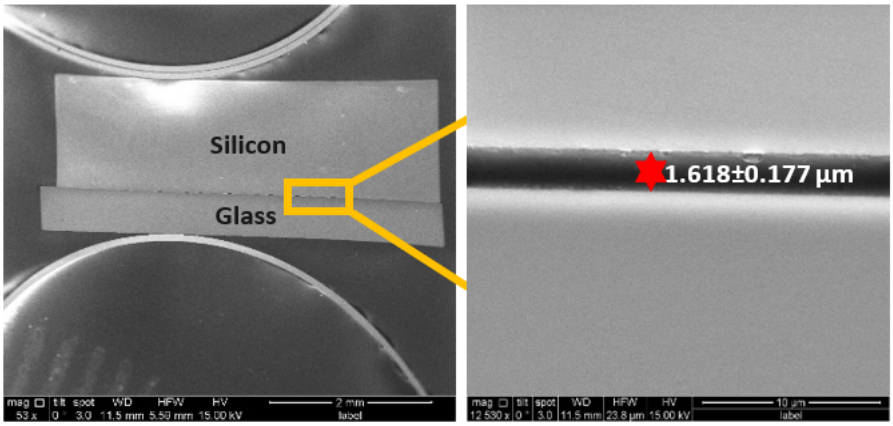

Figure 8: SEM images of measured silicon bonded on glass using optical epoxy showing vertical gap distance.

Summary

This work details the packaging approaches that are modified for different PIC and glass interposer coupling architectures based on their vertical integration requirements. The two vertical integration schemes, 3D printed free-form couplers and inverse tapers, for coupling light between PIC and glass interposer are required for allowing high-density off-chip optical interconnects and can enable these technologies to be used for wavelength division multiplexing in optical transceivers, broadband optical sensing, etc. These packaging strategies are scalable and geared towards using existing surface mounting processes such as solder reflow and optical epoxy bonding to optimize the optical coupling between the photonic chips and glass interposer.

Next steps include the development of photonic packaging demonstrators based on free-form couplers and inverse tapers. In addition, there are further experiments underway to test the mechanical reliability of solder joints and epoxies when exposed to varying temperature conditions.

Acknowledgments

Co-authors of this article are: Robert Bernson, Parnika Gupta, Kamil Gradkowski (Tyndall National Institute, University College Cork, Ireland), Samuel Serna (Massachusetts Institute of Technology and Bridgewater State University), and Drew Weninger, Juejun Hu (Massachusetts Institute of Technology). The authors acknowledge funding support provided by the MIT MISTI Global Seed Funds and the Irish Photonic Integration Center (IPIC). This article was presented at the 25th Electronics Packaging Technology Conference (EPTC 2023) and was edited for publication in *Chip Scale Review*.

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Biographies

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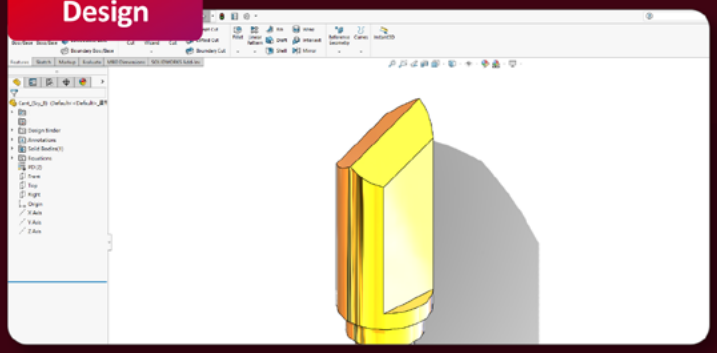
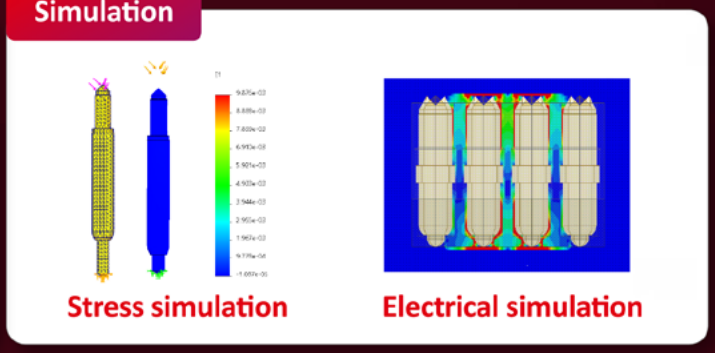


Customizable plunger

Simulation

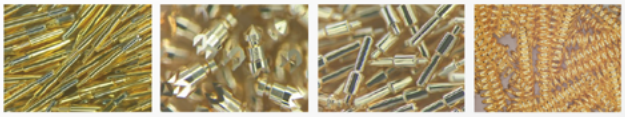


Ensuring probe performance and quality by simulation

Manufacturing

CNC

- √ Self-manufacturing parts
- √ Automated recipe configuration



Plating

- √ Various plating materials :

  Au/ AuCo/ AuCu/ Rh/ Ag/ PdNi/ NiP/ NiCo

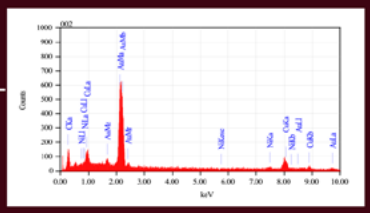
Choose coating based on product attributes: varying in anti-adhesion, anti-oxidation, wear resistance, and corrosion resistance

Assembly

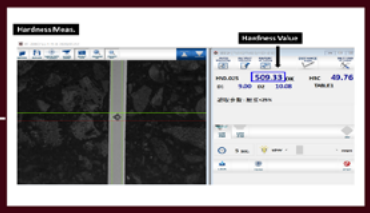
- √ 100% automation assembly and inspection (AOI)

Analysis

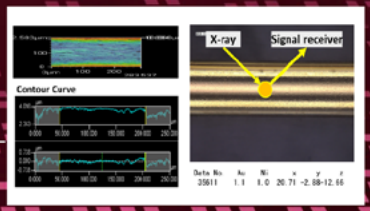
Material EDX



Mechanical property Hardness test



Plating Roughness Meas & Thickness Meas



A package solution for an optical engine in silicon photonics

By David Ho, Steven Lin, YP. Wang [Siliconware Precision Industries Co., Ltd]

Data center traffic is growing at a compound annual growth rate of nearly 30% because of the substantial growth of 5G, Internet of Things (IoT), artificial intelligence (AI) and high-performance computing (HPC) applications. Over the next two generations the switching throughput jumps from 12.8Tb/s to 25.6Tb/s, and 51.2Tb/s over the next two generations. The number of transceivers per switch and the data rates of those transceivers will increase as well. Scaling density will favor smaller connectors and lower power consumption. Additionally, in order to meet the tremendous bandwidth requirements derived from transmitting large amounts of data, optical communication technology has made great progress because the growth rate of conventional pluggable optical components is not able to catch up with the growth rate of data center traffic. Furthermore, traditional copper wire is limited by bandwidth, distance and power requirements. In parallel, the optical package is developing from wire bond, to flip chip and wire bond as a hybrid package, and then moving to 3DIC or fan-out technology to support optical engine (OE) development. Silicon photonics, therefore, is becoming a promising technology to replace copper wire and the industry is becoming convinced that it is a good option to transmit data with greater bandwidth, longer transmission distance and better energy efficiency than conventional electrical integrated circuits, which may suffer serious signal integrity distortion when transmitting data at high speed.

In this article, the critical co-packaged optics (CPO) concept was brought out to be the next-generation platform along with the fan-out embedded bridge (FO-EB) package as a robust option for an OE solution, to approach the enhancement of optical interconnection performance, broader bandwidth, lower power consumption and smaller form factor. CPO utilizes vertical 3D stacking technology to integrate the electrical integrated chip (EIC) and the photonics integrated chip (PIC) next to graphics processing units (GPUs) and router switches. Driven by artificial intelligence (AI) applications, silicon photonics technology will become a key technology in the semiconductor industry.

Introduction

As silicon scaling comes closer to the limits of physics, future reduction of the gate oxide does not decrease the cost per transistor. The demand for higher functionality and lower cost of electronic devices, however, will not be coming to an end. To improve yield and lower the total cost, the semiconductor industry is breaking down a large die to chiplet-based devices. Chiplet packaging, therefore, becomes a key technology to continue Moore's Law. The multiple chiplet packages can be horizontally/vertically stacked on a Si interposer using through-silicon via (TSV) technology (2.5D) or on an organic interposer to build up a fan-out multi-chip module (FOMCM) or a fan-out embedded bridge (FO-EB). Through such advanced packaging technologies and optimal integration of electronics chips and photonics chips, the length of electrical links can be significantly shortened. Therefore, the interconnect bandwidth density and energy efficiency can be much improved.

With the development of router/switch devices, with the bandwidth at 1.8T, the link speed of copper wire can still provide a matching transmission efficiency. However, with the evolution of application-specific integrated circuits (ASICs) and the addition of high bandwidth memory (HBM) die—when the bandwidth is increased to more than 10Tbps—an optical module needs to be used to provide a 200Gbps to 400Gbps transmission channel as shown in **Figure 1**. When reaching over 25Tbps, it is expected that the pluggable optical module will be transformed into an integrated silicon light engine to shorten the communication distance between the ASIC die and the optical engine to achieve a transmission speed >400G.

A CPO application is different from traditional pluggable optical transceiver module technologies. A CPO application combines a silicon photonic chip, a

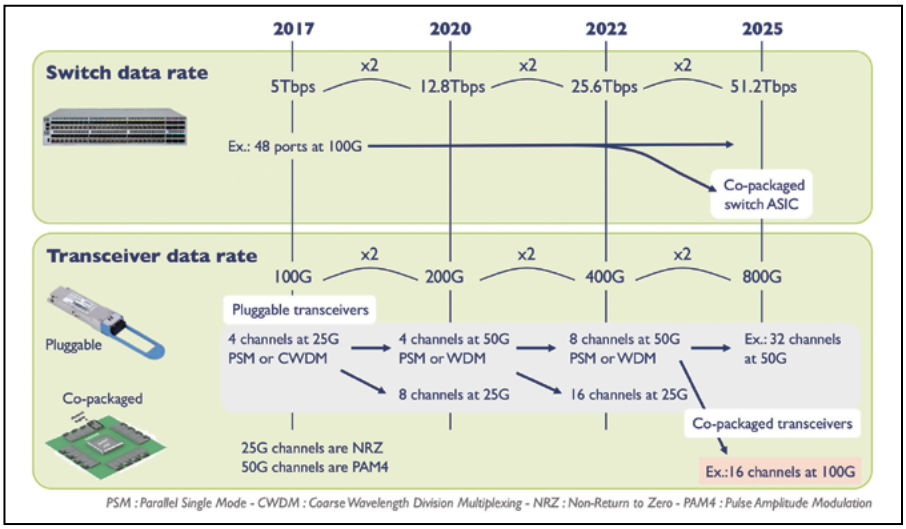


Figure 1: Trends in data center switches and transceivers. SOURCE: Yole Développement, Silicon Photonics, 2020

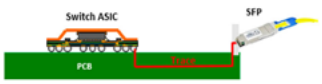
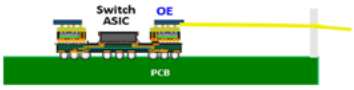
		As is	To be
CPO	Structure		
	Signal Path	Pluggable transceiver ⟷ PCB ⟷ Switch die	Optical Fiber ⟷ OE module ⟷ Switch die
	Data Rate	12.8 Tbps	**51.2 Tbps**

Table 1: CPO application structure comparison.

switch chip, a radio-frequency (RF) chip, etc. The package reduces the need for signal transmission through multiple media (including connectors, printed circuit boards [PCBs], and IC carrier boards). For example, as described in Table 1, in the past, electrons would travel from the chip through copper wires to a pluggable transceiver at the end of the server where they would be converted into light. The long intermediate transmission path results in problems such as delay and high loss, and it even increases the assembly cost because of the scattered components on the PCB board. However, because photons are faster than electrons, if the photoelectric signal conversion module (i.e., the optical engine) is placed directly with the switch chip using advanced packaging like FO-EB, the electrons will be converted quickly into photons after they leave the chip without following long, circulated copper wire paths. The signal, therefore, will be transmitted through the optical fiber into the optical engine and pass it to the switch die, which is a much smaller distance. This definitely allows the chip to be further upgraded in terms of reducing the data transmission path, signal loss or delay and, certainly, the power consumption, so as to be more effectively used in data communications and optical applications. According to further research data, this technology can roughly increase the amount of data transmission by 8 times, save power consumption by 50%, and computing power by more than 30 times. For these reasons, CPO technology should be implemented once the switch data rate exceeds 51.2Tbps. Furthermore, these findings have resulted in silicon photonics using CPO assembly technology becoming an imperative in the advanced packaging field.

OE integration technology in CPO

Currently, various OE structures have been demonstrated in the market, including wire bonding, flip chip, to fan-out RDL and 3DIC packaging types. Additionally, every assembly house or foundry has its own know-how and unique design capability with respect to an OE platform. As the interconnection between PIC and EIC dies is the key design feature needed to accommodate the OE electrical performance requirement, FO-EB technology was selected based on simulation results that demonstrated competitive performance with respect to the distance between the PIC and EIC, the insertion loss, and RC delay. Needless to say, within the signal transmission in the package, the use of FO-EB technology can also achieve energy consumption reduction and increases the communication speeds between these components. Figure 2 illustrates the OE buildup in a signal conversion module. We demonstrated an FO-EB being used to vertically stack a PIC and embedded EIC in which the PIC die was bonded onto the fan-out chip module with an overhang design. By using CPO to integrate the OE with the switch chip in the package-level assembly, we know that will not only shorten the distance between the switch chip and OE, but it will also reduce the CPO's form factor.

OE structure design introduction. Figure 3 shows a map of the FO-EB structure: the OE is comprised mainly of the PIC and the EIC. The PIC die is designed to integrate the digital signal process (DSP), which will dominate the transformation efficiency and performance between the light and the electrical signal. Other chips are integrated into the EIC die (e.g., driver amplifier (DRV), trans-impedance amplifier (TIA) and signal modulator function). Both the PIC and EIC are integrated into the design to cover various

key optical component functions, such as accommodating the signal conversion and processing to gain bandwidth/speed and lower power consumption. Furthermore, the PIC overhang design allows sufficient space to assemble optical fiber.

Application of the FO-EB process for an OE. The process flow of FO-EB for an OE is described in Figure 4. First, the bottom RDL layers and Cu post will be configured in parallel. The EIC die is then stacked onto the RDL layers, and the molding process is done; next, the top RDL layers are grown on the molding compound and the C4 bumps are grown afterward. Next, the PIC die is attached on top of the RDL using a die bond process with overhang design. Finally, this chip module (CM) will be singulated; and then a thermal compression nonconductive paste (TCNCP) is used to bond onto the substrate to provide warpage control of the OE module.

To further demonstrate this mature FO-EB structure readiness for use in an OE, a cross section was done after passage of the reliability test to identify if there were any open traces or solder shorts during thermal

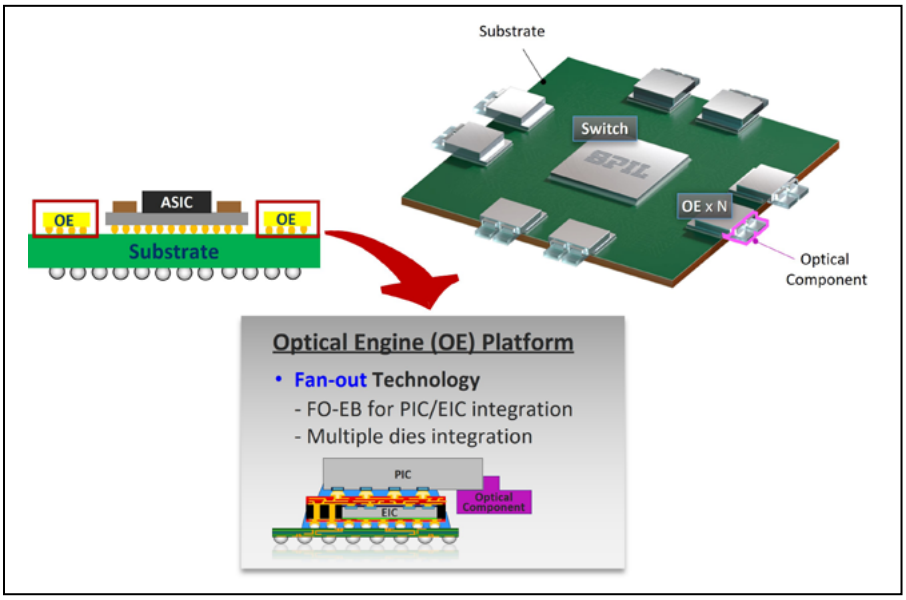


Figure 2: OE build-up as a signal conversion module.

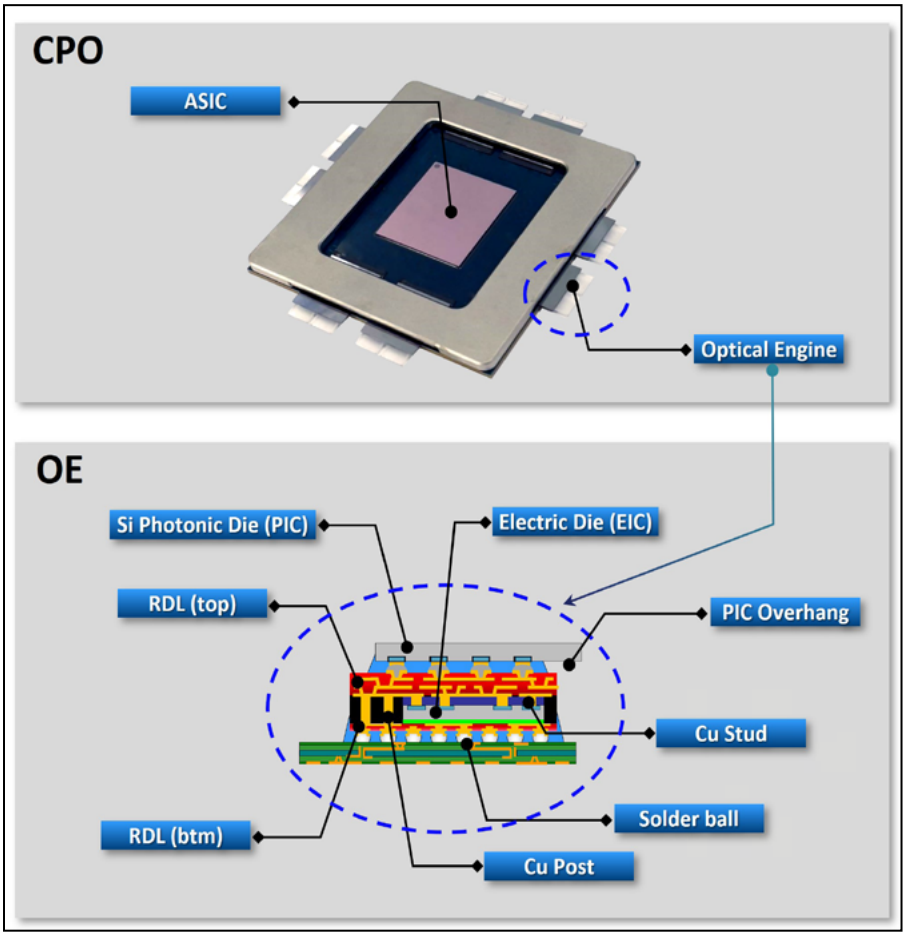


Figure 3: OE structure mapping with a FO-EB package.

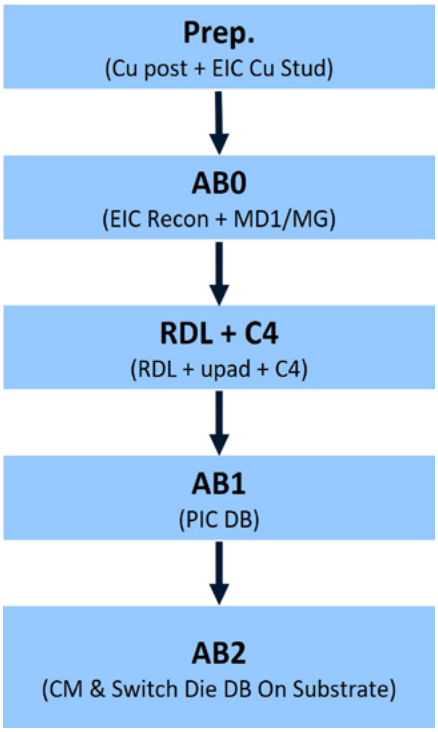


Figure 4: Application of the FO-EB process for an OE.

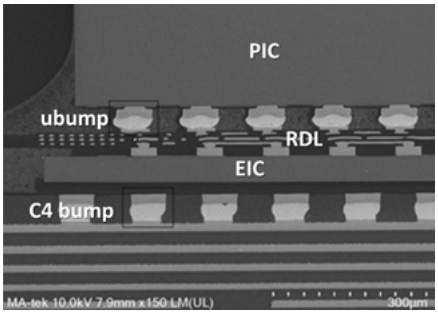


Figure 5: Cross section of an FO-EB-like OE.

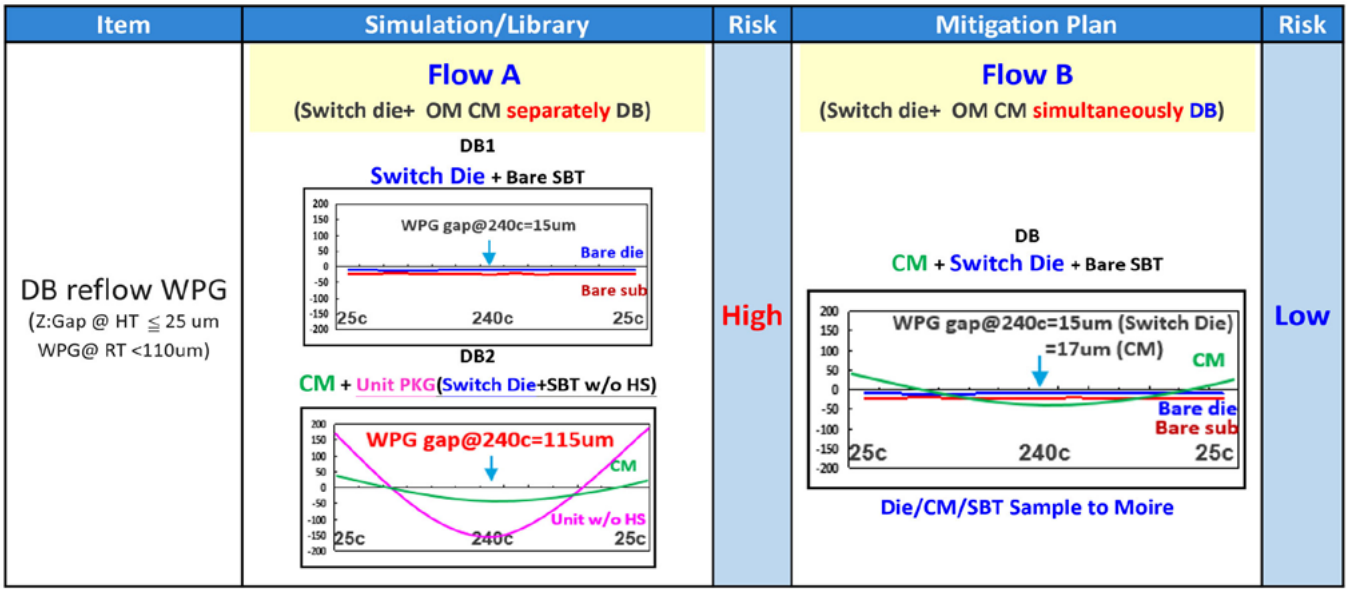


Figure 6: Simulation result of switch die and OE module bonding on a substrate.

stress testing. The cross section of the full OE structure is shown in **Figure 5**. The figure shows that the bond joint is reliable without any non-wetting or solder creep issue, thereby verifying the on-substrate process capability for the OE module.

The challenge for switch die and OE module bonding on a substrate. Returning to **Figure 3**, it can be seen that the standard scheme of the CPO platform includes one ASIC (i.e., a switch IC) with any number of OE modules. However, there is a challenging process in the flow selection for the sequence of OE and switch die bonding. For the OE attachment process, either thermal compression bonding (TCB) or mass reflow (MR) can be selected. The problem is that there will be a huge warpage gap if the switch IC and the OE CM are die bonded separately using process Flow-A as shown in **Figure 6**. This flow enables one to know if there is a good ASIC die before attaching it to the OE module. However, if Flow B is selected to bond the switch IC and the OE module onto the substrate while simultaneously using an optimized DB carrier and cover design, the CTE mismatch problem between these two entities can be significantly improved.

Summary

In this study we have shown how bringing photonics modules (optical engines) onto a package next to the switch ASIC contributes several benefits. Instead of inefficient copper traces running from the switch package to large pluggable interfaces, the fiber runs from the photonics modules to a faceplate connector. Those smaller connectors also help increase density. Additionally, wafer-scale manufacturing means reliable on-chip photonics engines can be integrated at a lower cost, which can also be accomplished by using an FO-EB solution for OEs.

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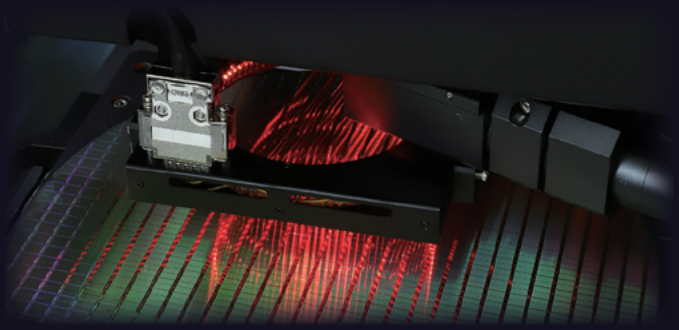

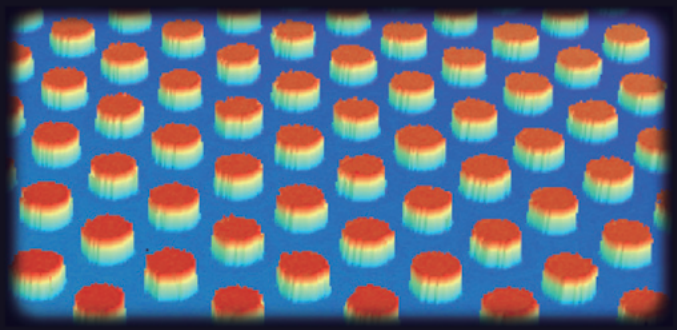

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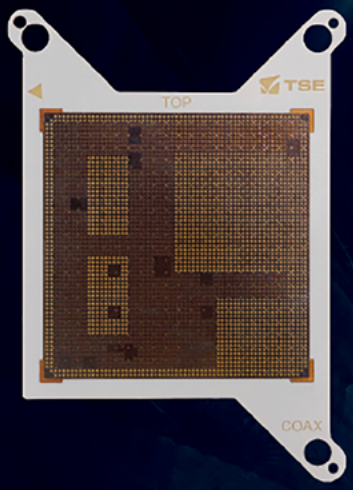
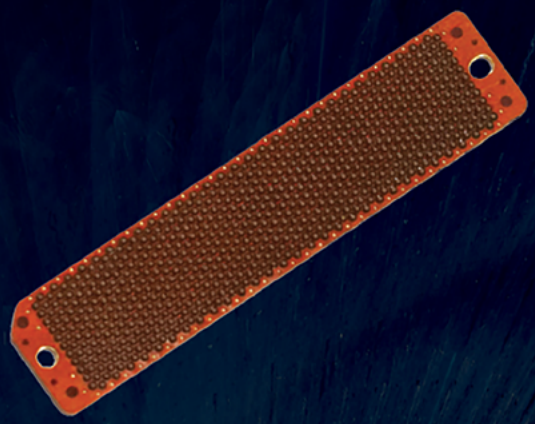


Semiconductor Package Test



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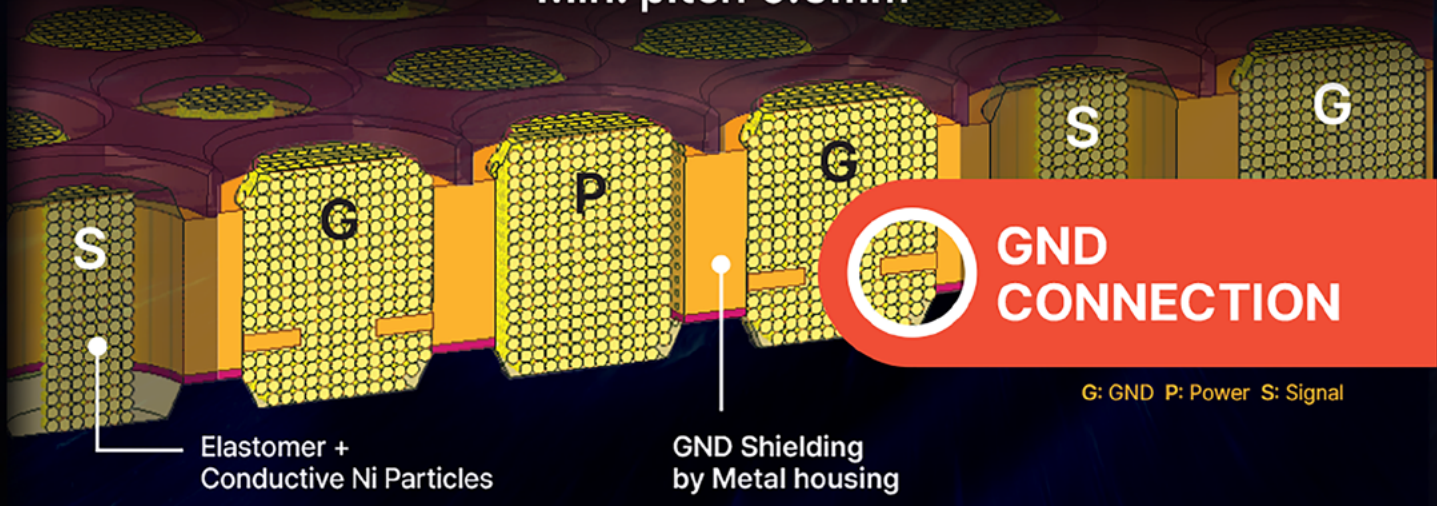

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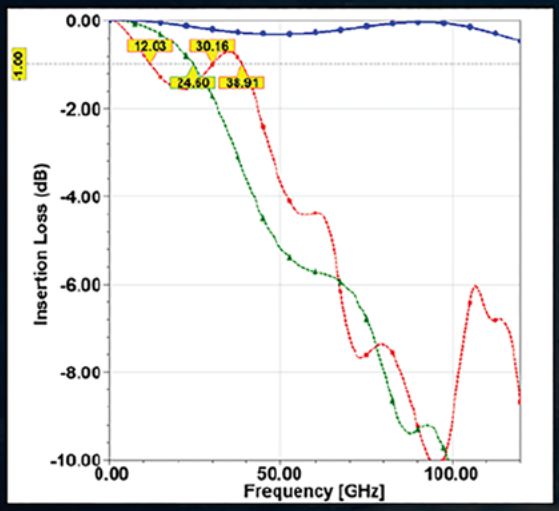
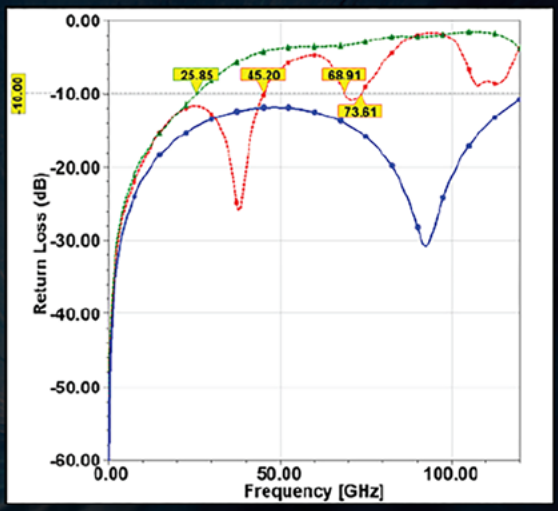
Insertion Loss(S21) @-1dB	12.03	24.60	>100
Return Loss (S11) @-10dB	45.20	25.85	>100
Crosstalk (S31) @-20dB	14.98	9.18	>100



Insertion Loss



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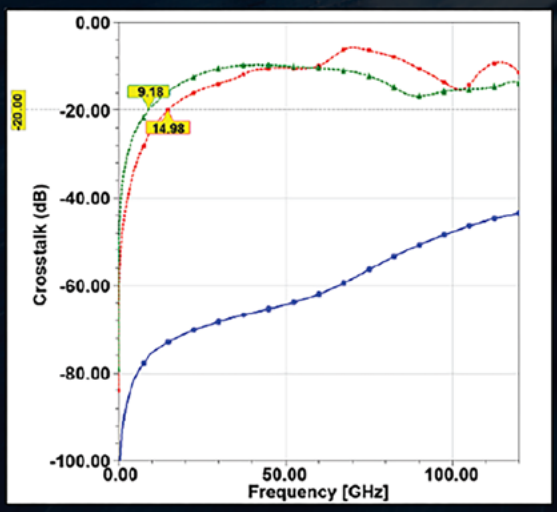

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Using an RDL-first FOWLP process to develop a large RDL interposer package

By Soon Wee Ho, Siew Boon Soh, Boon Long Lau, Hsiao Hsiang-Yao, Vempati Srinivasa Rao
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The chiplets packaging approach has emerged as a promising alternative to system on chip (SoC) technology, offering a low-cost and faster-to-market solution for building high-performance application systems. This work presents a redistribution layer (RDL)-first fan-out wafer-level packaging (FOWLP) fabrication process for creating a large organic RDL interposer for chiplets packaging. The process involves assembling chiplets with micro-bumps onto a high-density fine-pitch RDL stack, encapsulating them with mold compound, and creating a reconstructed wafer. Electrical and warpage measurements were conducted to assess the performance of the fabricated RDL interposer. Results show successful fabrication of the RDL interposer with good electrical continuity and solder joint formation, despite challenges related to warpage during assembly. A thermal compression bonding (TCB) process was implemented to address warpage issues, demonstrating effective assembly of the RDL interposer onto an organic substrate. This work highlights the potential of the RDL-first FOWLP process for large chiplets packaging and provides insights for addressing warpage challenges in RDL interposer assembly.

Introduction

In recent years, the semiconductor industry has witnessed a significant shift towards chiplets packaging as a compelling alternative to traditional SoC technology. Major semiconductor companies have shown a keen interest in exploring chiplets as a cost-effective and faster-to-market solution to address the challenges posed by the increasing complexity and cost of SoC designs. While SoC technology has historically been utilized to construct high-performance application systems by integrating multiple technologies and functional blocks onto a monolithic chip, the growing complexity of SoC designs has led to longer development times and higher manufacturing costs. In contrast, chiplets offer a modular and scalable approach that enables companies to build systems by combining chips from diverse technologies using advanced packaging platforms.

Various platforms for chiplets packaging have been developed, each offering unique advantages and challenges. These platforms include embedding chiplets in a FOWLP based on an RDL interposer technology [1,2], assembling chiplets on silicon interposers [3,4], or utilizing high-density build-up organic substrates [5]. The choice of platform depends on factors such as performance requirements, cost considerations, and scalability needs, with the RDL technology serving as a critical enabler for all chiplets systems. The demand for high-density RDL layers to facilitate routing between multiple chiplet I/Os poses challenges such as large package areas and the need for precise mask alignment in cases where multiple mask fields are stitched together.

Among the different chiplets packaging approaches, the RDL-first or chip-last FOWLP [6] approach has emerged as a novel and effective paradigm for fabricating chiplets packages. This methodology prioritizes the fabrication of high-density RDL layers on a temporary carrier substrate, allowing for the efficient processing of multiple RDL layers with minimal wafer warpage. By adopting the RDL-first approach, semiconductor companies can integrate chiplets with micro-bumps, create sophisticated chiplets systems, and develop large organic RDL interposers with embedded chiplets. This approach not only enhances performance and cost-efficiency but also streamlines the assembly process and ensures the continuity of RDL traces across the entire package area.

In this work, an organic RDL interposer with a large package size of 52 x 44mm, housing 12 embedded chiplets on a 60 x 60mm organic substrate was developed, showcased the effectiveness of the RDL-first FOWLP process in realizing complex chiplets systems.

Experimental procedure

The following sections address process flow and testing considerations.

Test vehicle design. The diagram in **Figure 1** illustrates the FOWL-based

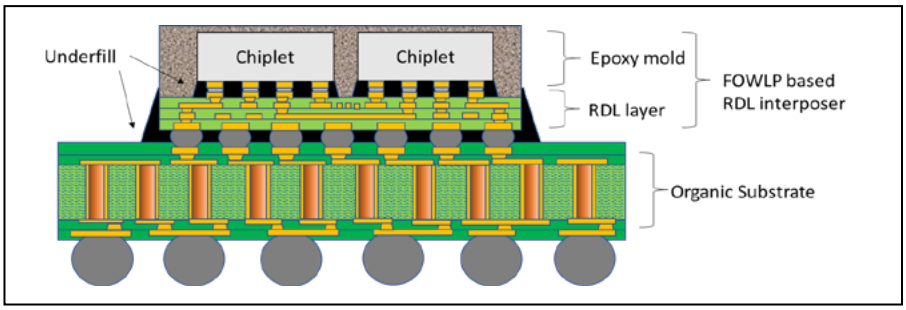


Figure 1: Illustration of an RDL interposer on organic build-up substrate based on RDL-first FOWLP.

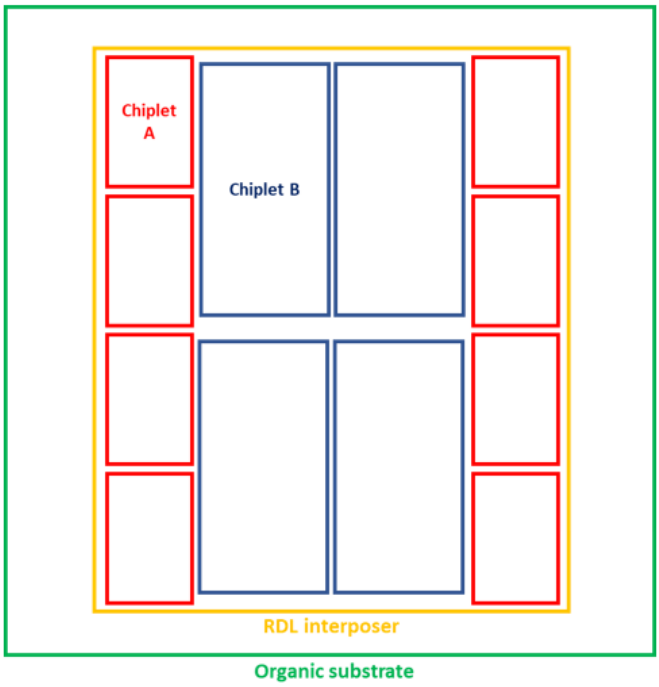


Figure 2: Top view of the RDL interposer showing the position and size of the chiplets, RDL interposer and organic build-up substrate.

RDL interposer assembled on an organic build-up substrate. The RDL interposer comprises 6 layers of high-density fine-pitch RDL with a minimum Cu trace of 2µm L/S. Chiplets with micro-bumps are affixed to the RDL stack. Subsequently, the chiplets are underfilled and encapsulated with an epoxy mold compound to create the RDL interposer package. This RDL interposer package is then mounted on a larger organic substrate. **Figure 2** provides a top view schematic of the chiplets' size and positioning. A total of 12 chiplets are integrated into the RDL interposer. The dimensions of the RDL interposer package are 52 x 44mm, while the organic substrate measures 60 x 60mm. **Table 1** defines the specifications of the chiplets and RDL interposer.

Chiplets	Die Size	Critical dimension
Chiplet A	11.87 x 7.75 mm	25 µm dia. bump / 55 µm pitch
Chiplet B	23 x 9.75 mm	25 µm dia. bump / 55 µm pitch
RDL interposer	52 x 44 mm	Top UBM: - 25 µm dia. UBM /55 um pitch Cu RDL (6 -layer): - Min. 2 µm L/S Cu RDL - Min. 3 µm contact via Bottom solder bump: - 100 µm dia. SAC305 bump/200 µm pitch
Organic substrate	60 x 60 mm	Solder mask defined pre-solder pad: - 100 µm dia. pad/ 200 µm pitch

Table 1: Specifications of the chiplets and RDL interposer.

Process Flow. The RDL interposer was fabricated on a 300mm diameter carrier using the RDL-first FOWLP process flow, as illustrated in **Figure 3**. First, high-density Cu redistribution traces were fabricated on top of the temporary transparent carrier. In this process, a low-temperature cured photodielectric acted as the interlayer passivation, and Cu distribution traces was achieved through

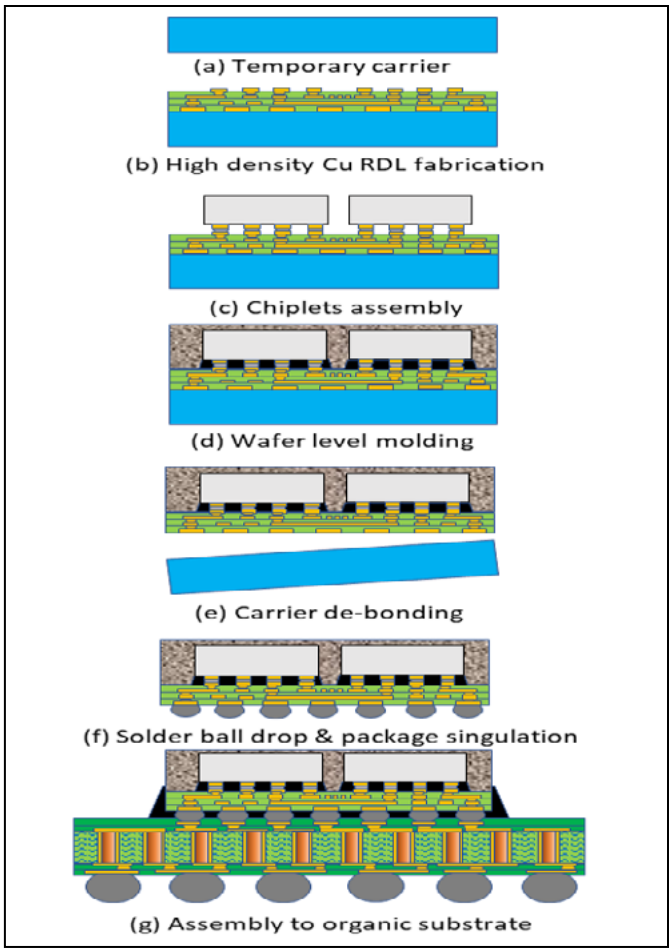


Figure 3: Fabrication process of the RDL interposer package using RDL-first FOWLP.

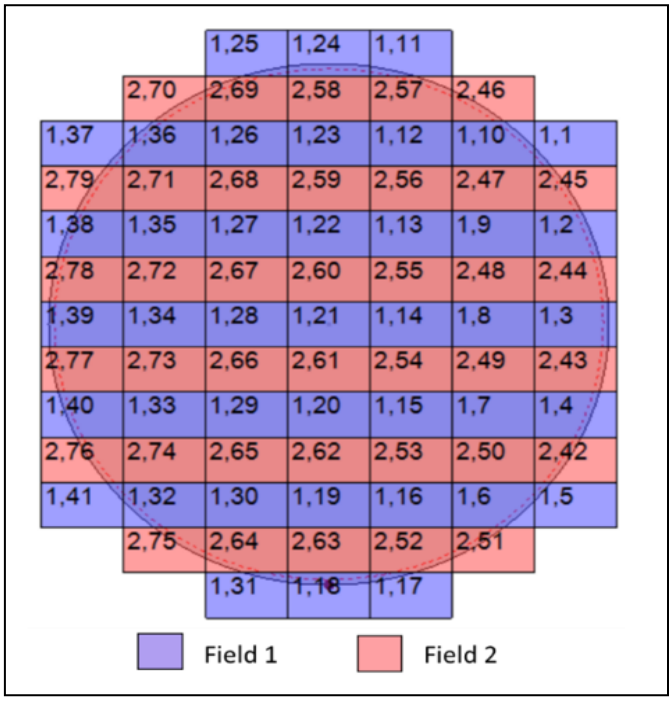


Figure 4: Wafer map during photomask exposure showing mask field and exposure sequence.

a semi-additive process (SAP). The photolithography stepper used in this work has a maximum exposure field size of 44 × 26.7mm, and two-field mask stitching was utilized to create the large package size of 52 × 44mm. **Figure 4** displays the wafer map during photomask exposure. The wafer map during photomask exposure was illustrated in **Figure 4**. Chiplets with micro-bump interconnects were assembled onto the top under bump metallization (UBM) pads on the RDL stacks using a mass reflow process. Wafer-level epoxy compression molding was applied to encapsulate the chiplets and RDL stacks with an expoxy molding compound, forming a reconstructed wafer. Following this, the temporary carrier was removed from the reconstructed wafer. Solder balls were affixed to the bottom UBM pads of the reconstructed wafer to create the solder ball grid array. The reconstructed wafer was diced into individual RDL interposer packages, which were then mounted to the organic substrate. Underfill material was dispensed and cured to bridge the solder bump gap between the RDL interposer and the organic substrate.

Testing. The fabricated RDL interposers were subjected to electrical and warpage measurement as follows:

1. Meander combs with 2µm L/S positioned at the stitched area between the 2 mask fields to verify the continuity of the of the two RDL traces. A daisy chain connecting the chiplets to the RDL layers was utilized to confirm the continuity of the solder bumps and RDL interposer.
2. Warpage measurement is crucial as it can impact the assembly process of the RDL interposer to the organic substrate and may result in poor solder joint formation, particularly for an interposer package of such large dimensions. The RDL interposer package warpage was assessed in a Shadow Moiré measurement tool and was subjected to a heating profile mimicking actual solder reflow conditions. The Shadow Moiré optical technique was employed to accurately measure the warpage of the RDL interposer under controlled conditions.

Results and discussion

The following sections discuss RDL interposer fabrication results: 1) Cu RDL process results, and 2) the chiplet assembly wafer-level molding and RDL interposer package assembly.

Cu RDL process results. **Figure 5a** shows the RDL and UBM layers fabricated on a temporary transparent carrier, prior to chiplets assembly. **Figure 5b** shows magnified optical images of a single RDL interposer package. **Figure 6** shows high-density 2µm L/S Cu RDL traces at different magnifications to meet the high-

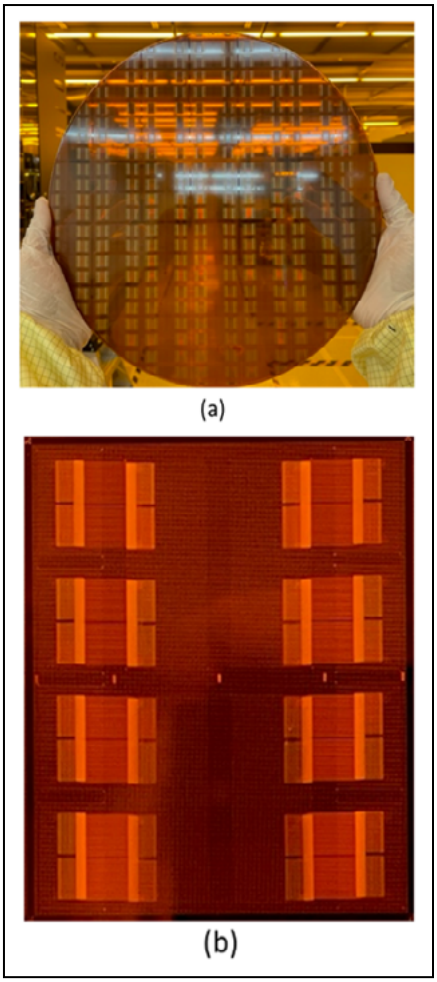


Figure 5: RDL processing on a temporary carrier: a) RDL layer fabricated on a transparent carrier; and b) a magnified image of a single interposer package.

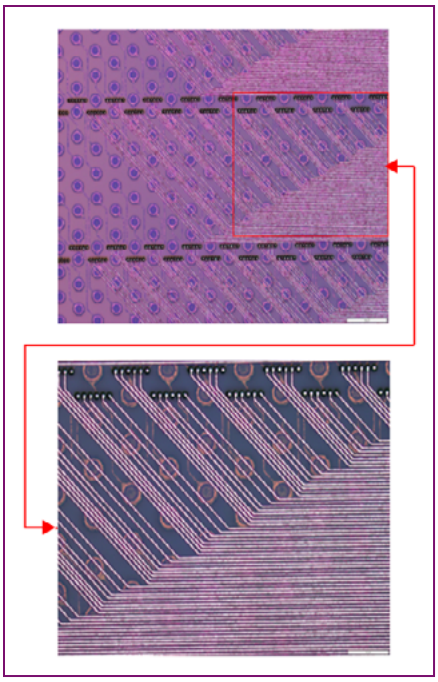


Figure 6: A segment of the high-density 2µm L/S Cu RDL traces at different magnifications.

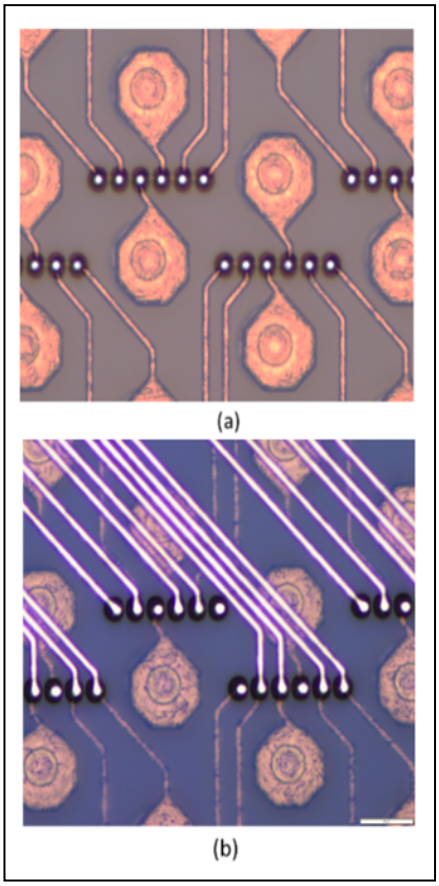


Figure 7: Contact vias for connecting the different Cu RDL: a) 3µm diameter contact via openings developed in a photodielectric film; and b) Cu traces and landing pad processed over the contact vias.

bandwidth requirement of the chiplets. **Figure 7a** shows the 3µm diameter contact via openings patterned in a photodielectric film for connecting the different level of Cu RDL, while **Figure 7b** shows the landing pads and Cu traces processed over the contact vias. **Figure 8** shows the fine-pitch Cu traces fabricated at the stitching section (blue dash line) between the two mask fields. No discontinuity in the Cu traces was observed along the stitching line boundary. The stepper tool mask alignment accuracy is maintained to below 0.2µm to ensure good stitching between the mask field.

Chiplet assembly, wafer-level molding and RDL interposer package assembly. **Figures 9a-b** show the optical images of the chiplets assembled onto the RDL stack on the carrier wafer and after wafer-level

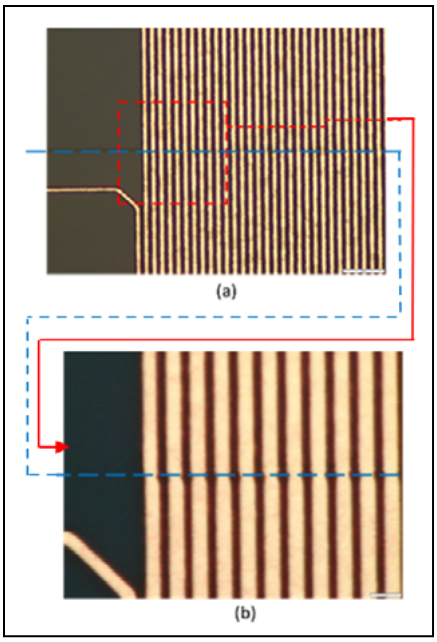


Figure 8: Cu RDL traces located at the stitch line (blue dash line) between the 2 mask fields: a) 2µm L/S Cu traces stitched; and b) magnified images showing the section of the stitched traces.

molding, respectively. X-ray inspection was carried out on the assembled chiplets, indicating good solder joint alignment and formation with the RDL stack layer (**Figure 10**). **Figures 11a-b** depict the fabricated RDL interposer package after singulation and solder bump attachment, respectively. Finally, the RDL interposer was assembled onto the organic build-up substrate using a TCB process, as illustrated in **Figure 11c**.

Electrical measurements

The following sections discuss various electrical measurements that were conducted.

Meander comb test structure at the stitch line. **Figure 12** shows a 2µm line/space meander comb test structure positioned at the stitch line between the two masks in the field. A slight taper is visible at the junction where the two traces converge. Additionally, **Figure 13a** presents the I-V curve of the meander trace, demonstrating good connectivity for the stitched Cu traces. The measured intra-layer leakage current is

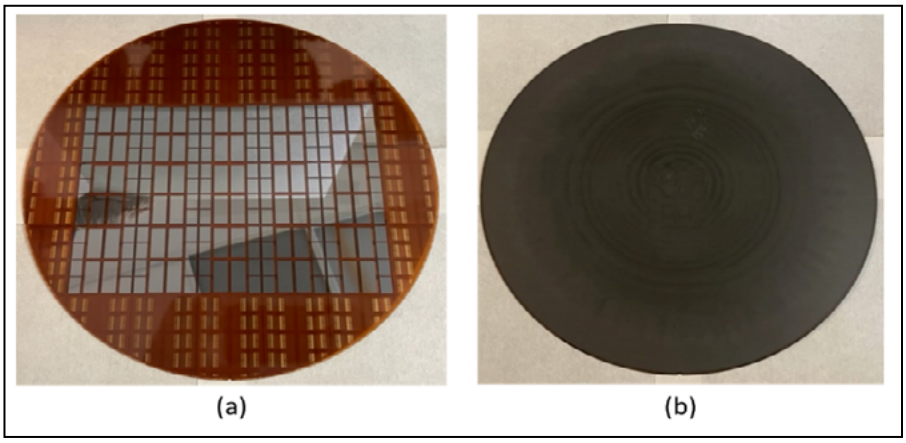


Figure 9: Chiplets assembled on a carrier: a) an array of chiplets assembled on the RDL layers; b) after wafer-level molding to encapsulate the chiplets assembly and RDL layer.

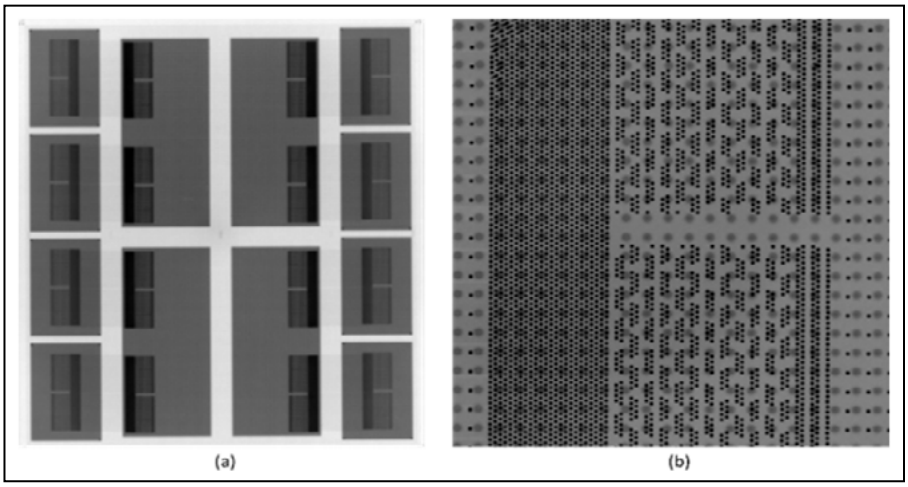


Figure 10: X-ray images of solder interconnects: a) a single RDL interposer with the 12 chiplets; b) magnified X-ray images of fine-pitch solder bumps.

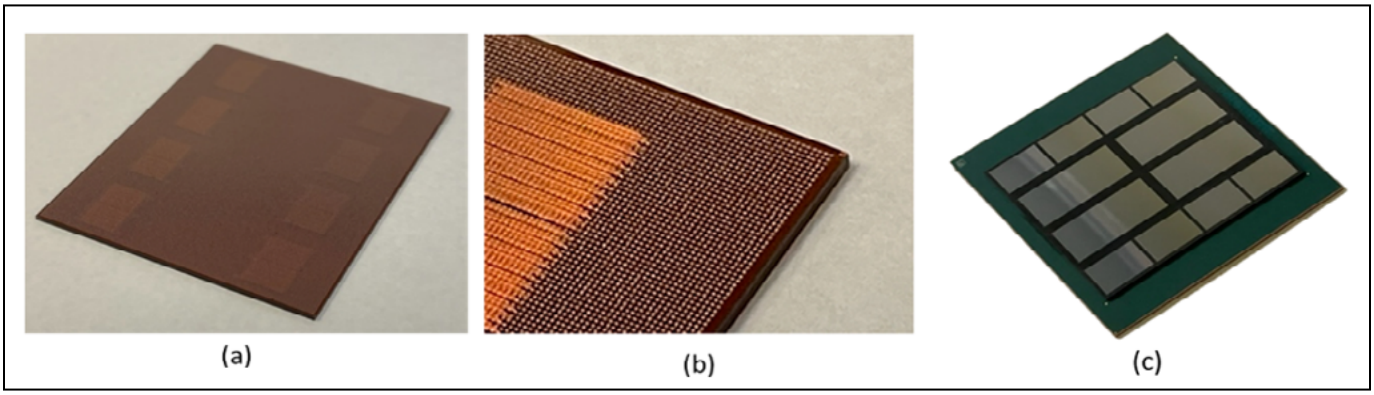


Figure 11: An RDL interposer package after solder ball drop and attachment to organic substrate: a) tilted optical image of the solder bump side of the RDL interposer; b) a magnified image showing the SAC305 solder bumps; and c) after attachment to organic substrate.

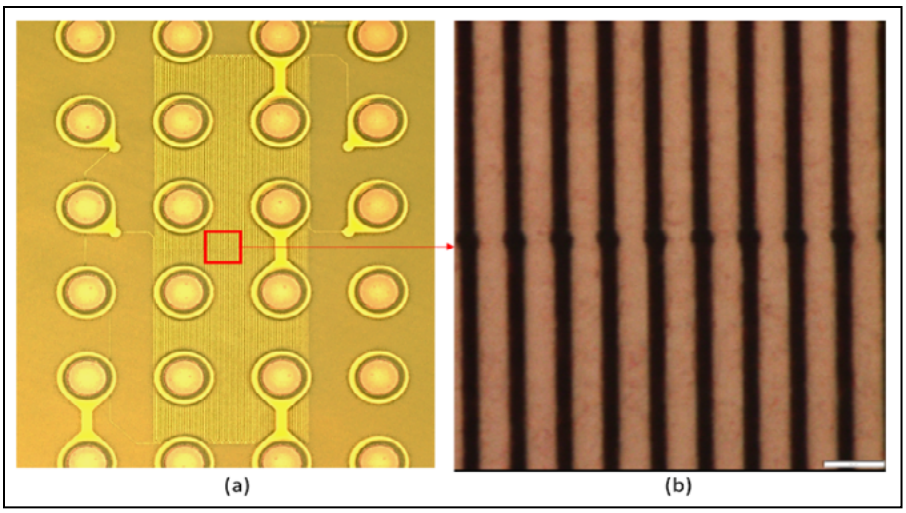


Figure 12: a) Meander comb test structure at the stitch line; and b) a magnified image of meander traces at the stitch line.

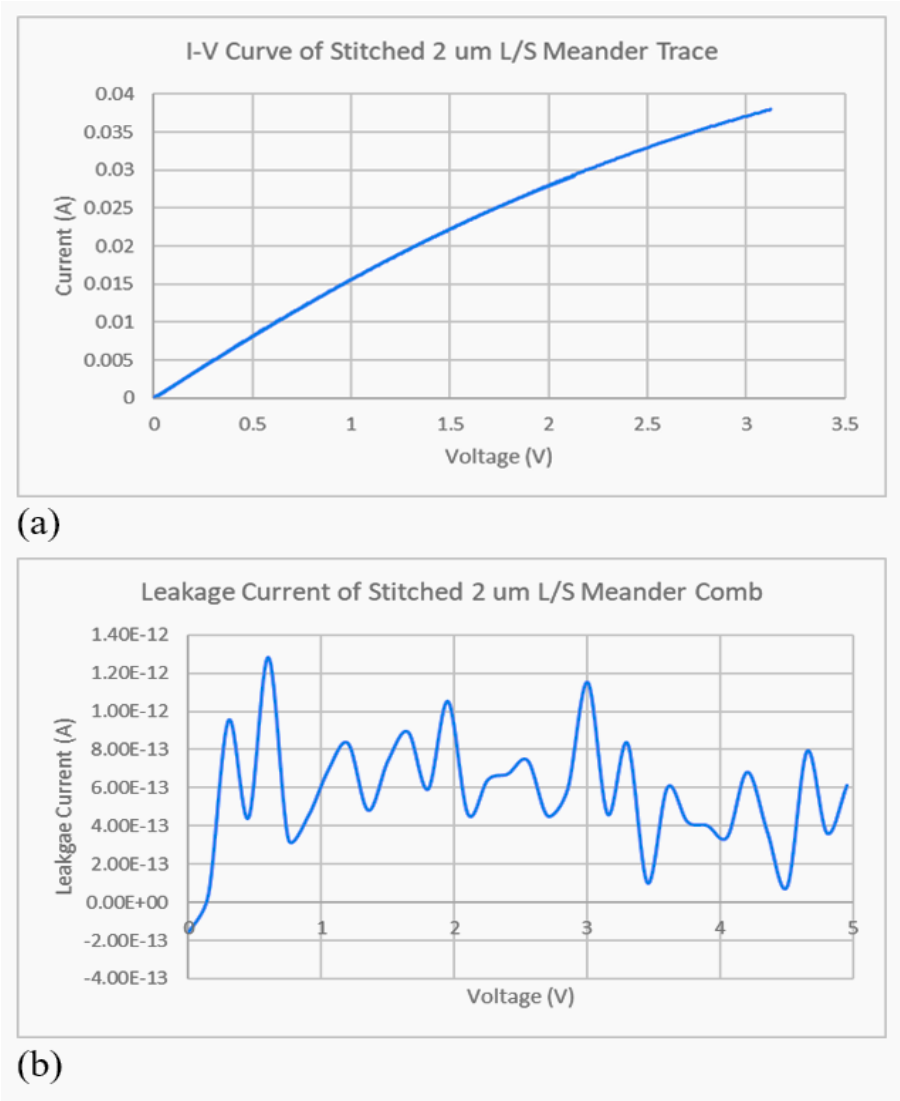


Figure 13: Electrical test results of a stitched meander comb structure: a) an I-V curve of meander Cu trace; and b) intra-layer leakage current of meander comb.

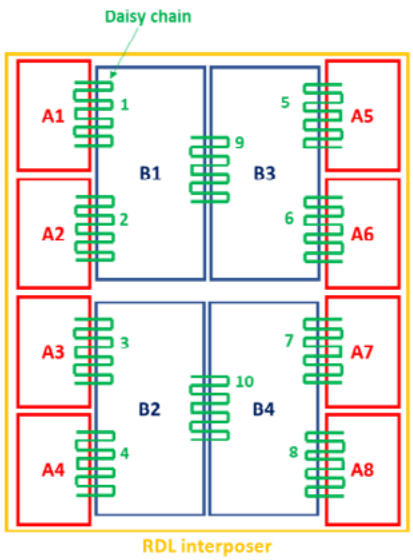
illustrated in **Figure 13b**, indicating a leakage current in the range of pico-amperes, which aligns with the target specifications.

Chiplets to RDL daisy chain. **Figure 14** shows the daisy chain locations between RDL and chiplets. Electrical testing was performed on the respective UBM pads connected to the RDL and chiplets; and all daisy chains showed good electrical continuity with no open connections, indicating good assembly yield of the chiplets using the mass reflow process.

Warpage measurement

The warpage of fabricated RDL interposer packages was measured using the Shadow Moiré technique during a reflow process. This assessment was conducted to evaluate the RDL interposer package's warpage when mounted onto the organic substrate. **Figure 15** illustrates the package warpage throughout the reflow process. The fabricated package was measured with the bump side facing down (live-bug), where positive values indicate a convex profile and negative values indicate a concave profile. Initially, the RDL interposer exhibited a convex warpage of 213µm. As the temperature increased, the package profile transitioned from convex to concave, reaching a maximum warpage of -736µm at a peak temperature of 275°C, before decreasing as the temperature was lowered. Upon cooling to room temperature, the final package warpage measured 277µm. This significant change in warpage is attributed to the coefficient of thermal expansion (CTE) mismatch between the RDL layers, chiplets, and mold compound. The observed warpage variation poses a significant challenge during the assembly of the RDL interposer to the organic substrate using a reflow approach, potentially leading to issues such as inadequate solder joint formations.

To address the challenge of large package warpage, a TCB process was implemented for assembling a large RDL interposer package. The process involved several steps to mitigate the warpage issue effectively. Initially, the RDL interposer was picked up on



Daisy chain	Connection
1	Chiplet A1 → RDL → Chiplet B1
2	Chiplet A2 → RDL → Chiplet B1
3	Chiplet A3 → RDL → Chiplet B2
4	Chiplet A4 → RDL → Chiplet B2
5	Chiplet A5 → RDL → Chiplet B3
6	Chiplet A6 → RDL → Chiplet B3
7	Chiplet A7 → RDL → Chiplet B4
8	Chiplet A8 → RDL → Chiplet B4
9	Chiplet B1 → RDL → Chiplet B2
10	Chiplet B3 → RDL → Chiplet B4

Figure 14: Designation of the chiplets and daisy chain locations.

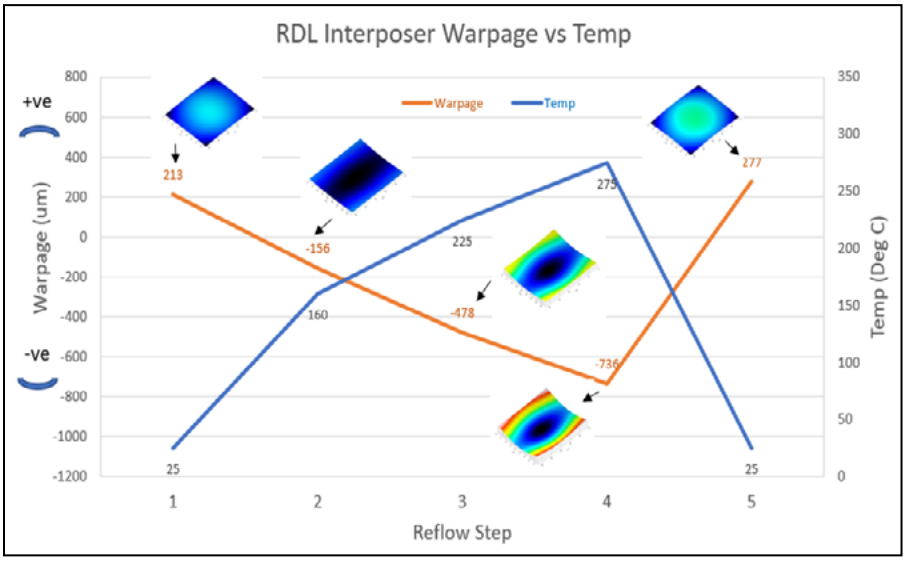


Figure 15: Package profile of an RDL interposer measured by Shadow Moiré at a key reflow temperature.

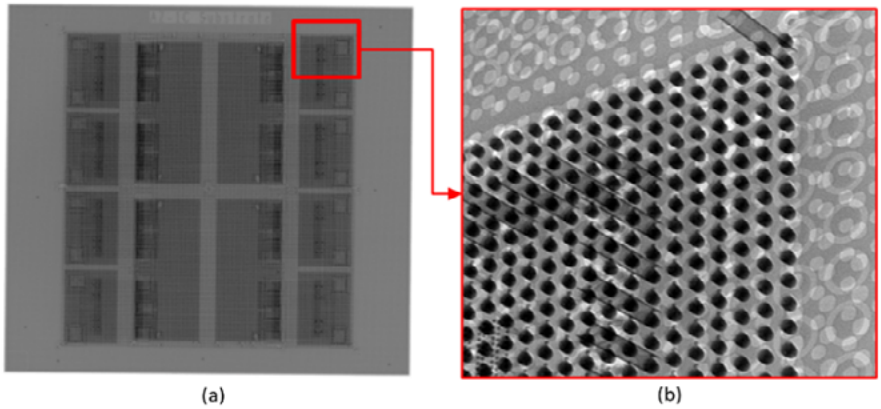


Figure 16: X-ray inspection of solder joints between the RDL interposer and the organic substrate: a) Plan view of the entire RDL interposer package; b) A magnified and tilted view of the solder joints.

the bond tool and pre-heated to 100°C to reduce the interposer warpage. Subsequently, the RDL interposer was aligned and gently pressed onto the organic substrate with a low bond force. The bond tool was then heated to a peak bond temperature of 300°C for a short duration and subsequently cooled down. During the cooling phase, the bond force was maintained to minimize the warpage of the RDL interposer. **Figure 11c** shows the RDL interposer successfully assembled to the organic substrate with the TCB process and X-ray inspection (**Figure 16**) shows good solder joint formation between the RDL interposer and organic substrate, showcasing the effectiveness of this method in addressing the RDL interposer warpage during package assembly.

The Shadow Moiré assessment of the assembled RDL interposer on the organic substrate displays a 380µm convex profile, surpassing the warpage outcomes of the unassembled RDL interposer package of 277µm (**Figure 17**). This elevated warpage is attributed to the CTE mismatch between the RDL interposer and the organic substrate materials. It should be noted that a metal stiffener frame is absent on the organic substrate used in the study. Incorporating a stiffener frame into the organic substrate is anticipated to alleviate the warpage results of the assembled RDL interposer package.

Summary

A large RDL interposer measuring 52 x 44mm was successfully fabricated using the RDL-first FOWLP process, accommodating 12 embedded chiplets. The fabrication process involved a 2-mask stitching process to produce the sizable interposer, with 6 layers of high-density RDL featuring 2µm L/S on a temporary carrier. Chiplets with micro-bumps were accurately placed on UBM bonding sites and soldered through mass reflow. X-ray inspection verified the alignment and successful solder joint formation between chiplets and RDL. The chiplets were then encapsulated with epoxy mold compound to complete the RDL interposer package. Electrical testing demonstrated good continuity

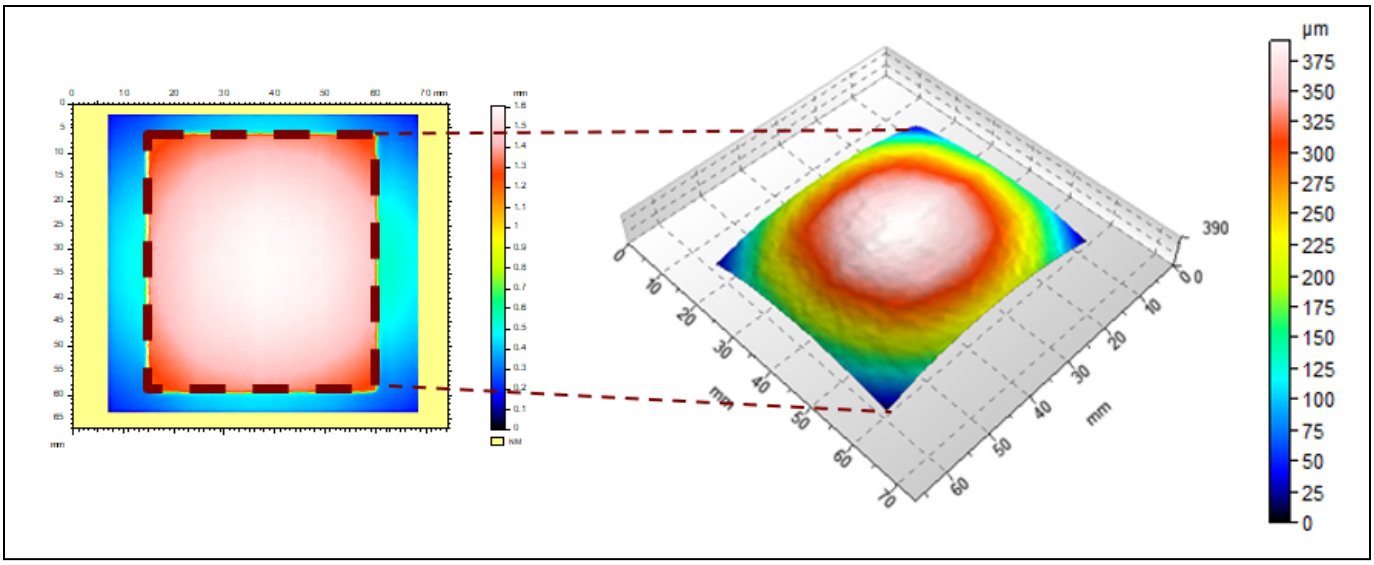


Figure 17: Shadow Moiré measurement of the assembled RDL interposer on an organic substrate.

in the stitched structure and low leakage current in the intra-layer RDL. A daisy chain connectivity test was also performed for the 12 chiplets, demonstrating good connectivity with the RDL layer. Shadow Moiré warpage measurement was carried out on the fabricated RDL interposer package revealed significant variations during temperature changes, prompting the implementation of a TCB process to mitigate warpage issues during assembly of the RDL interposer onto an organic substrate.

Acknowledgements

This research was supported by the Agency for Science, Technology and Research (A*STAR) under Centre of Excellence in Advanced Packaging 3.0 (Grant No I2101E0008). The authors would like to thank their colleagues: Sharon Lim Pei Siang, Eva Wai Leong Ching, and Jacob Jordon Soh for their support in the chiplets assembly, underfill and wafer-level molding process. Portions of this article were presented at the IEEE/EPTC2023 conference; the article was edited for publication in *Chip Scale Review.*

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Biographies

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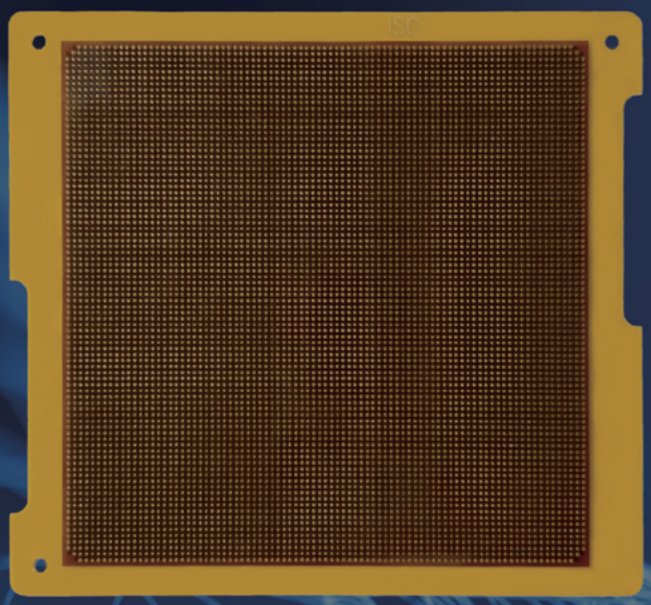

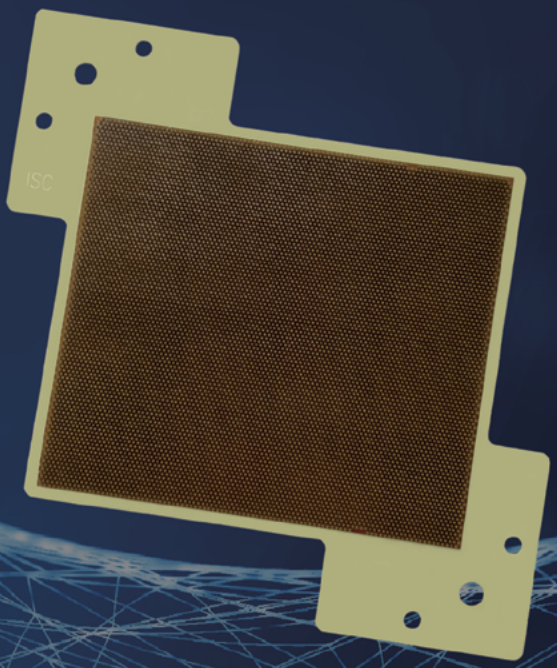

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Heterogeneous packaging: Optimizing performance and power consumption

By Jean-Charles Souriau [CEA-Leti]

Because of the increasing costs of advanced nodes and the difficulties of shrinking analog and circuit input-output signals (IOs), alternatives to single-die architectures are becoming mainstream. Chiplet-based systems using 3D technologies are compatible with scalable modular architectures, and with technology partitioning based on reusable intellectual property (IP) blocks. Moreover, 3D interconnects increase chip-to-chip bandwidth and limit overall power consumption. Industries across the whole range from automotive to high-performance computing (HPC) will soon be relying on advanced packaging to deliver simpler, faster, and cheaper chip designs that integrate more functions while offering greater performance and versatility.

The chiplet-on-interposer concept involves integrating a multiplicity of chips on the same silicon platform; it contrasts with large monolithic systems-on-chip (SoCs) platforms. The active interposer extends this concept by adding smart functions at the interposer level, such as complementary metal-oxide-semiconductor (CMOS) components. The interposer, thereby, becomes more than a simple interconnection platform; it provides the foundation for analog and low-power digital and photonic functions and increased 3D communication, especially with network-on-chip architectures.

In 2019, CEA-Leti and CEA-List presented the first CMOS active interposer measured on silicon, integrating power management and distributed interconnects to create an innovative scalable cache-coherent memory hierarchy. In this demonstration, six 28nm FD-SOI chiplets were 3D-stacked onto an active interposer in a 65nm process, to create a total of 96 cores [1].

To reduce the die-to-wafer (DTW) interconnect pitch, leading microelectronics manufacturers consider that direct hybrid bonding (HB), using mixed copper/oxide interfaces, will be essential for the success of future memory stacks, HPC, and to support the continued application of Moore's Law. Heterogeneous 3D integration has been identified as a way to increase functionality per unit area by optimizing space in the x, y and z directions. For over 10 years, CEA-Leti has been part of the French public Nanoelec Technological Research Institute ecosystem, gathering 22 partners from academic research institutions and industry [2]. Within this framework, to offer advanced packaging and HB solutions, we have teamed up with equipment manufacturers (SET, EVG, etc.) and adapted specific bonding processes—from pick-and-place technology to self-assembly (SA)—to improve yield and alignment accuracy. Today, we can bond chips from 1mm² × 1mm² to 10mm² × 10mm² by HB with interconnect pitches from 10µm to less than 5µm [3]. In addition, die spacing can be as low as 40µm. Current developments are focused on multi-stack DTW processes. We have demonstrated that signals and power supply from top-die circuits can be communicated to a substrate using through-silicon vias (TSVs) [4]. We are also working on new integration technologies such as SA. The advances made provide higher alignment performance (+/-200nm) and increased throughput (thousands of dies/h). Another key area of research relates to optimization of the temperature of the HB process, with the aim of preserving memory or active device performance.

To further improve data transmission during communication, we are contributing to the development of a disruptive approach to HPC: optical network-on-chip (ONoC) technology. Photons (light) have the potential to deliver fast on-chip communication for HPC, with increased bandwidth and reduced power consumption [5]. The main technological challenges faced by our architectural vision of an ONoC approach to chiplets were: 1) a scalable, low-profile interface between the chiplets and network; 2) decentralized routing to reduce data movement within the system; 3) thermal management compatible with optical communications; and 4) maintaining individual chiplet performance in multiple-chiplet integrations.

By tackling the issues noted above, we successfully co-integrated 3D interconnections and photonic devices using a newly demonstrated approach to form 10µm diameter by 100µm high TSVs through copper metallization inside a photonic chip [6]. Thermal insulation was improved by etching 40µm diameter backside cavities beneath the optical micro-rings, leading to a 70% reduction in the power required to tune the micro-rings. Moreover, we have shown efficient thermomechanical stress management of the thinned 100µm photonic interposer for assembly processes [7].

3D sequential integration makes it possible to achieve the best possible 3D contact densities between stacked tiers (<100nm pitch). This integration is attracting strong interest for more-than-Moore applications, such as CMOS image sensors with smart, scaled pixels, or mixed-signal applications where low-voltage analog and digital devices occupy separate levels, thereby allowing their independent optimization. The introduction of intermediate back end of line (iBEOL) between the stacked transistors will add to the variety of applications that this technology can address.

TSV: A key enabling technology for heterogeneous systems

In the framework of advanced dense interconnection, we have developed TSV processes since 2006, and consequently, we have the requisite experience to contribute to the design of new modules or system architectures. We started with the TSV-last process for CMOS image sensor applications that are still being optimized for new computed tomography X-ray scanners or detectors for advanced particle physics needs. We then worked on TSV mid-process for memory on logic, and afterwards on silicon interposers application to more recent high-density (HD) TSV for logic blocks interconnections combined with hybrid density, for example.

Each of the TSV developments noted above followed the same rigorous protocol, involving optimization of its electrical properties (resistance, leakage, capacitance) and qualification of reliability norms—at first using passive test vehicle integration, and then moving to active wafers (sensors, power or computing technologies). In 2023, we presented results on the TSV process with an aspect ratio of 10:1, i.e., with a diameter/space of 1µm/1µm (pitch 2µm) associated with a depth of 10µm; this application was for HD copper TSVs for use in advanced imaging applications or further backside power-delivery network architectures for nano TSVs.

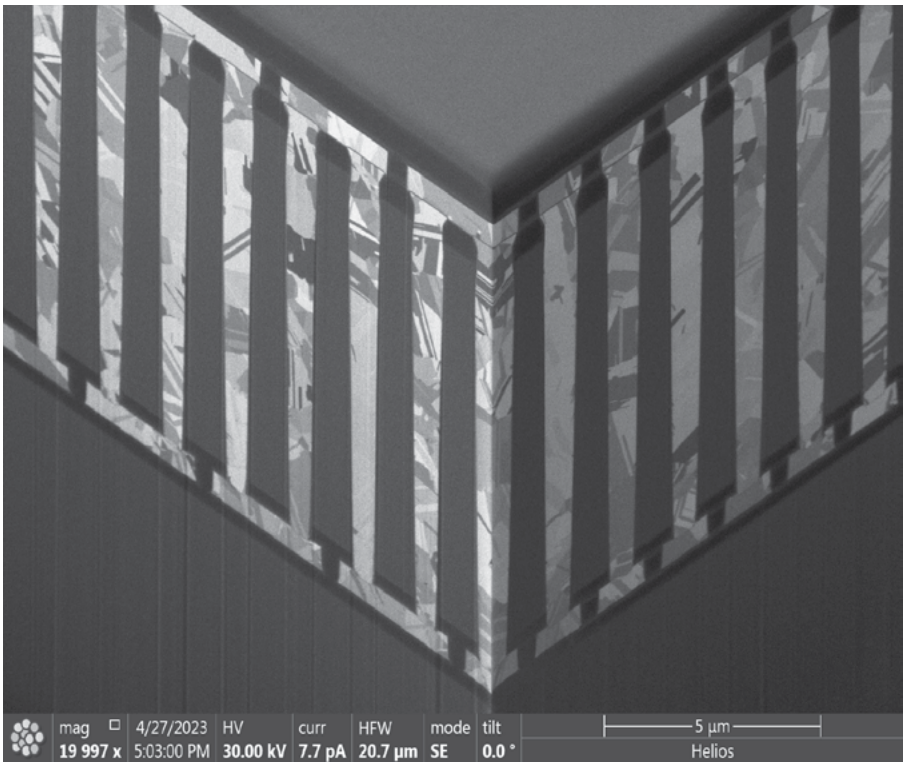

Figure 1: Field higher beam cross section of a HD TSV (Ø=1µm H=10µm) daisy chain. SOURCE: CEA-Leti/R. Vélard

A test vehicle consisting of a single metal level on each side of a thinned silicon (Si) substrate bonded to a thick carrier was produced to develop and optimize the process flow, ensuring that it would be compatible with the constraints of the subsequent HB process. Electrical resistance measurements revealed a median value of 0.7Ω on Kelvin patterns, with a 100% yield achieved on 10,000-TSV daisy chains. Remarkably, no failures were recorded during extensive reliability testing, including 2,000 hours of high-temperature storage (HTS) at 150°C, and 2,000 thermal cycling test (TCT) cycles between -55°C and +150°C [8]. These results, shown in **Figure 1**, are a major milestone for very highly-integrated architectures based on multiple-

layer wafer-to-wafer integrations. Emerging data will be the subject of a forthcoming conference presenting even more integrated TSVs landing on aggressively thinned metal 1, to mimic the integration of 22nm or smaller nodes.

Active interposers: Enhancing photonic and HPC applications

From an architectural point of view, our interest in interposers started in 2010 with the development of large passive interposers [9]. Since then, this theme has followed its own roadmap alongside developments in advanced HPC, requiring increased bandwidth, reduced latency and greater power efficiency. From passive interposers, the technology has moved to active interposers including active 3D links and embedded DC-DC (direct current) converters for pinpoint power delivery. It has finally matured for use in photonic interposers, making it possible to overcome the latency wall that emerges with increasing chip-to-chip distances even with these on-chip architectures. For each of these approaches, dedicated technological developments were required, starting from passive interposers with integration of the first 10µm diameter by 100µm high TSV [6]. The absence of devices on the substrate meant that less emphasis was required on thermal oxidation and planarization or metallic contamination of active parts, which facilitated TSV integration.

Moving to an active interposer, the compatibility with the production fab for BEOL completion represented a real challenge in terms of copper protrusion from TSVs, or other defects. These have been tackled thanks to the increased maturity of the TSV filling and annealing processes, combined with systematic close inspection of each TSV in the closed loop by industrial process teams to determine optimal process points. These developments related to photonic interposers represent a real breakthrough in terms of interconnections, as mentioned, and demonstrate the convergence of the photonic and 3D integration roadmaps.

The TSV aspect ratio and the metallization process have remained almost unchanged since the first integration, but the inclusion of a 2µm thick buried oxide (BOX) to avoid parasitic coupling between waveguides and the underlying silicon was a real challenge. First, the TSV etching was fully redeveloped to produce smooth sidewalls for later metallization and to eliminate the silicon etching below the BOX; then, the thermomechanical deformation of the thin substrate due to the thick BOX had to be compensated by balancing all the between-layer stresses linked to frontside and backside interposer integration. These adjustments were mandatory for the assembly of the top dies of the Popstar photonic interposer demonstrator (**Figure 2**) hosting four computation chiplets and six electro-optical driver chips. The successful TSV integration in this photonic interposer was demonstrated by assessing the electrical yields and electro-optical performances of TSV chains [10]. The first functional intermediate demonstrators have just been assembled (**Figure 3**). This study contributes to the ongoing progress in computing systems, particularly in the realm of HPC, by providing insights and solutions to integrate optical communication technologies within a heterogeneous computing architecture.

By combining 3D integration with mid-process TSV and advanced packaging, based on small-pitch flip chips and optic fiber pigtailing, heterogeneous integration of a photonic device on a silicon interposer was achieved. This represents the functional demonstration of the next generation of beam steering for a light detection and ranging (LiDAR) designed for autonomous vehicle driving. **Figure 4** shows integration of the flip chip in an optical phase array (OPA) generating the laser beam scanning a silicon interposer, thanks to a 10µm TSV and 40µm pitch

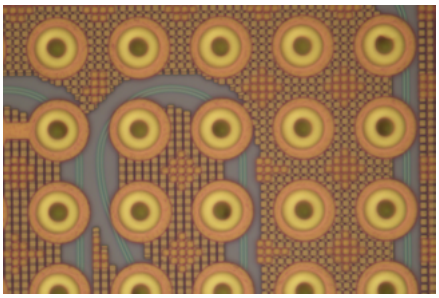

Figure 2: Photonic waveguides and micro bumps on a Popstar Interposer.
SOURCE: CEA-Leti/J. Charbonnier

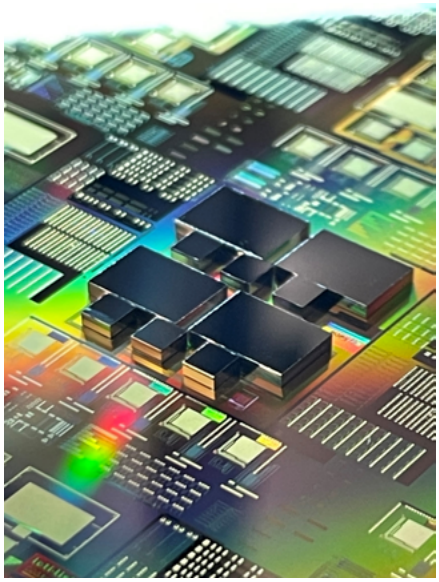

Figure 3: STARAC frontside module: Popstar photonic interposer, 4 chiplets and 6 electro-optical drivers in 28nm FD-SOI.
SOURCE: CEA-Leti/R. Franiatte

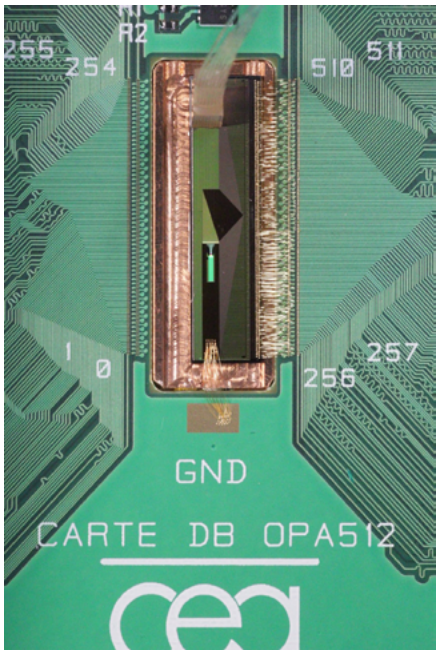

Figure 4: Solid-state optical phase array photonic device for an autonomous vehicle driving light detection and ranging (LiDAR) packaged device using a mid-process TSV and a fine-pitch flip-chip process on a silicon interposer.
SOURCE: CEA-Leti/ N. Miloud-Ali

copper pillar. The 256 channels of the OPA are wire bonded to a printed circuit board (PCB) and an 8-channel fiber array is connected to deliver the laser beam. The system is fully functional and complies with advanced driver assistance systems (ADAS) specifications for beam scanning angles, divergence and power consumption [11].

Hybrid bonding: A solution for heterogeneity

Hybrid bonding is a maturing technology in advanced fabs that is essential to the emergence of 3D devices. This technology is similar to direct bonding, but is applied to mixed Cu/dielectric surfaces to create an electrical interconnection between two parts. Direct bonding is quite distinct from thermocompression and adhesive bonding, which require temperature and pressure, or additional materials such as polymer, respectively, to ensure contact between the two surfaces. Following stringent surface preparation—i.e., topography and cleanliness—direct bonding is spontaneous, requiring no external loading.

HB is particularly suitable for interconnection densities with pitches from 0.5µm to 10µm. The race to achieve higher interconnection densities is the main driver on the HB development roadmap for HPC or imaging applications [12]. However, HB is also more reliable and results in a thinner total stack compared to micro-bumps, which are used in automotive applications and high-bandwidth memory applications.

HB has matured enough to have entered mass production, especially for stacked image sensors in its wafer-to-wafer version. Devices with two-die stacks are available on the market, and advanced research on three-die stacks are advancing well. Die-to-wafer (DTW) hybrid bonding will dramatically enhance designer creativity as several advanced technology nodes and substrates can be assembled on a single interposer to produce heterogeneous 3D (**Figure 5**).

For future research on HB, the development of low-temperature processes will be key to addressing technologies with a low thermal budget. For example, SA is being explored, as are horizontal die-to-die interconnections by HB [13]. In the latter context, interposer or bridges should make it possible to overcome stepper limitations.

3D sequential integration: Optimizing 3D contact densities

The strategy adopted at CEA-Leti to introduce iBEOL between sequentially stacked tiers introduced the following new challenges: 1) a limitation of the top CMOS field-effect transistor (FET) thermal budget process to 500°C, and 2) the need to ensure a safe return to only front end of line (FEOL) contamination when processing the top transistor. **Figure 6** shows the recent demonstration of one such integration [14]. Above a standard industrial 28nm fully-depleted silicon-on-insulator (FD-SOI) platform including four Cu/ultra low-k (ULK) dielectric metal levels, the top CMOS device

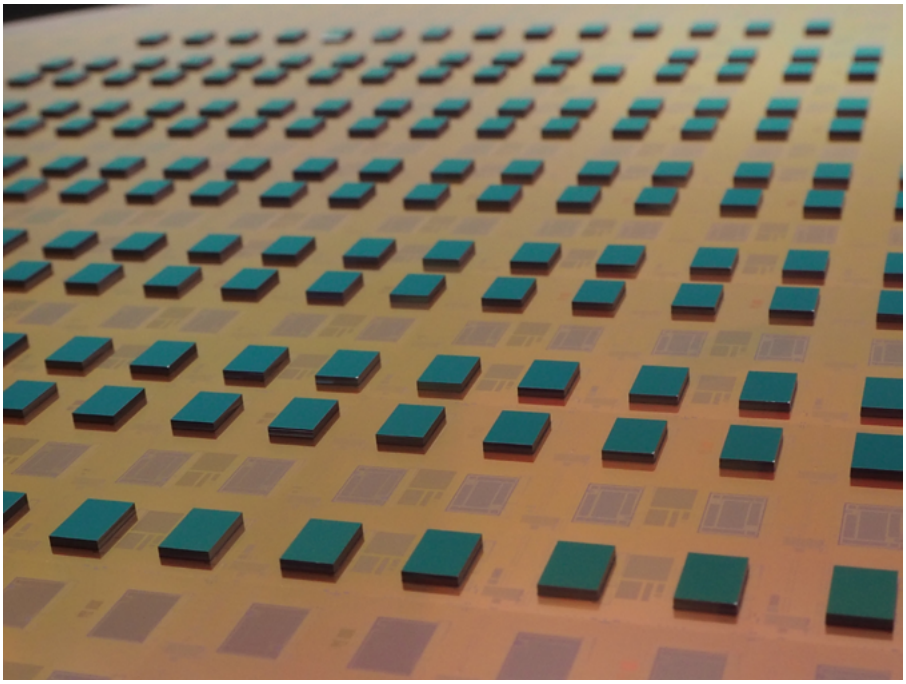

Figure 5: Die-to-wafer hydrid bonding. SOURCE: CEA-Leti/L. Sanchez

layer was fabricated within a 500°C thermal budget. A new Bevel Wrap Contamination module was introduced to allow a safe return in a FEOL contamination before proceeding with direct bonding of the top channel and full device processing in a FEOL clean room with state of the art 300mm tools. The CMOS FD-SOI top devices produced showed performance levels similar to those of high-temperature FD-SOI devices. The demonstrations of a ring oscillator and a high dynamic range (HDR) pixel, which are firsts, take 3D sequential integration to the next level in terms of maturity.

We envision 3D sequential integration in the fields of scaled and smart imagers, radio-frequency (RF) applications and highly efficient computing. The toolbox developed includes low-temperature devices with digital (<1V) and analog units of merit (>2.5V) fabricated at low temperatures on monocrystalline channels, with the goal of achieving

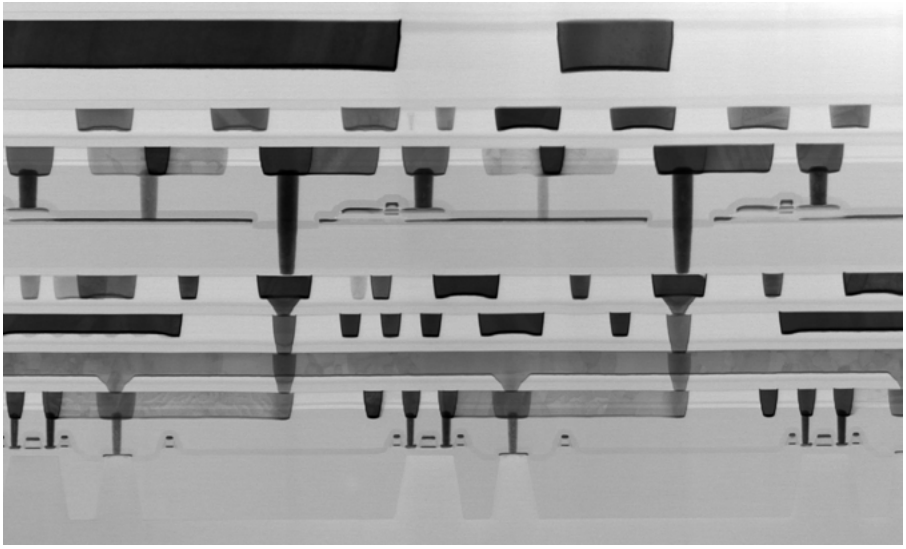

Figure 6: Transmission electron microscopy (TEM) cross section of the 2-CMOS layer stacking including iBEOL with Cu/ULK 28nm. SOURCE: CEA-Leti

fabrication of top-quality devices at low temperatures without limiting performance compared to traditional high-temperature CMOS devices. This capacity would be useful across a wide range of applications.

Advanced packaging: Toward a European 3D strategy

Future HPC, artificial intelligence (AI), image sensors, smart displays, etc., will be based on advanced packaging and 3D integration of components in increasingly complex architectures. The United States is at the forefront of this trend thanks to concrete examples from NVIDIA, AMD, and Intel. Strong competition also exists in Asia between giant players like TSMC and Samsung. Europe must reduce the gap with the U.S. and Asia, who are investing heavily in this advanced packaging and 3D. Indeed, performance improvements in the latest semiconductor nodes will not be sufficient to deal with the needs of emerging applications (e.g., generative AI). Advanced packaging is an alternative path allowing chips fabricated using different technologies to be combined to optimize performance and cost of the final "chip" assembly.

Summary

CEA-Leti is pursuing its historical interests in heterogeneous integration and 3D, and developing an ambitious roadmap for system and technology co-optimization. To support European ambitions for the semiconductor industry, we have also established partnerships with other European research and technology organizations (RTOs), like imec, Fraunhofer Institute, and Tyndall. As part of this, CEA-Leti has joined PREVAIL, the multi-hub Test and Experimentation Facility for edge AI hardware [15]. In addition to technological developments, we are also addressing environmental challenges through life-cycle assessments of technologies, low-power systems enabled by 3D, exploration of chip re-use, etc.

Acknowledgment

This work was partly supported by the French National program "IRT Nanoelec, n° ANR-10-AIRT-05 and by European Union's H2020 under the grant agreement n 958472 (Tinker) and n 780548 (3D-MUSE). This work is part of the IPCEI Microelectronics and Connectivity and was supported by the French Public Authorities within the frame of France 2030.

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Biography

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Cu-Cu hybrid bonding for high-bandwidth memory (HBM)

By John H. Lau [Unimicron Technology Corporation]

Hybrid bonding has achieved quite a bit of traction recently. For example, the 2023 IEEE Electronic Components and Technology Conference (ECTC) featured more than 80 papers related to hybrid bonding. In [1,2], it was mentioned that Cu-Cu bumpless hybrid bonding, i.e., so-called direct-bond interconnect (DBI), was invented by the Research Triangle Institute (RTI) in the U.S. [3-6] around 2000. At about the same time, Suga and his colleagues in Japan proposed a similar technology called room-temperature bumpless direct bonding [7-10]. DBI has been in very high-volume manufacturing since 2016 by Sony on its complementary metal-oxide-semiconductor (CMOS) image sensors (CIS) [1,2,7,8], and since 2021 by Yangtze Memory Technologies Company Ltd. (YMTC) on its 3D NAND flash memory [1,2,7,8].

The brief fundamentals and recent advances and trends of Cu-Cu bumpless hybrid bonding from the IEEE/ECTC 2022 papers and IEEE/ECTC 2023 papers have been reported, respectively in [1,2] and [7,8]. The recent advances and trends of Cu-Cu hybrid bonding for high-bandwidth memory (HBM) will be discussed in this technology review.

Samsung's hybrid bonding for HBM

During IEEE/ECTC (May 30-June 2, 2023), Samsung published at least 6 papers on hybrid bonding. In [11], they presented a multi-stack hybrid Cu bonding (HCB) technology development using ultra-thin chips. As mentioned in [2], Samsung has been in production for 3D-IC integration of its high-bandwidth memory (HBM) by flip-chip high-bonding force thermocompression bonding (TCB) of the C2 (Cu-pillar with solder cap or µbump) TSV (through-silicon via) chips with nonconductive film (NCF). **Figure 1a** schematically shows the 16H multi-stack using the flip-chip TCB solder reflow method. It can be seen that there are joint gaps between the chips. However, with HCB, the chips are bumpless and the Cu-pad to Cu-pad pairs are bonded with die-to-wafer (D2W) and die-to-die (D2D) methods [1,2,7,8]. **Figure 1b** schematically shows the 16H multi-stack using the HCB method. It can be seen that the total package thickness is smaller than the one using the TCB

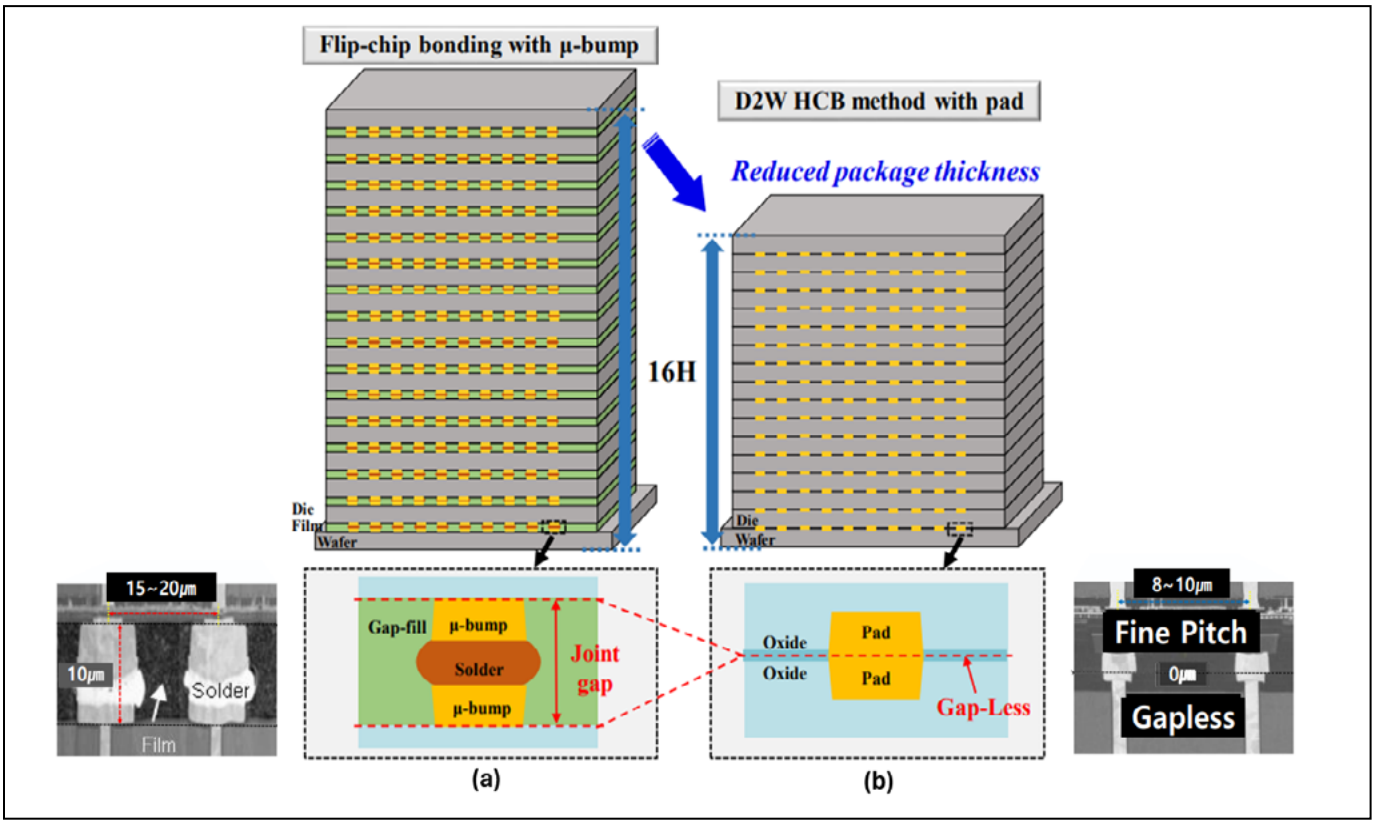

Figure 1: 16H HBM structure: a) Flip chip with microbump solder reflow with joint gap; b) D2W/D2D Cu-Cu hybrid bonding with gapless joint. SOURCES: [7,11]

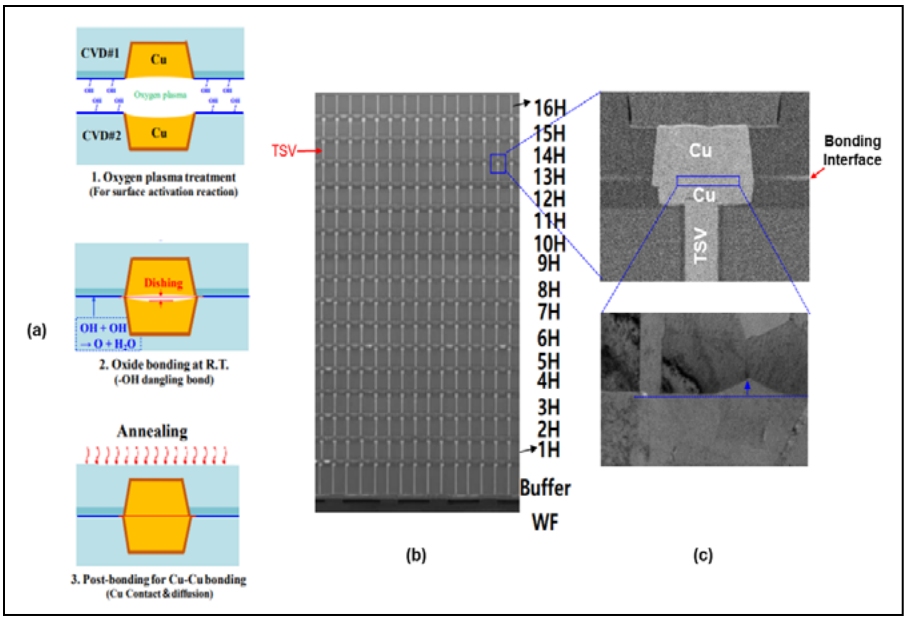

Figure 2: a) Key hybrid bonding process; b) 16H HBM structure; and c) SEM image of the Cu-Cu interface showing recrystallized Cu grains across the bonding interface. SOURCES: [7,11]

solder bumped flip-chip method and there is no gap (i.e., gap-less) between the chips.

The HCB mechanism is shown in **Figure 2a**. Chemical-mechanical polishing (CMP) is conducted for the bonding surface of the core memory die after dicing and the buffer wafer. Plasma processing on the passivation surface creates an activation state and generates the hydroxyl group (OH) when deionized (DI) water is sprayed onto the surface. Then, the chip is picked and aligned with the wafer (D2W), and the pressure applied for joining generates bindings among the oxides. These methods are repeated to stack several core memory dies as D2D layers. After pre-bonding is completed by stacking the layers, the bond between oxides is strengthened by high-temperature annealing; the Cu pads of the top and bottom plates expand and meet, electrically connecting as Cu diffusion occurs. **Figure 2b** shows the scanning electron microscope (SEM) image of the HCB 16H stacking HBM package. **Figure 2c** shows the following: 1) there are no voids at the interface, and 2) the Cu diffusion and grain growth at triple points was observed at the Cu interface.

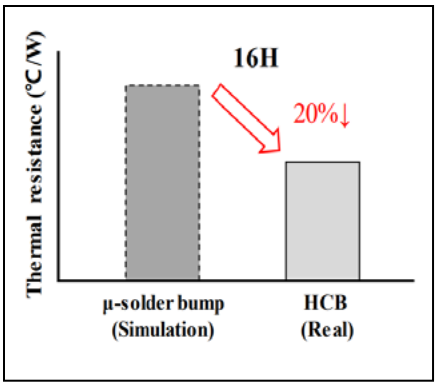

Figure 3: Thermal resistance in 16H HBM structure: conventional flip chip vs. HCB. SOURCES: [7,11]

One of the challenges of HBM is thermal management. Because there are no gaps between the chips, the vertical thermal resistance of the 16H HBM with the HCB is 20% lower than that for the flip-chip case with gaps for the μbumps and underfill (NCF) as shown in **Figure 3** [11].

At ECTC 2023, Samsung published another paper on thermal improvement of HBM with joint thermal resistance reduction for scaling 12 stacks and beyond [12]. The authors stated that there are two factors affecting the HBM temperature: 1) internally (HBM itself), thermal resistance, power magnitude and map (distribution), and temperature sensor location; and 2) externally (system), cooling performance, graphics processing unit (GPU), application-specific integrated circuit (ASIC), central processing unit (CPU) power, and system-in-package (SiP) structure. In [12] their focus is on the inside of HBM and dealing with thermal resistance improvement methods such as HCB.

Figure 4 shows the simulation results on joint thermal resistance with arbitrary units (A.U.) vs. joint gap thickness for mass reflow (MR)-molded underfill (MUF), TCB-NCF, and HCB. MR-MUF and TCB-NCF have been discussed in chapter 1 of [8]. It can be seen from **Figure 4** that: 1) the joint thermal resistance is the lowest for HCB; 2) the joint thermal resistance is highest for MR-MUF; 3) the reduction of joint thermal resistance from MR-MUF to TCB-NCF is 35%; and 4) the reduction of joint thermal resistance from MR-MUF to HCB is more

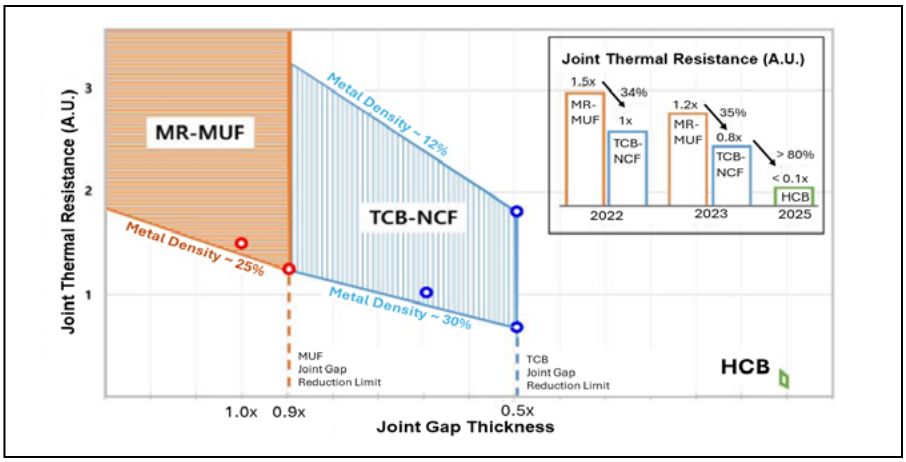

Figure 4: Joint thermal resistance of MR-MUF, TCB-NCF, and HCB. SOURCES: [7,12]

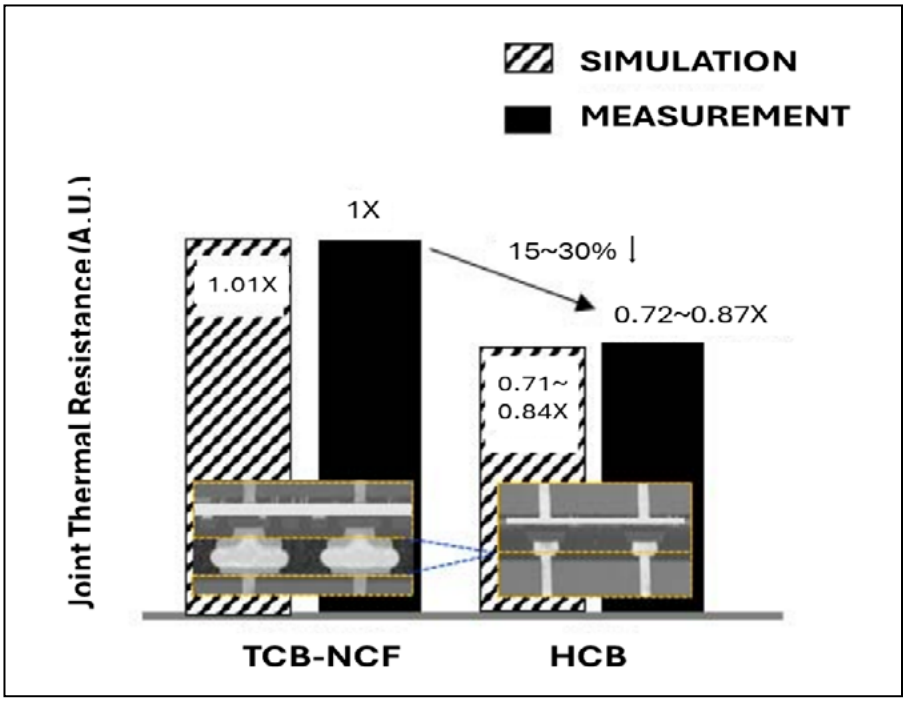

Figure 5: Measured and simulated stack thermal resistance of HBM with TCB and HCB. SOURCES: [7,12]

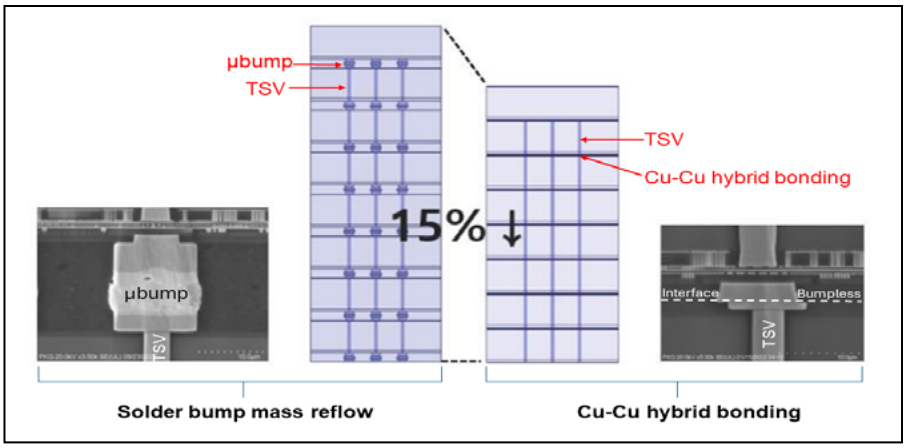

Figure 6: Comparison between a solder-bumped flip chip and hybrid bonding interconnect. SOURCES: [7,13]

than 80%. Again, this is because of the thinner packaging enabled by HCB; additionally, there are no Cu-pillar with solder cap and underfill/NCF structures, which increase the thermal resistance.

Figure 5 shows the simulation and measurement results of the 16H HBM package with the HCB and TCB-NCF methods. It can be seen that: 1) the simulation and measurement results correlate very well (more than 95% matched); and 2) the stack thermal resistance fabricated with the HCB is 15~30% less than that with the TCB-NCF.

SK Hynix's hybrid bonding for HBM

During IEEE/ECTC 2023, SK Hynix presented at least one paper on a chip-to-wafer (C2W) hybrid bonding interconnect technology for higher density and better thermal dissipation of HBM [13]. The paper's focus is on the demonstration of a 8Hi-HBI (hybrid bonding interconnect) with C2W multi-stack HBM as shown in Figure 6. It can be seen that comparing with the solder-bumped mass reflow method (chapter 1 of [8]), the thickness of the HBM package can be reduced by 15% with the Cu-Cu bumpless HBI method.

Plasma treatment is a key process step for preparing the bonding surface that makes oxide bonding at room temperature with CMP in HBI. The authors consider three different kinds of plasma conditions, namely, A, B, and C. Figure 7 shows the bonding strength and scanning acoustic microscopy (SAM) images of samples under plasma conditions A, B, and C after end-of-line and reliability testing. It can be seen that plasma condition B yields the highest bonding strength that is measured by the Maszara test in wafer-to-wafer base. The annealing temperature is 200ºC. There is no void after the end of line. However, there are voids after the reliability test.

Thermal resistances of MR+MUF (8Hi) and HBI (8Hi) structures with different pad densities are shown in Figure 8. It can be seen that: 1) for the same pad density (20%), the thermal resistance of the HBI (8Hi) is 22% lower than that of the MR+MUF (8Hi); and 2) the thermal resistance of the HBI (8Hi) (with 8% pad density) is 13% lower than that of the MR+MUF (8Hi) (with 20% bump density).

Micron's hybrid bonding for HBM

During ECTC 2023, Micron published at least one paper on critical challenges with copper hybrid bonding for C2W memory stacking [14]. Figure 9a shows a conventional stacking of TSV-dies with µbumps solder reflow method for HBM. The µbump pitch can go down to 20µm. However, with hybrid bonding, the Cu pad pitch can easily go down to 10µm and there is no bump, i.e., bumpless as shown in Figure 9b. Figure 9c shows the electron backscatter diffraction (EBSD) across the bonding interface where two Cu pads are joined together. Due to Cu-to-Cu diffusion, these two Cu pads become one with the Cu crystal

growth occurring across the bonding interface. However, there are some challenges of hybrid bonding for HBM as pointed out by Micron [14] and are discussed below.

Particles generated by conventional wafer dicing. Figure 10 shows the particle counts before and after a laser stealth dicing, classifications of dicing particles, and signatures of particles. Micron found that laser stealth dicing (Figure 10b) generated far more particles than that allowed by a Cu hybrid bonding process (Figure 10a)—an increase by 7x. The dicing particles can be classified as inorganics such as silicon dust (Figure 10c), and organics such as tape residues (Figure 10d). Both of them have different impacts on void formulation at the bonding interface. The signature of particle impacts on voids are circular shaped as shown in Figure 10e, and as shown in Figure 10f, circular shaped attached with a comet tail due to the bonding wave influence [14]. Both organic and inorganic particles are harmful, but inorganic ones will generate a much bigger void compared with organic ones.

Particle mitigation by combination laser grooving and plasma dicing. Figure 11a shows a typical memory scribe design with five dielectric films. Micron proposed a combination of laser grooving plus plasma etching to achieve an optimum balance between the dicing quality and a reasonable throughput. By doing this, an innovative cleaning method to successfully remove the debris and dust (due to lasering) before plasma etching was developed and the effects are shown before cleaning in Figure 11b, and post cleaning in Figure 11c. The post-wafer dicing and cleaning images at saw streets are shown in Figure 11d at the wafer center, and in Figure 11e at the wafer edge. The overall particle counts are shown in Figure 11f; Figures 11b-f show that the saw streets are clean, and the particle counts are significantly reduced.

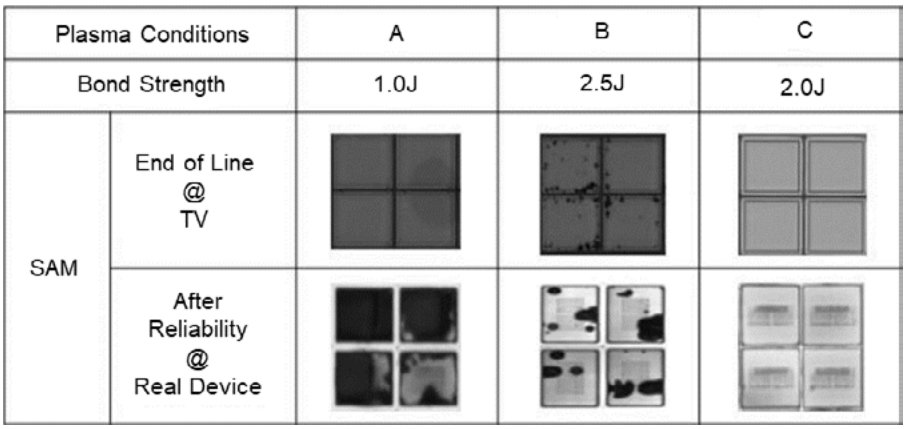

Figure 7: Bonding strength and SAM images of samples under plasma conditions A, B, and C after end-of-line and reliability testing. SOURCES: [7,13]

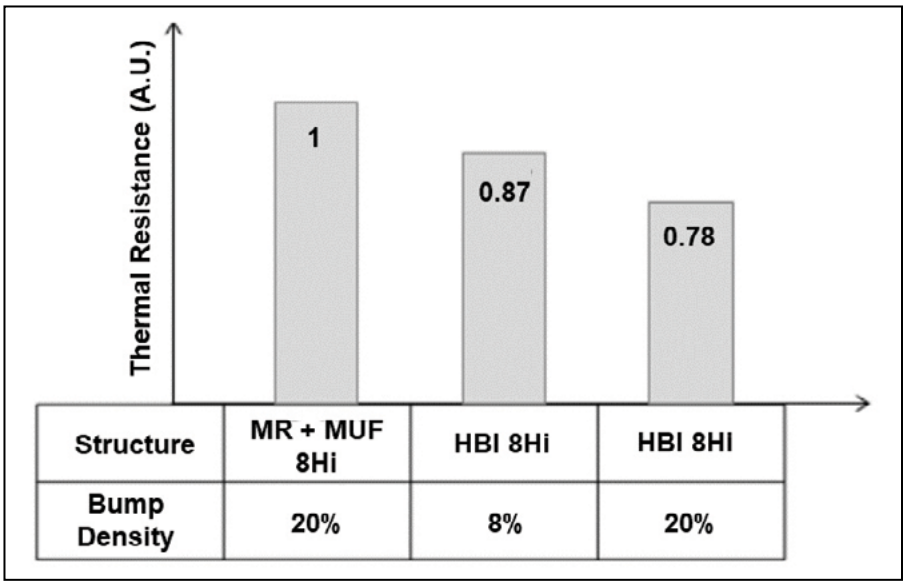

Figure 8: Thermal resistance comparison according to different structures (MUF vs. HBI). SOURCES: [7,13]

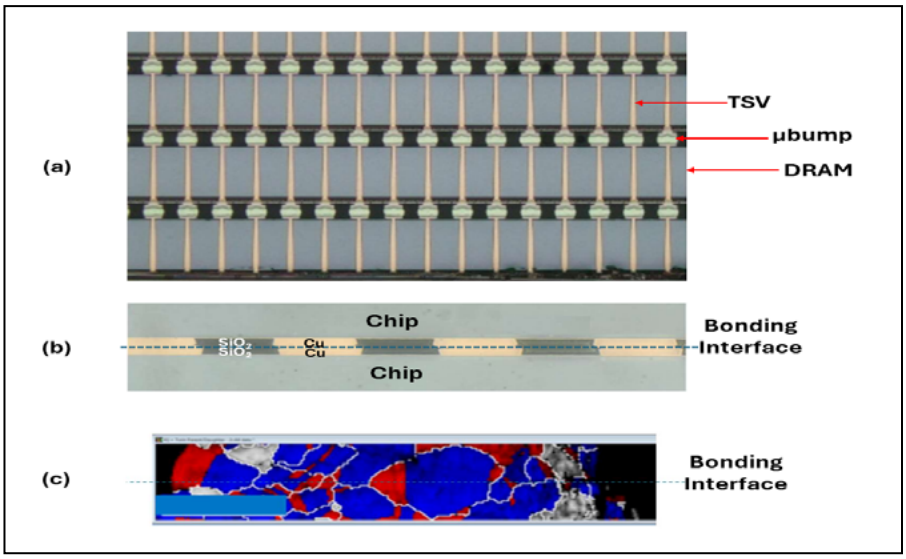

Figure 9: a) HBM with flip-chip solder reflow (20µm pitch); b) HBM with hybrid bonding; and c) Cu crystal growth across the bonding interface. SOURCES: [7,14]

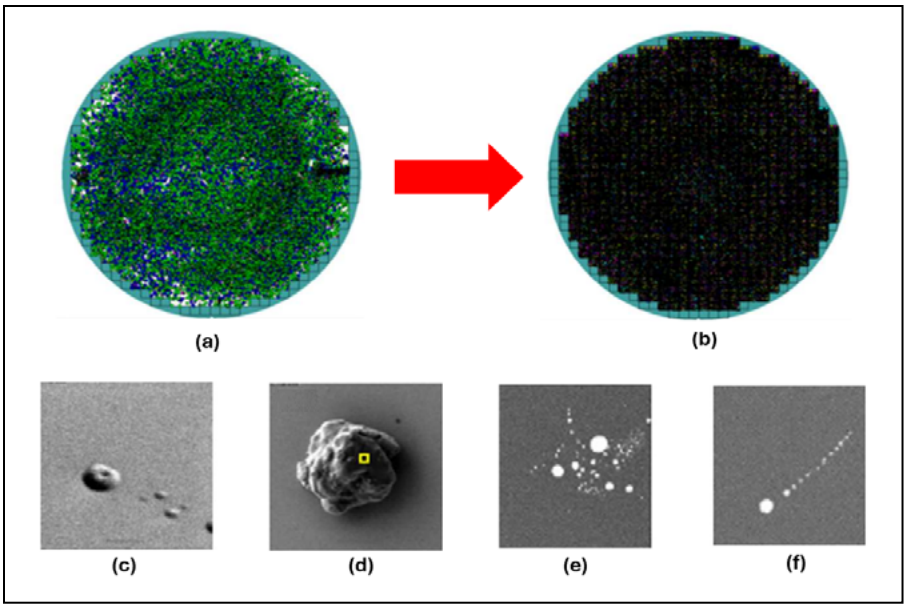

Figure 10: Particle counts: a) After post-debond clean (particle counts = X); b) After laser stealth dicing, GPTC wet clean (particle counts = 7X); and Classifications of dicing particles: c) inorganics, and d) organics; and Signatures of particle-induced voids: e) clusters, and f) comet tails. SOURCES: [7,14]

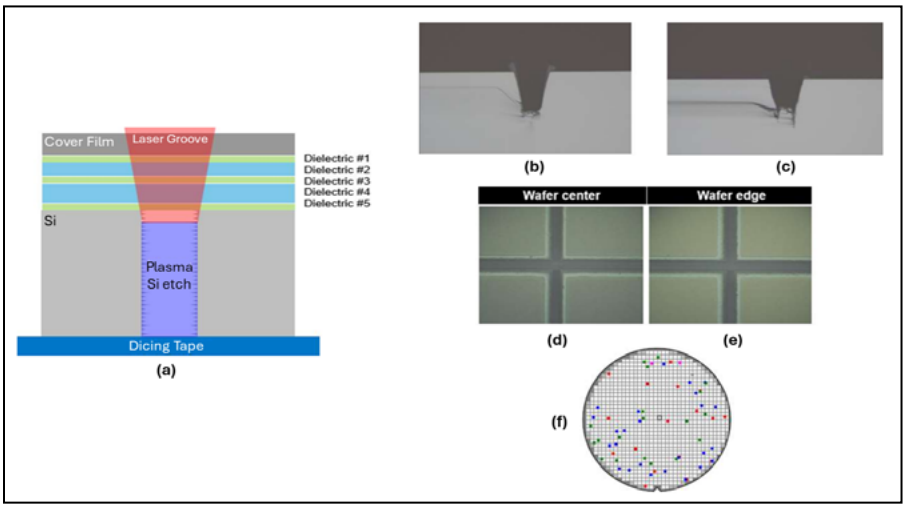

Figure 11: a) Wafer dicing by laser grooving and plasma etching. Innovative cleaning to remove the laser grooving induced edge burrs and Si dust: b) before- and c) post-cleaning. Post-wafer dicing images at saw streets at d) the wafer center; at e) the wafer edge; and f) overall particle counts. SOURCES: [7,14]

Summary

Some important results and recommendations are summarized as follows:

- The thickness, weight, thermal resistance, and electrical performance of HBMs with hybrid bonding are, respectively thinner, lighter, smaller, and better than that with the conventional flip-chip solder reflow.
- All the producers of HBMs—SK Hynix, Samsung, and Micron—are working on hybrid bonding. It is expected that high-volume manufacturing of HBMs with hybrid bonding could happen in 2025.
- Most of the HBMs with hybrid bonding are by C2C/C2W methods. Two of the most significant challenges are the flatness and cleanness of the oxide surface of the chips so after they are stacked, the oxide-to-oxide of all the chips can be bonded at room temperature (RT) with minimum-to-no voids/seams before annealing all the chips at once at a high temperature.
- HBMs with hybrid bonding is a 3D-IC integration packaging method. 3D NAND flash memory is a 3D monolithic manufacturing method within the chip. As mentioned in [1,2], Yangtze Memory Technologies Company Ltd. (YMTC) has been manufacturing its 3D monolithic NAND using the hybrid bonding method within the chip (not the package) since it licensed the Xperi (now Adeia) Cu-Cu hybrid bonding technology on October 12, 2021.
- Just like the 3D NAND, 3D DRAM is a 3D monolithic chip manufacturing method, which is a very hot topic today. With respect to the research and development results, such as patents (as late as October 2022) on 3D monolithic DRAMs, Micron (30) is leading Samsung (15) and SK Hynix (10). Recently, Samsung and SK Hynix have been diligently working on 3D DRAM.
- Just like the 3D NAND by YMTC, hybrid bonding can also be combined with the 3D DRAM monolithic manufacturing within a chip. In order to enforce this area, Micron licensed the Cu-Cu hybrid bonding technology from Adeia on February 23, 2022. 3D DRAM with hybrid bonding within a chip product could be shipped before 2030.
- As of today, Cu-Cu hybrid bonding is applied to the silicon chip to silicon chip or substrate. Since the announcement (September 18, 2023) of Intel's glass interposer (substrate) for supporting its one trillion transistors on a processor chip (scheduled to be shipped by 2030), the research and development of silicon chip on glass substrate such as the preparation of dielectric for oxide-to-oxide RT bonding and Cu dishing for Cu diffusion during annealing bonding should begin now.

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Biography

John H. Lau is a Senior Special Project Assistant at Unimicron Technology Corporation, Taoyuan City, Taiwan (ROC). He has more than 40 years of R&D and manufacturing experience in semiconductor packaging, 528 peer-reviewed papers (a principal investigator on 380), 50 issued and pending U.S. patents (a principal inventor on 34), and 23 textbooks (first author on all). He is an ASME Fellow, IEEE Fellow, and IMAPS Fellow. He earned a PhD degree from the U. of Illinois at Urbana-Champaign. Email John_Lau@unimicron.com

ECTC 2024: New, larger venue

By Michael Mayer [University of Waterloo, and 74th ECTC Program Chair]

It is my pleasure to invite you to the 74th IEEE Electronic Components and Technology Conference (ECTC) Program, which will be held from May 28–31, 2024, for the first time in the Centennial state, Colorado, at the Gaylord Rockies Resort and Convention Center in Denver. On behalf of the ECTC's Executive Committee and Program Committee, I welcome our colleagues from all over the world to this IEEE/EPS sponsored event.

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ECTC is the premier international conference in electronics packaging technology. Electronics packaging for microchips increasingly plays a pivotal role throughout the microelectronics production chain covering the function of microchip protection and allowing for increasingly complex and powerful systems. As microchips continue to evolve, their electronic packaging safeguards against premature failures and contributes to the overall durability and performance of all electronic devices, ensuring the microchips remain in their pristine shape for many years. To this end, ECTC covers a broad range of topics, including components, materials, assembly, reliability, modeling, interconnect design and technology, direct bonding and hybrid bonding, device and system packaging, heterogeneous integration, wafer-level packaging, photonics and optoelectronics, Internet of Things (IoT), 5G, quantum computing and systems, 2.5D and 3D integration technology, and other emerging technologies in electronics packaging.

The ECTC Program Committee comprises 200+ experts from diverse technical fields and is dedicated to creating an engaging technical program. ECTC regularly draws over 1,500 attendees from 20+ countries. The 73rd ECTC was held in person and welcomed 1,619 registered attendees from 26 countries. It featured 369 technical papers presented in 36 oral sessions and five interactive sessions, including a student-focused session. Additionally, nine special sessions covered various topics with respect to advanced packaging for harsh environments, hybrid bonding, high-density substrates, quantum computers, next-generation communication systems, photonics, as well as topics in workforce diversity and the CHIPS Act initiative. The Technology Corner Exhibits showcased products and services from 117 companies. The 73rd ECTC received valuable support from our awesome sponsors.

At the 74th ECTC Conference we plan to uphold ECTC's tradition as the premier platform to showcase the latest developments in the electronic components industry, where packaging drives device and system performance.

The 74th Electronic Components and Technology Conference (ECTC) promises an extensive technical program, featuring over 375 technical papers presented across 36 oral sessions and five interactive presentation sessions. Key topics span advancements in packaging technologies, heterogeneous integration, systems design, and next-generation substrate manufacturing. Reliability aspects cover advanced substrates, high-density packages, and harsh environment reliability, while assembly and manufacturing technology sessions delve into 3D integration, bonding, and die bond/board-level reliability. RF, high-speed components, and systems topics include antenna-in-package design, signal integrity, and chiplet interconnect validation; and emerging technologies sessions explore digital healthcare, AI, quantum computing, and additive manufacturing for printed electronics.

This year, hybrid bonding features prominently at ECTC. Hybrid bonding is a cutting-edge packaging technology that promises to achieve the benefits of heterogeneous integration using innovative techniques for direct-joining processes. Hybrid bonding plays a role in achieving enhanced reliability in advanced substrates and interconnects, including copper hybrid bonding for various applications. These sessions delve into the materials and processes driving the evolution of hybrid bonding in microelectronics.

Photonics takes center stage at ECTC with sessions like "Co-Packaged Optics," "Optical Interconnections," and "Photonics Integration, Materials, and Processes." These sessions explore the transformative role of photonics in microelectronics packaging, exploring the integration of optical components within semiconductor packages, optimizing communication within electronic systems, advancing data transmission through light, addressing signal integrity challenges, advanced materials and processes, all aiming at enhanced communication bandwidth and system efficiency, paving the way for even more energy-efficient and high-performance microelectronic devices.

Special sessions with industry experts include a focus on Industry-Government Co-Investments for the Advanced Electronics Sector globally, advancing metrology for next-generation microelectronics, and innovative solutions for power-hungry AI/ML applications in a session on Thermal Management for AI. An RF Packaging session above 100 GHz is scheduled, along with a Young Professionals Networking Event and an IEEE EPS Seminar on Substrates for Chiplets.

	Special Session Topics	Chair/Co-chair/Moderator	Date	Time
1	Exploring the Impact of Industry-Government Co-Investments for the Advanced Electronics Sector in North America, Asia and Europe	Przemyslaw Gromala (Bosch) Erik Jung (Fraunhofer IZM)	Tuesday 05/28/2024	8:30 a.m. – 10:00 a.m.
2	Challenges and Opportunities in Advancing Metrology for Next-Generation Microelectronics	Ran Tao (NIST) Benson Chan (Binghamton University)	Tuesday 05/28/2024	10:30 a.m. – 12:00 p.m.
3	Efficient and Innovative Thermal Management for Power Hungry AI/ ML Applications: Challenges and Opportunities	Zhi Yang (Groq) Sevket Yuruker (Tesla)	Tuesday 05/28/2024	1:30 p.m. – 3:00 p.m.
4	RF Packaging for Communication and Sensing Applications above 100 GHz – Technologies, Design Challenges and Emerging Solutions	Maciej Wojnowski (Infineon Technologies AG) Ivan Ndip (Fraunhofer IZM/ Brandenburg University of Technology)	Tuesday 05/28/2024	3:30 p.m. – 5:00 p.m.
5	Young Professionals Network Panel	Aakrati Jain (IBM)	Tuesday 05/28/2024	7:00 p.m. – 7:45 p.m.
6	IEEE EPS Seminar: Challenges of Chiplets on Large Substrates	Takashi Hisada (Rapidus) Yasumitsu Orii (Rapidus)	Tuesday 05/28/2024	7:45 p.m. – 9:15 p.m.
7	ECTC Keynote by Keren Bergman (Columbia University): Petascale photonic chip connectivity for energy efficient AI computing	Karlheinz Bock (TU Dresden; ECTC General Chair)	Wednesday 05/29/2024	8:00 a.m. – 9:15 a.m.
8	ECTC/iTherm Diversity Panel and Reception: Best Practices to Attract, Hire and Retain a Diverse Workforce	Vidya Jayaram (Intel) for ECTC Christina Amon (University of Toronto) for iTherm	Wednesday 05/29/2024	6:30 p.m. – 7:30 p.m.
9	ECTC Plenary: The Future of Semiconductor Industry. Emerging Start-ups and Technologies for Advanced Packaging	Rozalia Beica (Averatek) Farhang Yazdani (Broadpak)	Thursday 05/30/2024	8:00 a.m. – 9:15 a.m.
10	IEEE EPS President's Panel: Challenges in Education and Workforce Development in the New Chips Economy	Pat Thompson (TI, President of IEEE EPS) K. Pearsall (Boss Precision Inc.) Jeff Suhling (Auburn Univ.) Mark Poliks (Binghamton University)	Friday 05/31/2024	8:00 a.m. – 9:15 a.m.

On May 29, 2024, Prof. Keren Bergman of Columbia University will present the keynote on Petascale photonic chip connectivity for energy-efficient AI computing. This is important in data centers, where connecting numerous compute and memory resources will profit from lower energy and communication costs via integrated silicon photonics provided multi-chip packaging challenges are addressed. This talk explores approaches, including dense wavelength-division multiplexing, to achieve Petabit/s chip escape bandwidths with sub-picojoule/bit energy consumption.

Prof. Keren Bergman (Columbia University)

The conference also features a Diversity and Career Growth Panel and Reception, a Plenary Session on the Future of Semiconductor Industry, and a panel session on Workforce Challenges in Education and Workforce Development in the New Chips Economy.

In addition to the technical program, ECTC offers 16 CEU-approved Professional Development Courses (PDCs) on May 28th, co-located with the IEEE ITherm Conference. ECTC also includes an exhibition, running from May 29th to May 30th, showcasing the latest technologies and products from over one hundred exhibiting companies in the electronic components, materials, packaging, and services fields. Attendees can engage in networking opportunities during coffee breaks, daily luncheons, and nightly receptions.

ECTC invites engineers, managers, students, and executives in the microelectronics packaging and components industry to participate in this unique event, providing a platform for exploring cutting-edge advancements, fostering innovation, and addressing critical challenges. The conference is scheduled from May 28 to 31, 2024, at the Gaylord Rockies Resort & Convention Center in Denver. The hotel is renowned for its stunning architecture, luxurious amenities, and scenic surroundings. Boasting a majestic backdrop of the Rocky Mountains, the resort provides a picturesque and tranquil setting for the 74th ECTC. With its spacious accommodations and state-of-the-art facilities, the Gaylord Rockies offers an inviting atmosphere that complements the professional and collaborative spirit of ECTC. Attendees can expect an enjoyable and productive stay in this remarkable venue.

I sincerely express my gratitude to sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, program committee members, and volunteers for contributing to the success of the 74th ECTC. I look forward to meeting all of you on May 28 in Denver, Colorado!

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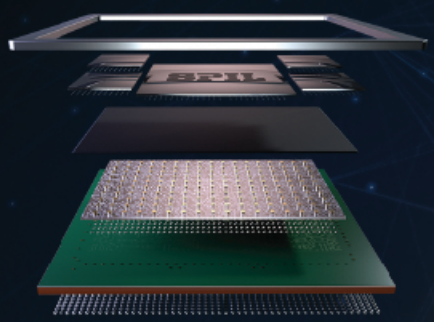

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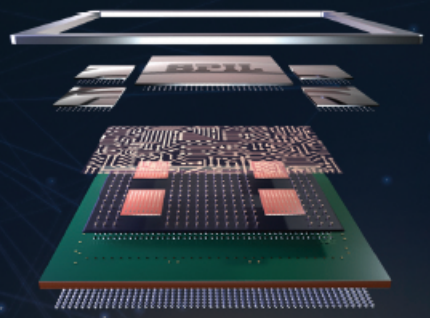

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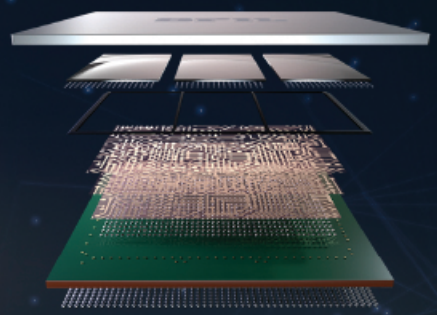

FO-MCM

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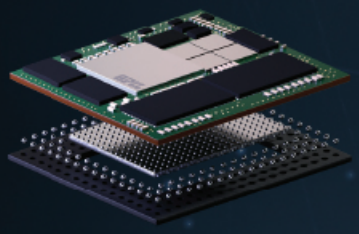

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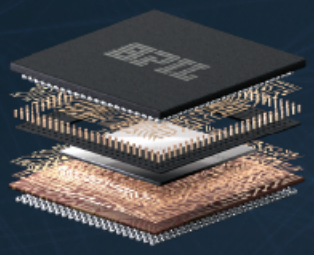

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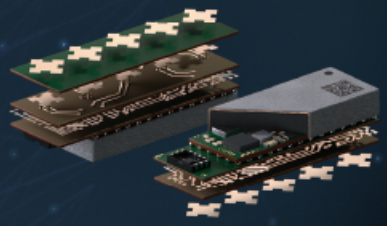

AiP

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