Chip Scale Review®

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The Future of Semiconductor Packaging

Volume 27, Number 6

November • December 2023

Automotive LiDAR: Photonics assembly requirements and trends

- Optimizing advanced IC substrates (AICS) for PLP
- Die-to-wafer hybrid bonding development for HVM
- High-speed probe card architecture for high-end devices
- Recent advances in bridges for chiplets communications
- Automotive gate driver package with galvanically-isolated communication linkage

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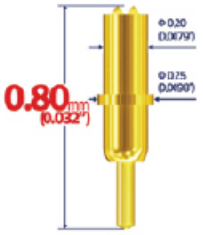
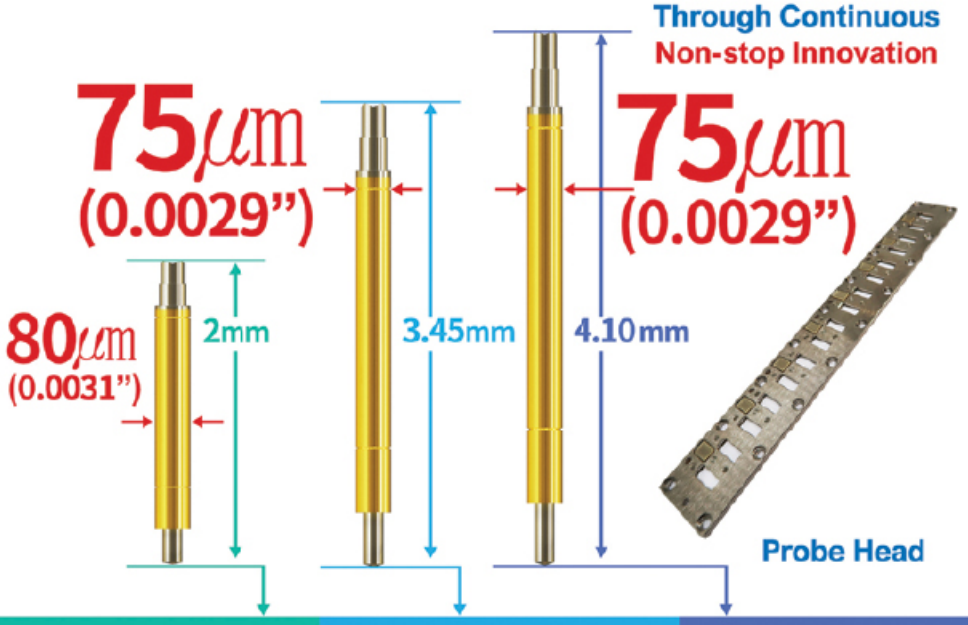




RF-300μm Pitch

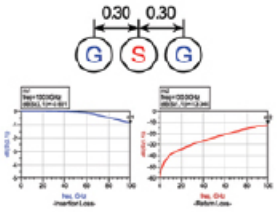
Mechanical Spec.

- Spring Force : 0.212oz (12.0g) @ .0079 (0.20mm)
- Recommended Travel : .0079 (0.20mm)
- Full Travel : .0098 (0.25mm)
- Current Rating : 2.0A

Material
Barrel - Alloy / Au plated
Plunger - Hardened BeCu / Au plated
Spring - Music Wire / Au plated

Electrical Spec. (Simulation data)

- Propagation Delay : 7.68ps
- Capacitance : 0.05pF
- Inductance : 0.25nH
- Insertion Loss : > 100GHz @ -1dB
- Return Loss : > 100GHz @ -10dB
(Dielectric material : MDS100)



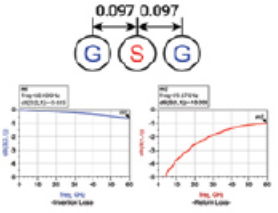
97μm Pitch

Mechanical Spec.

- Spring Force : 0.282oz (8.0g) @ .0079 (0.20mm)
- Recommended Travel : .0079 (0.20mm)
- Full Travel : .0098 (0.25mm)
- Material : Terminal – Pd Alloy / No Plated
Plunger – Pd Alloy / No Plated
Barrel – Ni-Au Alloy / Au Plated
Spring – Music Wire / Au Plated

Electrical Spec.

- Current Rating (Reference Only) : 1.0A
(Based on 20% force reduction)
- Inductance : 0.42nH
- Insertion Loss : > 60.00GHz @ -1.000dB
- Return Loss : 59.67GHz @ -10.000dB
(Dielectric material : CERAMIC)
- Capacitance : 0.22pF
- Propagation Delay : 18.00ps



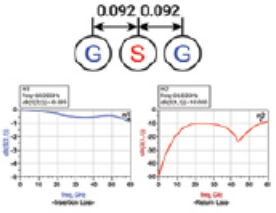
92μm Pitch

Mechanical Spec.

- Spring Force : 0.247oz (7.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
Plunger – Pd Alloy / No plated
Barrel – Ni-Au Alloy / Au plated
Spring – Music Wire / Au plated

Electrical Spec.

- Current Rating (Reference Only) : 1.0A
(Based on 20% force reduction)
- Inductance : 0.67nH
- Insertion Loss : > 60.00GHz @ -1.000dB
- Return Loss : 56.03GHz @ -10.000dB
(Dielectric material : CERAMIC)
- Capacitance : 0.43pF
- Propagation Delay : 33.90ps



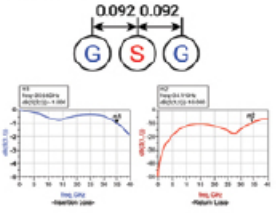
92μm Pitch

Mechanical Spec.

- Spring Force : 0.176oz (5.0g) @ .0098 (0.25mm)
- Recommended Travel : .0098 (0.25mm)
- Full Travel : .0118 (0.30mm)
- Material : Terminal – Pd Alloy / No plated
Plunger – Pd Alloy / No plated
Barrel – Ni-Au Alloy / Au plated
Spring – Music Wire / Au plated

Electrical Spec.

- Current Rating (Reference Only) : 1.0A
(Based on 20% force reduction)
- Inductance : 0.81nH
- Insertion Loss : 35.66GHz @ -1.000dB
- Return Loss : 34.19GHz @ -10.000dB
(Dielectric material : CERAMIC)
- Capacitance : 0.50pF
- Propagation Delay : 43.50ps



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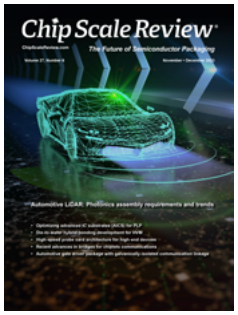

Legislation to support reduction in carbon dioxide emissions is driving the growth in the electric vehicle (EV) market. LiDAR is also driving trends in automotive photonics devices. This issue features two articles that cover these important needs. MRSI (a part of Mycronic Group) discusses the photonics device assembly requirements and trends in automotive LiDAR and presents a solution for typical edge-emitting lasers and VCSEL chips. To answer the need for on-board systems such as EV traction inverters, DC/DC converters, etc., which must be connected to high-voltage power sources, NXP Semiconductors, Inc., presents a package designed for automotive high-voltage gate driver applications.

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CONTENTS

FEATURE ARTICLES

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FUSION AND HYBRID BONDING FOR HETEROGENEOUS INTEGRATION

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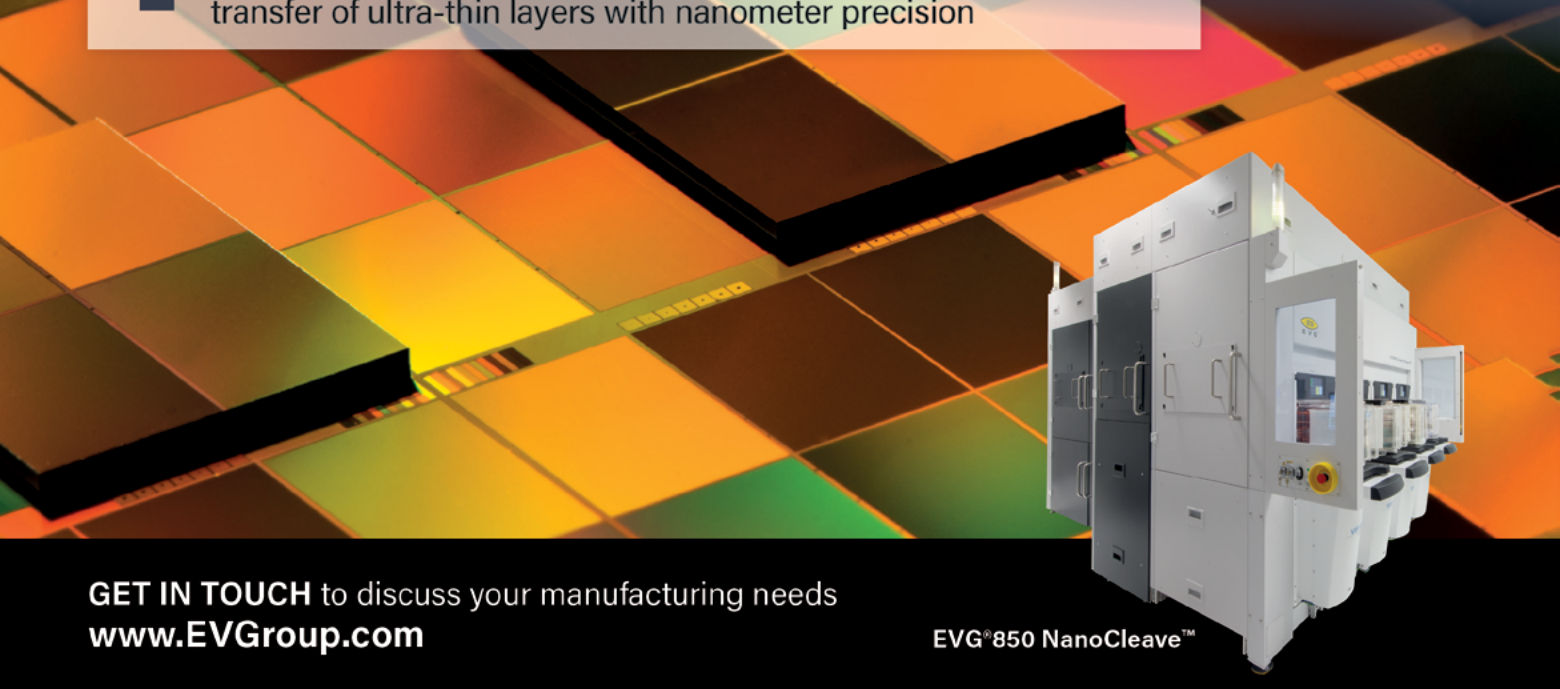

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FEATURE ARTICLES (continued)

DEPARTMENTS

INDUSTRY EVENTS

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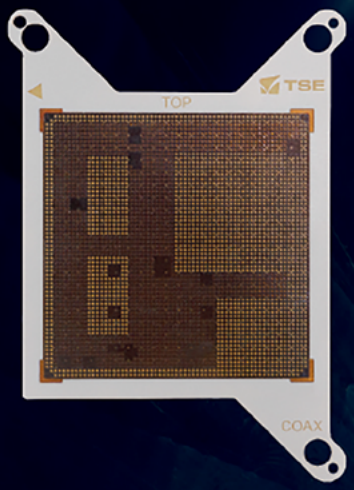
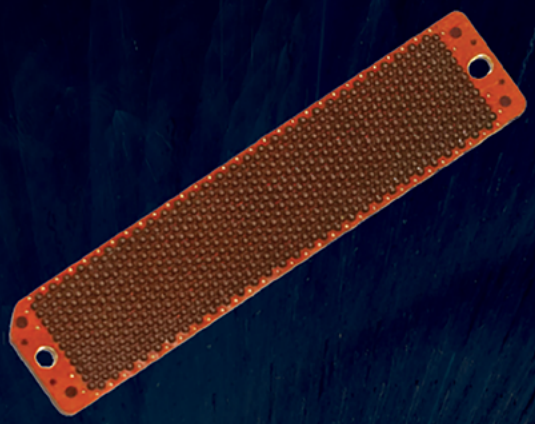
COAXIAL ELASTOMER SOCKET

for >64Gbps ATE/SLT Test
for Crosstalk free Board to Board Connector



Semiconductor Package Test



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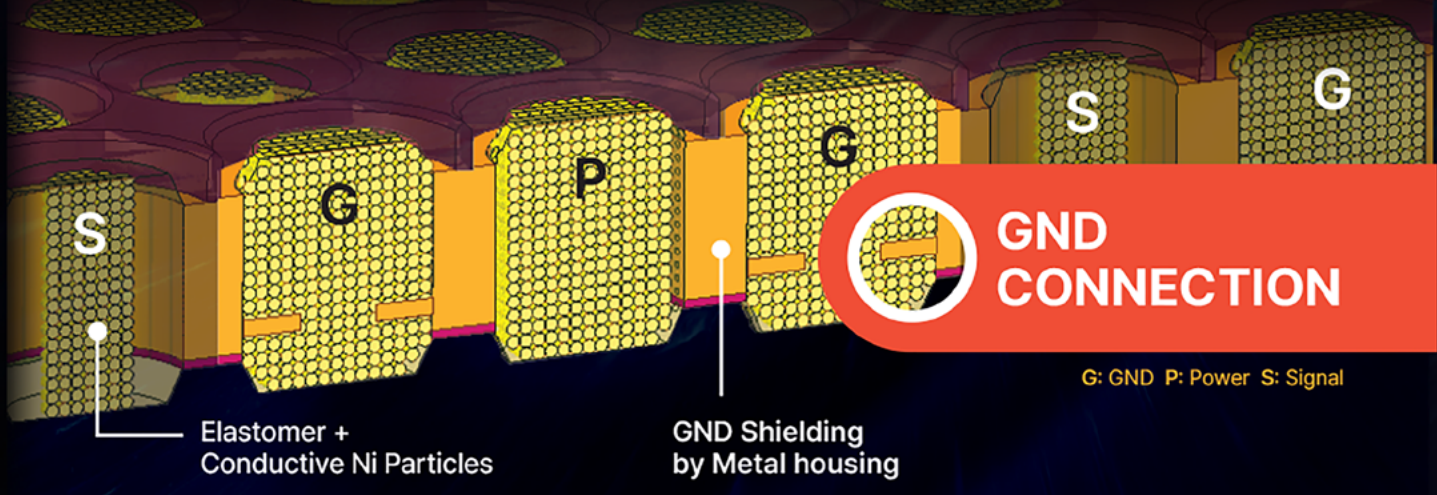
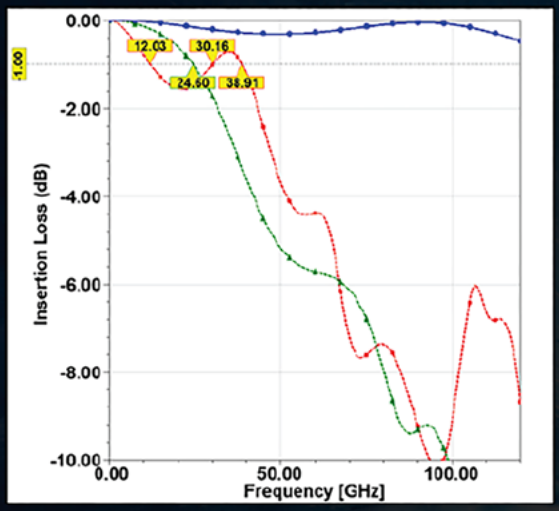


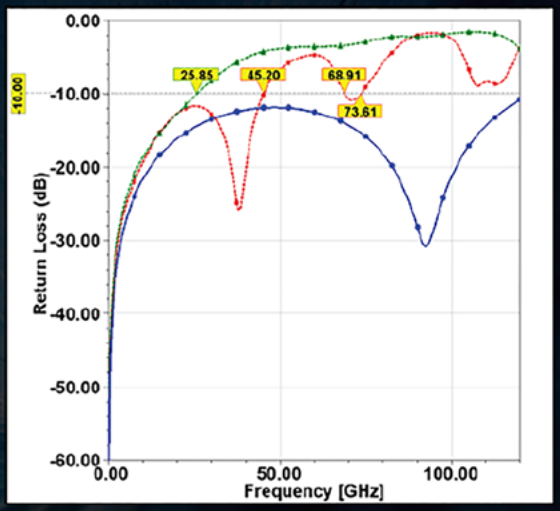
TSE

ELTUNE-coax™

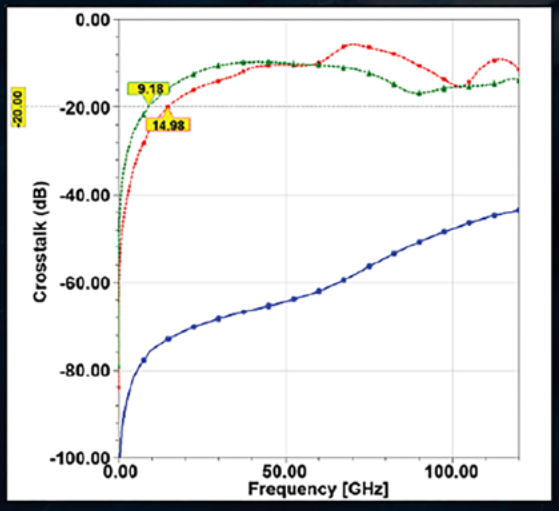
Electrical Specifications (unit: GHz)			
50Ω, 0.80mm pitch	Spring pin	Elastomer	ELTUNE-coax™
Electrical Length(mm)	3.05	0.60	0.60
Insertion Loss(S21) @-1dB	12.03	24.60	>100
Return Loss (S11) @-10dB	45.20	25.85	>100
Crosstalk (S31) @-20dB	14.98	9.18	>100



Insertion Loss



Return Loss



Crosstalk

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Die-to-wafer hybrid bonding development for HVM

By Jonathan Abdilla [BE Semiconductor Industries N. V.], Guan Huei See [Applied Materials, Inc.]

This article addresses the key requirements for a successful die-to-wafer (D2W) hybrid bonding process. The selected process steps from bonding pad formation to grind and singulation, as well as an integrated D2W bonding process will be addressed, providing key technical values for the various steps involved. The integrated bonding processes include wet cleaning, degassing and plasma surface treatment. Successful Cu-Cu diffusion through grain growth across the boundary interface will show the efficacy of such a tool, C-mode scanning acoustic microscopy (C-SAM) results will address the topic of voids, and electrical yield results will also be presented. Actual placement accuracy results will also be shared for both collective and direct D2W hybrid bonding.

Introduction

The adoption of 3D architectures in advanced packaging between chips is driven by high-performance computing (HPC) and artificial intelligence (AI) requirements [1, 2]. Flip chip has been the main technology of forming the die attachment in packaging. It requires a copper (Cu) pillar made out of a metal alloy, namely copper-nickel-tin-silver (Cu-Ni-Sn-Ag) that occupies an opening with a critical dimension (CD) of 20-40µm on a passivation polymer dielectric (e.g., polymide or polybenzoxazole [PBO]) for each of the contact points. Such a thickness is needed to allow underfill material to flow reliably and to act as a stress buffer for mechanical integrity. The flip-chip attach is done through thermal compression bonding (TCB) where at least one of the dies or substrates is heated to ensure that the Cu bump reaches the eutectic state so that Sn-Ag can form a good electrical contact. With this bonding technique, some amount of inter-metallic compound that is causing higher resistivity and weaker reliability is inevitably generated.

The migration toward Cu hybrid bonding (HB) will only require the use of standard back end of line (BEOL) inorganic dielectric and Cu, and is expected to improve over the issues noted above, as well as adding other benefits. Overall, the preparation needs for die bonding are simplified, Cu bump and underfill processes are removed, and TCB is replaced with room temperature HB. This directly translates into reduction of vertical form factor and scaling to higher input/output (I/O) density, thereby leveraging the mature BEOL that scaled well below the sub-micron range. The change of pad material from a complex alloy (Cu-Ni-Sn-Ag) to pure Cu and the direct connection through HB at room temperature are expected to offer shorter interconnect lengths, lower resistance and improvement in thermal diffusion. As a result, an increase in system-level performance with better bandwidth and/or speed can be expected.

HB is achieved as a two-step process: first, by leveraging on the initial forces of surface interaction at atomic proximity of the dielectric-dielectric interface to form the "tacking," which is the initiation of the bonding, and finally, following up with a fusion process by annealing at an elevated temperature (100°C-400°C) to form both stronger dielectric-dielectric covalent bonds with the release of excessive water (H_2O) molecules, as well as metal-metal diffusion that will enable the electrical connection. A successful bond can be achieved with careful surface engineering of the dielectric, typically with dielectric surface roughness values of <0.4nm [3]. Of the two HB flavors, wafer-to-wafer (W2W) or D2W, the latter enables higher system-level yield thanks to use of known-good-dies only. This paper describes the necessary conditions to achieve a successful D2W HB suitable for high-volume manufacturing (HVM) production.

PVD-CMP co-optimization for D2W HB

As elegant as it looks, HB also has many challenges. The bonding requirements that work for W2W HB, e.g., the Cu chemical mechanical polishing (CMP) process that ensures good roughness (<0.4nm), dishing (<5nm) and erosion, are not directly transferable to D2W. A D2W test vehicle and bonding flow was developed based on the illustration of the key process sequence shown in **Figure 1**. Previous work done on W2W test vehicles successfully demonstrated thick barrier and

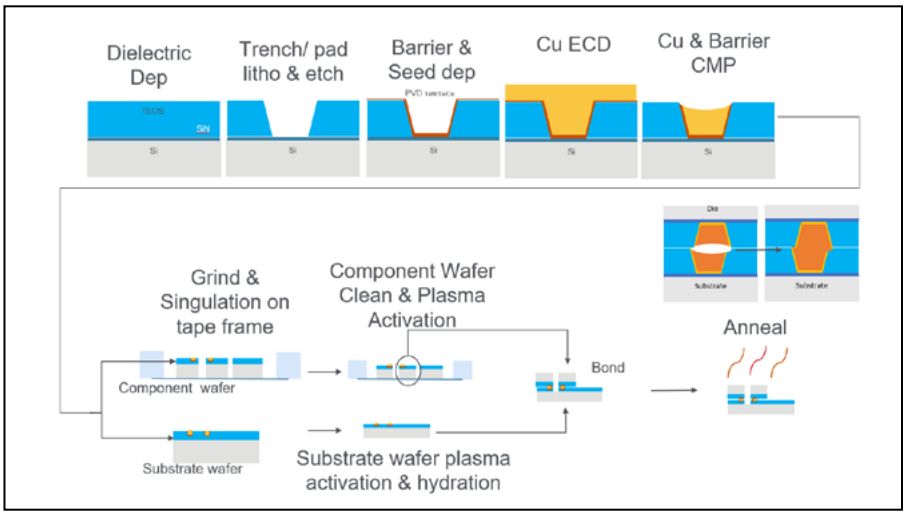

Figure 1: Selected process steps from bonding pad formation to grind and singulation.

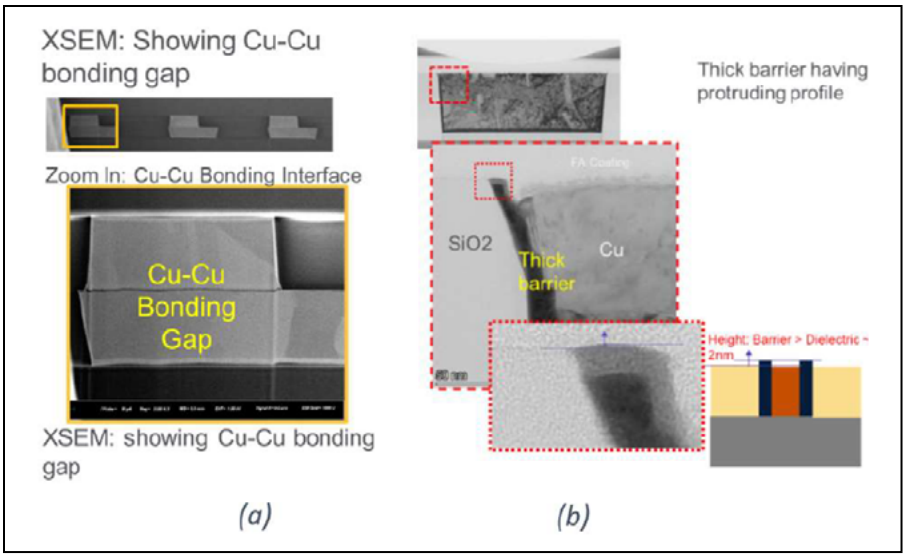

Figure 2: a) A PVD thick barrier-CMP interaction with zoom in focus and an illustration of barrier protrusion, which resulted in b) a Cu-Cu bonding gap due to barrier-CMP interaction (see the XSEM).

CMP optimization [4]. However, when the same process was applied to D2W HB, it resulted in a visible Cu-Cu gap from X-ray secondary emission microscopy (XSEM) analysis as shown in **Figure 2a** due to insufficient force (weight) to form good tacking (i.e., low force was used to bond the samples compared to the forces used in W2W bonding) as a result of thinning and dice. The failure analysis of a cross section with transmission electron microscopy (TEM) at the edge of the Cu bond pad (**Figure 2b**), indicated the barrier was higher than the dielectric by 1-2nm. One hypothesis suggested that this barrier protrusion was standing out from the rest of the dielectric at the corner of the bonding pads, and in addition to the already reduced force acting on the bond interfaces from grinded and singulated die, was preventing the "tacking" of dielectric-dielectric during die placement. At post-bond anneal, the protruded barrier has higher thermal expansion than the oxide (Ta: 6.5 10^{-6}/K vs. SiO_2: 0.65 10^{-6}/K [5]) and therefore was expanding faster, pushing the two bond interfaces apart and preventing the Cu pads from making contact and diffusing (or inter-diffusing), giving rise to a wider gap (20~40nm) than initial dishing. The physical vapor deposition (PVD) barrier-CMP process was optimized by using a thin barrier and a tuned CMP process to ensure that oxide was always higher than the barrier as shown in **Figure 3a**, while keeping the roughness, Cu dishing and erosion within the D2W bonding process requirements. The same bonding and annealing was repeated. The results showed that the Cu-Cu bond was fused, and was further validated with transmission electron-back-scatter-diffraction (T-EBSD) portraying a successful Cu diffusion across the bonding boundary (**Figure 3b**).

Surface activation, cleanliness, queue time and electrical yield

Once the interfaces were optimized as discussed in the section on PVD-CMP co-optimization, we moved on to study dielectric surface activation, the impact of a particle-free surface and queue time. These requirements are more stringent for D2W HB than for W2W HB because of the need to process dicing and singulated dies on flexible organic tape or on carrier wafers with organic adhesive.

Plasma activation has been demonstrated to increase hydrophilicity for dielectrics such as SiO_2 and SiCN [6]. Hydrophilicity is achieved by the presence of the silanol groups (Si-O-H) on the dielectric surfaces. Ion energy is one way to promote the silanol groups' attachment to the dielectric surface by creating disorders and high-energy states on the surfaces. The presence of these silanol groups is essential, as they enable initial bonding when dielectric surfaces from substrates and chiplets are brought together even at room temperature. The measurement of the hydrophilicity of dielectric surfaces is a way to evaluate the effectiveness of the activation

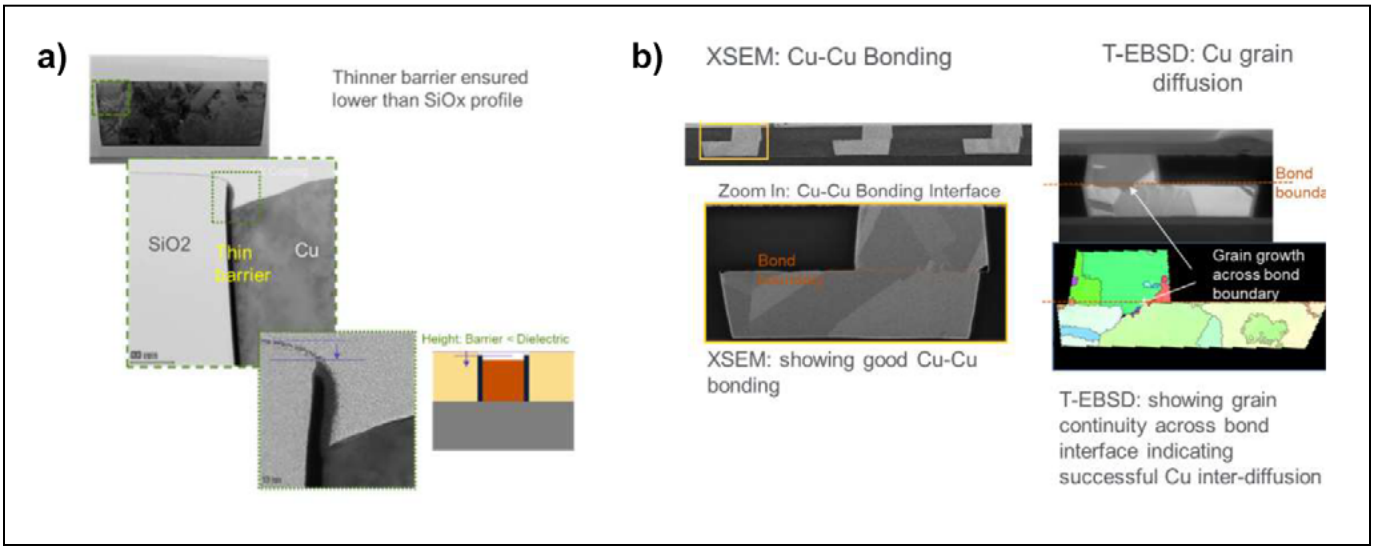

Figure 3: a) An optimized thin PVD-CMP, with zoom in focus and an illustration of higher dielectric than barrier in nm-scale, which resulted in a Cu-Cu diffusion (see the XSEM) and confirmation with T-EBSD showing grain growth across the bond boundary.

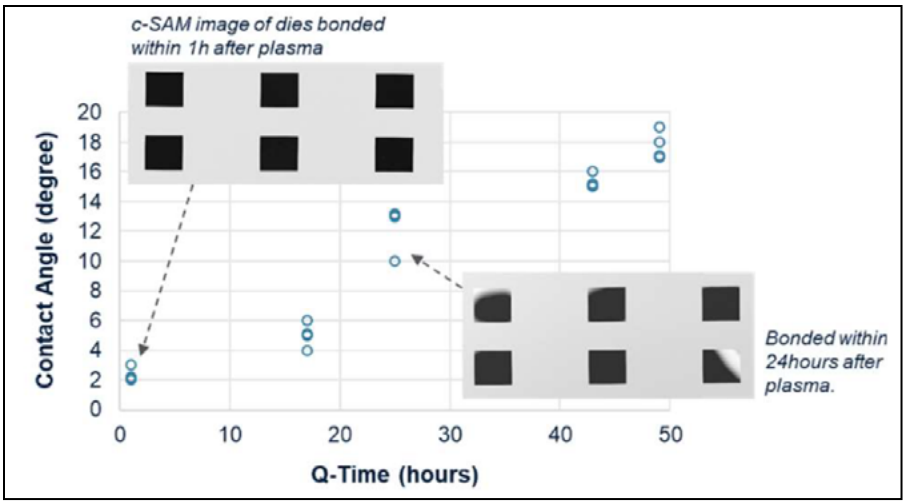

Figure 4: Plot showing the plasma activation effect on the initial contact angle on an SiO_2 surface and the queue time effect on the contact angle and bonding performance after activation. Bonding degrades with excessive queue time between activation and bonding as shown in the C-SAM images of the delamination around the die edges.

process. Macroscopic observations of the hydrophilicity of the SiO_2 surface are seen with water contact angle measurements. When the SiO_2 dielectric surfaces are treated with the right plasma conditions, superhydrophilicity with a contact angle of <5º can be achieved (**Figure 4**). It is also shown that the contact angle degrades over time if the wafers are exposed to air after activation. The degradation or the hydrophilicity leads to poor bonding performance, as shown in delamination at the die edges from C-SAM analysis (see insets of **Figure 4**). Therefore, controlling the queue time between activation and bonding is crucial to achieving the best bonding performance.

Proper selection of plasma conditions, including ion energy, density, and chemistry is essential for sufficient activation without causing physical or chemical damage to other materials, such as Cu and plastic tapes. As shown in **Figure 5**, when the ion energy is too high, the dielectric surfaces are roughened, which creates voids and diminishes the bonding performance. In addition, the sputtered materials from the dielectric surface and organic adhesive can further redeposit on the die surface under strong plasma conditions. The redeposition creates an undesired Cu diffusion barrier during the post-bonding annealing stage. Therefore, it is important to optimize the plasma activation conditions to achieve surface roughness of <0.5nm and etching of SiO_2 of <1nm while preserving the Cu dishing profile and ensuring the surface is free of organic residue and without excessive oxidation (**Figure 5e-h**).

Cleanliness is paramount to the performance of the HB. Any particle on the bonding surface can lead to poor adhesion, weak bonds, or complete failure of the bond (**Figure 6**). To ensure the best bonding performance, free particle control is a high priority for any pre-treatment system design. Particles should be controlled to meet the device specification in the activation chambers. In addition, a highly efficient wet clean process is essential to ensure the cleanliness before the wafer and the component dies enter the bonders. Efficient cleaning is particularly challenging for diced wafers on flexible tapes because the dicing processes could introduce additional particles or/and contaminants. Insufficient post-dicing cleaning could leave particles on the tape or die sidewalls (**Figure 7a-b**). In some cases, further cleaning, if not done correctly, can create more particles when stirred up from the tape or die sidewalls and land on die surfaces, causing delamination near die edges (**Figure 7c-f**).

After the whole integration, bonding process optimization and alignment were done, a 300mm substrate wafer was bonded (~230 dies) to validate the bonding performance. **Figure 8a** shows the post-bond C-mode scanning electron microscopy (C-SAM) result where no gross random void was observed, indicating high cleanliness efficiency. This is further confirmed with an electrical continuity test on a 10,000-daisy chain (DC) connectivity occupying an area of 1mm x 1mm (of a 6mm x 6mm die size) shown in the **Figure 8b** wafer contour plot and in the

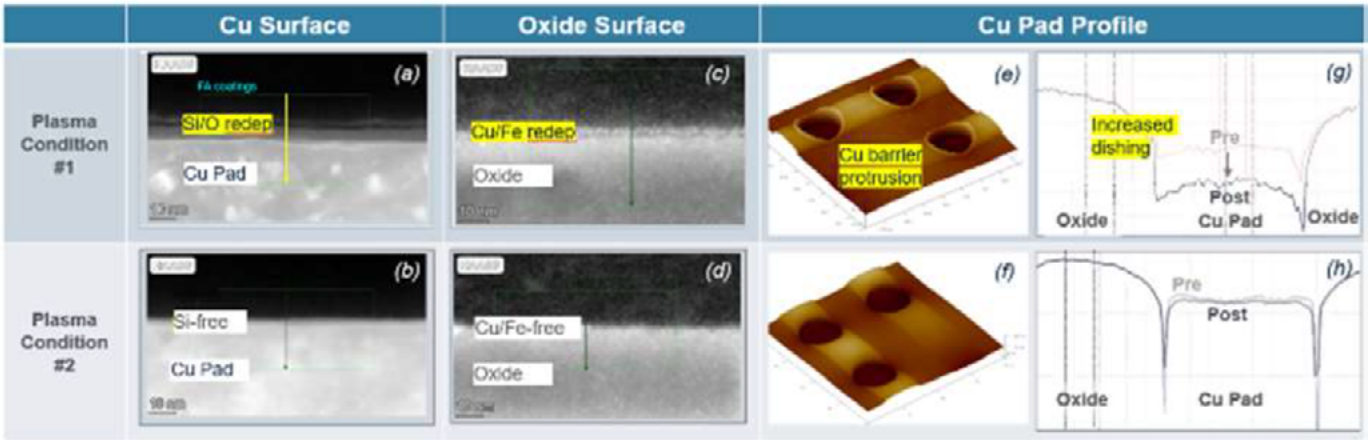

Figure 5: Surface and topography comparison between strong and soft plasma-treated patterned samples: a–d) TEM cross-sectional study of the Cu pad and dielectric oxide surface, revealing surface contamination from redeposition caused by a strong plasma; e–h) Atomic force microscope measurements showing that a strong plasma alters Cu pad profile, and an increased dishing amount.

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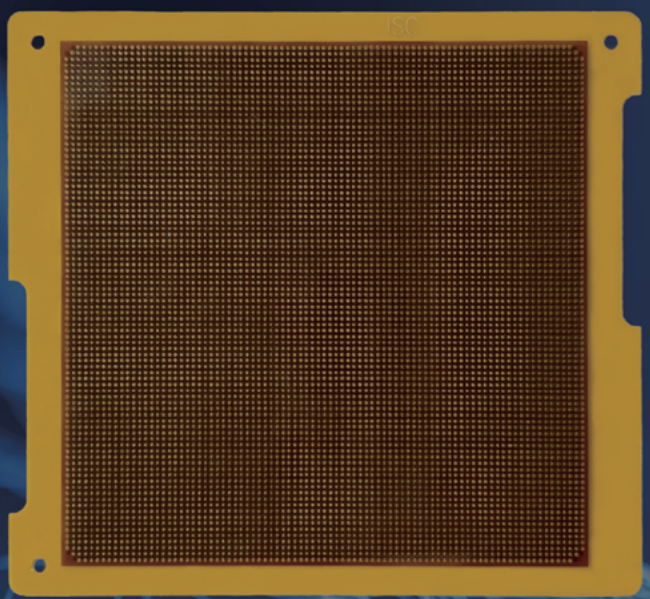

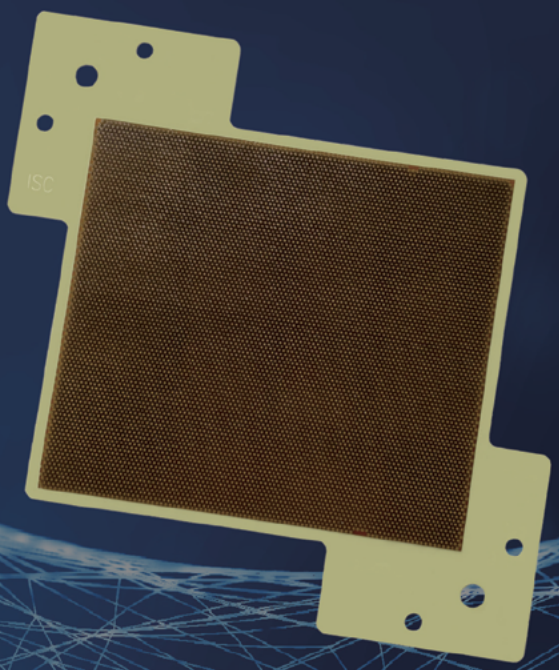

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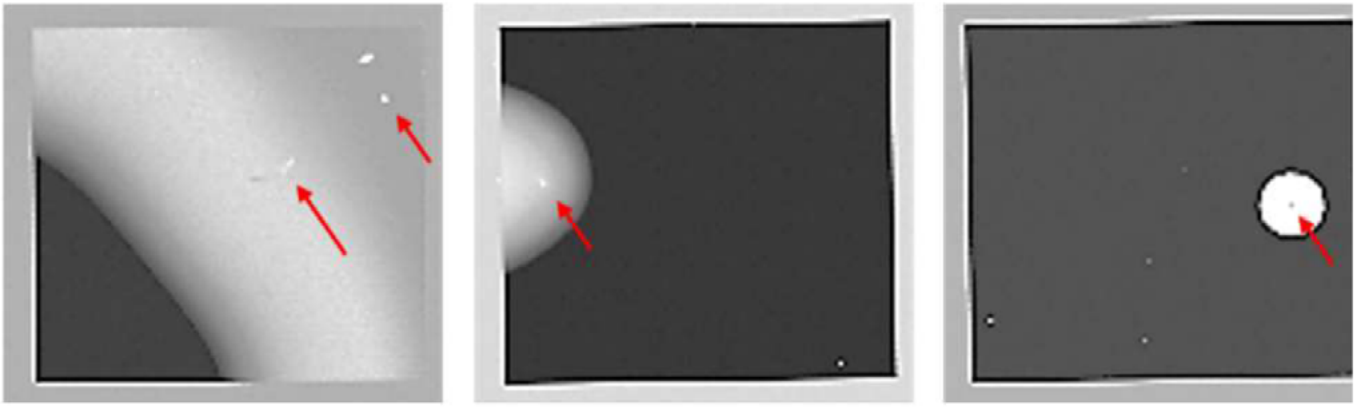

Figure 6: SAM images of defective bonding (delamination and voiding) caused by surface particles.

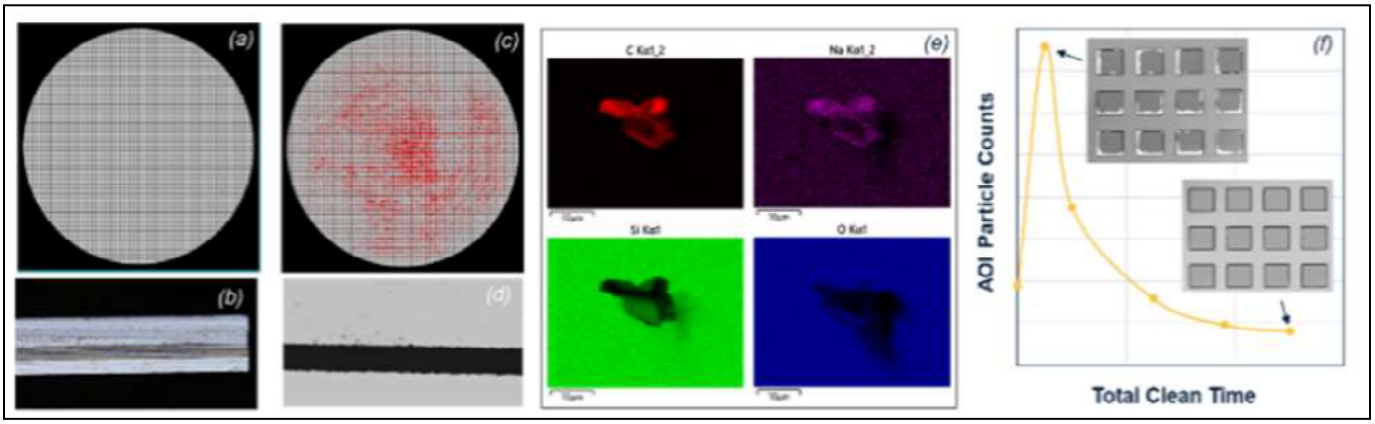

Figure 7: Automatic optical inspection (AOI) of the a) surface and b) sidewall of singulated dies of a tape-frame wafer after thinning and the saw-dicing process. A large number of particles (black) can be seen adhering to the sidewall. c-d) An incorrect further cleaning detaches and redeposits the particles onto the die surface. c-e) The organic nature of the particles revealed by energy-dispersive X-ray spectroscopy inspection suggests tape adhesive as the origin. If not properly removed, f) these particles can cause die delamination after bonding, as seen under SAM inspection.

normal quantile plot in **Figure 8c**, which shows a >99.5% continuity electrical test yield (a significant improvement from pre-optimization data). The process improvement was reflected in overall mean resistance and variability.

The same test vehicle was further used to characterize the process-induced possible yield impact of queue time between the various process steps, as batch-mode processing makes it difficult to control queue time. Samples were processed with a 36-hour queue time and compared with the baseline; in the high-volume production case, one could expect a queue time of 1 to 2 days, and not just time, but also its variance increases with a more complex bonding configuration, where >3-5 different chiplets are in the roadmap to be bonded to the same substrate. Three bonded wafers from the "delayed" lot were compared to the baseline in **Figure 9**. Adding queue time leads to significantly lower yield (80%) vs. the reference case (98%).

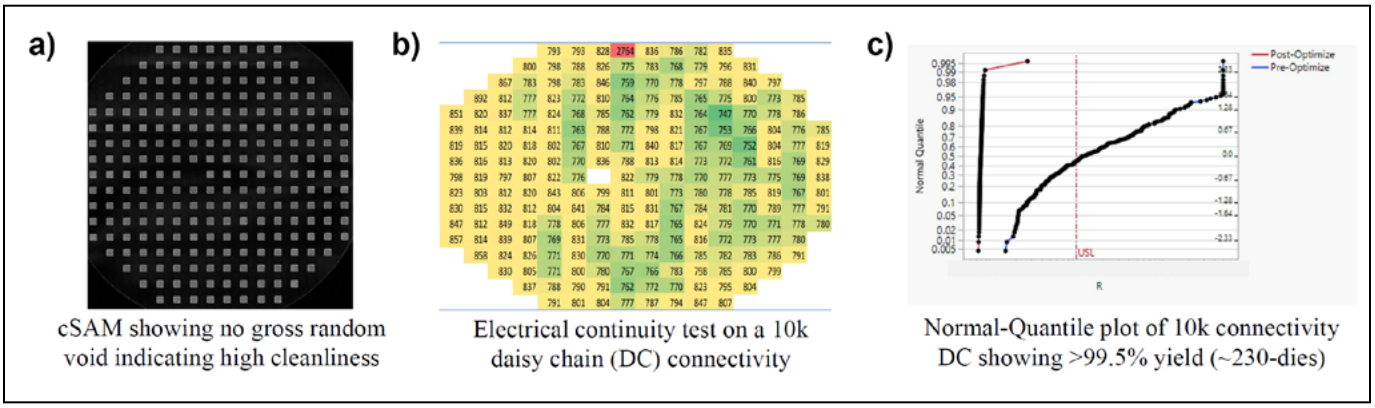

Figure 8: Post optimization: a) CSAM result showing void-free bonding, b) a wafer contour plot of 10,000-connectivity daisy-chains resistance, and c) Normal-quantile plot of 10,000 connectivity DC showing >99.5% yield (~230-dies)—a significant improvement from pre-process optimization.

Die placement accuracy

Two bonding process cornerstones include bond force control and bond front propagation, of which the latter can be controlled through several options—with die shaping being preferred. The die shaping is responsible for creating a controlled bond front, ensuring no void entrapment, and avoiding ablation generated from the high-speed die bond to substrate wafer. Bond force, in turn, can impact initial bond strength from dielectric fusion as well as damage to the die if force is not controlled or not optimized.

Our approach to die shaping and bond front propagation is to have a single point of initial contact between die and substrate wafer, which is at the center of the die. This approach ensures two things: first, the initial contact causes instant bonding through Van der Waals's forces, thereby locking the die laterally and rotationally and minimizing placement accuracy loss from possible mechanical influences. Second, this allows the air between die and substrate wafer to be expelled symmetrically outwards as the die is flattened, thereby ensuring equal conditions on all sides of the die as well as minimizing risks of void entrapment. Figure 10 shows the shape of the same die at different values of the variable-controlled factor for a 7x7mm die at thicknesses of 50µm and 100µm. The inner orange circle delineates that the die is at its highest warpage level taking on a convex shape. The graph shows that for the thinner 50µm die, the change in shape occurs at a much lower value for the controlled variable factor and that the maximum height is also higher. For the 100µm example, the die shows no deformation for the first four values of the controlled-variable factor. The maximum height is lower than the 50µm thick die, but both exhibit a similar behavior whereby the maximum die shape height flattens out. At all stages following the initial conditions however, the first point of contact is always in the center of the die.

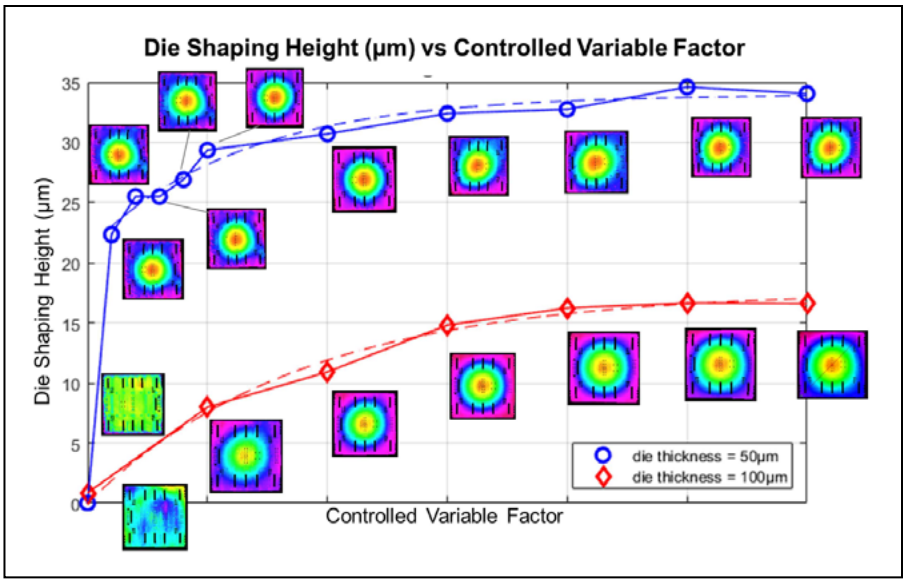

Figure 10: Die shaping height of die in µm vs. variation in the controllable factor for a 50µm (blue) and 100µm (red) thick die.

Two scenarios were explored to estimate bonding precision. The first scenario is bonding on a substrate wafer coated with a temporary bonding material (TBM) layer. The second scenario consists of direct, or fusion, bonding. The first scenario uses a process that does not rely on plasma activation because the bonding mechanism is not through instantaneous fusion by way of Van der Waal's forces, but through the temporary bonding material adhesive. However, this process is reliant on the TBM's properties of bonding reaction times, elasticity and viscosity among others, all of which have an impact on final accuracy. The process was carried out with ~7x7mm dies analyzed using infrared (IR) microscopy. The results are shown in Figure 11 and

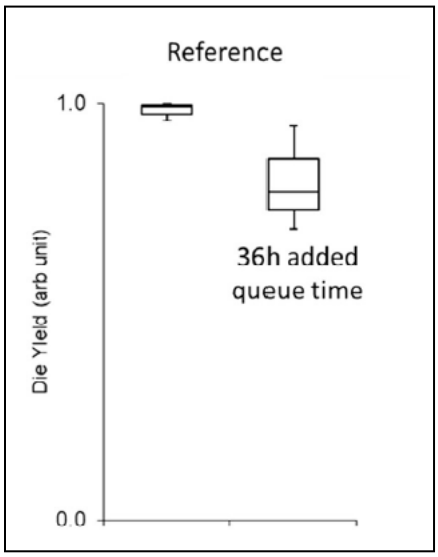

Figure 9: Plot showing the effect of added queue time on bonding yield.

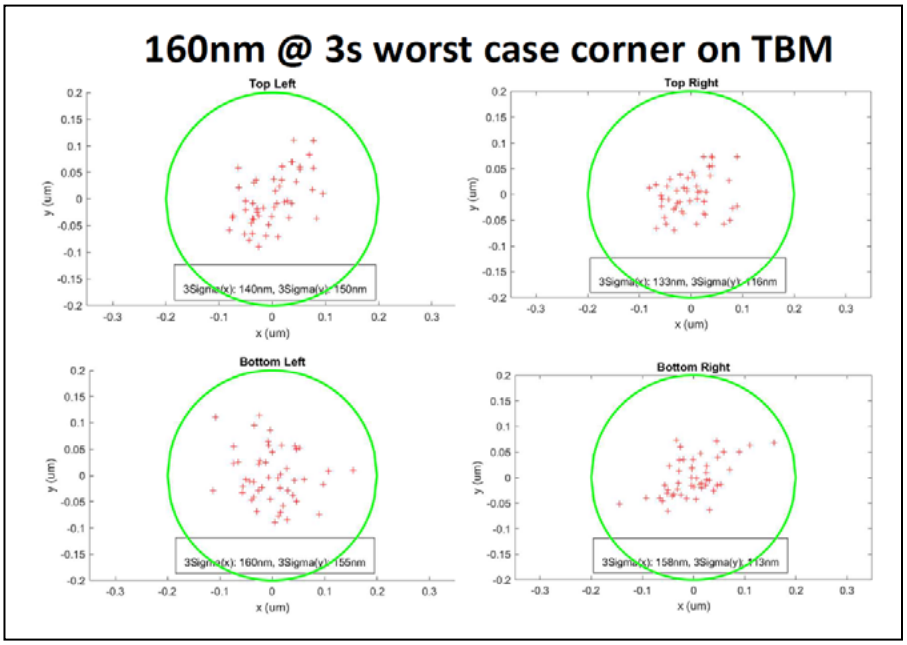

Figure 11: IR overlay for die placement on a wafer with a TBM layer.

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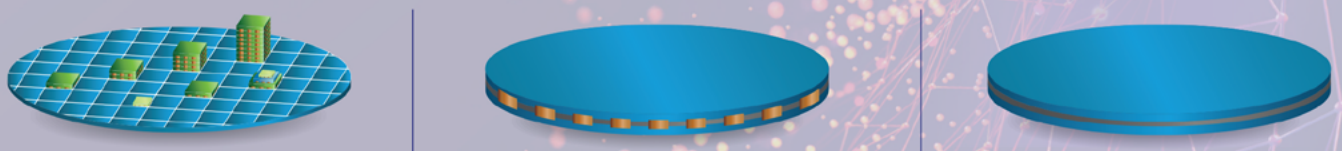

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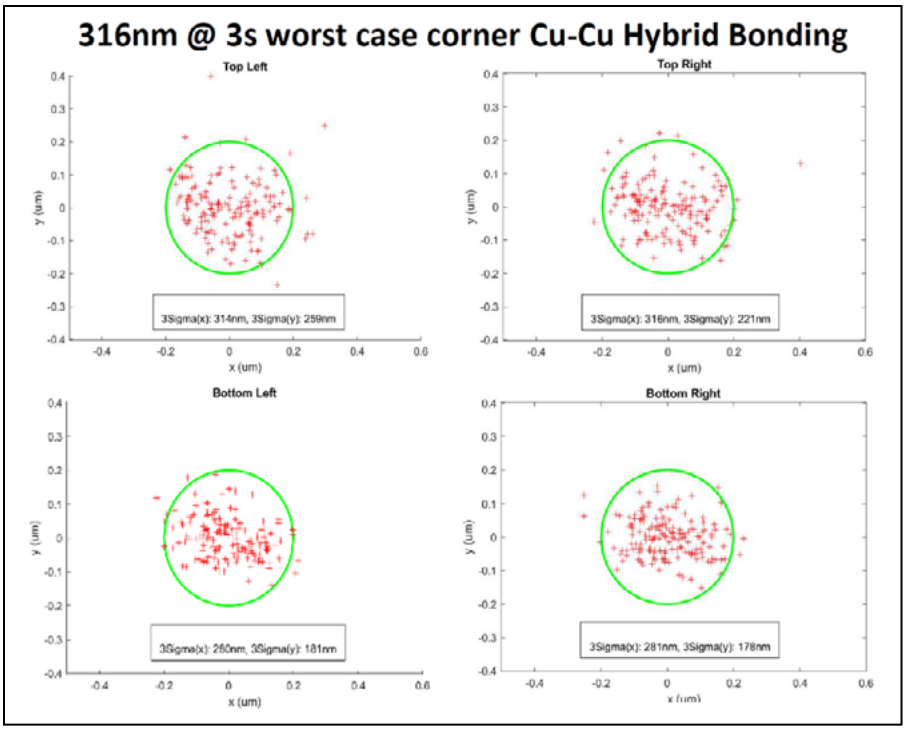

Figure 12: IR overlay for die placement on a wafer with direct bonding including a copper pad.

indicate that actual bond placement accuracy is an impressive 160nm @ ±3s for worst corner, which is currently one of the best die-to-wafer (D2W) accuracies. The green circle represents a ±200nm circle.

For the second scenario, the wafers were subjected to wet cleaning and plasma, as delineated in **Figure 1**. The dies in question were ~6x6mm. **Figure 12** shows placement accuracy results of 316nm @ ±3s for worst corner. The main factor for the gap in accuracy is that direct bonding is more prone to impact from customer material than any other bonding mechanism such as mentioned in the first part of this article due to its complexity and stringent requirements. Notwithstanding, 316nm @ ±3s for worst corner is still a very good result for a lab test vehicle and further trials with optimizations are planned in the future. The data shown in **Figure 12** was collected with an inline metrology system with feedback control capability.

Summary

A working process flow for D2W HB has been presented. Positive outcomes of an HVM-capable process heavily depend on the co-optimization of many pieces of a complex technical jigsaw. The bonding dielectric needs to be controlled in terms of surface roughness, and needs to be properly activated with plasma. Such plasma should not lead to damage to the dielectric, nor to the metal pads, which, in turn need to be controlled not just in terms of dishing, but also with regard to unwanted protrusions from the Ta barrier. The importance of cleanliness was clearly stated and demonstrated via studies showing void formations arising from particle entrapment. The bonding process itself was accomplished with advanced dynamic die-shaping capabilities, state of the art alignment (162nm @ 3σ), and using inline control capability. Finally, control of the queue time along the whole process is critical to guarantee optimal yield.

Acknowledgments

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Optimizing advanced IC substrates (AICS) for PLP

By Keith Best [Onto Innovation]

Faster data transfer, greater heat dissipation, less power consumption and increased functionality are all qualities that chipmakers and their customers want from their devices. Since the dawn of the semiconductor industry, the pursuit of increasingly advanced nodes has served as the industry's North Star. But for today's voyagers, rough seas are ahead: these nodes have decreased in size, input/output (I/O) bumps on the chip have grown smaller—and with the shrinking of these bumps, their ability to mate directly to printed circuit boards (PCB) diminishes. The way to avoid this is to use advanced IC substrate (AICS), i.e., an intermediary substrate that enables progress in panel-level packaging (PLP) and chiplets.

Chiplets are a type of advanced packaging in which multiple die—such as memory, analog and other devices—are assembled in a single, large package along with a central processing unit (CPU) or graphics processing unit (GPU). With AICS, all of these chiplets can be co-packaged together in packages that may be as large as 120mm x 120mm each, which is a considerable increase from the 10mm x 10mm-sized packages of fan-out panel-level packaging (FOPLP). These large packages allow multiple die with smaller interconnects to be assembled and then redirected to larger contact bumps compatible with a PCB. None of this means the industry has left the pursuit of next-generation advanced nodes behind, or smaller packages for that matter.

Although the semiconductor industry has turned to chiplets and other advances to meet various next-level performance needs and spur new innovations, advanced nodes remain key areas of development and advancement. But this move toward extra-large AICS packages signals the need for large exposure field, fine-resolution panel-level lithography systems that can expose entire panels using fewer exposures. The journey to a new era of chiplets and PLP, however, is fraught with challenges that must be overcome, including total overlay shift, yield loss and copper-clad laminate (CCL) substrate distortion. In this article, we will focus on these three challenges to the rapidly growing AICS market and outline several solutions that we have determined will enable manufacturers to address them.

Total overlay drift

The AICS substrate that enables PLP and the segments it serves (e.g., the emerging industry star artificial intelligence [AI]) features up to 24 redistribution layers (RDL) split between the frontside and backside of the substrate. While having such a large number of RDLs improves the package's I/O count and functionality, these improvements are not without their complications. For example, as the number of RDL layers increases, minimizing overlay errors becomes increasingly burdensome. Furthermore, the trouble with overlay errors is not merely a layer-to-layer issue. Total overlay drift—the compounded drift of all RDLs in an AICS—is a challenge that advanced packaging manufacturers will need to address. But first we need to discuss how RDL processing affects the substrate.

During the AICS process flow, the buildup film between the RDLs is cured after each laser-drilled via layer. This continuous thermal cycling of the CCL substrate has the potential to distort the substrate in each quadrant of the panel. The result is that each quadrant could have vastly different overlay results.

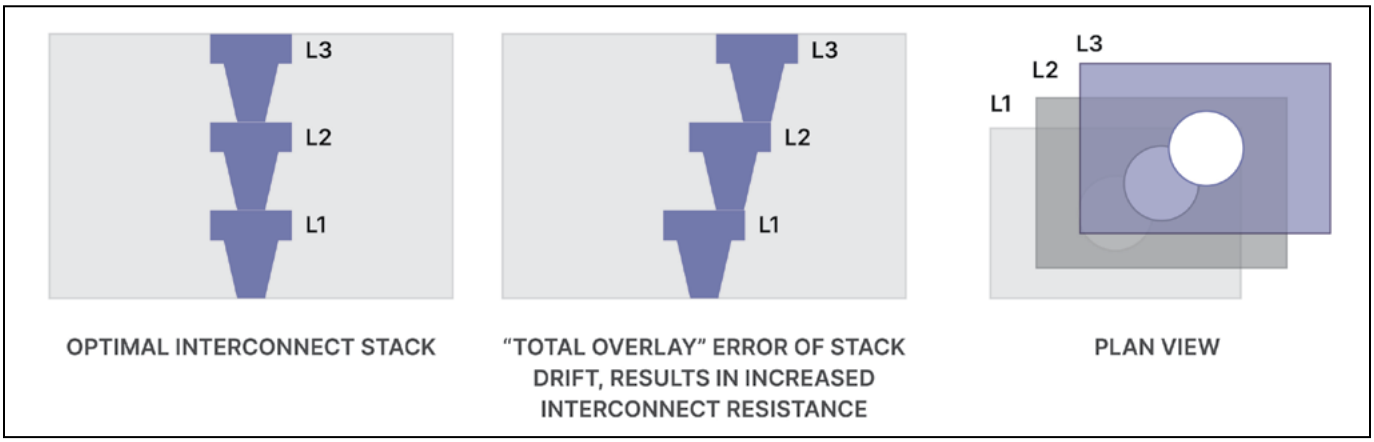


Figure 1: A visual explanation of total overlay drift.

And in the case of extremely large exposure field (e.g., 250mm x 250mm) lithography systems, these differences in overlay create a major yield challenge, especially for high-volume manufacturing.

First, let's define total overlay. Total overlay is the summation of the overlay errors for all RDL layers, with respect to the bookending final layers on either side of the panel (**Figure 1**). Cumulative overlay drift from individual RDL buildup layers can significantly increase overall trace length. This may result in higher interconnect resistance, parasitic effects and poor performance for high-speed and high-frequency applications.

As each RDL is added to the film stack, layer-to-layer overlay data needs to be continuously monitored. If the total overlay error exceeds specifications at any point, and at any location on the panel, corrective action must be taken to mitigate total overlay drift or else the design resistance specifications for a package may be exceeded.

You can think about total overlay like this: if the overlay drifts 5µm per layer, and there are 10 layers, the total RDL length will increase by 45µm. This problem is exacerbated as the number of layers increases, i.e., in a 24-layer RDL stack, the interconnect length would increase by 115µm.

To address the total overlay challenge, manufacturers should employ an overlay tracking system, one that incorporates metrology, lithography and analytics that records measurements for every RDL-to-via overlay across the entire panel and sums the vectors, from layer to layer, as the process stack grows. With such a system, the manufacturing team could use inspection and data analytics to track and compensate for multi-layer overlay drift. The tracking system would generate an error signal when cumulative overlay error exceeds thresholds, and the required overlay correction offsets would then be calculated and sent to the lithography system. Without a suitable tracking system in place, manufacturers have no way of knowing if RDL resistance meets specification until final electrical test (e-test). By that point, resources, time and money will have been wasted.

Yield challenges

Now that we've discussed total overlay drift, let's explore AICS package yield and its importance in fostering a cost-effective, high-throughput process. As previously mentioned, AICS have relatively few packages per panel. For example, a 510mm x 515mm AICS panel can only accommodate 16 packages (120mm x 120mm) compared to FOPLP, which could have over 2,300 packages. That's a significant difference. One defective package on an AICS could result in a 6.25% yield loss, whereas with FOPLP, one defective package may only represent a 0.04% yield loss.

To make matters even more complicated, the yield challenge is exacerbated because as the AICS package size increases to 150mm x 150mm, a single defective package failure results in an 11% yield loss, which is a significant decrease in an industry that operates under extremely narrow margins. In addition, the requirement to process both the frontside and backside of the AICS offers another risk: surface contamination leading to defects that result in yield loss.

It takes a few weeks to complete the processing of an AICS. Only by knowing the yield of an entire fab's AICS inventory, in real time, will productivity be evaluated accurately. Furthermore, panel yield needs to be assessed in terms of

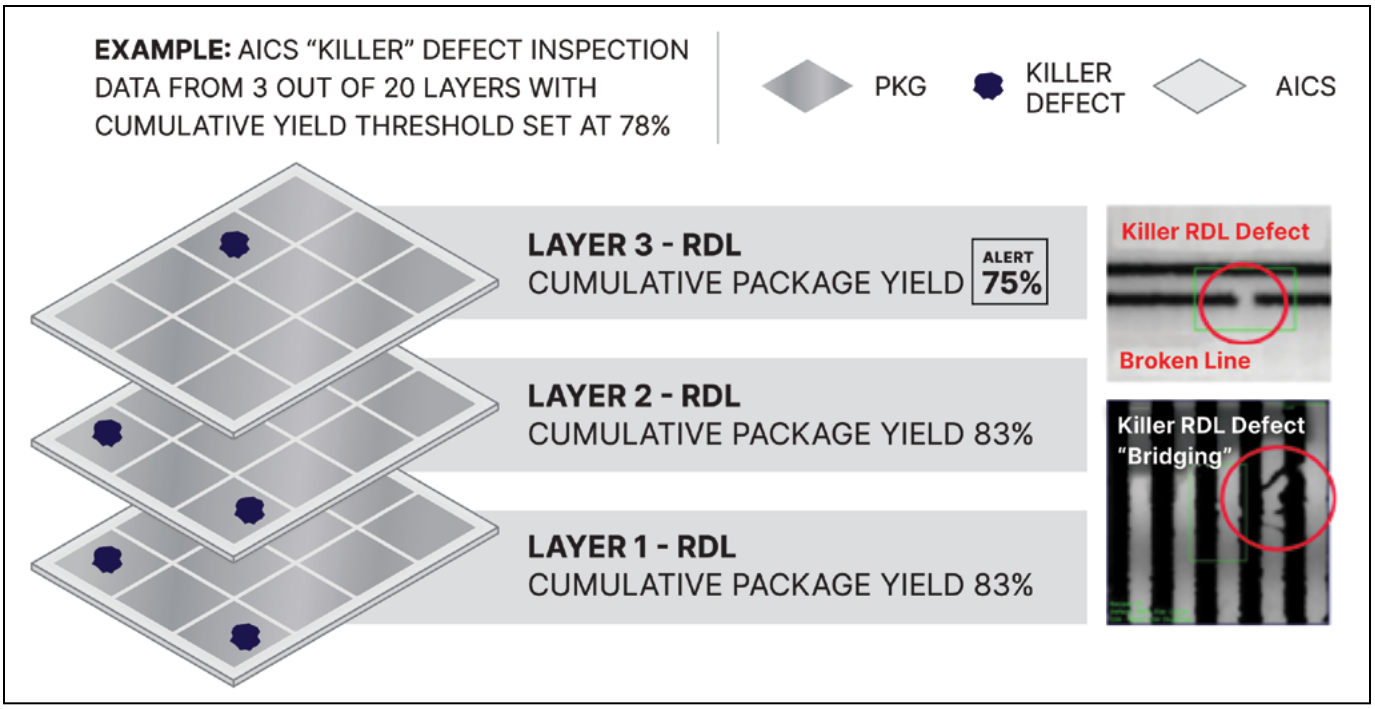


Figure 2: The effect of defects on cumulative package yield.

cost at each process step. The AICS process is a die-last process, so the panel is not of high value until the die are placed at the very end of the build. Knowing when to scrap, restart or continue to process low-yielding AICS becomes a business decision, one that relies heavily on accurate yield data. Of course, the yield loss needs to be investigated and root causes identified as soon as defects, both potential and actual, arise. With this in mind, if the manufacturing team learns that the panel at layer five in the process has a yield of 50% and it's a 40-layer process, is it worth processing the panel further? Should the panel be scrapped and restarted? The likely answer is, yes (**Figure 2**).

This is where the use of advanced automatic defect classification (ADC) and yield analytics are imperative for a quick and successful recovery. To track the panel yield, a comprehensive and intelligent yield-tracking database, with access to inspection data for each panel at each process step, is needed. In addition, the inspection data requires an ADC system trained to identify killer defects. These killer defects—such as RDL opens, RDL shorts, missing vias and via residue—must be classified with 100% accuracy, so that each defective package on the panel can be identified with confidence. However, some defects may not be apparent until later in the process. For instance, a large particle embedded in the build-up film may not impact the current via layer, but a later RDL pattern that is located on top of the particle could induce RDL bridging due to the particle creating an out-of-focus lithography condition.

As the industry transitions to glass core substrates that may allow for single-side processing, future AICS processes may become more robust. However, package sizes will continue to grow, and RDLs will continue to shrink below a line/space of 5µm. This is a problem for the build-up film because it is not capable of supporting laser-drilled vias less than 10µm. In other words, the technology roadmap will require new photoresist and photo-imageable dielectric processes.

Copper-clad laminate distortion

Now that total overlay and yield loss in AICS have been discussed, let's move on to a discussion about how CCL processing leads to panel distortion and how overlay correction solutions compensate for this. To start with, let's talk about the curing of buildup film. CCL substrate processing requires the curing of buildup film. During this process, the CCL substrate is subjected to repeated thermal cycling, resulting in the distortion of the X and Y coordinates of the interconnect patterns. This distortion impacts the registration of the laser-drilled vias to the lithography-printed RDL.

Here's where the CCL process gets challenging: RDL design typically includes a large landing pad at the end of each interconnecting line/space (l/s) that connects to the vias. The landing pad is significantly larger than the critical dimension of the RDL. By including this feature, the overlay tolerance is increased significantly. For example, if the diameter of the laser-drilled via hole is 30µm, the RDL landing pad could be 50µm to provide an overlay tolerance of +/-10µm. With the interconnect technology roadmap approaching a point of inflection—from 12µm/9µm l/s to below 5µm/5µm l/s—it becomes increasingly difficult for advanced packaging designers to meet this challenge because the large landing pads limit design space. This results in the need to increase the number of RDL layers, along with an increase in cost and potential yield loss. To mitigate this design quandary, smaller RDL landing pads are required, but this can only be achieved if process overlay is improved. With improved overlay performance, RDL and via structures with smaller landing pads can be squeezed into a smaller area, eliminating the need for additional RDL layers. Moreover, this reduces the cost and yield loss risk—i.e., fewer layers mean fewer worries.

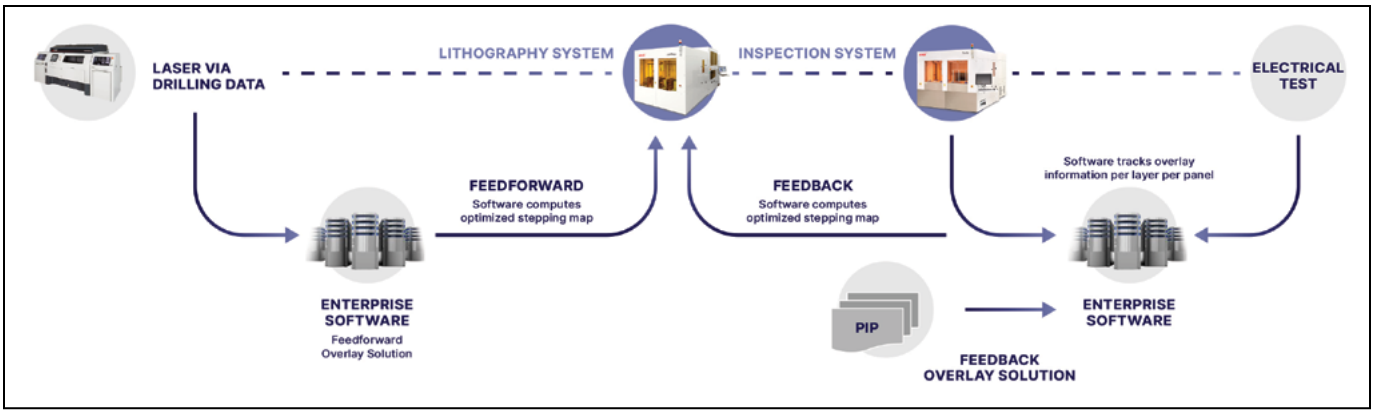


Figure 3: Overlay solution for AICS panels.

To improve process overlay, the lithography system, or stepper, must analyze and compensate for CCL substrate distortion errors. While this sounds simple in principle, the CCL distortion components are complex and extend beyond the traditional six-parameter model supported by most lithography steppers. This nonlinear distortion requires additional higher order lithography system corrections, thereby increasing the complexity of the model.

The stepper's ability to correct for the substrate distortion is only part of the solution. We also need accurate metrology data to generate optimum alignment solutions to compensate for distortion errors. Typically, this data is only available after the lithography process is finished and overlay of the vias to the RDL landing pad is measured. The data is then analyzed and sent back to the stepper to correct panel distortion for future incoming panels (a.k.a. feedback corrections). However, the feedback corrections are only relevant if the panel distortion remains constant for incoming future panels. Sampling plans and periodic metrology can help generate a run-to-run solution. These steps, together with artificial intelligence (AI) and machine-learning software, can correct the dynamic distortion errors exhibited by CCL substrates over time.

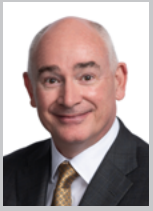
An alternative approach could be to gather metrology data from the substrates after the laser-drilled vias have been created and before the stepper is involved. These are known as feedforward corrections. Feedforward metrology requires a leap of faith, however, because it depends on a laser-drilling tool and stepper working in concert to produce an accurate and reliable dataset to create the stepper alignment solution (**Figure 3**).

In principle, the ideal solution to solve the overlay problem would be to use a feedforward approach where X and Y coordinate data from the laser-drilled via holes are employed to generate an alignment solution. The overlay metrology data will confirm if the feedforward correction is accurate and will highlight the residual errors. If the residual errors are significant, the feedforward model likely needs to be adjusted. Ironically, post-exposure, final overlay metrology could be used to optimize the feedforward model. With machine learning and continued iterations, the model could be continuously adjusted to achieve good overlay with low residuals.

The manufacturing of large packages requiring the heterogeneous integration of chiplets, high-bandwidth memory (HBM) and GPU/CPU is only achievable using AICS processing. To deliver this capability, substrate distortion needs to be characterized and compensation provided in order to maintain high yields and reduce costs. A comprehensive metrology and lithography solution is required. This solution should be used in conjunction with advanced software that can automatically adjust models to compensate for the dynamic substrate distortion components. This approach could extend the roadmap of CCL substrate manufacturing beyond its current design limits, thereby reducing costs and improving yields.

Summary

With the AICS market forecast to reach nearly $25 billion in 2027, according to Yole Group, there is little doubt that AICS will be one of the chief drivers of innovation. However, AICS brings with it significant challenges, like total overlay shifts, yield loss and CCL substrate distortion. And with the number of RDLs soaring to 24 with AICS, any unaddressed errors in any single layer can ruin a substrate that otherwise would have been used in a PLP. However, by applying the techniques in this article, manufacturing teams can improve yield and throughput and reduce costs in this emerging PLP segment of the semiconductor industry, guiding manufacturers away from turbulent waters and steering their ships toward smoother seas.



Biography

Keith Best is the Director of Product Marketing, Lithography, at Onto Innovation, Wilmington, MA. For more than 35 years he has held a range of semiconductor processing and applications positions for both device manufacturing and capital equipment companies. He also has numerous publications and holds 22 US patents in the areas of photolithography and process integration. Email keith.Best@ontoinnovation.com

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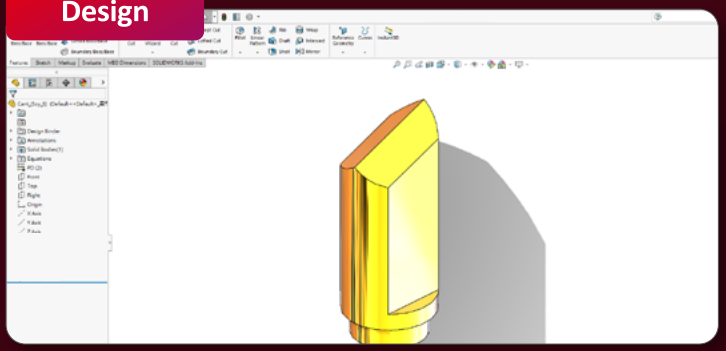
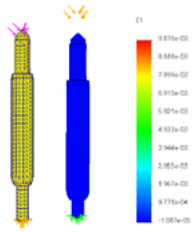
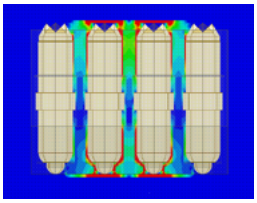


Customizable plunger

Simulation



Stress simulation



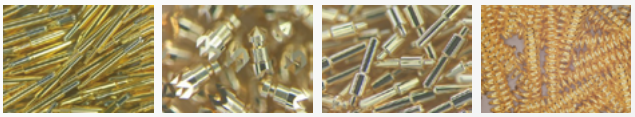
Electrical simulation

Ensuring probe performance and quality by simulation

Manufacturing

CNC

- √ Self-manufacturing parts
- √ Automated recipe configuration



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- √ Various plating materials :

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Assembly

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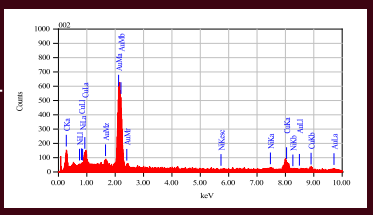
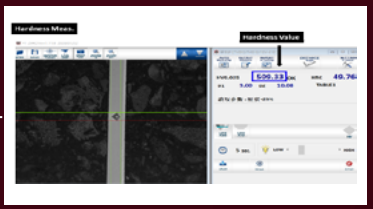
Analysis

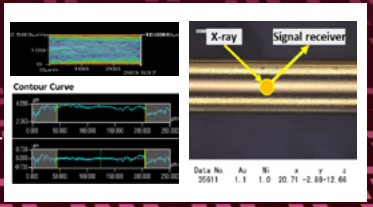
Material EDX



Mechanical property Hardness test



Plating Roughness Meas & Thickness Meas



Automotive gate driver package with galvanically-isolated communication linkage

By Ankur Shah, Burton Carpenter, Fred Brauchler, Di Liu, Pierre Calmes, JM Liu, Xueting Wu [NXP Semiconductors, Inc.]

With legislation driving to reduce CO_2 emissions, electric vehicles (EVs) are a perfect alternative to internal combustion engine (ICE) vehicles and government incentives are encouraging faster adoption from ICE vehicles to EVs. Approximately half of all vehicles sold by 2030 will contain an electrified powertrain [1]. Furthermore, vehicle electrification is driving advanced functional safety, control and protection features in automotive EV electronics. Many on-board systems such as EV traction inverters, DC/DC converters, and on-board chargers are powered by, or connected to, high-voltage power sources. For example, a traction inverter converts DC voltage from a high-voltage battery into a high-current, multi-phase AC voltage to drive the traction motor. Microcontroller unit (MCU) output is not capable of driving a power device (insulated-gate bipolar transistor [IGBT] or silicon carbide [SiC]), which in turn drives the traction motor. Therefore, to drive the power device, an isolated gate driver is essential because of features such as a strong gate drive and overshoot protection; additionally, faster switching allows for higher efficiency, faster reverse recovery, and lower input capacitance, etc.

A 32-lead small outline integrated circuit (SOIC) package with leads on only two sides was selected to meet the creepage and clearance requirements. Internal isolation was achieved by placing a high-voltage dielectric barrier between two stacked die that could communicate by inductive (magnetic) coupling. Galvanic isolation, therefore, was achieved between the high voltage (HV) and low voltage (LV) sides, thereby meeting the UL 1577 requirement for $5000V_{rms}$ isolation for 60 seconds. Accelerated lifetime tests confirmed working voltages up to $1500V_{pk}$ can be maintained for at least 20 years. Finally, the package passed the full suite of Automotive Electronics Council (AEC) Q100 Grade 1 component reliability requirements, including AEC Q006 Cu wire criteria.

Galvanic isolation

Galvanic isolation is the principle of isolating functional sections of electrical systems to prevent current flow—no direct conduction path is permitted. However, energy or information can still be exchanged between the sections by other means, such as capacitive, inductive (magnetic), optical, acoustic or mechanical coupling. Furthermore, the device must meet certain performance criteria and pass AEC Grade 1 component qualification for under-the-hood operation.

An advanced gate driver package makes direct physical electrical connections to both HV and LV domains, therefore, safety and functional requirements necessitate that design, testing and manufacture of the gate driver component ensure galvanic isolation between these domains.

In a typical application as shown in Figure 1, the gate driver is electrically connected to two isolated voltage domains, termed LV and HV. The LV leads connect to the automobile control system powered by the 12V~48V battery grounded to the vehicle chassis. Meanwhile, the HV leads connect to the 400V~800V battery that powers the drivetrain motors. For safety and functional reasons, the package must maintain galvanic isolation between the LV and HV domains. Functional safety requirements for the gate drivers is at Automotive Safety Integrity Level D (ASIL-D).

The development and release of this gate driver package occurred in two phases. A summary for the initial 7.72mm creepage automotive drivetrain application was summarized by Carpenter, et al. [2]. This paper provides an overview of the upgraded package with greater creepage, enhanced design criteria, and improved HV performance: achieving a comparative tracking index (CTI) >600V (Material Group 1), creepage >8mm, and common mode transient immunity (CMTI) >200V/nsec.

Product features

NXP's gate driver IC (GDIC) is functionally safe (ASIL C/D compliant) and can be used with both 400V and 800V traction inverter systems. These new isolated GDICs have features optimized for operation with both IGBT and SiC power devices. These features include dynamic gate strength control (+/-10A to +/-30A)

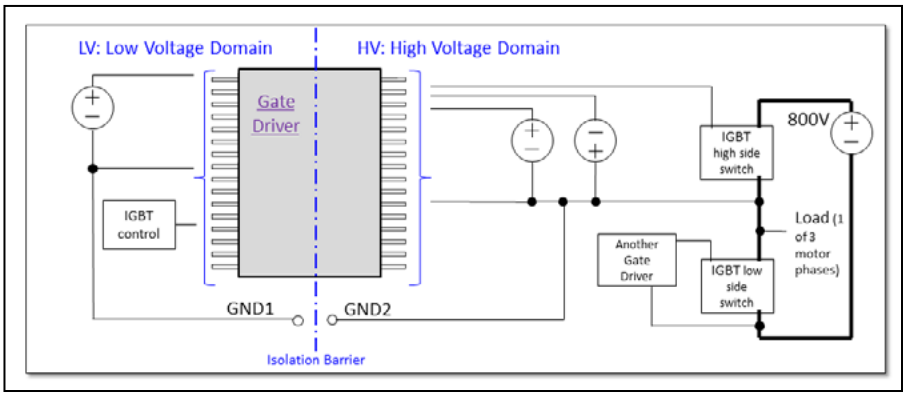


Figure 1: Schematic of gate driver application.

Category	Item	Criteria
Communication Performance	Noise Immunity	CMTI > 200 V/ns
	Comm Delay	<10 ns
	Direction	2-way communication
	Power	<2.5mW per channel
Reliability	Component	AEC Grade 1 + Cu Wire
Galvanic Isolation	High Side Voltage	Drive motors powered by 800V DC battery
	LV-HV Isolation	Galvanic isolation 5000V_{rms} for > 1 min
Manufacturing	Yield	Equivalent to similar package

Table 1: Key design criteria.

for optimized drive capability. Several external bill of materials (BOM) components are reduced or removed though features integrated into the gate drivers, thereby providing system-level board space and cost savings. This new GDIC incorporates programmable control for protections, monitoring, and diagnostic features such as <1µs short-circuit detection, temperature, over-voltage/over-current protection and power device aging detection, which enable optimized performance and predictive maintenance of the traction inverter and power devices.

System Level Standards	
IEC 60065-1 [3]	Audio / Video Safety requirements
IEC 60950-1 [4]	Information Technology Equipment - Safety
IEC 61010-1 [5]	Electrical equipment for measurement, control, and laboratory - Safety
IEC 61800-5 [6]	Motor Drives & Inverters Safety requirements
IEC 61000-4-5 [7]	Surge immunity test (needed for connection to European line voltage)
Component Level Standards	
AEC Q100 H [8]	Automotive Component Qualification
AEC Q006 A [9]	Addendum to Q100 for components with Cu wirebond
UL 1577 [10]	Universal Digital Isolator Standard – Accepted/Mandated for all Digital Isolators worldwide
IEC 60747-17 [11]	Magnetic and capacitive coupler safety standard
VDE 0884-10 VDE 0884-11 [12]	Magnetic and capacitive coupler safety standard
Coordination Standards: attempt by IEC to harmonize disparate electromechanical standards	
IEC 60664-1 [13]	Insulation Coordination for equipment within low voltage systems
Test Methods	
IEC 60270 [14]	High-voltage test techniques – Partial discharge measurements

Table 2: Applicable standards and description.

Design objectives

Key performance, reliability, isolation and manufacturing criteria necessary to satisfy the application requirements are summarized in Table 1. Communication performance refers to data transfer between voltage domains. In fact, galvanic isolation demands a multitude of requirements driven by a variety of industry standards, summarized in Table 2 (references in table). Component reliability qualification followed the norms of AEC Q100 and Q006.

Package design

To achieve galvanic isolation, the package is divided into LV and HV regions that could electrically connect to their respective system domains but remain insulated from each other by appropriate isolation barriers. The design required isolation strategies external to the package (outside the mold body) and internal to the package (inside the mold body). The standards in Table 2 define a variety of metrics to ensure packages and systems can meet their stated isolation specifications. Table 3 summarizes exemplary parameters from these standards.

External isolation is achieved by selecting a package outline to meet the first two parameters in Table 3: creepage and clearance. A 32-lead 7.5mm x 11.0mm wide-body SOIC package is ideal. With leads on only two sides, leads 1-16 are connected to the LV domain and leads 17-32 to the HV domain. Figure 2 illustrates that the creepage path around

Purpose	Parameter	Standard/Definition	Target Spec
Prevent flash over or arcing between package external leads	Creepage	IEC 60664-1 Shortest distance along the surface of a solid insulating material between two conductive parts	≥ 8 mm
	Clearance	IEC 60664-1 Shortest distance in the air between two conductive parts	≥ 8 mm
Surge protection Ex. Lightning strike	V_{IOSM}	IEC 60747-17 Maximum Surge Isolation Voltage	10 kV_{pk} 50x ~50µsec pulses
Allow time for system safe shutdown	V_{ISO}	UL 1577 Maximum Withstanding Isolation Voltage	5 kV_{rms} 1 min
Lifetime working voltage	V_{IORM}	VDE 0884-11 Maximum Repetitive Peak Isolation Voltage	1.5 kV_{pk} 20 years
Production screen to weed out defective units	PD (Partial Discharge)	VDE 0884-10, -11 A localized electrical discharge that partially bridges the insulation between conductors	≤5pC @ 2.9 kV_{pk}
Classify surface insulation resistance of mold compound	CTI (Comparative tracking index)	VDE 0884-10, -11 An insulation material's resistance to damage and surface current when exposed to conductive contamination.	≥ 600V

Table 3: Isolation metrics.

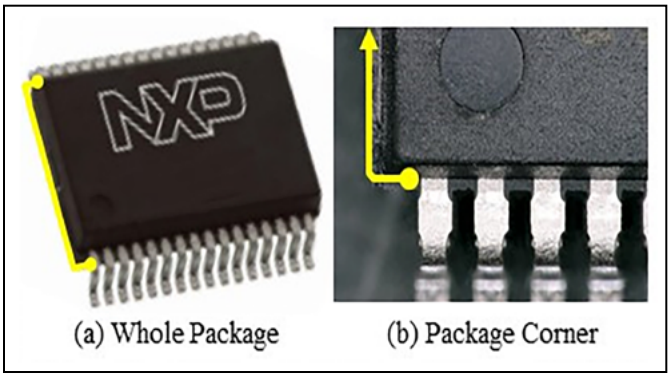


Figure 2: 32-lead SOIC package (7.5mm x 11.0mm). The yellow line indicates creepage path.

Figure 3: Package side view. The red line indicates clearance path.

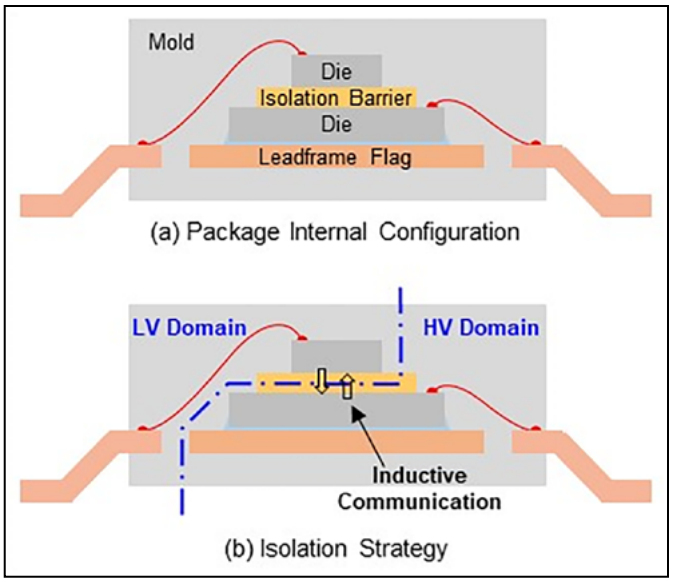


Figure 4: Schematic of package internal structure.

the package edge could maintain the specification value even with worst-case tolerance stack-up (lead placement, body size, etc.). Similarly, the heels of the leads could maintain clearance under the package mold body as shown in Figure 3.

The package internal configuration and isolation strategy are shown in Figure 4. Device functionality is partitioned into two dies—one for each domain. The stacked structure permits communication elements on each die to directly transfer data using inductive coupling across the galvanic isolation barrier. The materials and internal spacings are designed to pass the last five HV isolation tests in Table 3. Note that maximum surge isolation voltage (V_{IOSM}), maximum withstanding isolation voltage (V_{ISO}), and maximum repetitive peak isolation voltage (V_{IORM}) are intended to ensure isolation integrity on three very different time scales: microseconds, seconds and years, respectively. Known as Type Tests, these three can only be performed on representative samples not intended for shipment. In other words, the tests are considered destructive even for passing devices. On the other hand, Partial Discharge (PD) method B1 is an industry standard production screening method. Furthermore, safety compliance to UL 1577, IEC 60664, IEC 6074717, and VDE 0884-10 have been certified. VDE 0884-11 certification is ongoing.

Discussion

Critical distances in the definitions of creepage and clearance (Table 3) ensure external isolation. While not explicit, minimum spacing must be maintained between HV and LV domains within the package to pass the internal isolation requirements. The cross section in Figure 5 highlights three critical geometry locations in the package as follows: A: Isolation barrier within the die stack; B: LV leads and die flag; and C: Wire loop from the LV die crossing over the HV die. Each specific critical distance depends on the dielectric breakdown strength of intervening material.

The isolation barrier (A) thickness balanced competing requirements: thicker improved isolation, but thinner

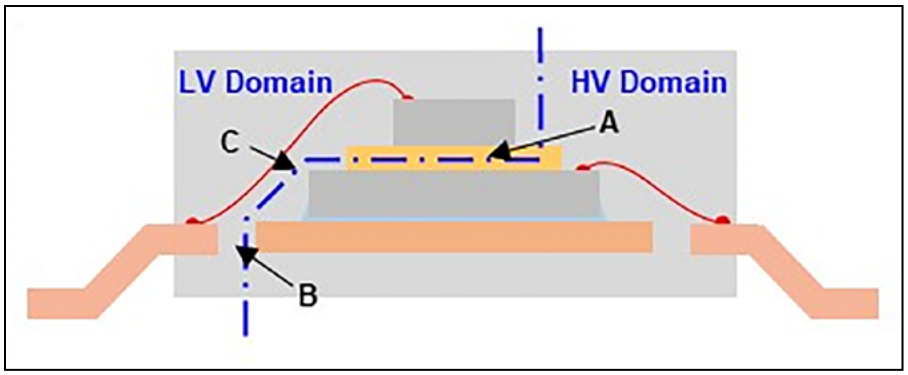


Figure 5: Critical internal package geometries.

reduced communication loss and power consumption. The final design value achieved this balance. Margin was demonstrated through electrical simulations and experimental studies. Maximum and minimum thickness barriers maintained both device functionality and V_{ISO} isolation (5kVrms for over 60 seconds). Likewise, the inner lead to flag spacing (B) was designed to perform at the worst-case manufacturing tolerance. V_{ISO} actually passed greater than 8kVrms before failing in these locations. Finally, wire looping (C) always maintained the same minimum distance required for location B.

Defectivity control was critical in the isolation barrier (A) because the narrow spacing between die intensified the electric field strength. Small voids or foreign matter could cause either short-term failures under voltage peaks or premature wear-out over time due to degradation of the insulation around the defect. PD testing effectively identified such units. Void area was correlated to PD capacitance, and suitable production control limits were established. The two-stage production PD test (isolation barrier check at the first voltage plus capacitance measurement at the second voltage) ensured that all units could meet the field isolation requirements on all time scales: microseconds, seconds and years.

Summary

A package designed for automotive high-voltage gate driver applications was partitioned into two galvanically-isolated domains to meet functional and safety requirements. Inductive coupling between two stacked dies permits die-to-die communications through an isolation barrier. This package was tested to a variety of industry system and component safety standards from UL, VDE and IEC. Representative HV stress tests were described with an explanation for their relevance to the application. The package passed the representative HV type tests, including V_{IOSM}, V_{ISO}, and V_{IORM}. Additionally, all requirements of AEC Grade 1 copper wire qualifications were met.

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Biographies

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Automotive LiDAR: Photonics assembly requirements and trends

By Limin Zhou, Avy Yi [MRSI, a part of Mycronic Group]

In this paper, the similarities and differences between automotive light detection and ranging (LiDAR) and optical transceivers are compared. The photonics device assembly requirements and trends in automotive LiDAR are introduced. From the analysis, an assembly solution for automotive LiDAR is explained. Finally, a demonstration of the solution with actual assembly experiments for typical edge-emitting lasers (EELs) and vertical cavity surface emitting laser (VCSEL) chips for automotive LiDAR are presented.

Overview

Vehicular safety has always been very important to the automotive industry—and the situational awareness enabled by advanced sensors plays a critical role in building safe self-driving vehicles. Most car makers believe LiDAR is necessary and important for both advanced driving assistance systems (ADAS) and autonomous vehicles (AVs). The demand for automotive LiDAR in ADAS applications is growing at a high double-digit compound annual growth rate (CAGR), and mass production of automotive LiDAR is rapidly becoming a reality. Driven by new technologies and economies of scale, automotive LiDARs are becoming lighter, thinner, and cheaper. The high-reliability assembly of photonics devices is the key challenge for the mass production of highly-reliable automotive LiDAR. To address this challenge, it is necessary to understand the assembly needs and technology trends of automotive LiDAR, and then provide the best photonics device assembly solution.

Photonics devices assembly in automotive LiDAR

Automotive LiDAR is a complex photonics sensor system that consists of multiple optical components, including lasers, amplifiers, phase and amplitude-control low-noise photodiodes, mode converters, and optical waveguides, etc. Table 1 shows the comparison of automotive LiDAR and optical transceivers. Based on the table entries, automotive LiDAR is in an earlier phase of product life cycle than the optical transceiver.

Items	Automotive LiDAR	Optical Transceiver
Performance	Range, resolution, frame rate...	Data rate, distance...
Package	No industrial standard, Customer Spec	Industrial standard, SFP/CFP/QSFP/OSFP/...
Standard	AEC-Q	Telcordia GR-468
Temperature	Reliability: (AEC-Q100-REV-H)	Reliability: (Telcordia GR-468-CORE)
	Grade 0: -40°C to +150°C	Storage temperature range is from -40 °C to 85 °C
	Grade 1: -40°C to +125°C	Operation temperature range is from -5 °C to 75 °C (Datacom 0°C to 70°C, 15°C to 55°C)
	Grade 2: -40°C to +105°C	
	Grade 3: -40°C to +85°C	
	(ambient operating temperature range)	
Volume	High mix and volume from low to high, depends on customer application	High volume for datacom transceiver
Innovation	Fast-paced innovation and NPI, need flexible multi-dies and multi-processes	Steady pace of innovation and NPI, need a relatively flexible die bonding process machine
Customer expectation	Lower cost, higher reliability, higher performance	Lower cost, higher bit rate, lower consumption
Lifetime	10k-100k hrs/>10 years	Datacom >3~5 years
Quality System	IATF 16949	ISO 9000
Manufacturing	No mature solutions for assembly & testing, developed by LiDAR suppliers and customers	Proven solutions for assembly and testing

Table 1: Automotive LiDAR vs. optical transceiver.

From Table 1, we know automotive LiDAR does not have industry standards for packages and optoelectronics (OE) interfaces at this point in time. The end users of automotive LiDAR have diverse package design requirements to fit it into their cars. This means that the vehicle manufacturers decide on the package form and interface of automotive LiDAR devices. If a LiDAR supplier targets multiple vehicle models from multiple car companies, there will be a wide range of package form factors. Manufacturing in the automotive LiDAR industry, therefore, will be high-mix low-volume for the time being. As a result, LiDAR suppliers have to provide flexible equipment to support different customers' packaging and assembly process designs.

The quality system of the LiDAR supplier has to pass the IATF 16949 certification process. Additionally, automotive LiDAR has to pass the AEC-Q series reliability test, especially the higher temperature operation reliability test. While the reliability of the photonics chips/dies must be high enough to ensure the final products meeting the AEC-Q reliability requirements, the chip assembly solution must also meet the same reliability standard. Laser chips and their assembly are the most critical factors in determining the reliability of the LiDAR system. High-reliability laser chip assembly can enable the high-reliability automotive LiDAR volume manufacturing to meet IATF 16949 zero defect requirements. To that end, advanced equipment and processes are needed.

With the advancement of new technologies, we find that automotive LiDAR imaging technology has evolved from mechanically-scanned LiDAR to hybrid solid-state LiDAR, and then to solid-state LiDAR. The packaging of automotive LiDAR evolved from discrete

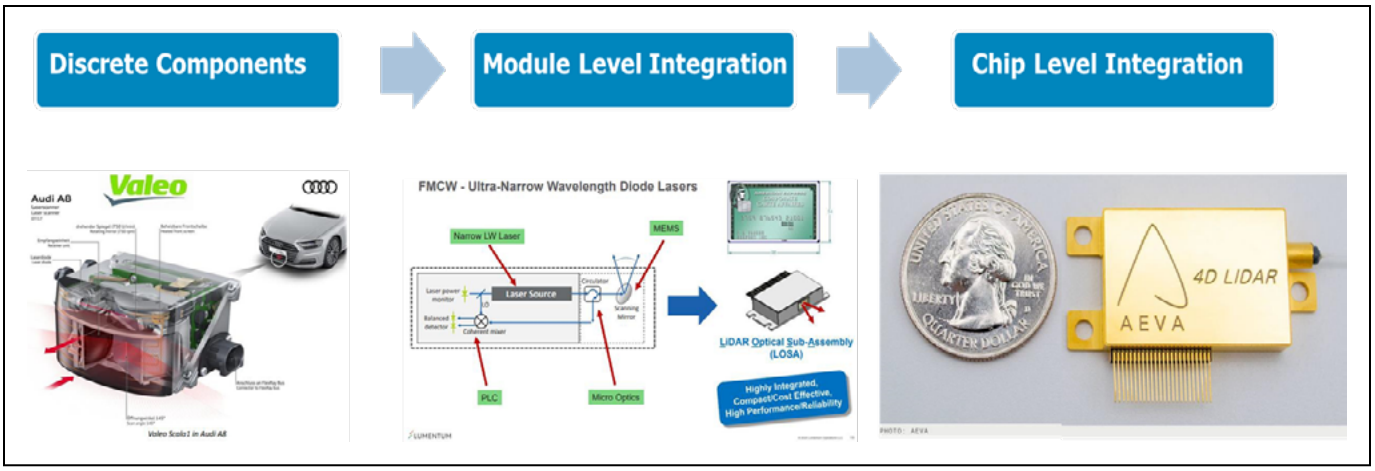

Figure 1: Automotive LiDAR package design trends.

components to module-level integration, and even chip-level integration (see Figure 1). The market is trending towards highly-integrated, thinner and cheaper products [1-4]. Consequently, higher accuracy assembly is required to manufacture the photonics devices. Automotive LiDAR has a similar photonics device assembly process to that of the optical transceivers, and the assembly accuracy and other requirements are also similar. Depending on the different laser package designs, from 5µm to 0.5µm is the typical high-accuracy requirement for laser die; other parts, however, may have less critical accuracy requirements. In general, most edge-emitting laser dies are attached with a eutectic process (some may use an epoxy process); VCSEL laser dies are usually attached with an epoxy process, and an optical lens with ultraviolet (UV) epoxy plus in situ curing.

According to Yole Intelligence [5], "The LiDAR market for passenger cars (PC) and light commercial vehicle (LCV) and robotaxis is expected to reach $4.5B in 2028 with a 55% CAGR from 2023." So the LiDAR volume will ramp up very fast. In the long run, technological choices will have to be made to be aligned with mass production, low cost, and high performance, and pricing pressure will increase. Lower cost and high-reliability mass production will be essential. Therefore, the photonics devices assembly solution for automotive LiDAR must have higher efficiency for low-cost volume manufacturing. To summarize, the photonics assembly requirements for automotive LiDAR are high reliability, high flexibility, high accuracy, high speed and fully automated.

Solutions for photonics die assembly

Similar to optical transceivers, higher flexibility, higher reliability, higher accuracy, and higher speed (efficiency) are the solutions to address the challenges of volume manufacturing in the automotive LiDAR industry. We have provided solutions to the industry challenges with our MRSI-H-LD die bonder (Figure 2).

Our bonder has an accuracy of ±1.5µm@3σ. Higher accuracy is also available as an option (±1µm @3σ). This bonder has a very stable gantry head and is equipped with a patented tool changer that does not require recalibration after the tool change. The tool changer is equipped with a 12-tip turret to achieve "on-the-

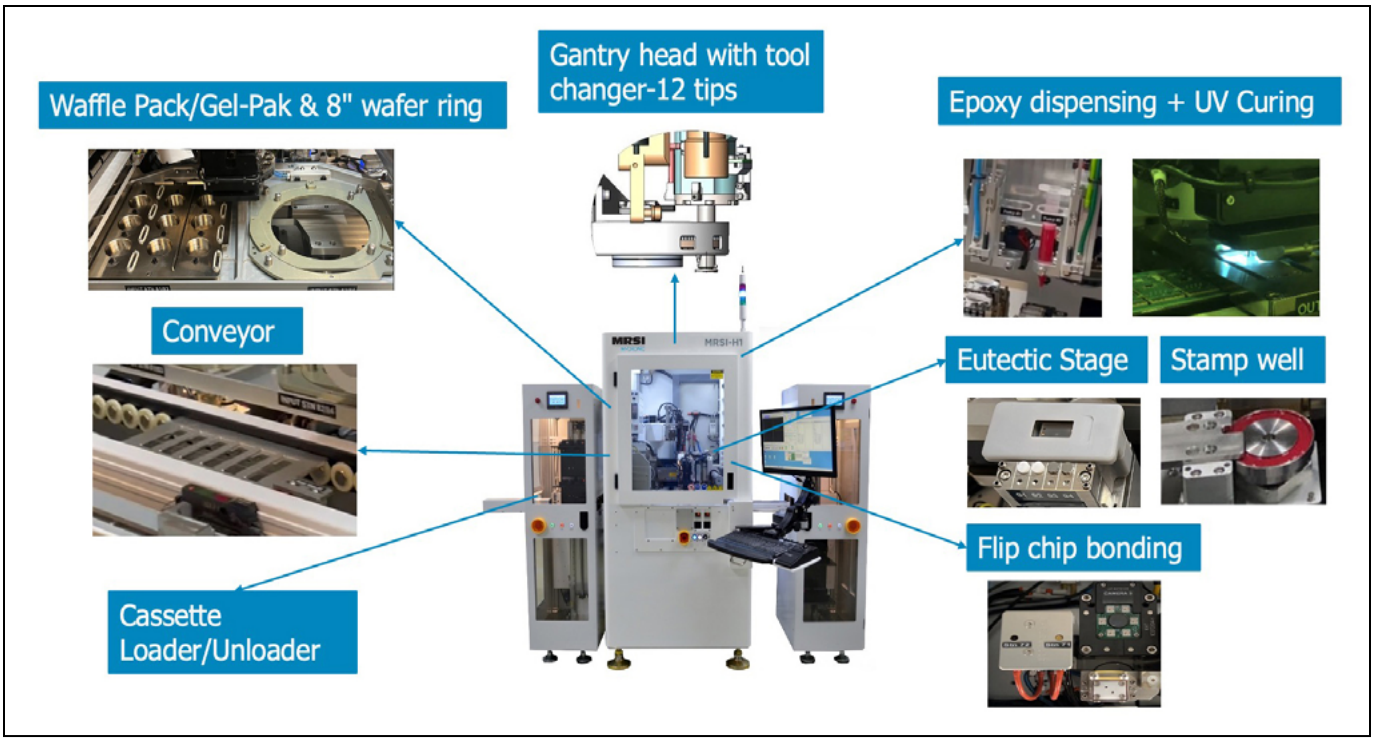

Figure 2: MRSI-H-LD die bonding machine features.

fly" tool change for the multi-die process. The bonder also has multiple die bonding process capabilities and supports eutectic bonding, epoxy stamping and dispensing, UV curing, and flip-chip bonding.

Experiments

The laser chip assembly process is the most critical step that affects the reliability of automotive LiDAR assembly. The experiments we performed involved the selection of two typical laser chips that are used for automotive LiDAR applications. One is the 905nm EEL high-power laser chip and the other is the 905nm high-density multi-junction VCSEL chip.

For the 905nm EEL high-power laser chip bonding, both eutectic and epoxy processes are used in automotive LiDAR depending on the laser package design. We completed experiments for eutectic bonding and had the following results: 1) Both X/Y post-bonding accuracy measurements are 2.7µm@3σ and the angle accuracy is 0.13°@3σ; and 2) For the epoxy process experiment, the post-bonding accuracy for X/Y is 2.8µm@3σ/3.0µm@3σ, respectively, and the angle accuracy is 0.27°@3σ. **Figure 3** shows the 905nm EEL high-power laser die bonding results for the eutectic and epoxy processes.

Typically, for 905nm high-density multi-junction VCSEL chip bonding,

Eutectic Post Bonding Results (*mm*)

Item	X	Y	Angle
MAX	0.0085	0.7241	0.14
MIN	0.0069	0.7223	0.053
Range	0.0016	0.0018	0.087
3σ	0.0027	0.0027	0.132

Epoxy Post Bonding Results (*mm*)

Item	X	Y	Angle
MAX	0.0011	0.0011	0.218
MIN	-0.0007	-0.0011	0.057
Range	0.0018	0.0022	0.161
3σ	0.0028	0.0030	0.276

Figure 3: 905nm EEL high power laser die bonding results by eutectic and epoxy processes.

Die Post Bonding Results *(mm)*

Sample x30	X	Y	Angle
MAX	1.0017	0.0018	0.2090
MIN	0.9991	0.0001	-0.0100
Range	0.0026	0.0017	0.2190
3*stdev	0.0019745	0.0013476	0.1784532

Figure 4: High-density multi-junction VCSEL chips epoxy COB bonding results.

photonics device manufacturers use the epoxy chip on board (COB) process for automotive LiDAR applications. We completed experiments for the epoxy COB die bonding and had the following results: 1) The X/Y post-bonding accuracy is 1.9µm@3σ and 1.3µm@3σ, respectively, and the angle accuracy is 0.17°@3σ. Figure 4 shows the high-density multi-junction VCSEL chip epoxy COB die bonding results.

Summary

Based on our discussions about automotive LiDAR assembly requirements and technical trends, and the experiments on laser die assembly using the MRSI-H-LD 1.5µm high-accuracy die bonder, the following conclusions can be drawn:

1. The automotive LiDAR photonics device assembly process is similar to the process used for optical transceivers but has higher reliability requirements.
2. High-flexibility, high-reliability, high-accuracy, and high-speed process equipment is the best solution to support automotive LiDAR high-mix/high-volume manufacturing.

Acknowledgment

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High-speed probe card architecture for high-end devices

By Xin-Reng Foo, Chee Hoe Lin [AMD Singapore] Alberto Berizzi [TECHNOPROBE Italy]

Demand for artificial intelligence (AI), machine learning (ML), high-performance computing (HPC), hyperscale data centers and Cloud computing has led to a rapid development of advanced technologies. These technologies allowed the processing of a high-volume of data as well as solving complex and performance-intensive problems. This changes the overall landscape of product development by enabling a faster time to market and a short prototyping cycle while maintaining control of the overall product development cost. The global HPC market was valued at US$ 41.22 billion in 2022 and is expected to hit around US$ 85.34 billion by 2032; it is poised to grow at a compound annual growth rate (CAGR) of 7.6% during the forecast period 2023 to 2032 [1]. Nearly every company in the Fortune 100 list uses HPC, and its popularity is increasing at a rapid rate. Some of the industries using HPC include aerospace, manufacturing, finance technology (Fintech), healthcare, and retail [2-3].

Leveraging of advanced packaging used in chiplets technology is driving demand for on-chip interconnect between the computing cores, I/Os and memory controllers (MCs). For next-generation devices, developers are driving even greater computing power, higher resolution graphics, and improved media processing into the integrated chips that enable these systems. This high level of integration is causing on-chip communications and transaction handling to become a system constraint, thereby limiting the achievable performance of multi-die packaging regardless of the level of optimization of the individual central processing units (CPU), graphics processing units (GPU), and other intellectual property (IP) blocks [4]. This rapid development of technology pushes the requirement for high-end probe cards, specifically in terms of meeting the ever-increasing speed requirement for reliable, high-speed, and low-latency interconnects.

Sort hardware design

Achieving design targets in sort hardware design is a challenging and complicated process. The standard probe card solutions are not able to meet all HPC testing requirements inclusive of high-speed I/O (HSIO), high current-carrying capacity and high insertion count. The bump pattern of a HSIO system on chip (SoC) block from an IP vendor is often not optimized for signal integrity that may contribute to impedance mismatches at the transitions from wafer to probe head and probe card. These impedance mismatches cause reflection that affect signal quality at the transceiver and receiver. Additionally, the combination of channel loss, signal to noise ratio (SNR), and cross talk will impact the channel performance. Eye diagram, S-parameters and time domain reflectometry (TDR) plots are some of the ways to assess probe card SI figures of merit. It is possible to optimize a probe card design by analyzing these plots. Figure 1 shows an example of a closed eye due to probe card impedance mismatches at 25GT/s.

Sort hardware design sign off is mainly based on simulation data. Therefore, discrepancies may exist between design expectations and the

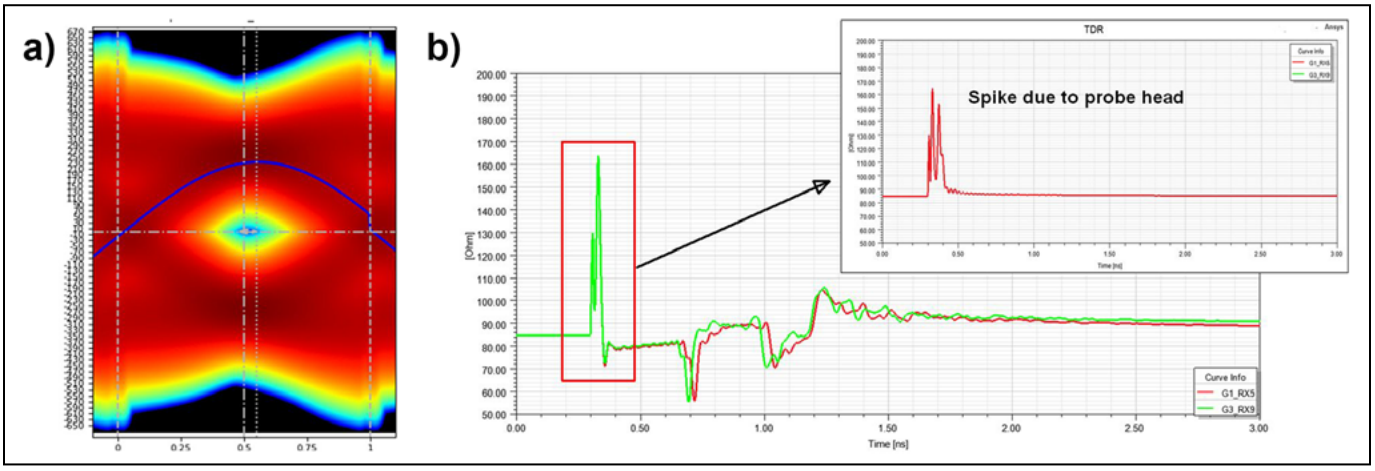

Figure 1: a) (left) Closed eye at NRZ 25GT/s; and b) (right) TDR plot of probe card signal path from the device under test (DUT) to the tester channel.

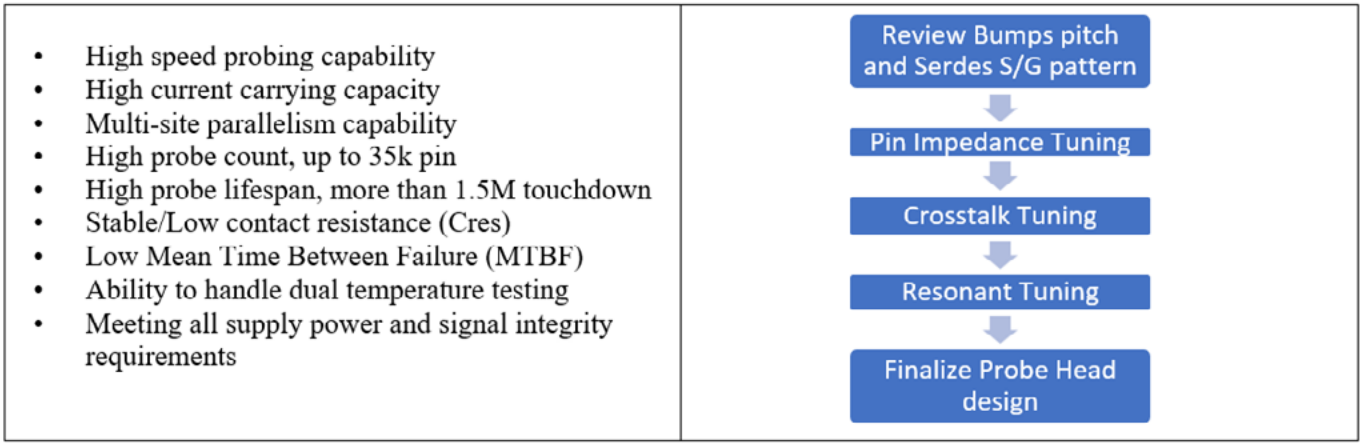

Figure 2: Main design challenges for high-end probe cards for HPC applications and the development process flow.

final hardware deployed in high-volume manufacturing (HVM) product testing. These discrepancies will have a negative impact on product binning and performance tuning thereby leading to a deviation in speed binning results and can lead to a product definition that is not optimized. An incorrect or compromised product definition can lead to a high rate of false negatives and result in the scrapping of good dies or result in more re-screen testing to compensate for the yield loss. Furthermore, such incorrect product definitions can also lead to a high rate of false positive test results that increase the cost of test because the die may have gone through a higher number of test insertions before being flagged as failed. In the worst-case scenario, an underperforming die may escape the tests and result in a possible return materials authorization (RMA) request (from the field) in the future.

The objective of this work is to document the design process

to develop a high-performance probe card that meets the design requirements. This learning could be applied for future designs.

Sort hardware optimization

Figure 2 shows the main design challenges for a high-end probe card for HPC applications and the development process flow formulated by the authors.

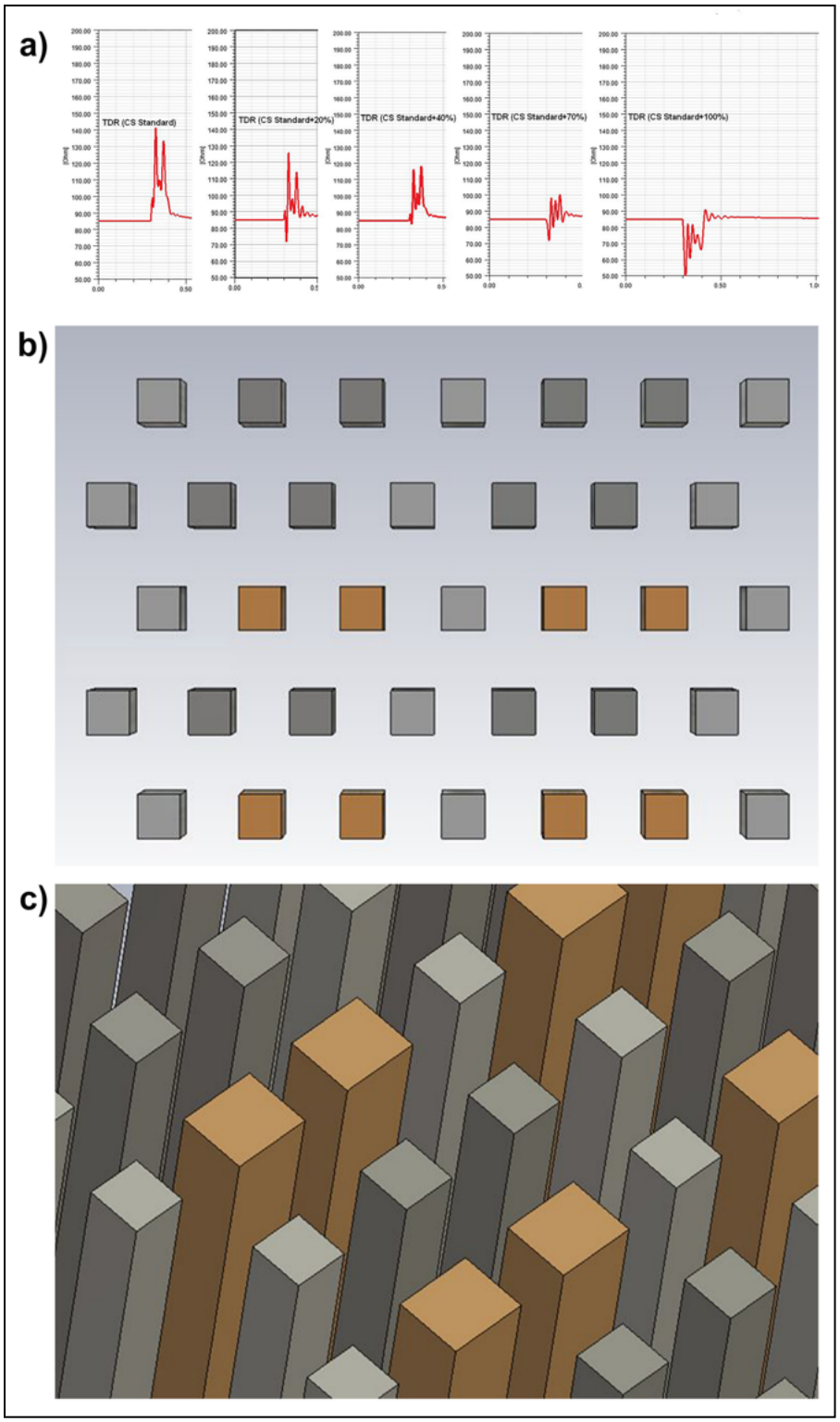

Figure 3: Probe dimension optimization: a) (top panel) TDR of HSIO probe cross-section (CS) variation; b) (middle panel) Top view of enlarged CS probes; and c) (bottom panel) Top view of enlarged CS probes.

The following sections describe the development and characterization processes of new probe technology dedicated to addressing high-speed performance. This new technology needs to be compliant with both new high-speed performance requirements for advanced chip-to-chip interconnects and other challenges required by high-end devices like high current carrying capacity, force control, lifetime, and so on.

Probe cross-section tuning. For an 85Ω system impedance HSIO channel, both driver and receiver must align with the required impedance matching by design. The impedance control methodology for a printed circuit board (PCB) and package using trace line/space width, dielectric material and stack up, is

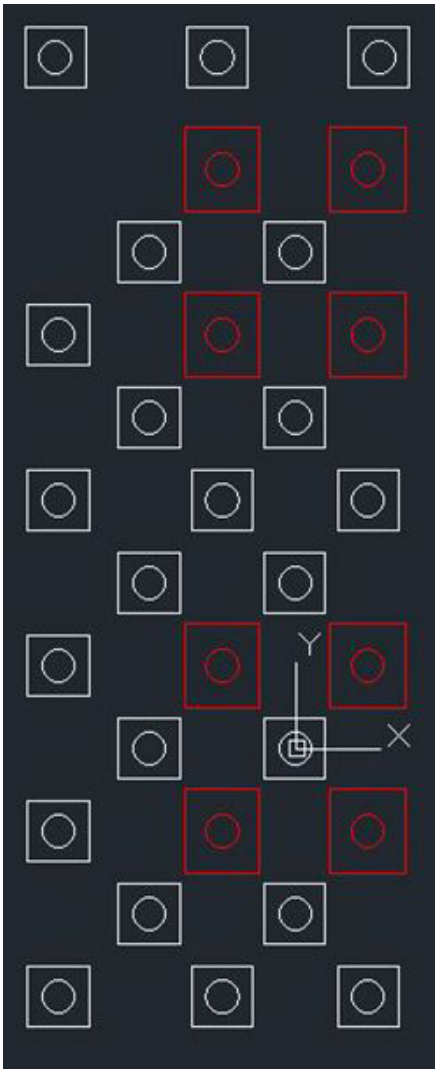

Figure 4: Probe cross-section physical constraint.

well developed. Probe impedance control on the other hand, is not well defined; it is also highly dependent on the bump pattern. Designing a probe with a target impedance is highly challenging as the probe dimensions must meet both signal integrity and mechanical requirements. The probe technology we are presenting in this article allows the modification of a probe's dimensions while keeping the same mechanical behavior among probes of different dimensions that are inside the same probe head. This technology improvement allows the fine tuning of the HSIO probe cross section (CS), which varies the gap between each probe with the building block to match the target impedance. CS changes can be observed in Figure 3. The simulations show that probes enlarged at +20% and +40% in CS are the best optimized case for a target impedance of 85Ω.

Faraday's cage concept. The cross-section optimization concept has two main limitations: 1) physical constraints based on the probe head mechanical structure; and 2) a probe's coupling effect that contributes to cross talk. Although performance improvement can be seen with the probe cross-section optimization, which leverages new technology that allows larger cross-section variation, the primary limitation for the probe dimension is due to the keep-out zone in the placeholder design rule constraint.

Each probe is inserted in a placeholder (holes). As the cross-sectional area of the probes increases, the dimension of the holes will increase at the same time. To maintain structural integrity of the probe head, the hole clearance between the closest probes must comply with the mechanical design rule. Any design rule violation will result in the probe head guide plate cracking during test operation. With an enlargement of +20% cross-sectional area, structural integrity can still be met. But with more than +20% enlargement, structural integrity will be impacted as seen in Figure 4. To achieve signal integrity improvement solely through the probe's cross-sectional area increase is not sufficient.

Another limitation on the probe's dimensions arises from concerns about cross talk. As the probe's cross section increases by +20% and beyond (Figure 5) it reduces the impedance peak, thereby improving the return loss (RL). The cross-talk performance, however, is decreased compared to the standard cross section. Further optimization has been required to improve RL, insertion loss (IL) and cross-talk performance all together. Various design of experiment (DOE) trials were conducted to find a balance among the three trade-offs.

The final optimized results were achieved by replacing the ground probes with probes of larger dimensions than the signal probe (inversion probe placement) and changing the probe orientation inside the probe head. A large ground probe enables the same return loss and insertion loss improvement without decreasing cross-talk performance. In addition, the rotation of the probe placement by 45°, as shown in Figure 6, will further improve the cross-talk performance of the setup so that it approximates the performance of a Faraday cage.

High-end probe card features. The new concept of using cross-section optimization and a Faraday cage must be integrated with all other technologies needed by high-end probe cards to achieve all the features required by a high-end device. A collaboration effort with Technoprobe was established to develop a product line of hybrid probe solutions called Merlion. This new probe solution featured the Technoprobe patented HiP architecture whereby additional features are inserted in the probe head with the aim of distributing the current more evenly at power (PWR) and ground (GND) levels (Figure 7). SA2 probe alloy was adopted as the probe material. SA2 provided high strength and high conductivity coupled with low and stable contact resistance. The extended lifetime (XLT) probe head design is also being integrated into the probe head design to extend the probe head lifetime (Figure 8). The combination of HIP and SA2 resulted in a high current-carrying capacity probe solution that was able to support the coming challenges in probing applications for HPC with a lower cost of ownership when using the XLT solution.

Probe head resonant optimization. The cross-section tuning and Faraday cage concept have been applied to different probe classes to evaluate performance (i.e., the probe's self-resonance frequency is length dependent and therefore, probe-class

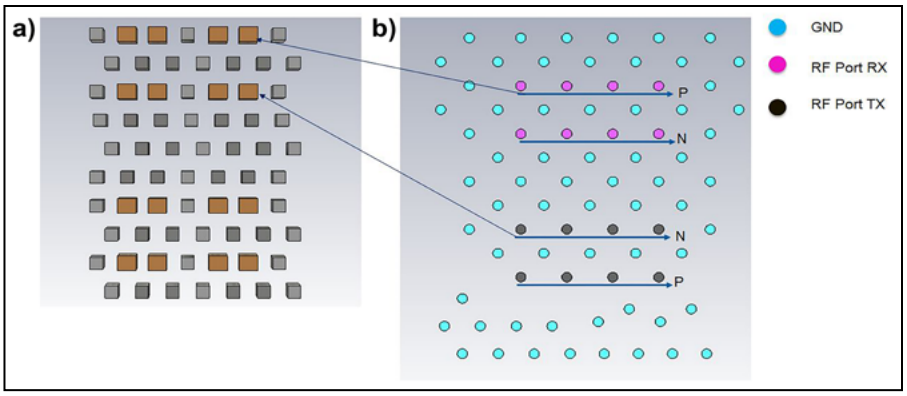

Figure 5: Probe array with enlarged probes: a) (left) Enlarged placement of non-rotated probes; and b) (right) Probe placement positions.

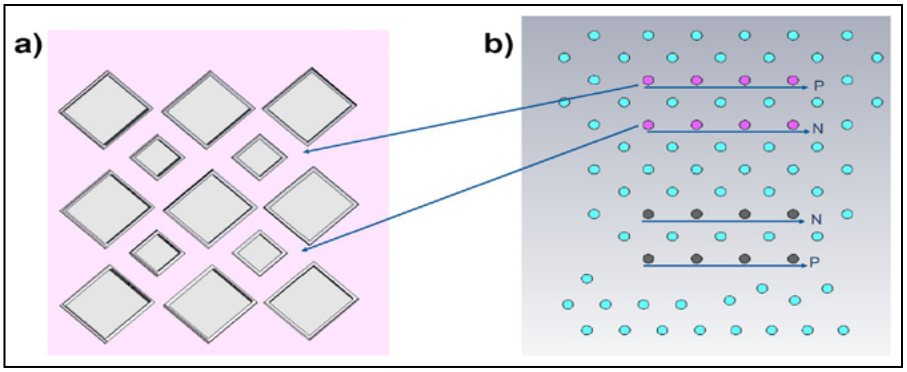

Figure 6: Probe cross-section physical constraints: a) (left) Inversion probe placement of rotated probes; and b) (right) Probe placement positions.

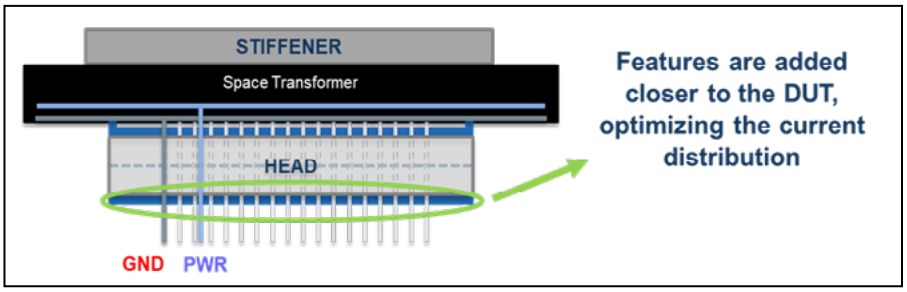

Figure 7: Techoprobe HIP architecture.

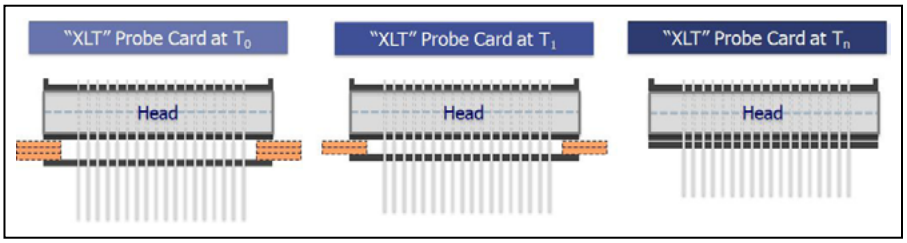

Figure 8: Techoprobe XLT architecture.

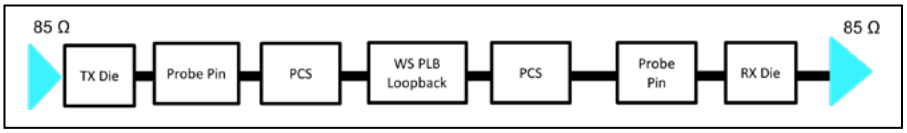

Figure 9: External loopback channel model.

Name	Length	CSA	Rotation angle
Merlion 1	REF	REF+ 40%	0°
Merlion 2	REF – 25%	REF+ 40%	0°
Merlion 3	REF – 40%	REF+ 40%	0°
Merlion 4	REF	Optimized	45°
Merlion 5	REF – 25%	Optimized	45°
Merlion 6	REF – 40%	Optimized	45°

Table 1: Probe dimension combinations.

dependent. An external loopback channel simulation was conducted based on different combinations of probe length (Figure 9), cross-sectional area (CSA) and rotation angle. The aim is to find the optimal insertion to cross-talk ratio (ICR) and nominal channel eye width (EW) and eye height (EH) for a 32GT/s application as shown in Figure 10 and Table 1.

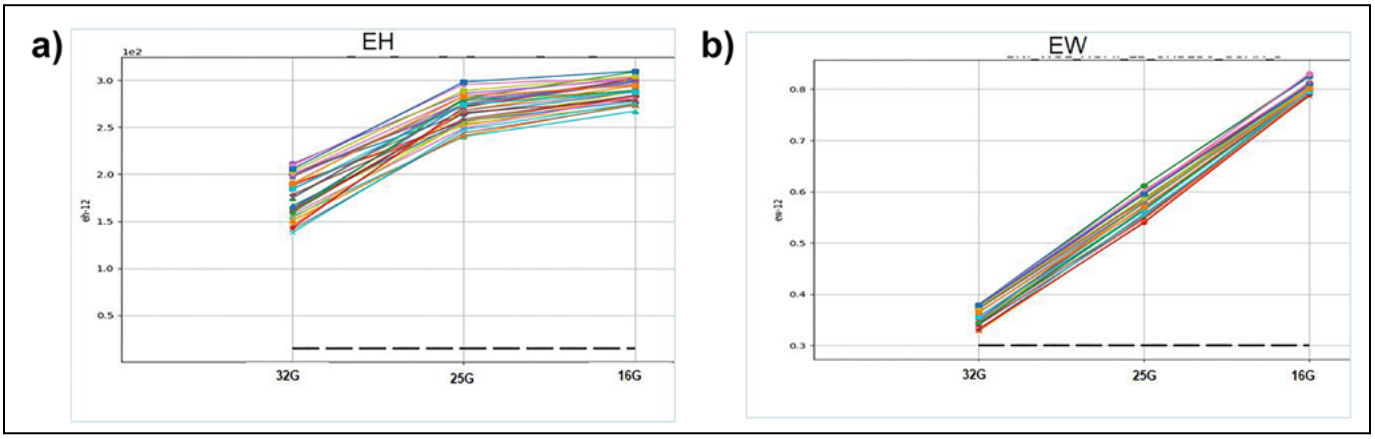

Figure 10: Eye diagram of Merlion 6 at: a) (left) Eye height, and b) (right) Eye width.

Probe Needle (Hybrid)	Probe Length	Probe Dimension	Rotation	Probe Intrinsic Resonant	Insertion to Crosstalk Ratio (ICR)	Nominal Channel Eye Width and Height
Merlion 1	REF	CS + 40%	0°	25GHz	20dB	120mV , 0.25UI
Merlion 2	REF - 25%	CS + 40%	0°	30GHz	26dB	130mV , 0.28UI
Merlion 3	REF - 40%	CS + 40%	0°	40GHz	26dB	150mV , 0.31UI
Merlion 4	REF	Optimized	45°	27GHz	28dB	169mV , 0.32UI
Merlion 5	REF - 25%	Optimized	45°	34GHz	26dB	184mV,0.36 UI
Merlion 6	REF - 40%	Optimized	45°	40GHz	25dB	184mV,0.36 UI

Table 2: Summary of six different trials.

Technology name	Merlion 6a	Merlion 6b	Merlion 6c
Tip	Flat	Flat	Flat
XLT	YES	YES	YES
Radial alignment [µm]	8	8	8
Z planarity [µm]	Δ = 20	Δ = 20	Δ = 20
CCC/MAC [mA]	1450/1300 HiP: 2700/2400	1500/1400 HiP: 2800/2500	1900/1700 HiP: 3000/2700
Force (at 75 um OT)	1.8 g	2.3 g	3.2 g
Temperature range	-45 to +175 °C	-45 to +175 °C	-45 to +175 °C
Probe alloy	SA2	SA2	SA2

Table 3: Merlion 6 probe head variations.

Figure 10 shows the eye diagram of Merlion 6 hybrid probes. This new probe series provided the best loopback @ 32GT/s meeting both EH and EW requirements with the best margins. From Table 2, we can conclude that Merlion 6 hybrid design is the best optimized selection because it has the best combination of probe intrinsic resonant, insertion to cross-talk ratio, and nominal channel EW and EH. The new probe head (Table 3) consists of three different probe designs to optimize current-carrying capacity and high-speed performance.

Figure 11 shows the Merlion 6 contact tests conducted on a bumped wafer at room temperature. The hybrid probe solution shows stable contact resistance, which will help in minimizing probe burnout and maximize the mean time between failure (MTBF) of the probe card.

Probe head characterization: test fixture. To validate the actual Merlion 6 probe head frequency performance in terms of S parameter

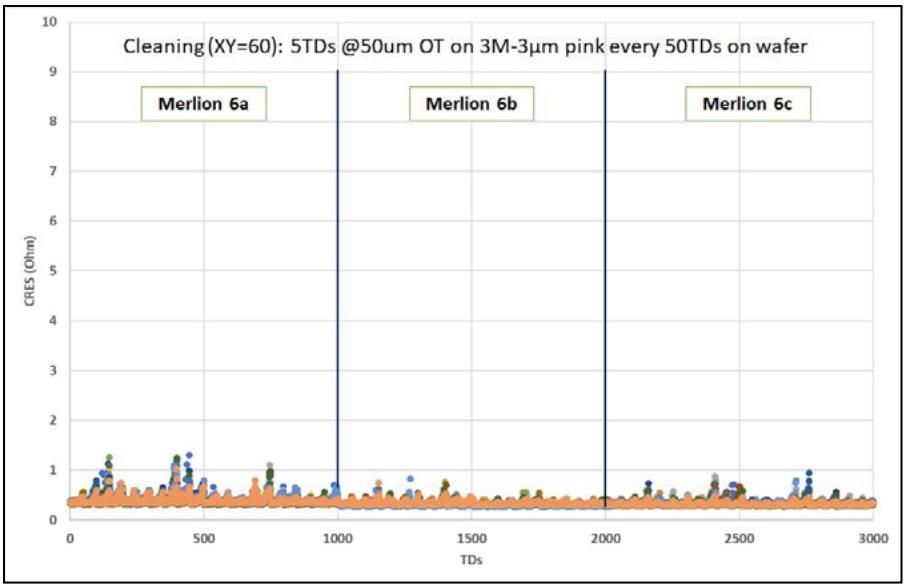

Figure 11: Contact test results of Merlion 6.

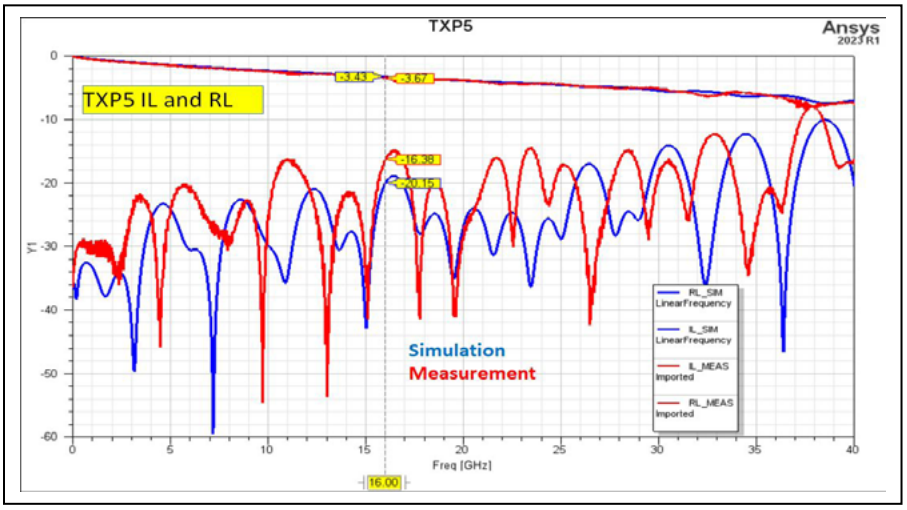

Figure 12: Test fixture SE S parameters simulation vs. measurement.

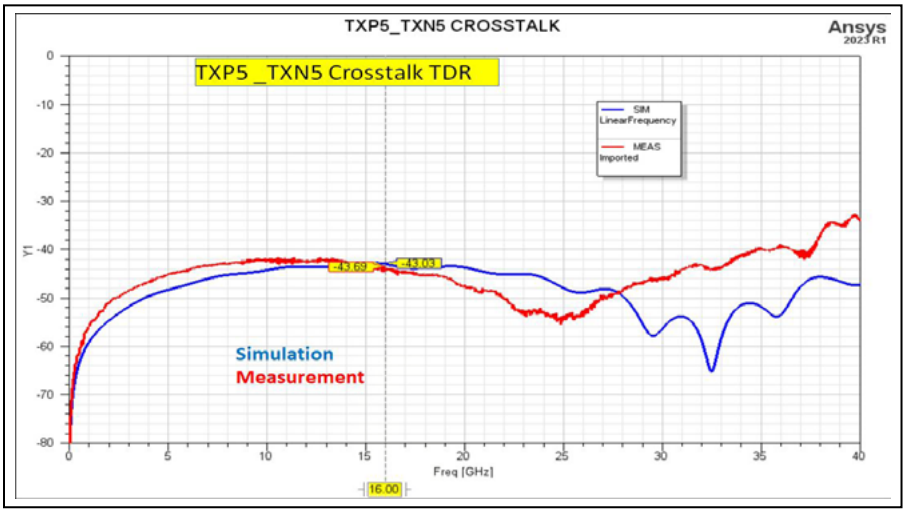

Figure 13: Test fixture SE cross talk TDR parameters (simulation vs. measurement).

and impedance matching with simulations, a test fixture was required. A customized test fixture (test PH with 27 needles—8 RF loopback and 19 GND needles) was designed to "sandwich" the probe head between 50Ω impedance-controlled traces at each end to allow VNA interface. A total of 16 2.92mm connectors (8 head side + 8 tip side) enabled four simultaneous port measurements.

The following is a discussion of the test fixture measurement results. We found that IL and RL have a high degree of variability due to radio frequency (RF) space transformer microstrip manufacturing tolerance, impedance mismatches between the SMA connector to the trace and mechanical assembly (see **Figure 12**). **Figure 13** shows that the single-ended cross-talk simulation of the probe needle matches the measurement. Because it's possible to evaluate the plot in **Figure 14**, the TDR measurement shows good agreement in predicting the probe head impedance profile. De-embedding is performed on test points with the best impedance profile. De-embedded S-parameters measurement shows good IL and RL correlation with simulation.

Probe head characterization: probe card external loopback end-to-end measurement. In order to improve characterization data, further measurements have been done, e.g., four (RF) microprobes were used to directly contact the signal probes and the nearest ground probe. The test setup included microprobes that were positioned and put in contact using a probing station with four manual micro-positioners, RF microprobes have been connected to a vector network analyzer (VNA) for S-parameter acquisition. The TDR plot was generated by simulation.

RF microprobe measurement results compared to simulation results are shown in **Figure 15**. To better match the measurements with the simulation results, it is necessary to take into account the buckling

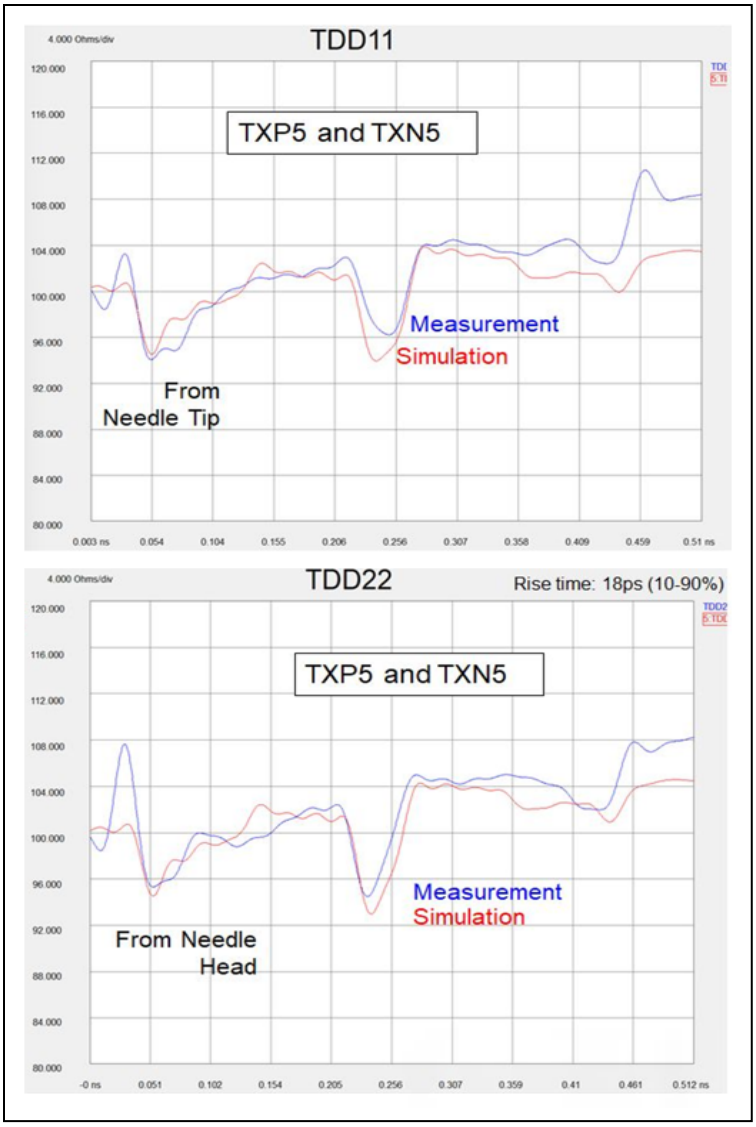

Figure 14: Test fixture DIFF TDR simulation vs. measurement.

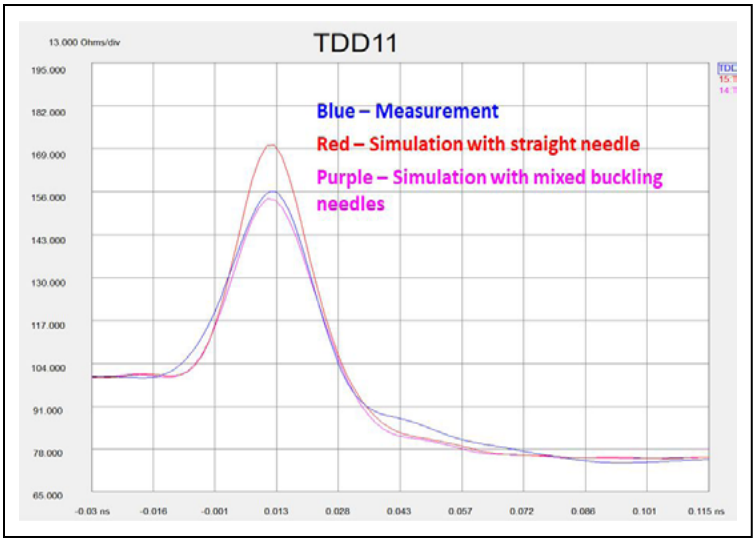

Figure 15: RF microprobe measurement results compared with simulation results.

effect of needles during the measuring process. The measurement results show a high impedance due to the measurement setup itself. The microprobe setup used a dual-pin probe (ground-signal), however, only the nearest ground was contacted by the probe ground pins, therefore, the return current flow is only through the probe ground pins. This situation causes a higher inductance compared to both the direct measurement data and the stimulation data. High inductance causes signal bandwidth degradation, so the measurement results suffer a degradation in quality. Therefore, a direct probing measurement set up is not recommended.

Summary

The Merlion 6 hybrid probe solution has been demonstrated to have the capability to meet all the performance requirements of a high-end probe card for HPC test applications. This probe technology—in use since 2022—has met the high-speed test requirements during wafer sort at AMD.

The probe solution also provides low and stable CRES with high strength and conductivity. From the simulation and TDR measurement correlation data, we were able to show good agreement in predicting the probe head impedance profile. Additionally, the de-embedded S-parameters measurement shows good IL) and RL correlation with the simulation results.

This paper summarized the various aspects of probe characterization for a high-speed performance probe solution, and coupled with the high-power PH (HiP) architecture, we were able to show a minimal probe burnout while maximizing MTBF in production.

As HPC workloads drive demand, the future will have more stringent test requirements in terms of higher speed and higher current-carrying capacity. The design methodology from this paper will form the baseline to meet the ever-increasing test requirements that will catapult the industry to a new way of designing for advanced applications.

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Recent advances in bridges for chiplets communications

By John H. Lau [Unimicron Technology Corporation]

Recently, because of the drive of artificial intelligence (AI) such as OpenAI's GPT, generative AI and conversational AI, and 5G/6G, the applications such as high-performance computing (HPC), autonomous vehicle, internet of things (IoTs), big data (for cloud computing) and instant data (for edge computing) are demanding more advanced semiconductor packaging technology [1-3].

One of the most popular advanced packaging technologies is the 2.5D or 3D integrated circuit (IC) integration [4] as schematically shown in **Figure 1a**. It can be seen that the system on chip (SoC) devices, such as the central processing unit (CPU) and graphics processing unit (GPU), and high-bandwidth memory (HBM) are supported by a passive (2.5D) or active (3D) through-silicon via (TSV)-interposer and then on a build-up package substrate. Finally, the whole module is attached to a printed circuit board (PCB) with ball grid array (BGA) solder balls and solder paste. This multiple chiplet system and heterogeneous integration packaging are driven by performance and form factor and for extremely high-density and high-performance applications [4].

The very first 2.5D IC integration papers were published by CEA-Leti [5] at IEEE/ECTC 2005 and [6] at IEEE/ECTC 2006. The very first product (Virtex™-7 HT family) of 2.5D was shipped in 2013 by Xilinx and TSMC. Since then, AMD shipped its Radeon™ R9 Fury X GPU, Nvidia shipped its Pascal™ 100 GPU, Fujitsu shipped its Fugaku (A64FX CPU), and Graphcore shipped Bow (an intelligence processing unit), etc. Very recently, Nvidia shipped its A100 GPU (826mm^2) with six HBM2 supported by a very large TSV-interposer and AMD/Xilinx published a paper of their Versal Premium VP1902 field-programmable gate arrays (FPGAs) with a huge TSV-interposer (>160mm x 160mm = 25,600mm^2) at the IEEE Hot Chip Conference on August 29, 2023.

TSMC called 2.5D IC integration chip-on-wafer-on-substrate (CoWoS®). The 2.5D or 3D with TSV-interposer is known for its high cost. One of the key reasons for its high cost is because the TSV-interposer manufacturing (with the 64nm process technology) yield loss is high because of its large size. The objective of this brief note is to present some of the recent advances in using silicon bridges to replace the TSV-interposer.

Intel's embedded multi-die interconnect bridge (EMIB)

At IEEE ECTC 2016, Intel published the first paper on bridge for chiplets communication [7]. One of the key objectives of the paper was to show the replacement of the TSV-interposer (**Figure 1a**) with its embedded multi-die interconnect bridge (EMIB) as schematically shown in **Figure 1b**

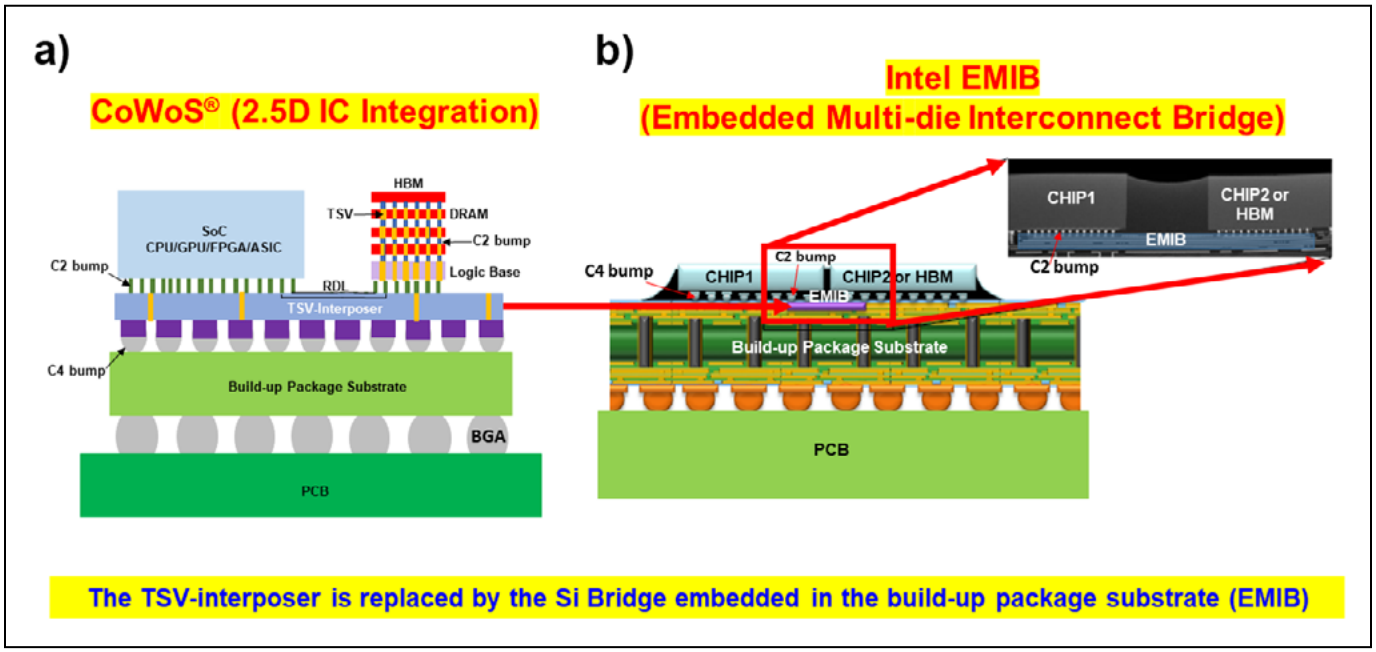

Figure 1: a) 2.5D or 3D IC integration with a TSV-interposer; b) Chiplets without a TSV-interposer (EMIB) [7].

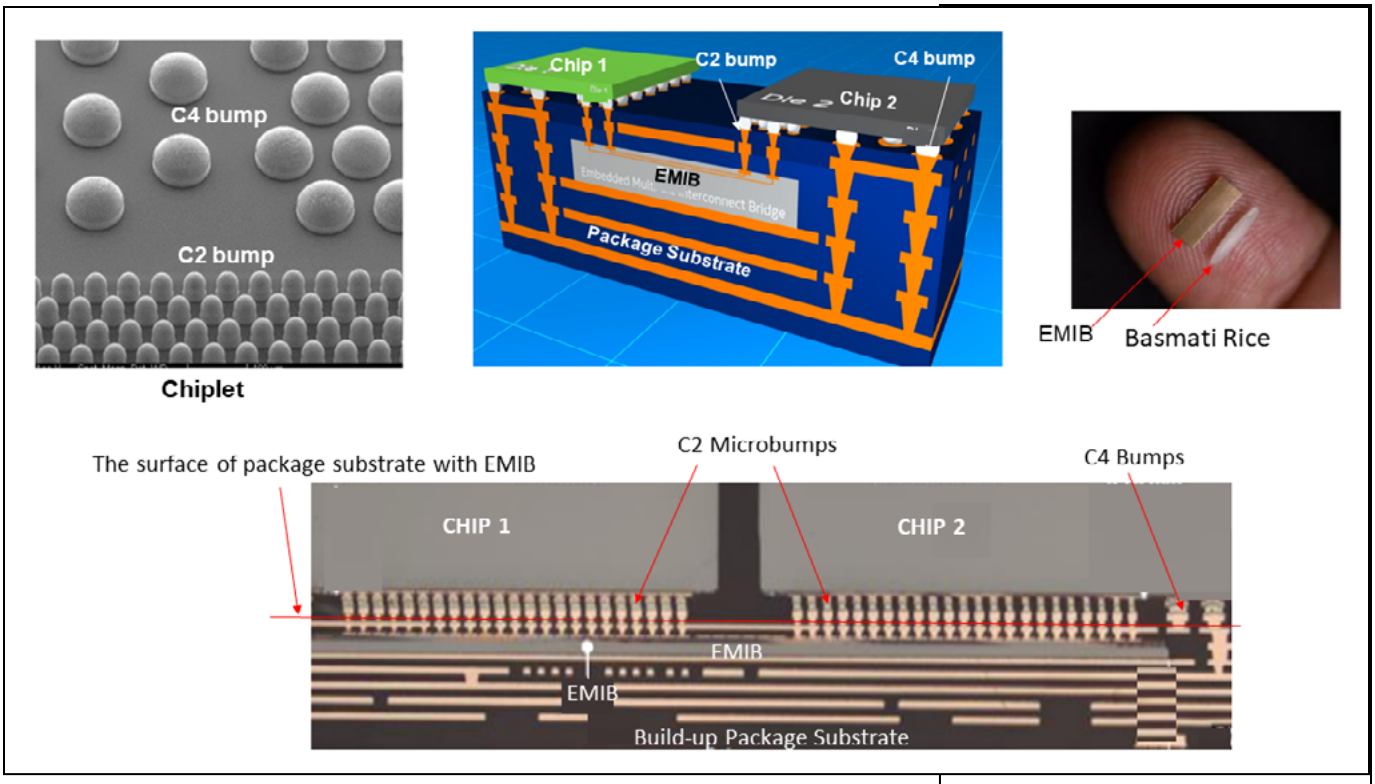

Figure 2: Intel's EMIB [7].

and **Figure 2**. It can be seen that the EMIB die is embedded in the cavity of a build-up package substrate, which is supporting the chiplets with fine-metal linewidth (L) and spacing (S) redistribution layers (RDLs). The size of the bridge is very small as shown in **Figure 2**. The large TSV-interposer is eliminated.

For EMIB, there are at least three important tasks (see **Figure 1b** and **Figure 2**): 1) wafer bumping of two different kinds of bumps, namely, chip connection (C2 or microbump), and controlled collapse chip connection (C4) on the chiplet's wafer (but there are no bumps on the bridge); 2) embedding the bridge in the cavity of a build-up substrate and then laminating the top surface of the substrate so it is flat enough for chiplets bonding; and 3) bonding the chiplets on the substrate with the embedded bridge.

The first product (Intel's processor Kaby Lake and AMD's Radeon™ graphics) with one EMIB connecting the AMD's graphics processor to a HBM2 was shipped from 2018 until October 2019. Since then, Intel has been shipping its Agilex® with two to five EMIBs in 2019, and the Ponte

Vecchio GPU with 11 EMIBs in 2022. Sapphire Rapids [8] is the next-generation of Intel's Xeon® scalable processor. It consists of four SoCs and they are connected with 10 EMIBs. There are another four EMIBs that connect the four SoCs and the four HBMs (**Figure 3**). Lately, Intel has been discussing reducing the number of SoCs to two and shipping a new iteration of the product by the end of 2023 or early 2024.

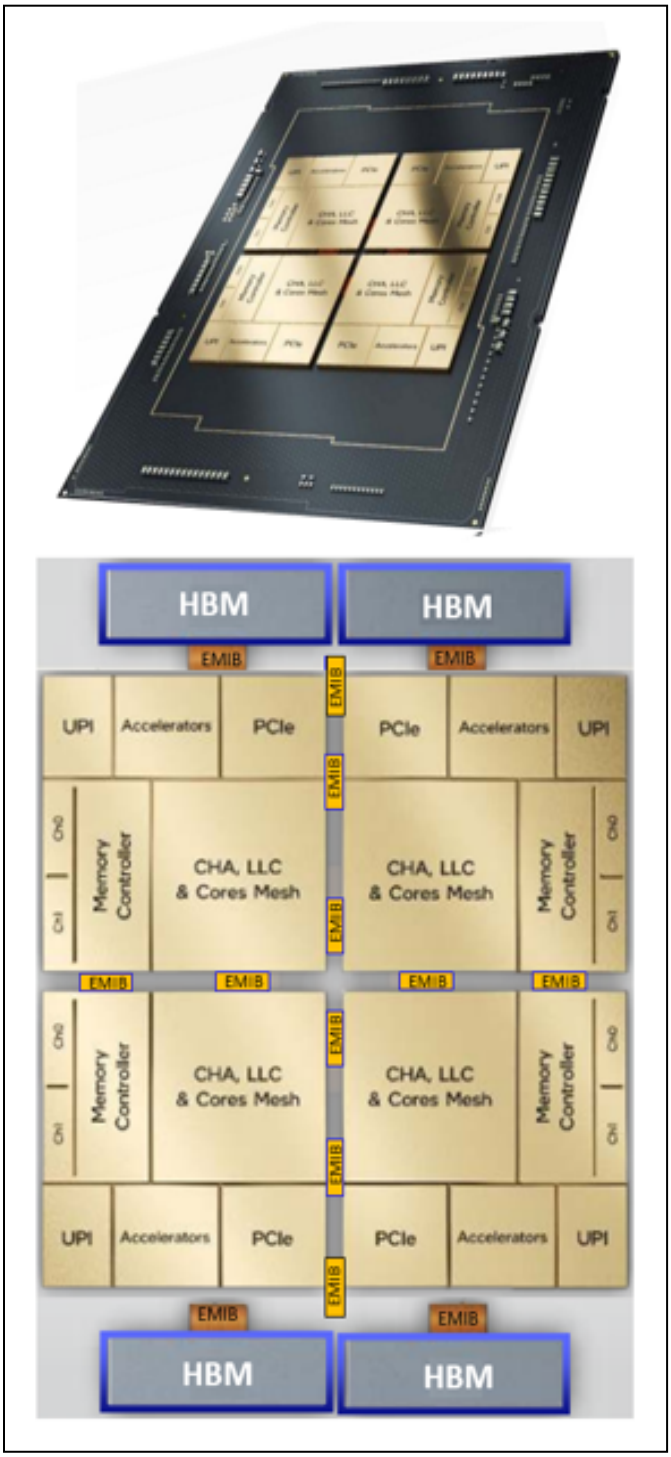

Figure 3: Intel's Sapphire Rapids with four SoCs and 14 EMIBs [8].

IBM's Direct Bonded Heterogeneous Integration (DBHi)

During IEEE/ECTC 2021 and 2022, IBM presented seven papers on "Direct Bonded Heterogeneous Integration (DBHi) Si Bridge" [9-15] (**Figure 4**). The major differences between Intel's EMIB and IBM's DBHi are as follows: a) Intel's EMIB has two different bumps (C4 and C2) on the chiplets (and there are no bumps on the bridge) (**Figure 2**), while IBM's DBHi has C4 bumps on the chiplets and C2 bumps on the bridge (**Figure 3**); and b) Intel's EMIB has the bridge embedded in the cavity of a build-up substrate with a die-attach material and then laminated with another build-up layer on top, while IBM's DBHi has a substrate that is just a regular build-up substrate with a cavity on top as shown in **Figure 4**.

The bonding assembly process of DBHi is very simple (**Figure 4**). First, nonconductive paste (NCP) is applied on Chip 1. Then, Chip 1 and the bridge are bonded using thermocompression bonding (TCB). After bonding, the NCP becomes the underfill between Chip 1 and the bridge. NCP is then applied on the bridge and Chip 2 and the bridge are bonded with TCB. Those steps are followed by placing the module (Chip 1 + bridge + Chip 2) on the organic substrate with a cavity and then going through the standard flip-chip reflow assembly process.

During IEEE/ECTC 2023, IBM presented a paper on "Direct Bonded Heterogeneous Integration (DBHi): Surface bridge approach for die tiling" [16]. The authors demonstrated that the cavity of a build-up package substrate is not necessary for their Si bridge technology as shown in **Figure 5**

AMD's Instinct™ MI250X compute accelerator

The AMD Instinct™ MI250X compute accelerator is shown in **Figure 6**. It can be seen that there are two GPUs (the second-generation matrix cores for HPC driven by AI) with each having a size of 790mm^2. Each GPU is connected to four HBM2E with Si bridges on microbumps. The GPU and the HBM2E are supported by a build-up package substrate without any cavity.

Apple's UltraFusion

UltraFusion is Apple's innovative packaging architecture that interconnects the die of two M1 Max chips to create a SoC with unprecedented levels of stunningly compact design, extensive connectivity, performance and capabilities. This architecture doesn't combine two M1 Max dies into a single chip package—it also makes the two dies present themselves as a single chip. The interconnection between the two M1 Max dies is by a "silicon bridge" as shown in **Figure 7**. The chiplets and the Si-bridge are supported by an ordinary build-up package substrate without any cavity.

TSMC's local silicon interconnect (LSI)

During IEEE/ECTC 2023, TSMC published two papers on replacing its CoWoS® by Si-bridge embedded in epoxy molding compound (EMC) with fan-out RDLs [17,18]. The key reason for this technology is to deal with the manufacturing yield loss of the ever-increasing size of the TSV-interposer—the yield loss is so high that the cost becomes unbearable. Just look at two examples: TSMC

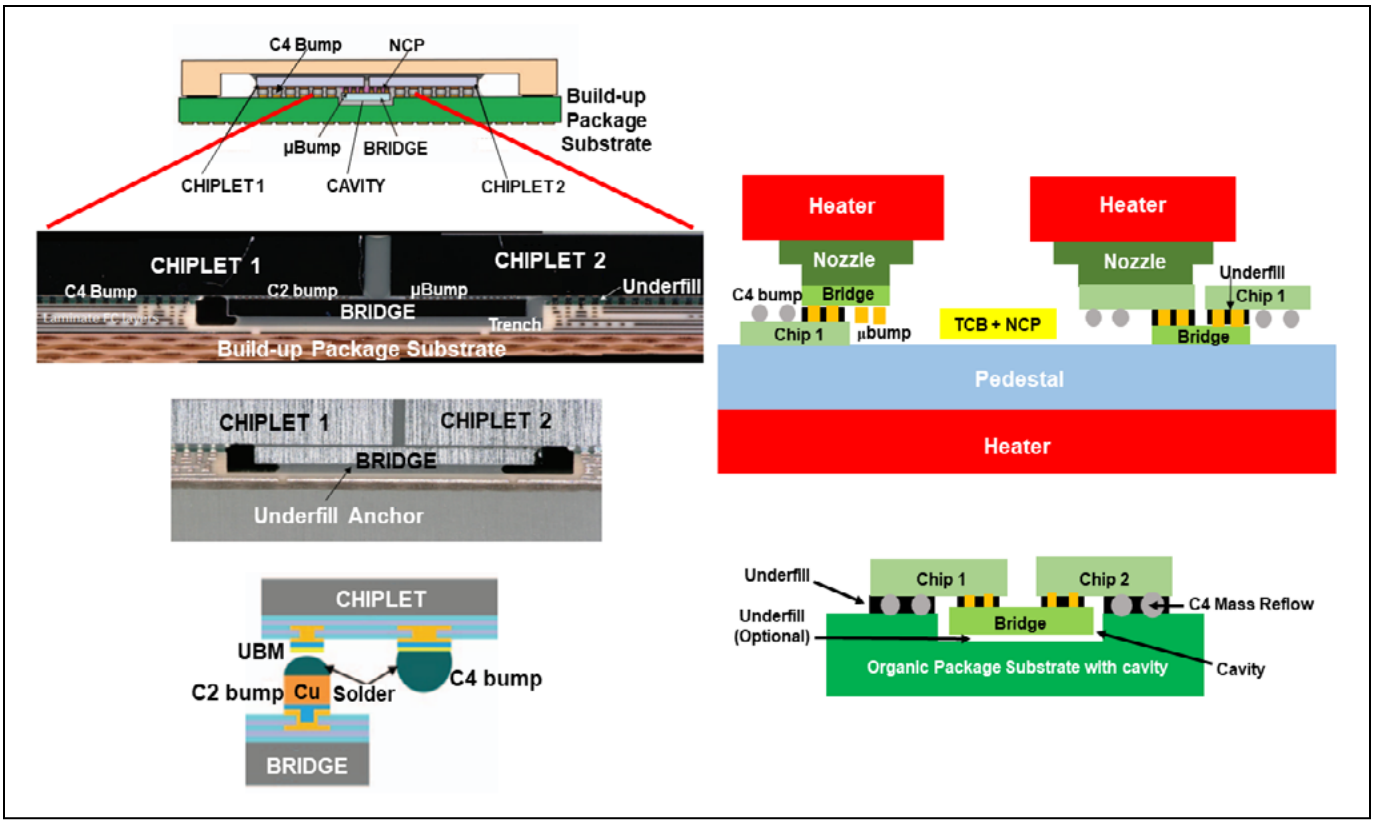

Figure 4: IBM's DBHi [9].

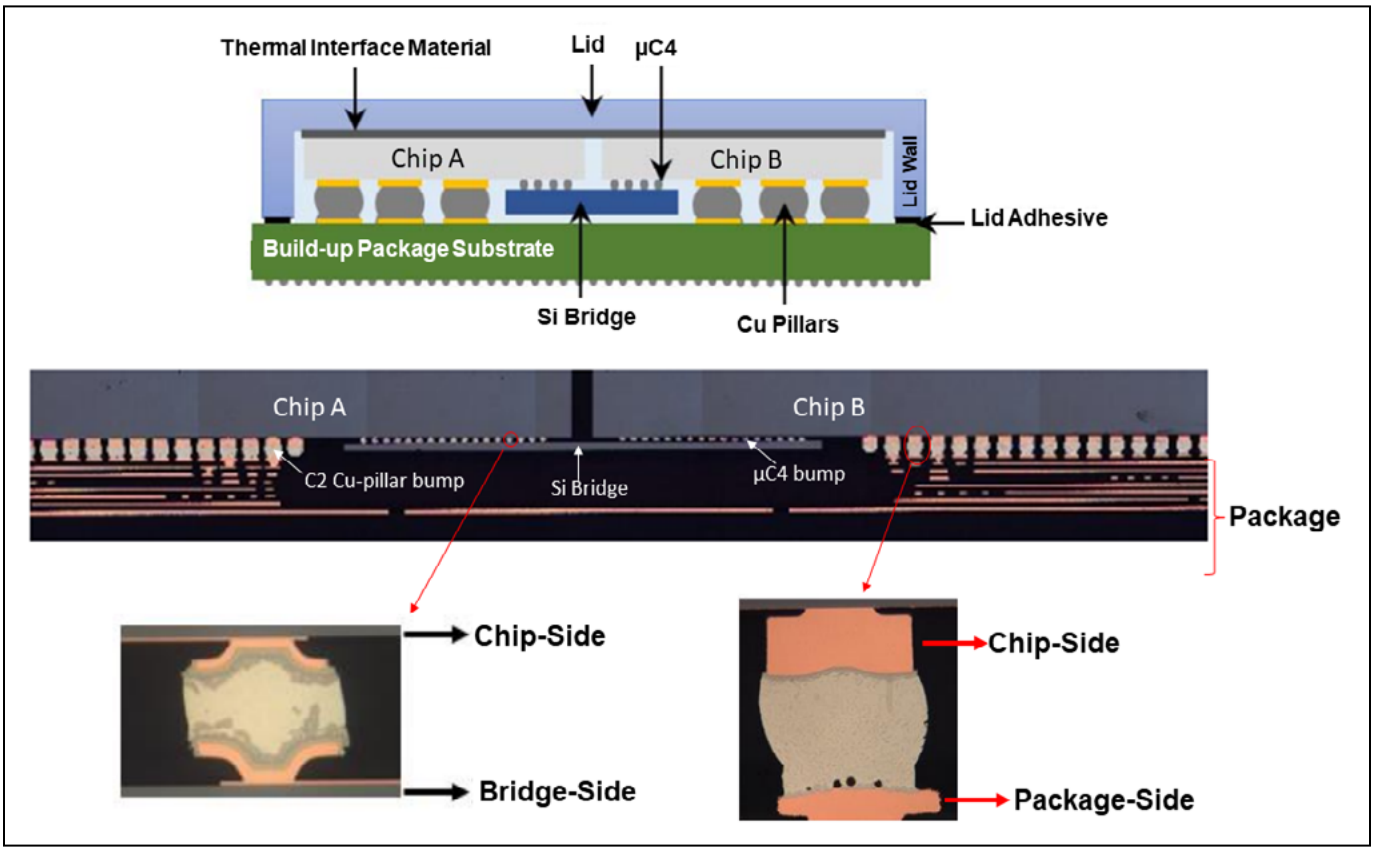

Figure 5: IBM's Si-bridge DBHi for chiplets on the build-up package substrate without a cavity [16].

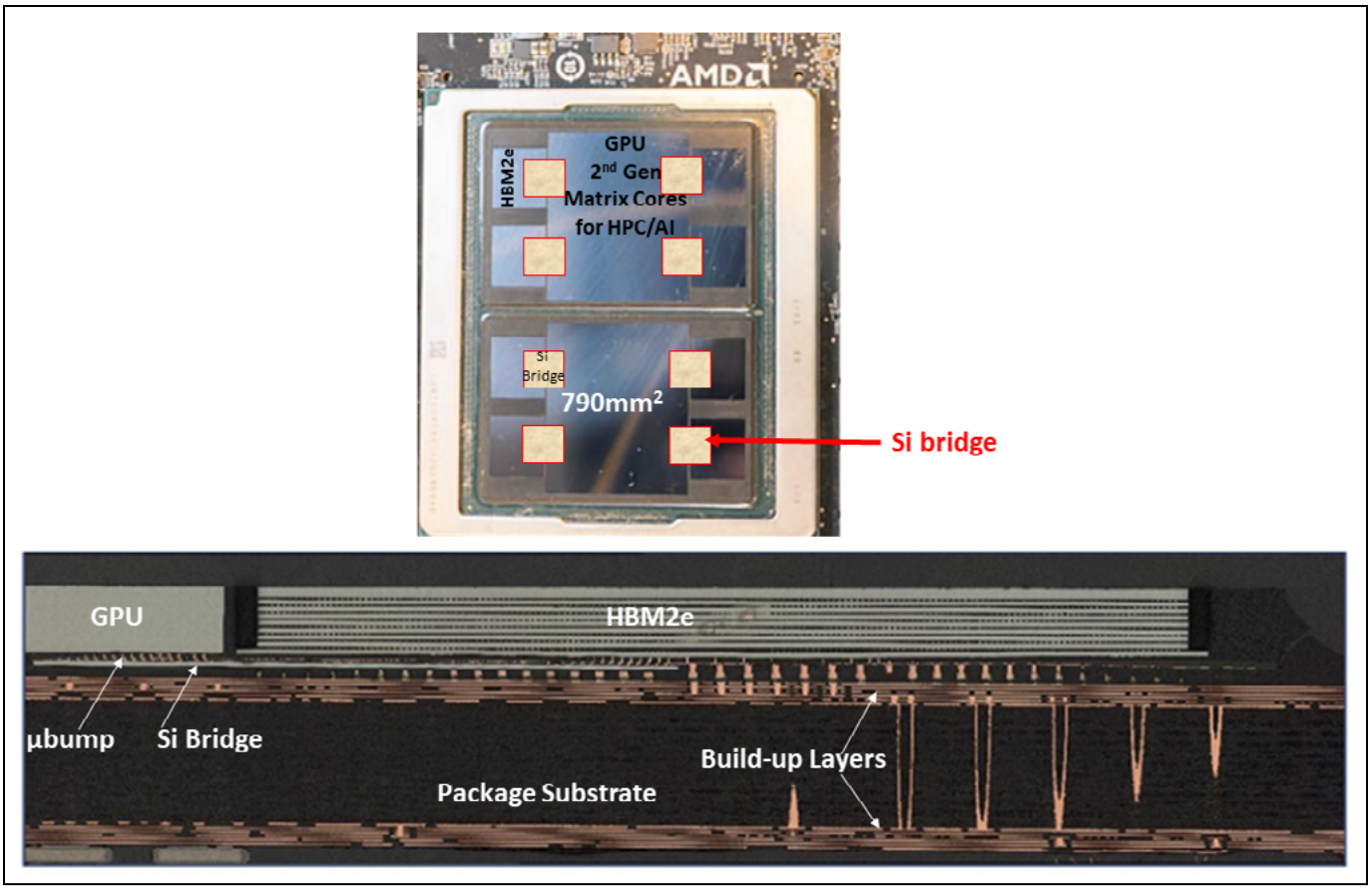

Figure 6: AMD's Instinct™ MI250X compute accelerator with Si-bridge for chiplets on the build-up package substrate without a cavity.

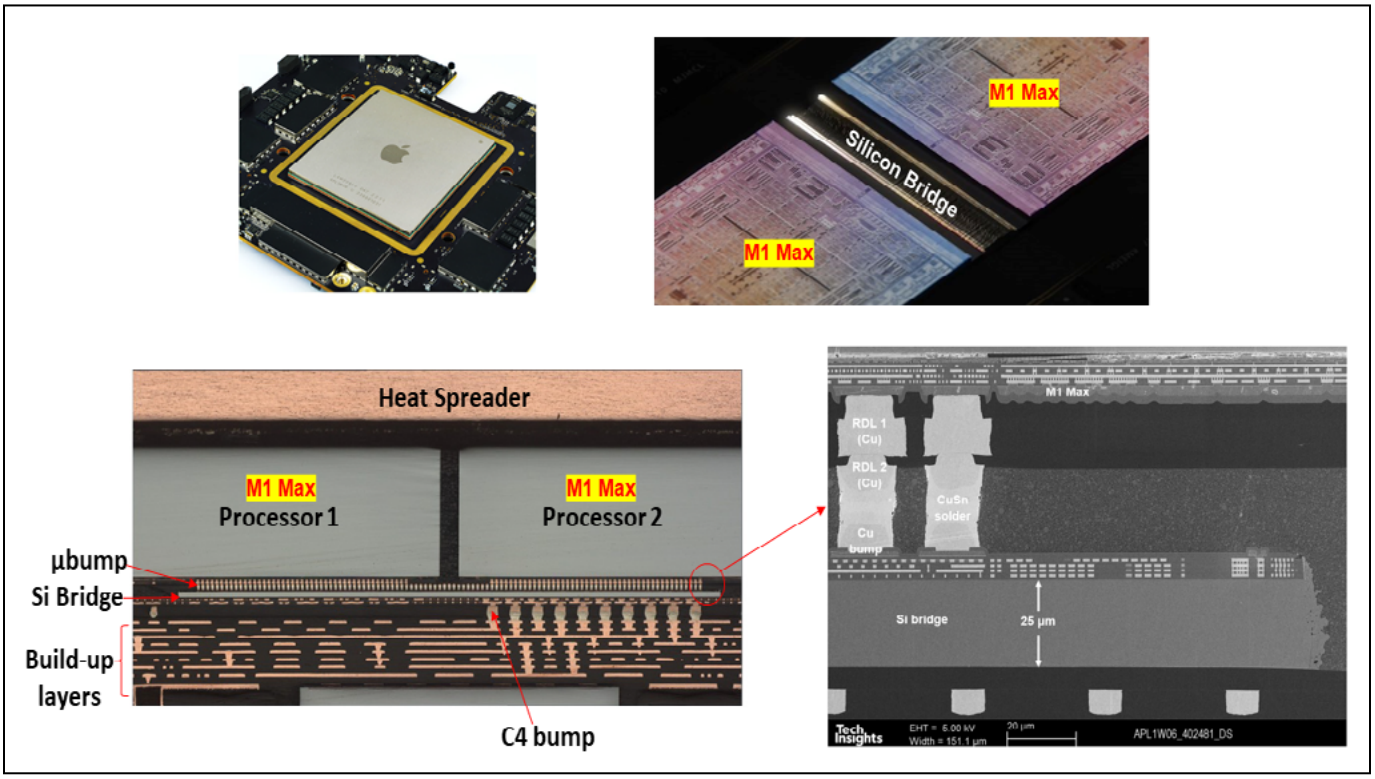

Figure 7: Apple's UltraFusion with Si-bridge for SoCs on the build-up package substrate without a cavity. (SEM image provided by TechInsights Inc.)

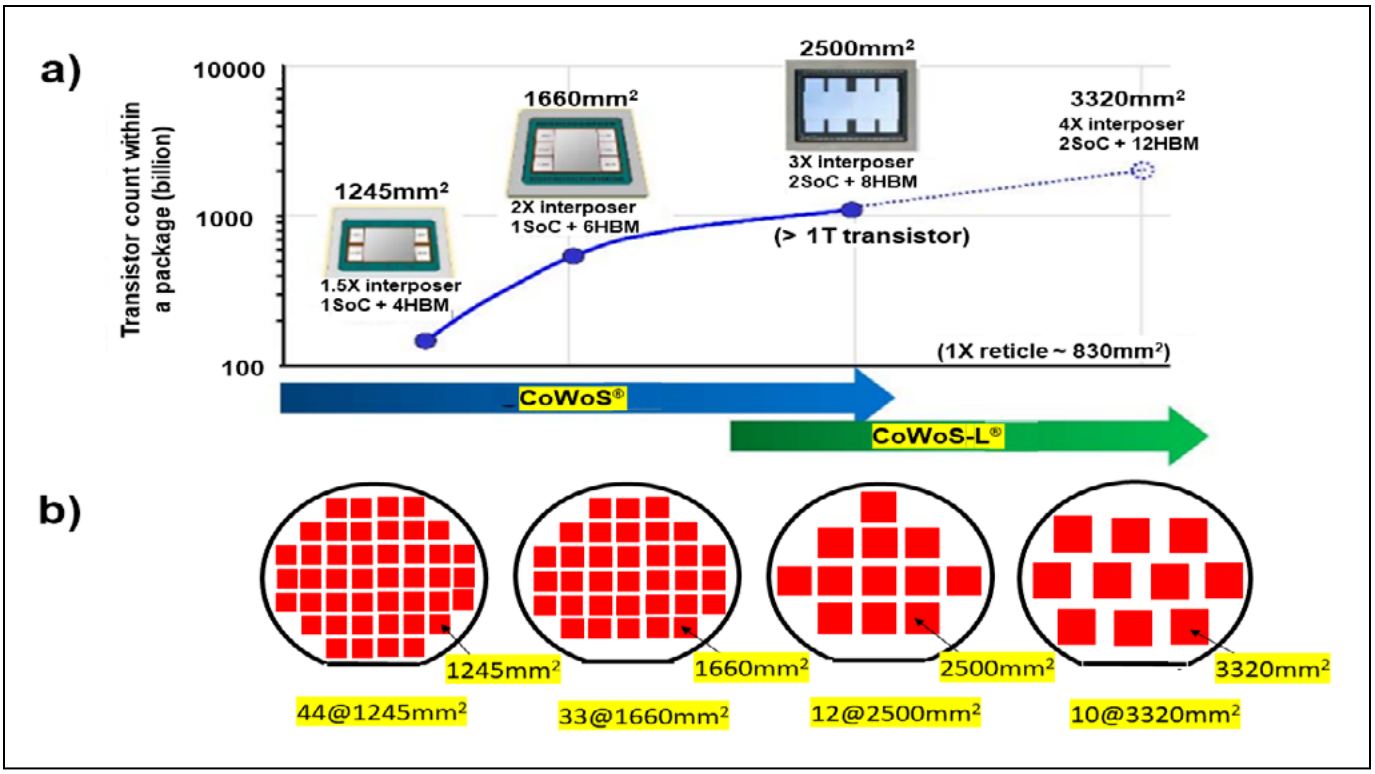

Figure 8: a) TSMC's roadmaps for CoWoS® (TSV-interposer) and CoWoS®-L (reconstituted-interposer) [17]; b) Number of TSV-interposers vs. the size of the TSV-interposer.

has been using CoWoS® with the 1X reticle (830mm^2) for Xilinx, and with the 2X reticle (1660mm^2) for Nvidia. For a 3X reticle (2500mm^2), the yield loss is too high so TSMC is going to recommend a new chip-on-wafer-on-substrate-LSI + RDL interposer (CoWoS®-L) as shown in **Figure 8a**. **Figure 8b** shows the number of physically possible TSV-interposers vs. the size of the TSV-interposer on a 300mm-wafer. The impact of TSV-interposer size on yield loss per wafer is obvious.

Figure 9 shows the replacement of the TSV-interposer of CoWoS® by the LSI. **Figure 9b** shows the Si-bridge embedded in an EMC with fan-out RDLs (CoWoS®-L). CoWoS®-L is a new interposer that consists of at least an LSI (or Si-bridge) with or without TSVs and integrated fan-out (InFO) RDLs to form a reconstituted interposer (RI). The small-size LSI inherits all the attractive features of the TSV-interposer by retaining sub-micron Cu interconnects (RDLs), TSVs, and embedded deep trench capacitors (eDTCs) to ensure good system performance. At the same time, the small-size LSI avoids the issues associated with the large-size TSV-

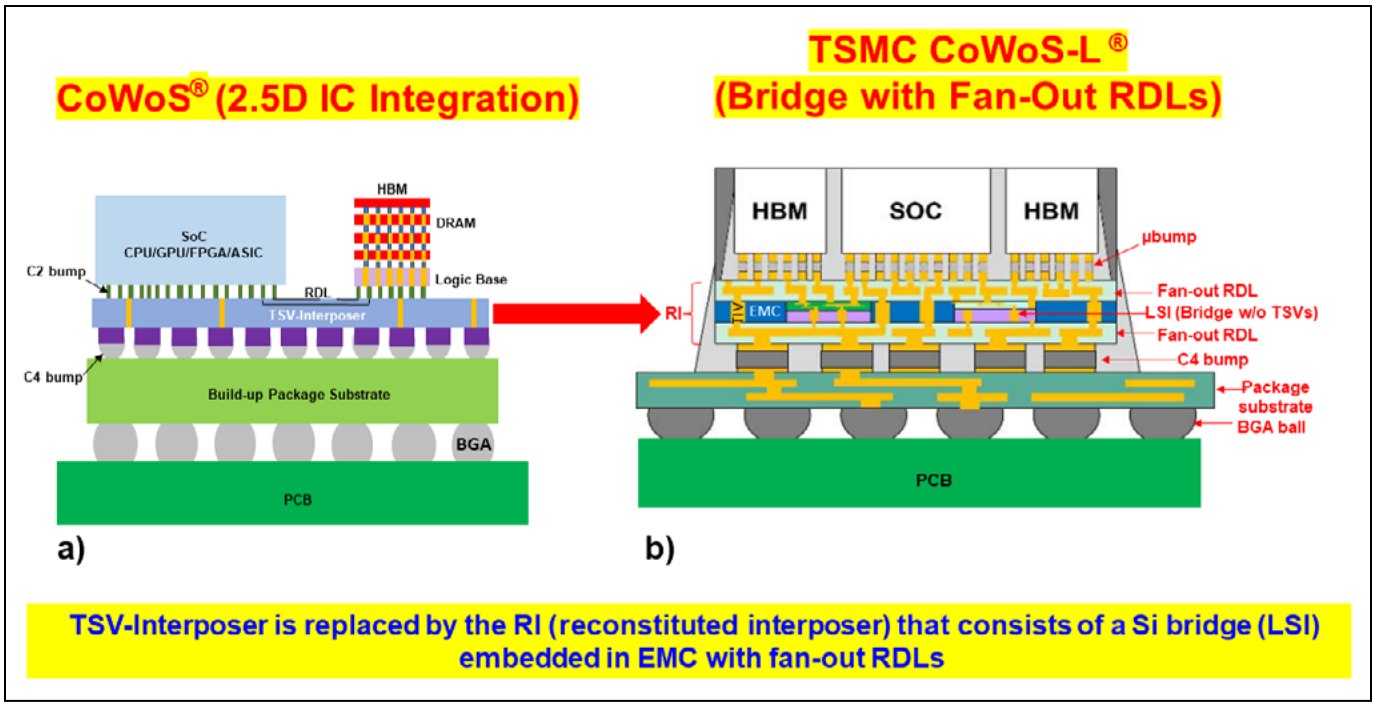

Figure 9: a) CoWoS® (2.5D IC integration); b) TSMC's CoWoS®-L (reconstituted-interposer) that consists of a Si bridge (LSI) embedded in EMC with fan-out RDLs [17].

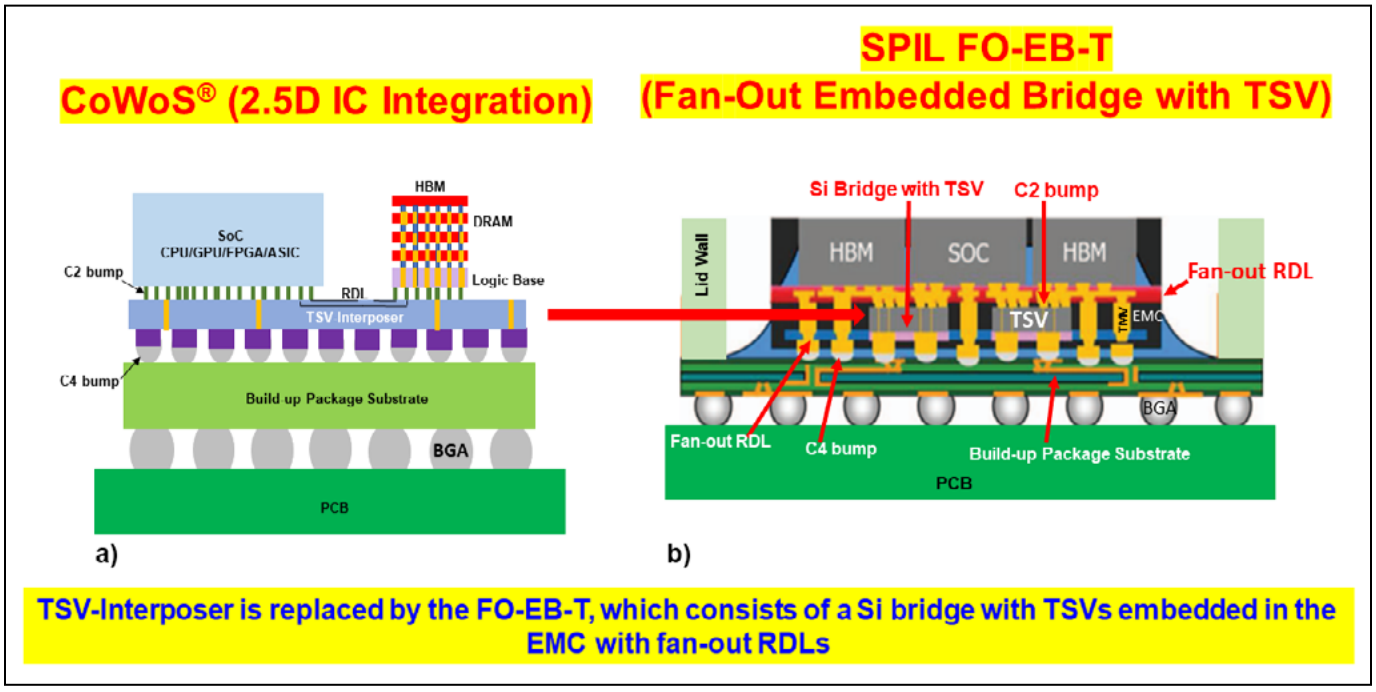

Figure 10: a) CoWoS® (2.5D IC integration); b) SPIL's FO-EB-T, which consists of a Si bridge with TSV-interposer and RDLs embedded in the EMC with fan-out RDLs [19].

interposer, such as manufacturing yield loss. The metal L/S of the small-size bridge (LSI) has a pitch (minimum) = 0.4µm. At the end, the large-size TSV-interposer is replaced by the RI, which consists of the EMC, small-size bridge (LSI) with RDLs and with or without TSV + InFO RDLs.

SPIL's fan-out embedded bridge with TSV (FO-EB-T)

During IEEE/ECTC 2023, SPIL presented two papers on FO-EB-T [19,20]. Very similar to TSMC's CoWoS®-L architecture, SPIL replaced the TSV interposer with a Si-bridge with TSVs and RDLs embedded in an EMC with fan-out RDLs as shown in **Figure 10**.

CoWoS®-L/FO-EB-T and US Patent 11,410,933

Figure 11 shows the structure of TSMC's CoWoS®-L and SPIL's FO-EB-T, and the US patent 11,410,933. It

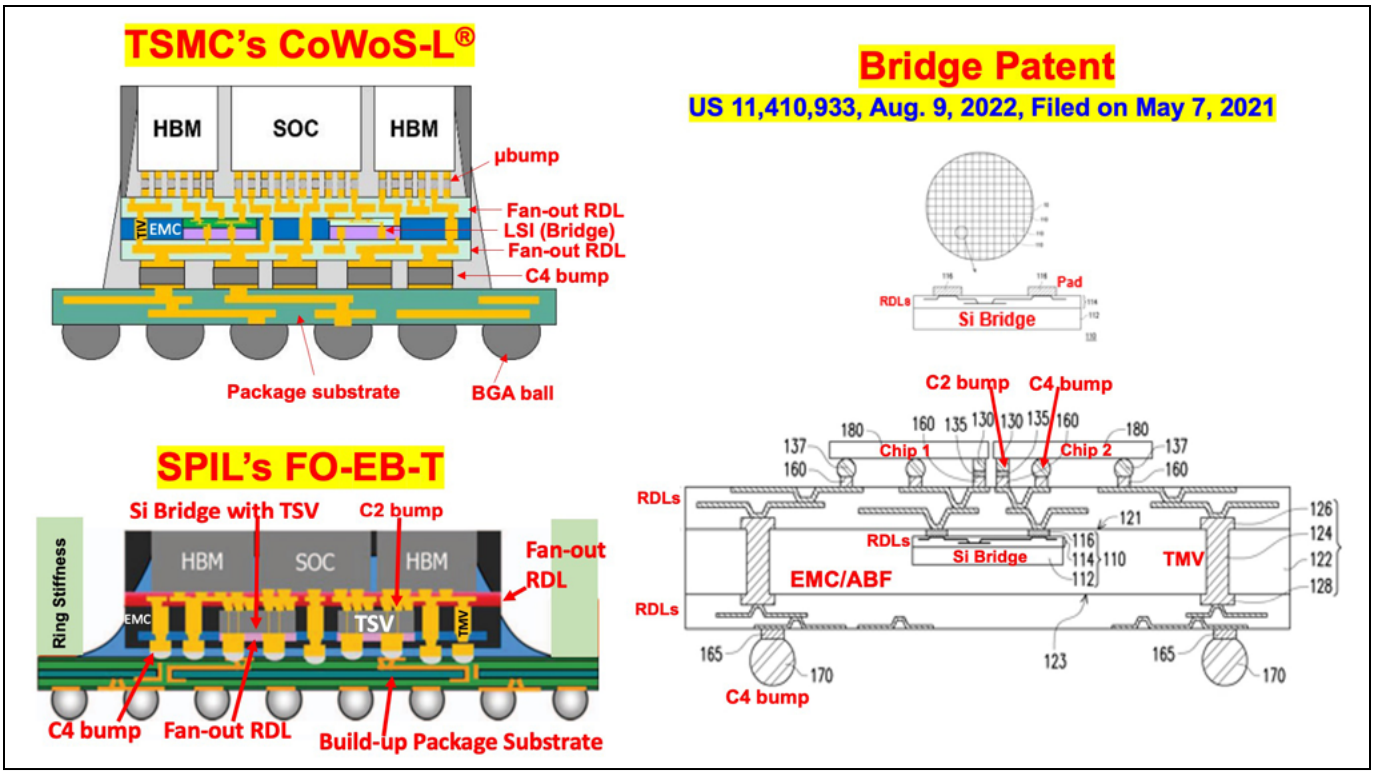

Figure 11: Similarity between the structure of CoWoS®-L and FO-EB-T and US patent 11,410,933 [17,19].

can be seen that they are very similar, except TSVs are not used in the Si bridge of the patent.

Summary

Some important results and recommendations are summarized as follows:

1. At present, 2.5D and 3D IC integrations with TSV-interposers are the key advanced semiconductor packaging technologies for HPC, IoTs, autonomous vehicles, big data and instant data applications driven by AI and 5G/6G.
2. The manufacturing yield loss of the ever-increasing size of the TSV-interposer is so high that the cost becomes unbearable.
3. The TSV-interposer is replaced by the Si-bridge (with RDLs) embedded in the cavity of a build-up packaging substrate, such as the EMIB by Intel.
4. The TSV-interposer is replaced by a Si-bridge (with RDLs) that is connecting the chiplets with microbumps such as those developed by IBM, AMD, and Apple. There is no cavity on the build-up package substrate.
5. The microbumps discussed in item #4 can be eliminated by using Cu-Cu bump-less hybrid bonding as proposed in [21].
6. The TSV-interposer is replaced by at least a Si-bridge (with RDLs and with or without TSVs) embedded in EMC with fan-out RDLs such as those developed by TSMC (CoWoS®-L) and SPIL (FO-EB-T).
7. The structure of TSMC's CoWoS®-L and SPIL's FO-EB-T is very similar to the structure of US patent 11,410,933 proposed in [22], except TSVs are not in the patent.

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Biography

John H. Lau is a senior special project assistant at Unimicron Technology Corporation, Taoyuan City, Taiwan (ROC). He has more than 40 years of R&D and manufacturing experience in semiconductor packaging, 528 peer-reviewed papers, 50 issued and pending US patents, and 23 textbooks. He is an ASME Fellow, IEEE Fellow, and IMAPS Fellow. He earned a PhD degree from the U. of Illinois at Urbana-Champaign. Email John_Lau@unimicron.com

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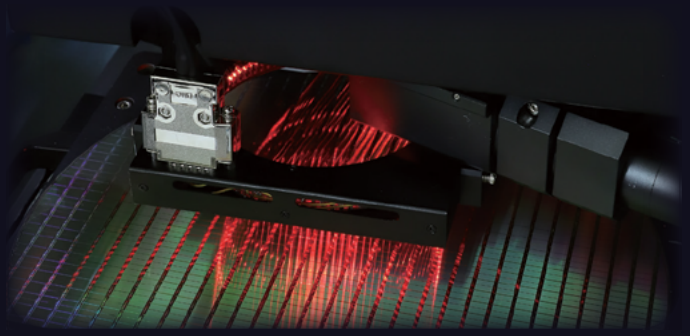

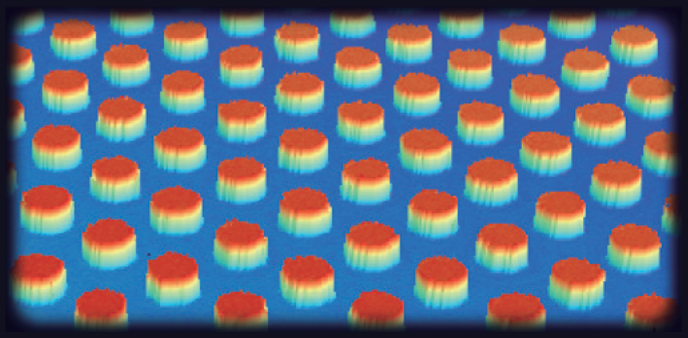

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IMAPS Symposium 2023: A cornucopia of technical content, networking and exhibits

By Suresh Jayaraman [General Chair of IMAPS Symposium, 2023, and Amkor]

As General Chair, it was a great pleasure to captain the 56th IMAPS Symposium (**Figure 1**). It was a successful event all around and would not have been possible without the help of the wonderful staff and volunteers working behind the scenes to make sure the attendees had a great experience. Thanks to the committee for working tirelessly in putting an excellent program together—it takes a village to organize a conference of this magnitude. Nearly 800 people joined the event, including 87 from outside the U.S.

Figure 1: Suresh Jayaraman, General Chair.

This year we had an unprecedented 14 Professional Development Courses (PDCs), with one added in the topical area of artificial intelligence (AI), which was very well attended. There is also a thrust to post the PDCs online through IMAPS Academy, which would serve the student community well. The DEI (diversity, equity, and inclusion) town hall was very well attended and engaging. The panel had some interesting thoughts and responses to various questions relating to DEI in the workplace, mentoring, and how the glass ceiling for women is being broken in the packaging field.

We had a terrific lineup of keynotes starting with Kevin Anderson (Qorvo) providing an overview of the SHIP program and a good summary of the capabilities. Jeff Burns (IBM) enlightened attendees about foundation models and how they help scale up AI for various applications. He also provided some insight into the various research thrust areas in the heterogenous integration (HI) domain at IBM Research Centers. Shin-Puu Jeng (TSMC) showed how organic interposers (chip-on-wafer-on-substrate-RDL interposer, CoWoS®-R) will likely take the baton from Si interposers (CoWoS®-S) and extend the reach of HI to help address the exponential growth in compute requirements for AI applications. An answer to the question regarding manufacturability of organic interposers suggested that a lot needs to be done to increase yields sufficiently to scale to high-volume manufacturing. My takeaway was that there is probably room for both technologies, as well as other variants, such as silicon bridges (chip-on-wafer-on-substrate-local silicon interconnect +RDL interposer [CoWoS®-L]).

C. P. Hung (ASE) underscored the importance of HI in addressing emerging automotive, high-performance computing (HPC), and AI applications. It was encouraging to see that advanced packaging is getting a lot of attention and traction.

The topic for the panel discussion, "The Future of Packaging for Artificial Intelligence," also addressed the theme of the conference and the eminent panelists provided great insights into the current state of affairs, as well as what they saw coming down the pipeline (**Figure 2**). Advanced packaging and HI to address chiplets are here to stay!

Everyone enjoyed the networking at the welcome reception (**Figure 3**, **4**), lunch breaks, exhibit hall happy hour, and poster

Figure 2: AI panel.

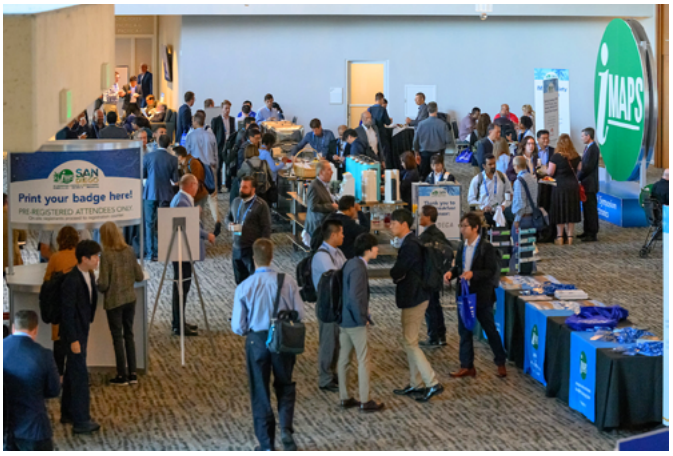

Figure 3: Networking break.

Figure 4: Welcome reception.

Figure 5: Visiting students.

session. These events provided an excellent opportunity to catch up with colleagues and make new connections. The attendees enjoyed a busy exhibit hall with companies representing the entire supply chain, and there was a slight increase to 96 total 10x10 booths.

This year we were very pleased with the student participation (**Figure 5**) including the university booths, student speakers and visiting high school students. The students seemed to be in awe of many of the exhibits, including watching a wire bonder in action!

See you next year in Boston at a new location: The Encore Boston Harbor, a new state-of-the-art conference facility. Mark your calendars for Sept. 30 – Oct. 3, 2024.

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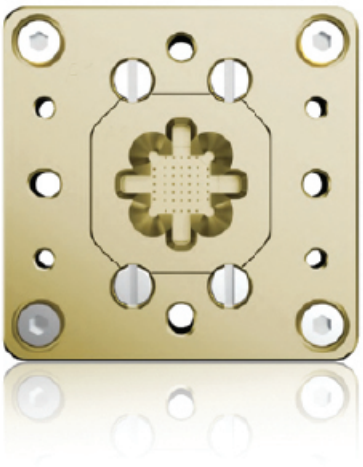

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