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The Future of Semiconductor Packaging

Volume 27, Number 5

September • October 2023

Improving wafer test efficiency and minimizing cost per die

- Mitigating the thermal bottleneck in advanced interconnects
- Challenges with self-assembly applied to die-to-wafer hybrid bonding
- Efficiency and cost implications of multi-die heterogeneous integration
- Advanced packaging: Fueling the next era of semiconductor innovation
- Packaging innovation drives inspection requirements for automotive apps and more

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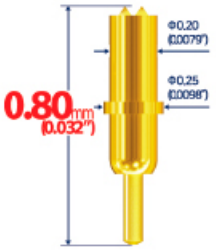
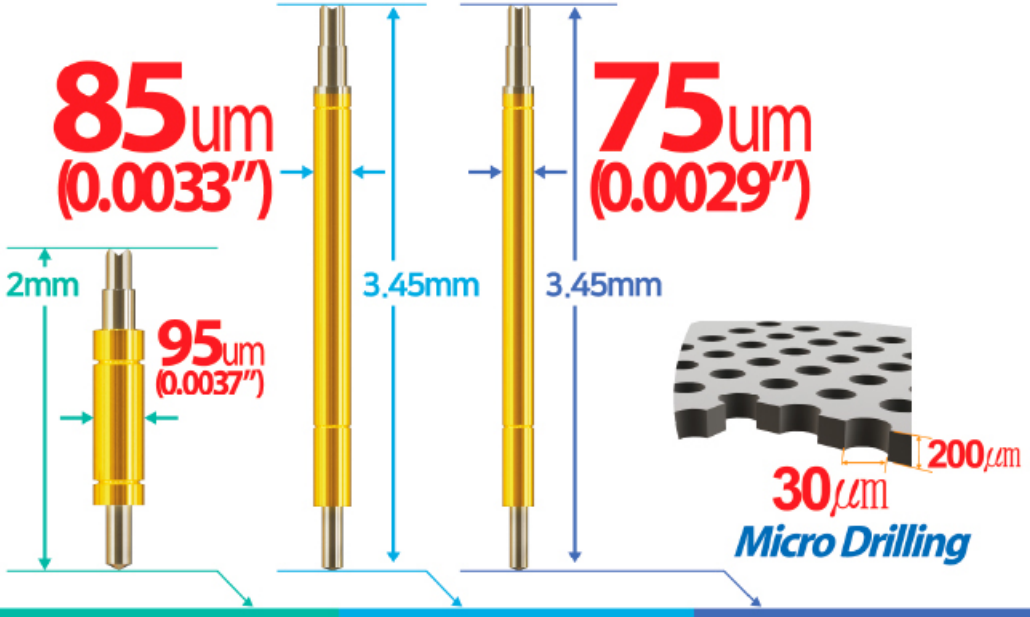
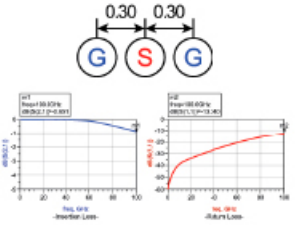
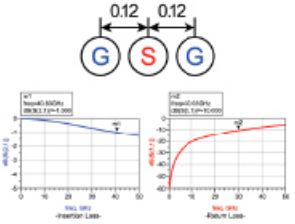
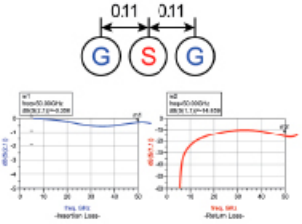
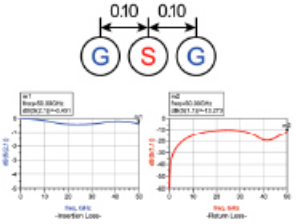




RF-300μm Pitch	120μm Pitch	110μm Pitch	100μm Pitch
Mechanical Spec. • Spring Force : 0.212oz (12.0g) @ .0079 (0.20mm) • Recommended Travel : .0079 (0.20mm) • Full Travel : .0098 (0.25mm) • Current Rating : 2.0A Material Barrel - Alloy / Au plated Plunger - Hardened BeCu / Au plated Spring - Music Wire / Au plated	**Mechanical Spec.** • Spring Force : 0.281oz (8.0g) @ .0098 (0.25mm) • Recommended Travel : .0098 (0.25mm) • Full Travel : .0118 (0.30mm) • Material : Terminal – Pd Alloy / No plated Plunger – Pd Alloy / No plated Barrel – Ni-Au Alloy / Au plated Spring – Music Wire / Au plated	**Mechanical Spec.** • Spring Force : 0.212oz (6.0g) @ .0118 (0.30mm) • Recommended Travel : .0118 (0.30mm) • Full Travel : .0138 (0.35mm) • Material : Terminal – Pd Alloy / No plated Plunger – Pd Alloy / No plated Barrel – Ni-Au Alloy / Au plated Spring – Music Wire / Au plated	**Mechanical Spec.** • Spring Force : 0.247oz (7.0g) @ .0118 (0.30mm) • Recommended Travel : .0118 (0.30mm) • Full Travel : .0138 (0.35mm) • Material : Terminal – Pd Alloy / No plated Plunger – Pd Alloy / No plated Barrel – Ni-Au Alloy / Au plated Spring – Music Wire / Au plated
Electrical Spec. (Simulation data) • Propagation Delay : 7.68ps • Capacitance : 0.05pF • Inductance : 0.25nH • Insertion Loss : > 100GHz @ -1dB • Return Loss : > 100GHz @ -10dB (Dielectric material : MDS100)	**Electrical Spec.** (Simulation data) • Current Rating : 1.0A • Propagation Delay : 20.80ps • Capacitance : 0.21pF • Inductance : 0.38nH • Insertion Loss : 40.83GHz @ -1.000dB • Return Loss : 30.03GHz @ -10.000dB (Dielectric material : CERAMIC)	**Electrical Spec.** (Simulation data) • Current Rating : 0.9A • Propagation Delay : 38.25ps • Capacitance : 0.47pF • Inductance : 0.63nH • Insertion Loss : > 50.00GHz @ -1.000dB • Return Loss : > 50.00GHz @ -10.000dB (Dielectric material : CERAMIC)	**Electrical Spec.** (Simulation data) • Current Rating : 0.8A • Propagation Delay : 35.55ps • Capacitance : 0.44pF • Inductance : 0.66nH • Insertion Loss : > 50.00GHz @ -1.000dB • Return Loss : > 50.00GHz @ -10.000dB (Dielectric material : CERAMIC)
			

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HEAD OFFICE
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CONTENTS

New semiconductor materials, alternative pad designs, and ever-shrinking geometries are raising the complexity and the cost of wafer test, posing tough challenges—especially on the probing side. These trends are driving the need for innovative test techniques able to increase capacity and control capital equipment cost. A new approach to wafer testing, based on flying probe technology, has been introduced in order to allow manufacturers to increase test efficiency, thereby minimizing the cost per die.

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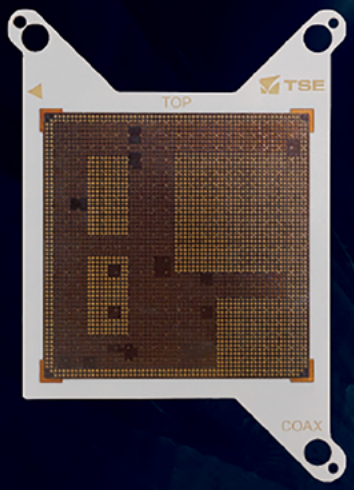
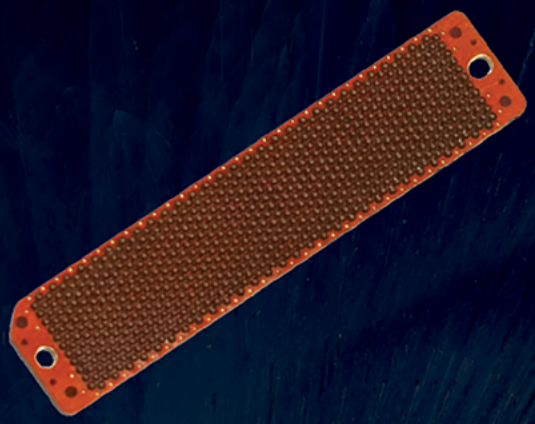


Semiconductor Package Test



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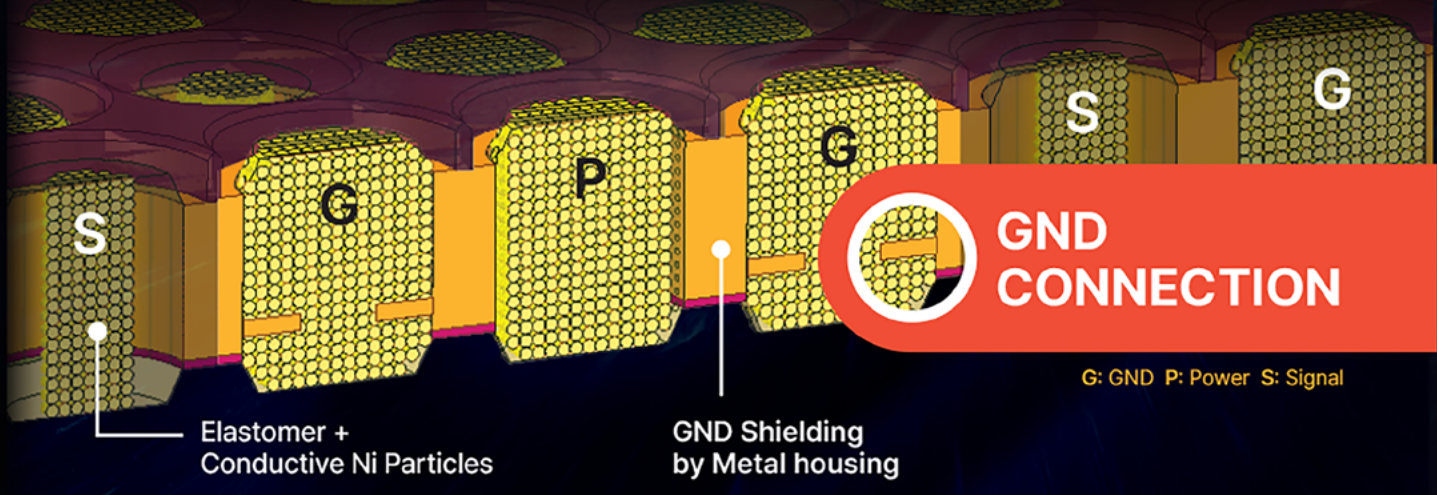

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50Ω, 0.80mm pitch	Spring pin	Elastomer	ELTUNE-coax™
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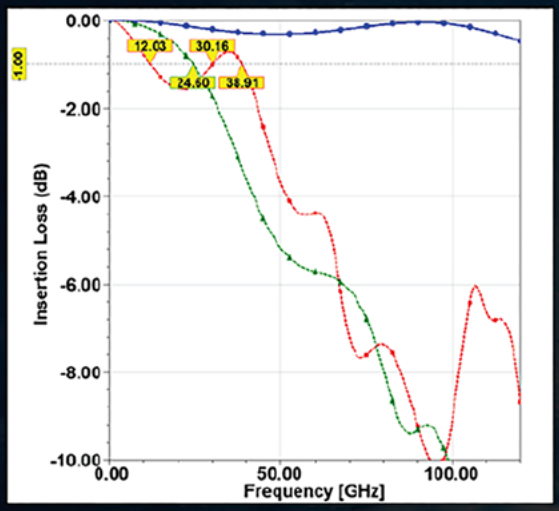
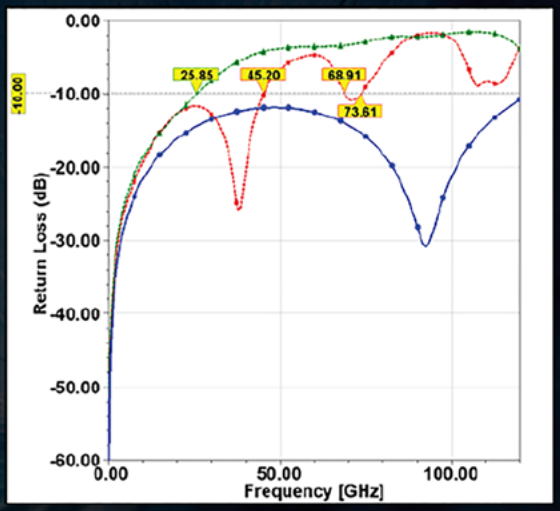
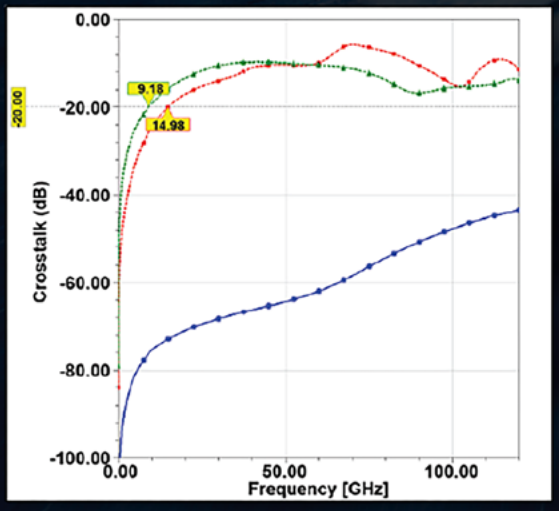
Insertion Loss(S21) @-1dB	12.03	24.60	>100
Return Loss (S11) @-10dB	45.20	25.85	>100
Crosstalk (S31) @-20dB	14.98	9.18	>100



Insertion Loss



Return Loss



Crosstalk

TSE USA

Jong M. Lee jmlee@tse21.com
Kevin Kim kevin.kim@tse21.com

TSE HQ

Justin Yun justice@tse21.com
Jimmy Hwang jimmyhwang@tse21.com

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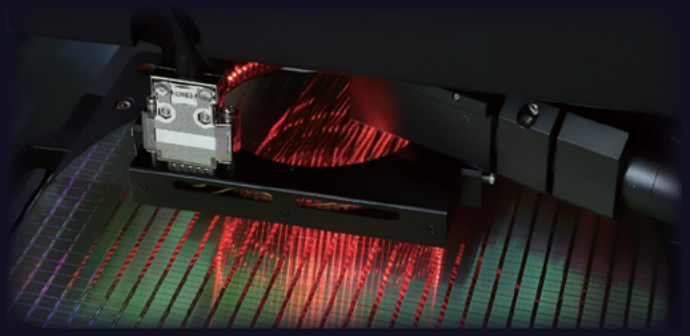

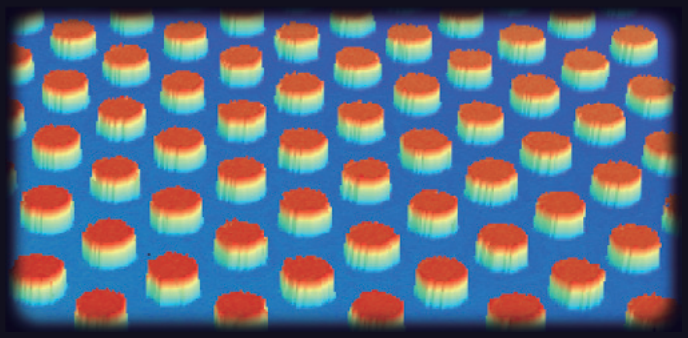

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Sales person : Kevin Lin
hisonic12@intekplus.com

INTEKPLUS TW Office
Sales person : Arthur Tung
arthur@intekplus.com

INTEKPLUS JP Office
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Advanced packaging: Fueling the next era of semiconductor innovation

By Bilal Mohammed Hachemi, Emilie Jolivet [Yole Intelligence]

Today, the semiconductor industry is at the forefront of technological innovation, revolutionizing various applications such as artificial intelligence (AI), 5G communications, and high-performance computing (HPC). As we venture into the generative AI era, there is an ever-growing demand for more powerful, compact, and efficient electronic devices. In this pursuit, advanced packaging has emerged as a crucial enabler, pivotal in the More-than-Moore era. This article delves into the definition of advanced packaging platforms and how they shape the future of semiconductors.

Advanced packaging (AP) refers to a diverse set of innovative technologies that package integrated circuits (ICs) to increase functionality, improve performance, and provide added value compared to traditional packaging methods, with different I/O density and I/O pitch depending on the targeted application's requirements, performance, and cost (**Figure 1**). In our recent report [1] we consider the following as AP platforms: fan-out (FO) packaging, wafer-level chip-scale packaging (WLCSP), flip-chip ball-grid array (fcBGA), flip-chip CSP (fcCSP), system-in-package (SiP), and 2.5D/3D stacked packaging, including complementary metal-oxide semiconductor (CMOS) image sensors (CIS) using hybrid bonding, high-bandwidth memory (HBM), 3D-stacked dynamic random access memory (DRAM) (3DS), 3D system-on-chip (3D-SoC), 3D NAND, Si interposers and embedded Si bridges.

The significance of AP cannot be overstated, especially in the context of emerging technologies and applications. The following sections present the main drivers fueling the need for AP.

AI and machine learning. AI applications require high-performance computing with low latency. AP platforms like 2.5D/3D stacked packaging, HBM, and Si interposers allow for higher memory bandwidth and improved system integration, critical for AI inference and training tasks.

Generative AI era. The generative AI era emphasizes the ability of AI models to create new data, content, or solutions autonomously. This era demands highly efficient hardware capable of processing vast amounts of data and generating complex algorithms in real time, which is made possible by AP technologies.

5G communication. The rollout of 5G technology demands compact and efficient devices to accommodate complex communication systems. AP solutions like WLCSP and fan-out packaging enable smaller form factors, lower power consumption, and improved

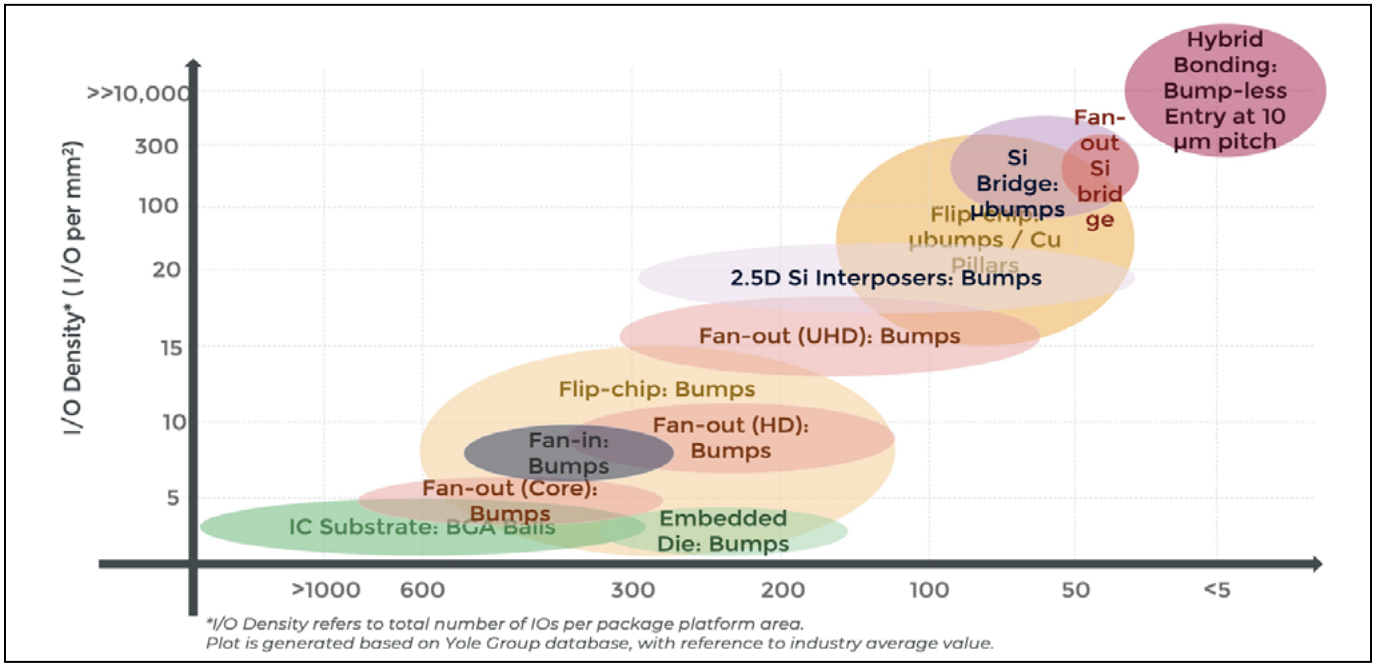

Figure 1: Advanced packaging technology roadmap: I/O density vs. I/O pitch. I/O density refers to total number of I/Os per package platform area. The plot was generated based on a Yole Group database, with reference to the industry average value. SOURCE: [1]

thermal management, making them ideal for 5G devices.

HPC. HPC applications, such as data centers and supercomputers, require fast and reliable processing. Technologies such as fcCSP and FCBGA offer superior electrical performance and higher I/O density, making them well-suited for HPC systems.

Exploring advanced packaging platforms

The following sections describe major advanced packaging platforms.

FO packaging. FO packaging includes three main categories: core fan-out, high-density fan-out, and ultra high-density FO. Core fan-out packaging eliminates the need for wire bonding or flip-chip interconnects, providing improved I/O density, enhanced electrical performance, and efficient thermal management. High-density (HD) FO takes the same concept further, employing advanced redistribution layers (RDL) and interconnect structures to achieve higher I/O densities. Ultra high-density (UHD) FO uses finer-pitch and higher-density multi-layer RDLs for increased component integration, greater bandwidth, and advanced functionality within a compact package. UHD FO is typically applied to larger packages and multi-die integration, using an IC substrate to bridge the gap between the fan-out package and the printed circuit board (PCB).

Wafer-level chip-scale packaging (WLCSP). WLCSP involves packaging ICs directly on a wafer, eliminating individual die singulation and packaging steps. The WLCSP offers compact form factors, enhanced electrical performance, and cost efficiency, making it an ideal choice for mobile devices and wearables, for which size, weight, and performance are essential.

fcBGA/CSP. These techniques involve directly mounting ICs face-down onto organic substrates using solder micro-bumps or copper pillars. Flip-chip BGA/CSP solutions provide a smaller footprint, shorter interconnection paths, higher I/O density, and improved electrical performance than conventional wire-bonded technology. These characteristics are especially critical in HPC applications like servers, gaming consoles, and networking devices.

2.5D/3D stacked packaging. 2.5D/3D stacked packaging involves vertically stacking multiple dies or chips, creating a three-dimensional structure. This platform allows for higher integration levels, improved performance, and reduced form factors, making it an essential technology in addressing the challenges of AI, 5G, and HPC applications. Specific applications within 2.5D/3D stacked packaging include CIS using hybrid bonding technology, HBM for faster data access and improved memory bandwidth, 3D-SoC for highly-integrated systems, and 3D NAND for increased storage density and capacity.

System-in-package (SiP). SiP is a type of AP that integrates multiple ICs, or "chiplets," into a single module. These chiplets, which can include various components like processors, memory, radio-frequency (RF) transceivers, and power management ICs, are interconnected within the package. This high level of integration allows a complete functional system to be contained within a single package, making SiP a space-efficient solution perfect for applications where form factor and integration are paramount, such as mobile devices and wearables. SiP also offers significant flexibility in design and manufacturing, because each chiplet can be fabricated using the most suitable process technology for its function.

Market shares and industry focus

The market for AP platforms is witnessing significant growth, fueled by the increasing demand for advanced solutions. As shown in **Figure 2**, the AP market was estimated at $44.3B in 2022

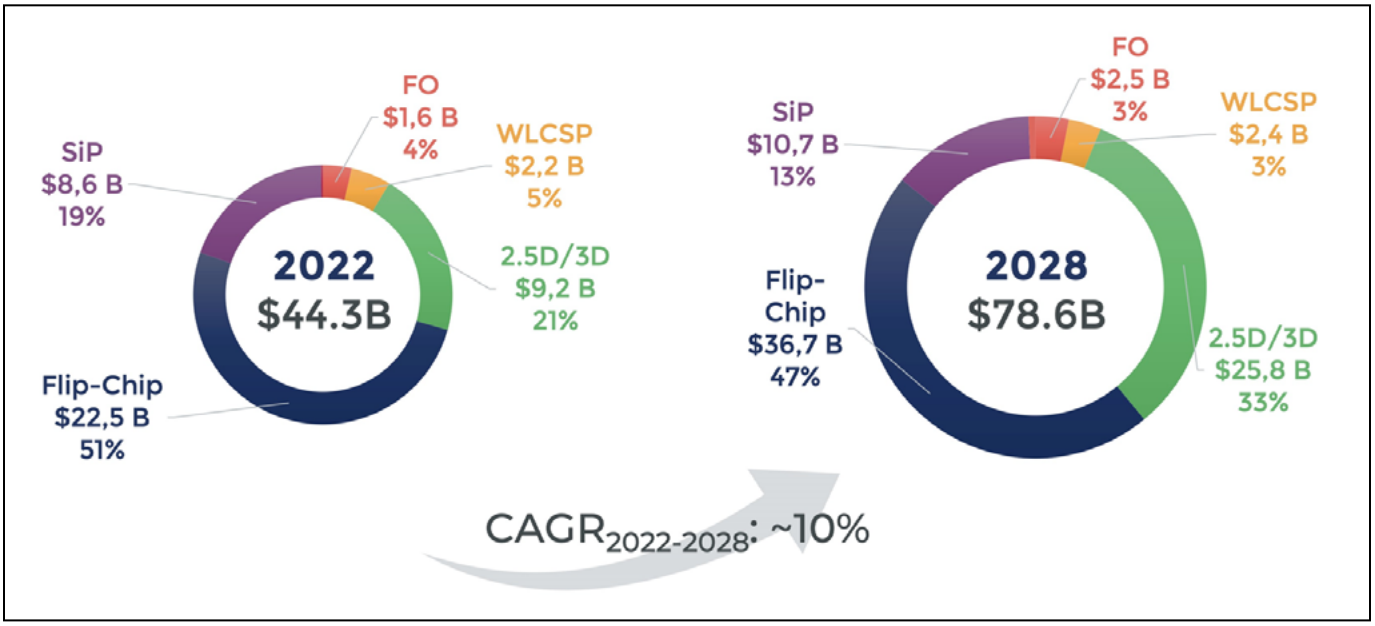

Figure 2: Advanced packaging platform market shares in 2022. SOURCE: [1]

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[1], split as follows: flip-chip with 51% market share, followed by 2.5D/3D with 21% of the market—and expected to be the fastest-growing AP platform by 2028. SiP is estimated at 19% market share, followed by WLCSP and FO packaging with 5% and 4% market share, respectively.

Among the key players, outsourced semiconductor assembly and test (OSAT) companies and major integrated device manufacturers (IDM) and foundries, such as TSMC, Intel, and Samsung, are heavily investing in high-end packaging solutions, with a focus on 2.5D/3D stacked packaging.

As an IDM, Intel has been actively investing in AP technologies. Intel utilizes AP techniques such as its Embedded Multi-die Interconnect Bridge (EMIB) and Foveros for its products and offers customers foundry and packaging services. The company's strong emphasis on innovation and vertical integration positions it as a significant player in the AP arena.

TSMC, a global leader in semiconductor foundries, offers AP services through its 3DFabric™ platform, featuring technologies like Integrated Fan-Out (InFO), chip-on-wafer-on-substrate (CoWoS®) and 3D System-on-Integrated-Chip (TSMC-SoIC®). The company provides a comprehensive wafer-to-packaging solution, covering wafer front-end manufacturing, wafer-level processes, packaging, and on-substrate assembly. Collaborating with packaging companies such as ASE, SPIL, and Amkor, TSMC has solidified its position as a dominant player in the AP market.

Being the world's largest OSAT, ASE specializes in AP technologies, including flip-chip, fan-out, and SiP solutions. The company's collaborations with Intel, TSMC, and other leading semiconductor companies underscore its crucial role in driving advancements in AP technologies.

Amkor, a significant player in the semiconductor packaging and testing industry, offers a diverse range of AP solutions. These include wafer-level packaging (WLP), 2.5D/3D packaging, flip-chip, and SiP solutions. Amkor remains a key contender in the rapidly evolving advanced packaging market with a broad portfolio of AP offerings.

As an IDM, Samsung has a strong presence in the AP market offering solutions such as WLCSP, SiP, and heterogeneous integration (HI) technologies. Samsung uses its fan-out panel-level packaging (FOPLP), flip-chip, wire bond, and 3D stacking packaging capabilities to package its accelerated processing units (APUs) and memory, but it also outsources production to companies like ASE, Amkor, and PTI. Samsung has also started manufacturing FOPLP for Google's Tensor G2 and Baidu's I-CubeS.

HI and chiplets: Revolutionizing AP roadmaps

HI and chiplets represent a paradigm shift in semiconductor design and packaging. The HI concept involves combining different materials, processes, and devices to create a unified system. This approach allows for the seamless integration of diverse functional chiplets on a single package, unlocking new possibilities in semiconductor design and manufacturing.

Chiplets, on the other hand, are a fundamental aspect of HI. According to our definition at Yole, the chiplet approach represents an emerging semiconductor design philosophy that combines two or more discrete dies in a disaggregated SiP design. Chiplets offer more design flexibility, faster time to market, better yield, and economic benefits over possible monolithic alternatives. The functions of chiplets encompass essential intellectual property (IP) blocks found in typical processor SoCs, including central processing units (CPUs), graphics processing units (GPUs), neural processing units (NPUs), I/Os and memory controllers and interfaces, cache memory, and analog functions (SerDes, PLLs, DAC, ADC, PHYs, etc.).

Hybrid bonding: Bridging the gap in HI

Hybrid bonding is a novel technology that enables the vertical stacking of semiconductor devices, potentially significantly boosting device performance, functionality, and reliability. It is a critical enabler in HI, offering exceptional precision and reliability in the bonding process. Hybrid bonding ensures a robust and reliable connection between chiplets, enhancing their integration within the advanced packaging platform. This technology has unlocked new possibilities in semiconductor design, enabling the development of cutting-edge solutions that were once considered impossible.

Hybrid bonding is a cutting-edge technology that enables diverse chip architectures, catering to high-end applications like HPC, AI, servers, and data centers. As the technology matures, it is expected to expand further into consumer applications, memory devices, and mobile and automotive applications, benefiting from high-performance die-to-die connections. The concept of HI is driving innovation in packaging technologies to meet specific performance, size, power consumption, and cost requirements. Hybrid bonding emerges as a feasible pathway for high-end HI applications, with tiny copper pads embedded in dielectric, forming both dielectric-to-dielectric and metal-to-metal bonds. This bonding technology provides numerous advantages, such as significantly increased I/O connections, minimal signal delay, expanded bandwidth, higher memory density, and improved power and speed efficiencies.

The AP technology roadmap illustrated in **Figure 3** presents an intriguing progression of miniaturization and increasing density in four key elements: 3D stack pitch, bump I/O pitch, RDL line/space, and ball I/O pitch over a decade. The 3D stack pitch highlights a clear trend toward miniaturization across hybrid bonding methods: wafer-to-wafer, die-to-wafer, and die-to-die. With wafer-to-wafer, we observe an impressive reduction from 2µm in 2019 to a projected 0.8µm–0.5µm by 2029. This represents a significant achievement in reducing pitch size, which might enable the integration of more components and potentially enhance performance.

Similarly, die-to-wafer hybrid bonding is expected to shrink from 10µm in 2022, to 6–4.5µm by 2029. This also suggests a push towards higher-density packaging, which can lead to smaller, more efficient devices. However, the reduction rate in pitch size appears

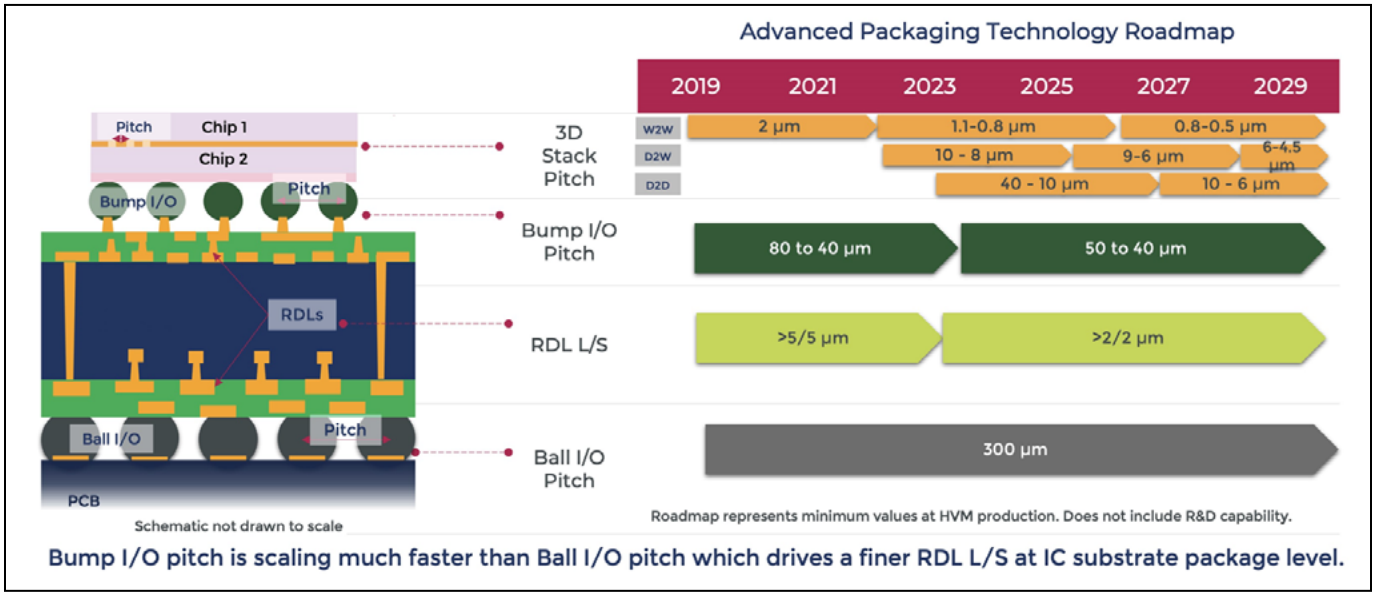

Figure 3: Advanced packaging technology roadmap: I/O pitch and RDL L/S. SOURCE: [1]

slightly slower than in wafer-to-wafer bonding, reflecting some challenges in deploying this technology.

Though appearing later in the timeline, die-to-die hybrid bonding will see a substantial reduction from 40–10µm in 2023, to 10–6µm by 2029. The significant drop in pitch size may reflect rapid advancements in this method, which could offer an alternative route to high-density packaging.

For bump I/O pitch, there is a considerable reduction from 80–40µm between 2019 and 2023. However, the following years up to 2029 show a slowdown in the reduction trend, with the pitch ranging between 50 and 40µm. This plateau could suggest that technology is reaching its physical limits or encountering manufacturing challenges. The RDL line/space is expected to shrink, decreasing from less than 5/5µm in 2019, to less than 2/2µm by 2029. This consistent trend toward smaller dimensions signifies the push for higher-density interconnects and more compact packaging designs, potentially leading to increased performance. Lastly, the ball I/O pitch demonstrates remarkable consistency, maintaining a size of 300µm throughout the decade. This stability might indicate a mature and optimized technology.

Summary

Advanced packaging has become a linchpin of progress in the semiconductor industry, paving the way for AI, 5G, and HPC. The diverse range of AP platforms, including fan-out packaging, WLCSP, fcBGA/CSP, SiP, and 2.5D/3D stacked packaging, coupled with the transformative potential of HI and chiplets, is reshaping the landscape of semiconductors.

As the generative AI era unfolds, AP technologies will continue to drive innovation, enabling smaller and more powerful electronic devices and propelling us into a future of limitless possibilities. The semiconductor industry will continue to evolve, and AP will remain at the forefront, unlocking new capabilities and shaping tomorrow's technology.

With continuous advancements in AP technologies, even more groundbreaking applications and solutions that will redefine how we interact with technology in the years to come can be anticipated. The roadmap embodies the evolution of AP technologies, highlighting a clear trend toward miniaturization and increased density. However, it also highlights areas where innovation is plateauing, indicating the need for breakthroughs or alternative approaches in the future.

Reference

1. Status of the Advanced Packaging Industry 2023 report, Yole Intelligence.

Biographies

Bilal Mohammed Hachemi is a Technology & Market Analyst at Yole Intelligence, part of Yole Group, Lyon, France, working within the Semiconductor & Software division. He is a member of Yole's packaging and manufacturing teams and contributes daily to the analysis of packaging technologies, their materials, and manufacturing processes. Bilal obtained a PhD in nanoelectronics from Grenoble Alpes U. (France). He also studied at IAE Grenoble for a Management Master's degree. Email bilal.hachemi@yolegroup.com

Emilie Jolivet is Director of the Semiconductor, Memory & Computing Division at Yole Intelligence, part of Yole Group, Lyon, France, where her specific interests cover packaging and assembly, semiconductor manufacturing and computing, and software fields. Emilie manages the expansion of the technical and market expertise of the Semiconductor, Memory and Computing Team. She holds a Master's degree in Applied Physics specializing in Microelectronics from INSA (Toulouse, France) and also graduated with an MBA from IAE Lyon.

Improving wafer test efficiency and minimizing cost per die

By Luca Fanelli [SPEA America]

The ever-growing electronics demand for increasing performance and functionality, and for reducing system form factor, power and cost at the same time, is driving the rollout of innovative chip architectures. New semiconductor materials, alternative pad designs, and ever-shrinking geometries are raising the complexity and the cost of wafer test, posing tough challenges—especially on the probing side. These trends are driving the need for innovative test techniques able to increase capacity and control capital equipment cost. This article surveys the trends impacting wafer test today and the industry's response to these challenges. In particular, a new approach to wafer testing, based on multiple flying probe cards, has been introduced in order to allow manufacturers to increase test efficiency, thereby minimizing the cost per die.

Efficient use of the silicon surface

The need to reduce costs and maximize yield often calls for a more efficient use of the semiconductor silicon, both on a planar level and on a vertical level. The following sections discuss these two levels.

Efficient use at the planar level. On the planar level, varied wafer layout geometries, differing from the traditional squared-based dies, are seeing wider adoption. To understand how geometry can be used to maximize a surface area utilization, we can take our starting point from one of the world's most famous graphic artists: Maurits Cornelis Escher. Born at the end of the 19th century, this mathematically-inspired genius has made wide use of a technique called "tessellation" that involves the covering of a plane surface by repeating over and over again a shape, without any gaps or overlaps. The shape itself can be more or less complex, as long as its repetitions on the plane can intersect perfectly, without leaving any gaps. Other than creating beautiful and visionary images, a similar technique can also be used as a cue when designing silicon wafer layouts (**Figure 1**). Certain non-square dies, such as triangular dies, greatly elongated rectangular dies, parallelogram dies, trapezoidal dies, L-shaped dies, and the like, are able to be laid out in the area of a circular semiconductor wafer more efficiently than square dies. Further, a peripheral area of these certain non-square dies is advantageously increased relative to the area contained within the peripheral area to accommodate increased I/O connections to the active elements of the die.

In addition to varied die geometries, multi-project wafers (MPW) are also often used, especially in the case of low- to mid-volume production runs. They amalgamate different chip designs—with different shapes—on the same silicon wafer, thereby amortizing the wafer fabrication costs across many designs, teams, and users.

Optimizing on a vertical level. As the form factor of chips is continuing to shrink, while the demand for increased connectivity and functionality shows an unabated rising trend, the adoption of technologies that require 3D approaches for the integration of devices and system design is growing. In particular, for some complex applications (e.g., we can think about miniaturized medical devices requiring multiple functions to be squeezed into the size of an ingestible pill), a vertical silicon optimization allows higher packing densities as well as shorter chip-to-chip interconnects.

In the past, we used to have a silicon substrate, on top of which we had the silicon structure of the die. However, it's not uncommon today to have 3D structures that include dies on both sides of the silicon with exposed pads on the top and the bottom. In other cases, the dies are made of multiple layers covering the entire vertical structure, so that we have a single die with access from the top and the bottom. Applications like microelectromechanical systems (MEMS) require such multi-layer structures in order to achieve the mechanical functionality of the device (**Figure 2**).

The fabrication of vertically-interconnected multilayer stacks is enabled by specific wafer bonding techniques and can use silicon-top-silicon layers or varied materials, such as glass (**Figure 3**). The advantages offered in terms of performance, form factor, and integration, are fueling the spread of both double-sided wafers with single side dies, and double-sided wafers with pass-through dies.

Impact on the testing process

As we have seen, non-square dies, non-regular geometries in the wafer layout, and MPWs are all ways to use the semiconductor wafer area in the most efficient way. Besides having advantages with respect to manufacturing costs, they also have an impact on manufacturing and test processes, posing enormous challenges on the probing and test side.

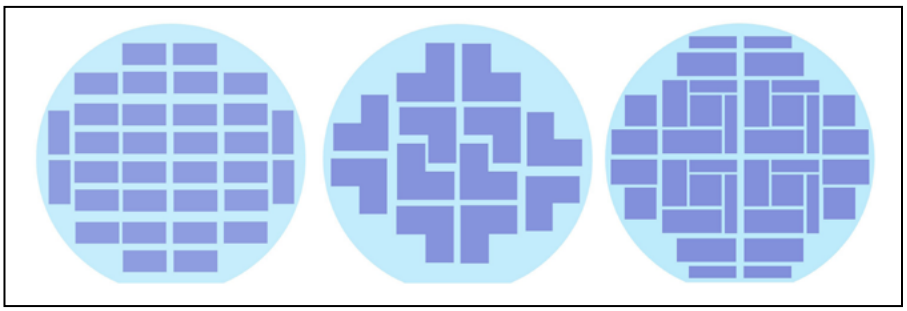

Figure 1: Geometry designs that maximize a surface area utilization can be seen.

Many wafers cannot be tested at all using standard prober architectures that involve a wafer prober where the wafer is docked on a chuck, and a probe card that is docked to the tester positioned on the top of the wafer. If you have uneven geometries on the wafer, the conventional way of probing the wafer with a probe card is not viable because the probe card requires all the dies with the same shape and orientation. If you have different dies with different shapes on a MPW, you also cannot use a traditional prober unless you change the probe card to test different parts of the wafer with multiple insertions. As for the wafers that have dies mounted on both sides, they can be tested with two insertions: you test one side first, then you flip the wafer and test the opposite side. Conversely, a wafer with pass-through dies cannot be tested at all.

To enable the adoption of these technologies and designs, new test methodologies are being developed to leverage probing technologies that enable higher parallelism and lower the cost of test, while meeting the rapidly evolving technical challenges posed by trends in IC design and manufacturing.

Overturning the concept of probing

An alternative approach to probing consists in inverting the way you probe wafer dies: instead of moving the wafer under a probe card that is docked to the tester—as it is commonly done on every test floor—we have developed a prober architecture able to move multiple mobile probe cards over the wafer surface. This new technology combines our experience in both flying probe technology and mixed-signal testing. With this new technology, up to eight different small probe cards (four on the top, and four on the bottom side) can be equipped simultaneously on our TH2000 prober. Each one is mounted on an independent robotic axis that moves in the X, Y and Z directions (Figure 4).

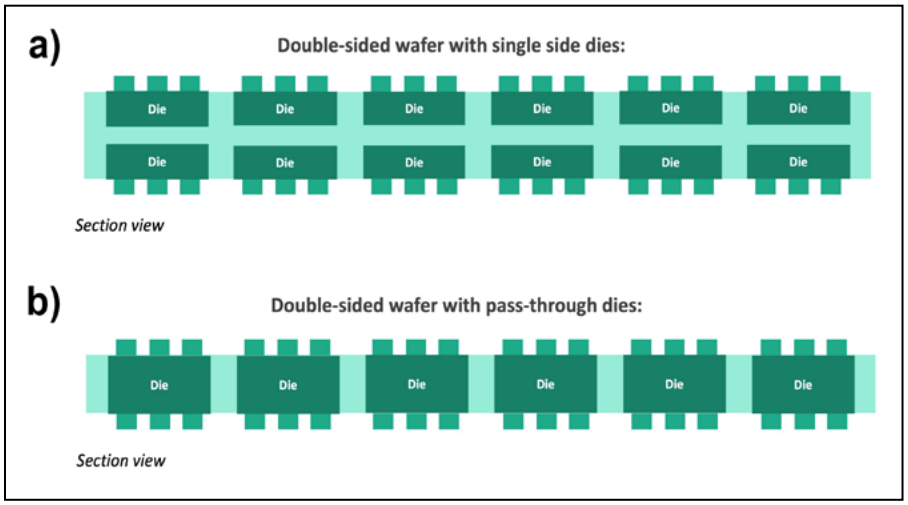

Figure 2: Double-sided wafer layouts can include: a) dies on both sides of the wafer; or b) pass-through dies with access pads from the top and the bottom sides.

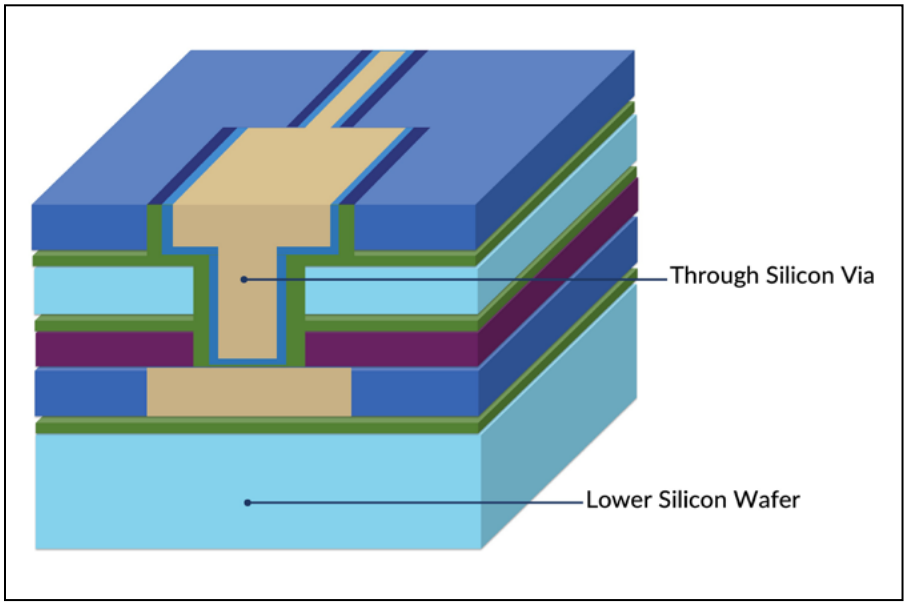

Figure 3: Vertically-interconnected multilayer stacks offer advantages in terms of form factor and functional integration.

Testing wafers with varied geometries

Each of the eight probe cards on our new prober can have a different design, adapting to different die shape or pitch, including unconventional and high-density geometries. This design feature extends the range of applications that can be fully tested at the wafer level.

With a single prober insertion, it is possible to: 1) perform both control pattern test and pad test; 2) test MPWs, dedicating a probe card to each specific device layout; and 3) test wafers with uneven geometries (e.g., with mirrored or rotated layout for the different dies). In all these cases, each probe card fulfills a specific test function, with a proper probing layout, working on the whole wafer area or in a portion of the wafer according to the wafer layout.

Probing on both wafer sides

Because the double-side probing on a single die (Figure 5) can be performed with any combination of top and bottom axes, testability issues are no longer a limitation to the wafer layout, which can be designed in order to minimize the cost per die. The possibility to contact a pad on the wafer from both sides simultaneously enables several limitations to be overcome. For example, continuity testing of pass-through dies becomes possible, as well as testing of multi-layer wafers (top-top, bottom-bottom, top-bottom), and also "virtual known-good die (KGD) testing." All these test operations imply that in addition to the probing capability, there is the necessity to rely on extremely accurate measurement instrumentation—so our prober includes dedicated test resources. A set of built-in measurement modules was designed to offer the required

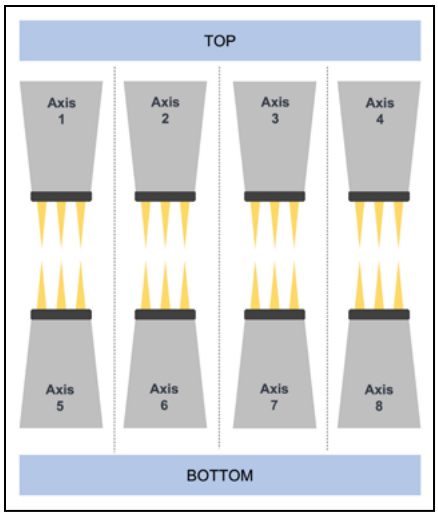

Figure 4: Instead of moving the wafer under a probe card that is docked to the tester, the architecture of the TH2000 prober includes eight independent robotic axes, each one moving a small probe card over the wafer surfaces.

performance, thereby minimizing the signal path length that ensures signal integrity and measurement reliability.

The top-bottom continuity test, as an example, consists in measuring the continuity between the two sides of every pad, and can be performed with resistance values ranging from micro-ohms to giga-ohms, and capacitance values ranging from pico-farads to milli-farads.

The extreme accuracy in resistance test, combined with the possibility to contact a pad from both sides simultaneously, makes it possible to perform a "virtual KGD test" on power devices that executes at the wafer level some challenging measurement, such as the dynamic RDSon. This is possible as the architecture of our prober eliminates the influence of traditional prober chuck resistance, thereby making the current path length equivalent for every die, which is contacted by a couple of probes (one on top, one on bottom) as shown in Figure 6.

Probe card technologies for different applications

The probe cards can be based on different technologies (cantilever, spring probes, MEMS probes, wiring probes), and can be designed according to the die density, shape and map. The different probe card technologies address different applications. Cantilever probes represent the best option for testing discretes, diodes, and transistors that require high current (often exceeding 512A). For testing digital devices with a short distance between the pads, vertical probes and wiring probes offer better performance because they can work with pitches of a few tens of micrometers.

Testing multi-layer stacked wafers

As we have seen, vertical integration is very effective as a way to reduce the chip form factor while increasing the device functionality Looking closer, we observe that multi-layer silicon wafer layouts often include verification patterns in addition to the device dies. These patterns are meant to simplify the volume production test of the devices because the quality of the wafer can be validated through a kelvin test performed on the verification patterns, with no need to contact every single die individually. However, the manufacturing process of these products often need to be refined through a long characterization to ensure that the process itself does not introduce high rates of product failures. During the process characterization, it is important to perform additional tests on every die in order to have a complete and precise control of the effects of process variations. To cross-check the manufacturing process goodness and validate the reliability of the verification pattern tests, top-bottom capacitive and resistive tests should be performed on every chip, in addition to the kelvin tests performed on the verification patterns. To keep under control every phase of the process, this same test sequence should be repeated as every layer of the structure is added.

The prober architecture based on multiple mobile probe cards can be used to satisfy the test requirements noted above, during both the characterization phase and the volume manufacturing phase. The same prober can mount—on the different axes—probe cards for contacting the verification patterns and probe cards for contacting the single pads of individual dies. Without changing the machine setup, the prober can then be used for the production test on the verification patterns, keeping the possibility to perform additional tests on specific individual pads as needed.

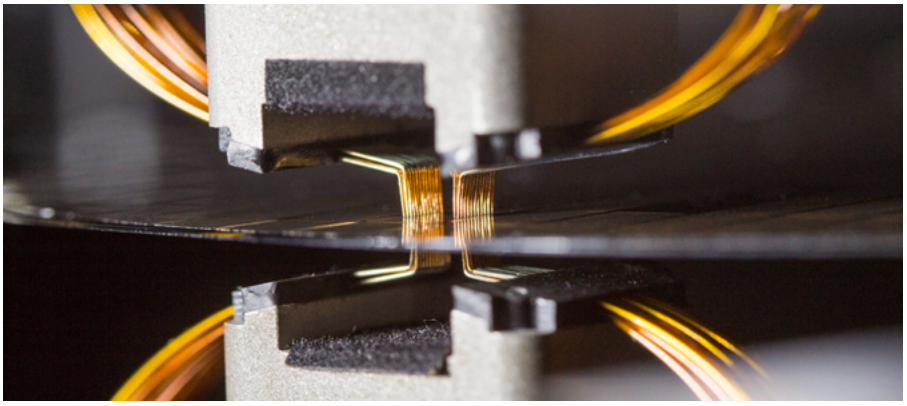

Figure 5: Simultaneous probing on both sides of the wafer.

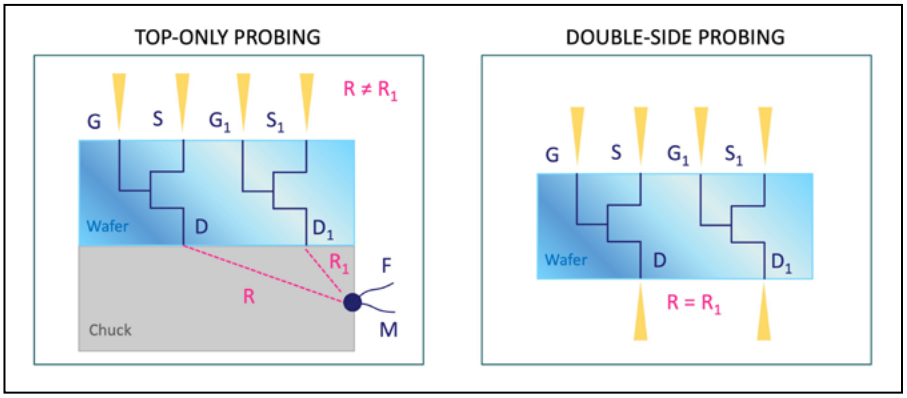

Figure 6: Probing on both sides of the wafer permits extremely accurate resistance measurements because the signal path length is the same for all the dies (there is no influence because of the chuck resistance).

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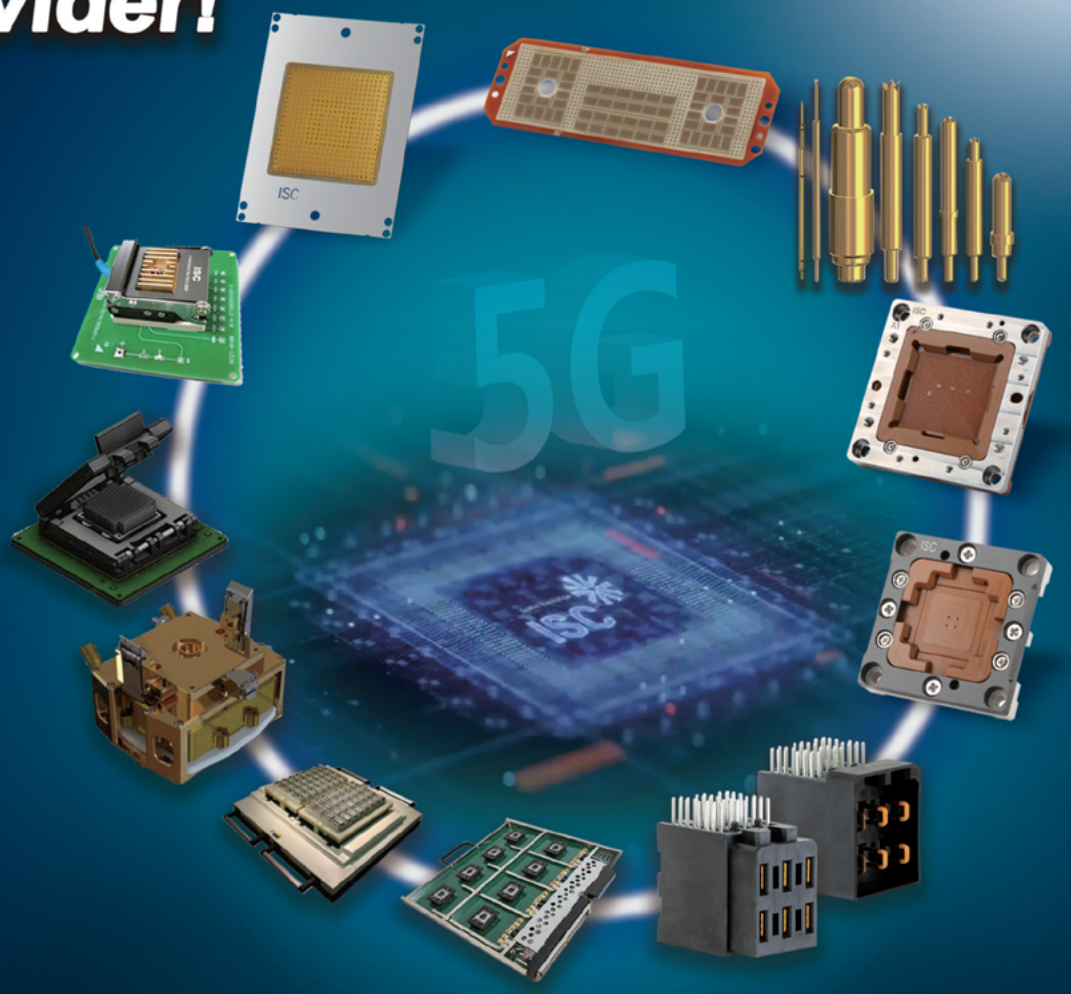

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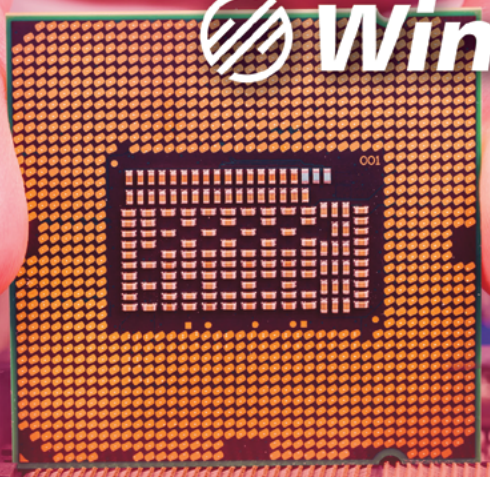

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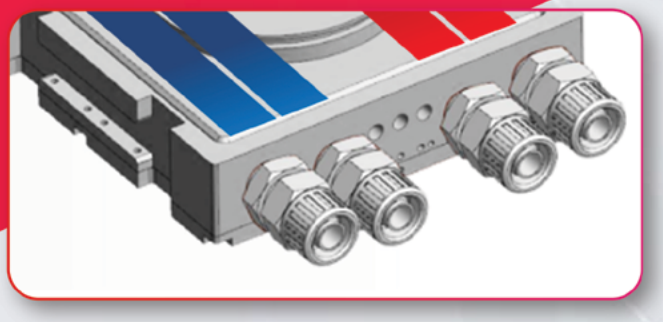

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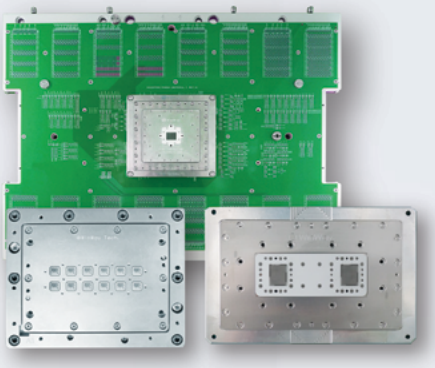

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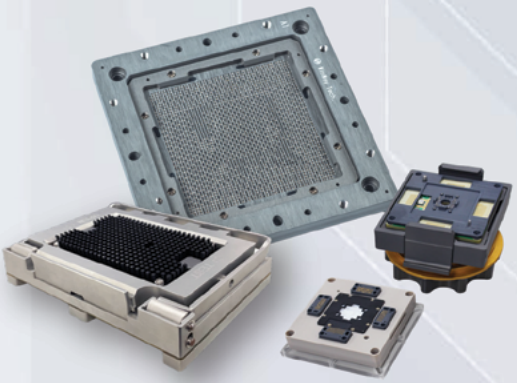

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Spring Probe

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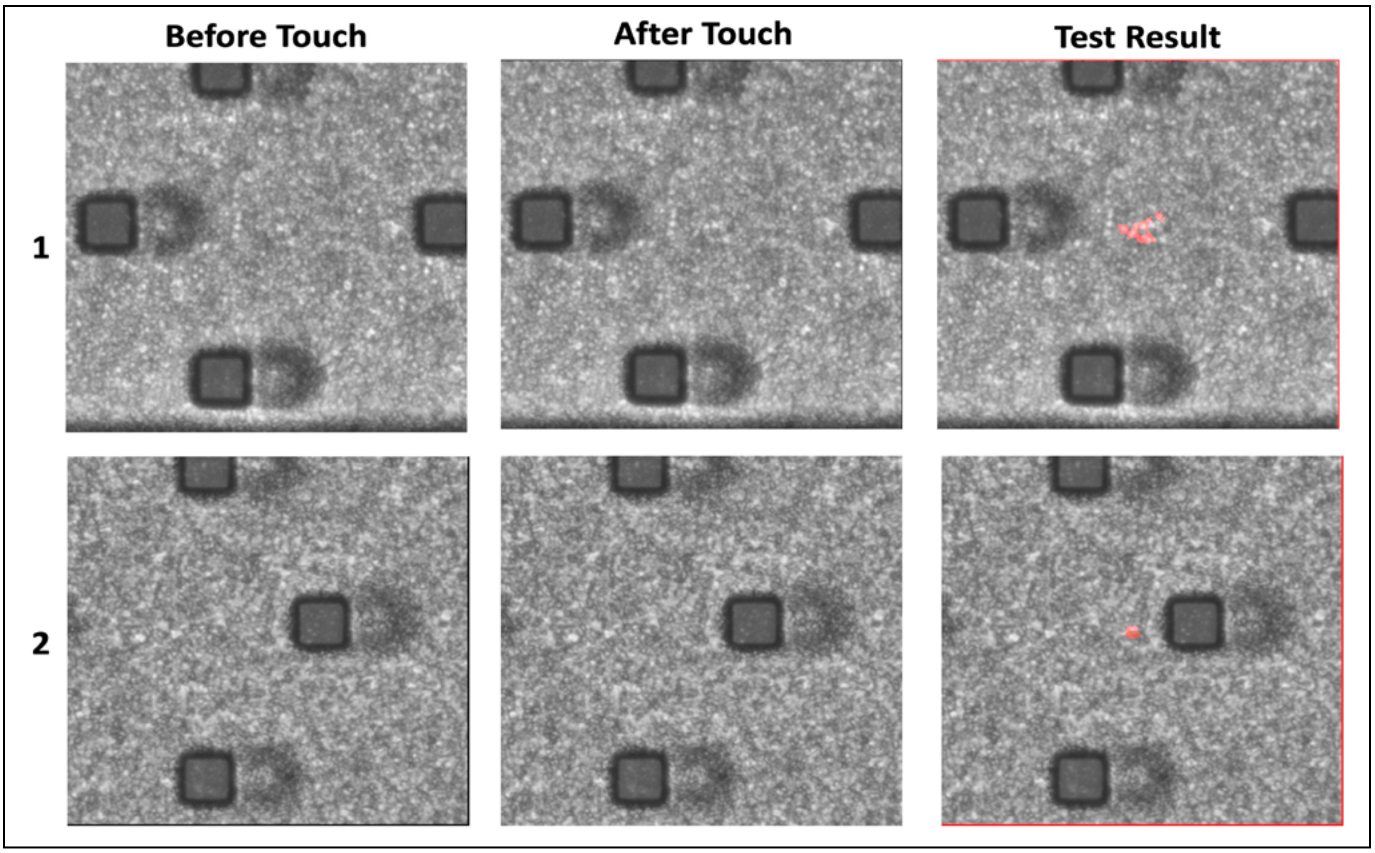

Figure 7: Examples of automatic probe mark detection. A specific combination of standard geometrical algorithms and AI-based algorithms detects the touch point and makes the required corrections. The probe used has a diameter of 20µm, while the red mark is approximately 16x12µm.

Automatic warpage compensation and probe mark auto detection

Innovations in wafer designs and technology are not the only challenge to be faced when it comes to the development of a wafer prober for production testing. In order not to transform testing operations into a bottleneck in the manufacturing process, the prober should embed as many automation features as possible and be autonomous and require minimal human intervention.

The need to compensate for possible wafer warpage and the need to detect the mark left by the probe on the wafer surface represent two challenges where automation can be advantageous. The verification of the wafer planarity is essential before probing to be sure of the exact pad position. The adjustment of probing offset and overdrive parameters can be tough and time-consuming. To speed up and automate this operation, an automatic optical inspection performed before and after the probing can be helpful.

On the TH2000, warpage is measured by a laser surface mapping and automatically compensated. A specific combination of standard geometrical algorithms and artificial intelligence (AI)-based algorithms has been developed to efficiently and accurately detect the touch point and make the required corrections. In order to be able to visually identify the touch, images are acquired before and after the probe touch. At the end, it is possible to see the result of the identification of the touch by the developed image processing algorithm. Two examples of automatic probe mark detection are shown in **Figure 7**.

Summary

While traditional prober architecture remains the standard choice for most wafer products, a different approach based on multiple mobile probe cards can solve many tough challenges in testing. Solving these challenges allows for a complete test at the wafer level of the most complex and innovative technologies, as well as of those layout designs that break the rules of square-die geometries in order to maximize the yield. Testability issues can be solved for non-square dies, mirrored and uneven geometries, as well as double-sided wafers and multi-stack wafers, giving a boost to their adoption by the industry.

Biography

Luca Fanelli is president and GM of SPEA America, the US-based subsidiary of the automatic test equipment manufacturer SPEA, that has three branch offices in Tyler, TX, Phoenix, AZ, and Santa Clara, CA. He joined SPEA in 2006 and has held various positions within the company including managing the entire Semiconductor Engineering Team. He was later appointed Technical Sales Manager for the North America Sales Team. In March, 2017 he was appointed as Manager of the entire Semiconductor Division in North America. He received his MS degree in Electrical Engineering from the Polytechnic of Turin, Italy. Email luca.fanelli@spea.com

Packaging innovation drives inspection requirements for automotive apps and more

By Olivier Dupont [KLA Corporation]

The chip packaging challenges that emerged in the development of segments like mobile and high-performance computing (HPC) were complex, but the solutions developed so far are proving to be valuable to the evolution of chip packaging for the automotive domain as well—and this is no coincidence (**Figure 1**). In-vehicle advanced driver assistance systems (ADAS) and infotainment technology are fundamentally mobile and likewise constrained for power and space. Yet the compute and graphics horsepower increasingly required to drive automotive systems is giving rise to a new generation of artificial intelligence (AI)-guided supercomputers on wheels.

Large, single-die monolithic designs are struggling to remain cost competitive for many applications, including advanced automotive applications. But the evolution to modern 2.5 and 3D multi-die, disaggregated architectures (chiplets, systems in package (SiP), etc.) isn't just an economics play (**Figure 2**). Rather, the advanced packaging technologies have become essential to overall chip performance itself, making it possible to outperform monolithic designs in several dimensions.

SiP and antenna in package (AiP) integrations introduced quality challenges related to their multi-die layouts, electromagnetic interference (EMI) shielding, non-traditional package shapes, and more, as package geometries shrink. The lessons learned while developing strategies to increase yield for these packaging types are guiding our approach to inspection and metrology for automotive applications today as they evolve to more advanced technologies.

More traditional packages like quad flat package (QFP), quad flat no-lead package (QFN) and wire bond ball grid array (BGA) continue to be the dominant automotive packages. They are highly reliable and very cost-effective to

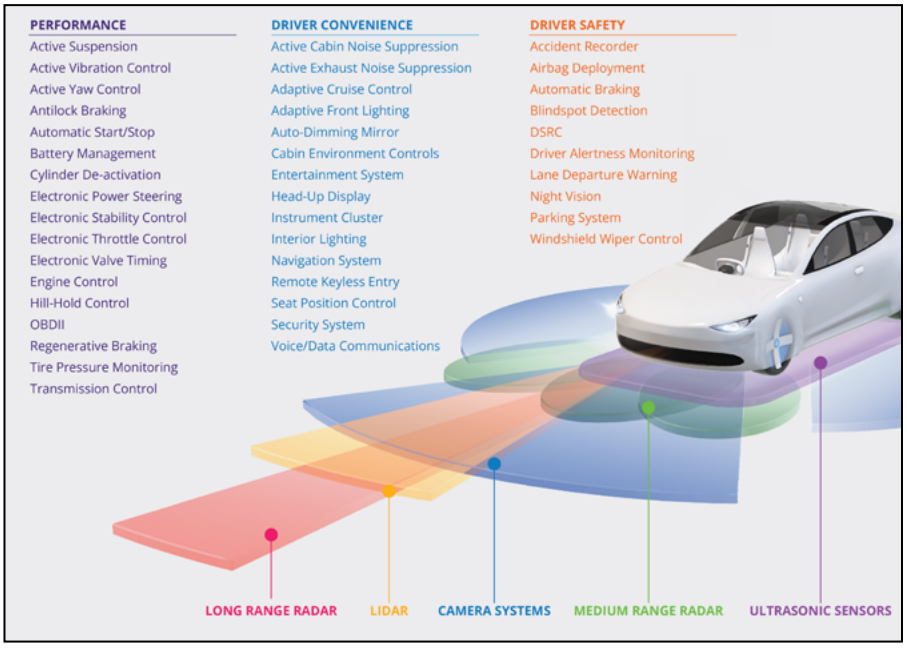

Figure 1: Semiconductor chips play a major role in the evolution of automotive features toward more advanced capability.

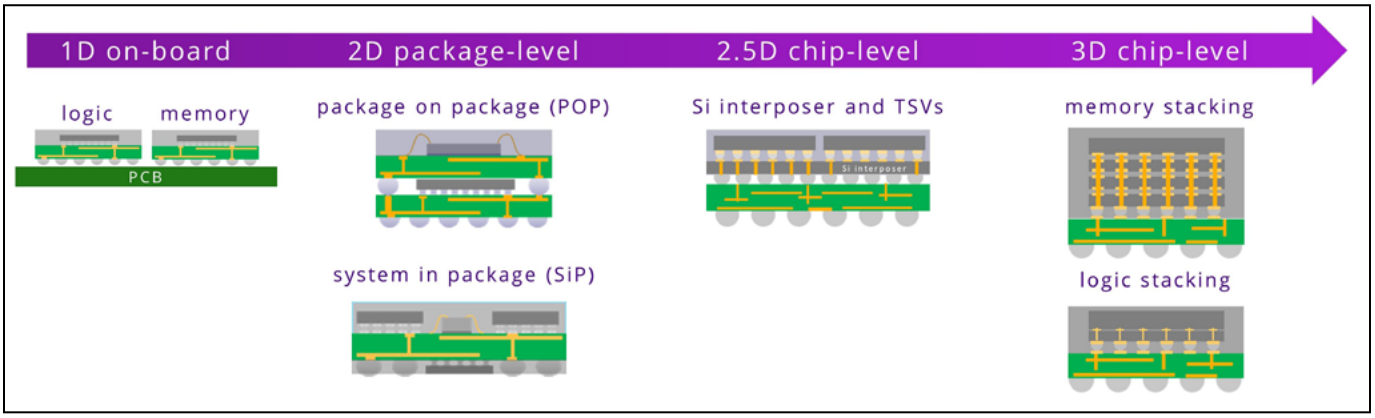

Figure 2: Evolution of advanced packaging technology.

manufacture. Advanced packages such as flip-chip BGA (fcBGA), flip-chip chip-scale package (fcCSP) and low-density fan out (LDFO) or complementary metal-oxide semiconductor (CMOS) image sensors (CIS) are increasingly used in advanced driver assistance system (ADAS) applications. Diverse package designs are being adapted to automotive functions to promote efficient and capable in-vehicle component configurations despite significant space, power and thermal constraints.

Lessons learned in mobile and HPC apps

Inspection and metrology technologies evolved in lock step with mobile device technology (smartphones, tablets, etc.) to accommodate advanced integrations and varied chip form factors optimized to fit within compact device enclosures. Separately, HPC technology has established multi-die package designs for optimized thermal management leveraging advanced heat sink techniques, which is invaluable knowledge for vehicles designed for harsh operating environments.

Together, mobile and HPC innovation have demonstrated the communication improvements achievable between chips—the memory and processor, for example—by moving the chip die physically closer together. By stacking the chips on top of each other (3D), or by placing them on an interposer side-by-side (2.5D), or facing each other on both sides of the substrate (SiP), packaged devices can be more compact while also achieving improved communication bandwidth, which is critical.

Over time, the semiconductor content has adapted to the environmental conditions and available real estate; this has paid-off through improved design flexibility that is now directly relevant and applicable to the automotive domain. But automotive applications also invite new and similarly daunting challenges.

Automotive challenges

The automotive industry is, for good reason, extremely conservative in its approach to developing vehicle platforms. Risk is to be avoided at all costs, and chip reliability is naturally paramount to automotive safety. As a consequence, automotive system designers prefer tried-and-true technologies that are validated and field-proven over decades. However, automotive original equipment manufacturers (OEMs) and Tier 1s may no longer have this luxury for cutting-edge features. Vehicles are getting increasingly electrified, for one thing, as electric vehicle (EV) adoption and regulation gain steam. Vehicle componentry is getting dramatically more sophisticated in the evolution to levels 4 (high automation) and 5 (full automation) autonomous driving (**Figure 3**). Furthermore, recent automotive semiconductor shortages have served to remind us that semiconductor content requirements will only continue to grow in the automotive domain.

Meanwhile, the zero-defect directive is getting harder and harder to achieve. The demand for automotive innovation is pushing for the adoption of more leading-edge chip technology into vehicles and therefore is shrinking the "comfort zone" time lag separating adoption cycles for leading-edge consumer and automotive

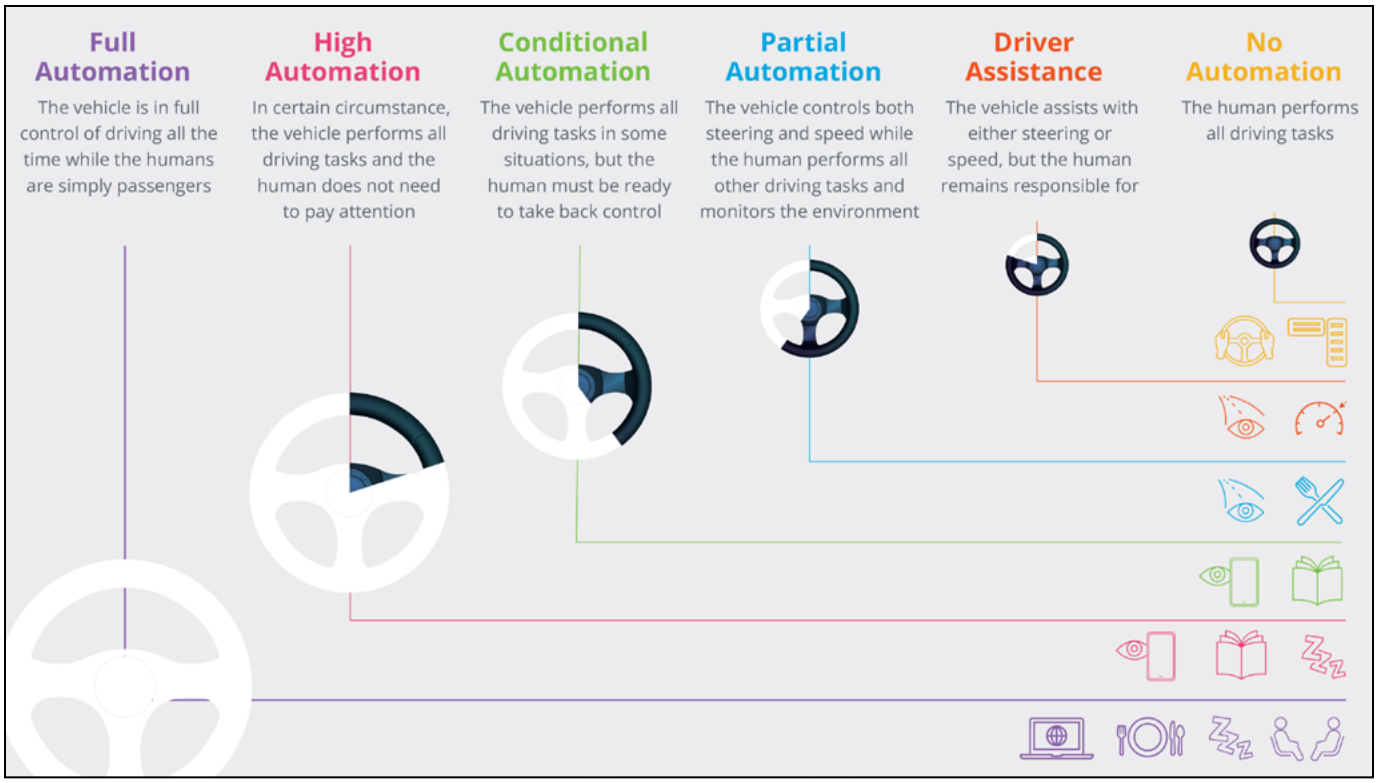

Figure 3: There are five levels of autonomous driving from: 1) driver assistance, 2) partial automation, 3) conditional automation, 4) high automation, and finally, to 5) full automation.

devices (**Figure 4**). There's a growing imperative [1] to achieve reliability faster on newer technologies, from front end to packaging. As a consequence, high-end defect screening is being increasingly adopted by automotive fabs to reduce escapes for reliability-sensitive devices.

Chip reliability is inextricably linked to yield because the defects that affect reliability can be very similar to the ones that affect yield, occurring perhaps in a different location or at a slightly smaller size. Actions taken during manufacturing to reduce defectivity and improve yield also have a positive impact on reliability. To ensure high reliability on complete multi-die assemblies, the quality must be assured for each individual chip within the package. A defect in any one chip in the stack can have real-world safety implications for vehicle occupants and pedestrians. Furthermore, as packaged multi-die chips proliferate throughout vehicles, the failure risk is compounded.

Though the stakes are much higher in automotive applications, there's an opportunity to apply the multi-die integration lessons learned in mobile and HPC applications to optimize packaged component inspection and metrology for optimal yield with no escapes of faulty packages into the supply chain. Reaching the highest yield is particularly crucial for the economics of the industry. Indeed, as 3D chip integrations grow more complex and expensive—a single multi-die package can cost thousands of U.S. dollars—it's simply no longer feasible, in many cases, to discard an entire multi-die package due to one defective chip. In these loss scenarios, not only do chipmakers sacrifice the value of the completed device, they also squander all of the manufacturing time and the power and resources it required, multiplied for each and every

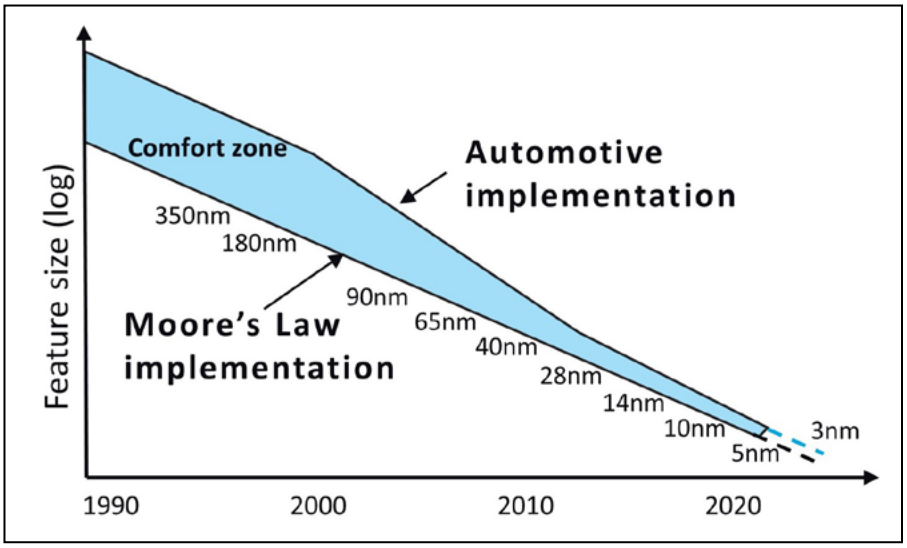

Figure 4: Traditionally, there has been a delay between the development of leading-edge Moore's Law semiconductor technology and the implementation into automotive applications for the increased reliability that comes with process maturity. SOURCE: Oliver Senftleben, BMW

chip within that package. This time and cost lost in the process itself are substantial, yet they are often overlooked. These kinds of challenges result in an increased need for advanced process control throughout chip manufacturing.

360° inspection for classification and reclamation

For 2.5 and 3D multi-die packages, six-side packaged chip inspection has become essential to ensuring device integrity. By optimizing the resolution and illumination of the inspection system, smaller defects can be identified and classified with increased accuracy. The flexibility of tuning illumination (angle and color and combinations thereof) can enable increased contrast for higher detection and more accurate defect classification. Advanced image processing algorithms are also used to further differentiate defects by types.

Achieving automated inspection at high speed also requires continuous advancements in data processing and high-performance cameras with large fields of view (FOV). This provides the ability to inspect more packages simultaneously or inspect larger packages in one single FOV for greater efficiency. Advanced inspection capabilities like these can help avoid escapes, which is the primary concern for the automotive OEM and Tier 1 supplier where safety and reliability are concerned. Moreover, enhanced inspection adds the ability to correctly classify the specific nature of a defect—i.e., scratch, crack, copper exposure, etc.

Reliable classification ensures that chip manufacturers can, in multiple cases, rework packages that were first identified as defective and get them qualified again—another important yield boost. An inspection system's precision ability to distinguish, for example, a fiber from a more troublesome crack across a wide range of advanced package types makes this reclamation capability possible. The broader implications for automotive device integrity and safety speak for themselves. For the automotive OEM and Tier 1, yield optimizations like these are likely to be directly reflected in updated pricing models set by outsourced semiconductor assembly and test (OSAT) services. Yield improvements aided by advanced inspection and metrology will likely make a significant impact on the economics of these pricing arrangements going forward.

Deep learning enhancements

AI implemented as a deep learning solution for component inspection can deliver additional gains in sensitivity, productivity and classification accuracy. Deep learning technology has already proven instrumental in increasing packaging yield, and going forward it will continue to be essential.

Deep learning satisfies a robustness to process variation, instilling greater stability by enabling the inspection tool to automatically cope with variations in the devices' surface features caused, for example, by changes in raw materials or surface roughness. Deep-learning models can automatically adjust for minute process and material changes to keep inspection tools running without the need for manual tuning by engineering. This advanced capability contributes to increased mean time between assists (MTBA) and reduced tool downtime.

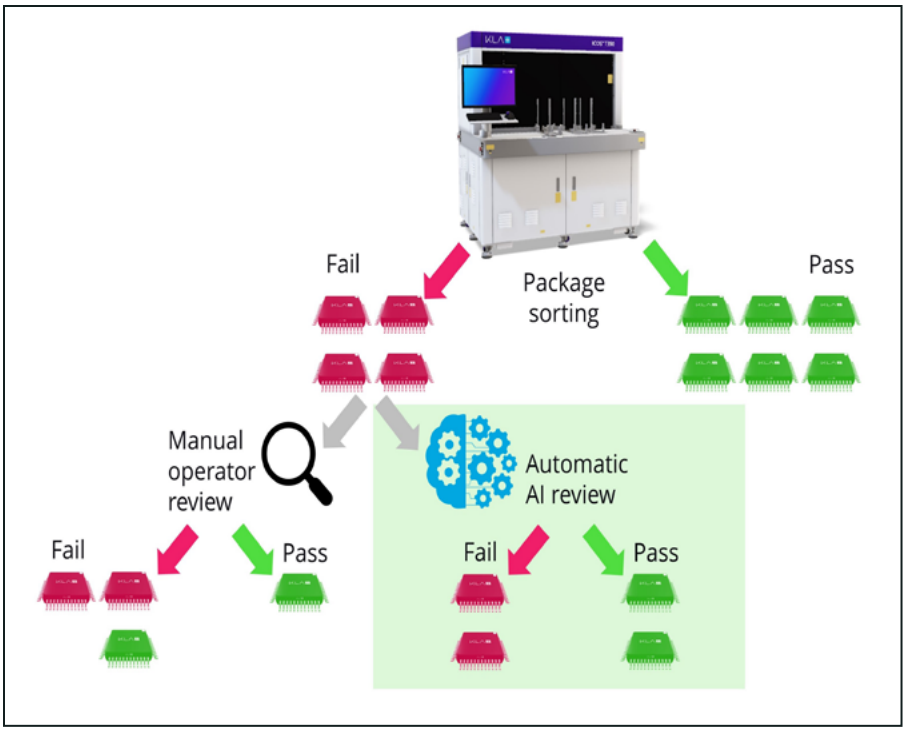

Figure 5: Sorting process for packaged semiconductor components based on defect inspection and metrology. AI-based solutions can provide additional speed and consistency for the best sorting accuracy.

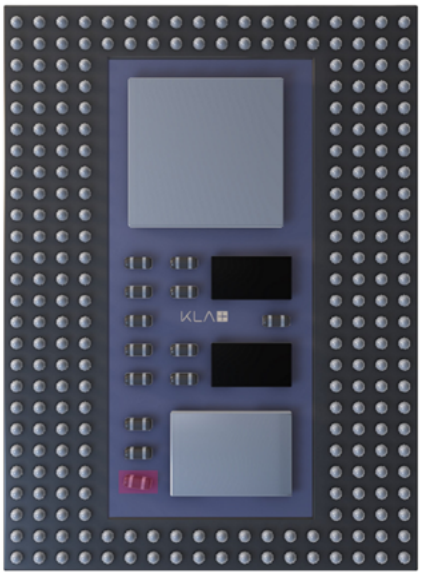

Figure 6: Measurements for every feature on six sides of the package are required at high-speed to ensure all critical dimensions are within specification. One capacitor here within all the solder balls is out of place and would be flagged.

On-tool deep-learning capabilities can enable real-time smarter automatic binning of defect types, thereby providing more accurate feedback on package quality to sort good and bad parts, and requiring less operator review. By doing so, throughput of the sorting process is improved, and manual handling is reduced. This latter benefit can help reduce additional risk of device damage and blind spots in traceability. These improvements ensure that defects are correctly identified and sorted for superior, automotive-grade quality control and yield learning (**Figure 5**).

Evolving metrology requirements

High-speed metrology is essential for checking critical dimensions of chip features. Similar to defect detection, meeting automotive quality requirements at speeds required for high-volume production is a difficult challenge to tackle. Advanced multi-die packages require an increase in the number of overall measurements to be taken, further stressing the need for high-speed automation with higher repeatability and accuracy.

An example of the increased requirements noted above include the measurement of capacitors in a

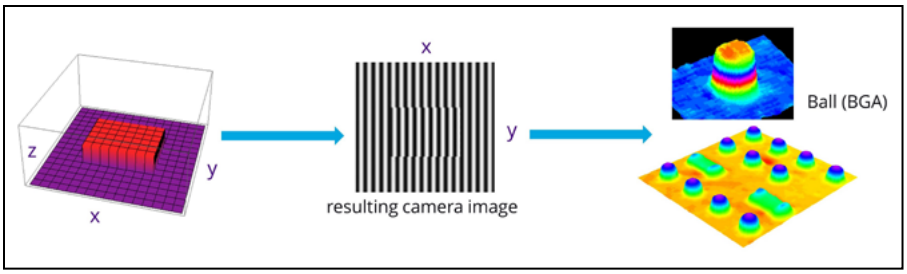

Figure 7: Advanced 3D metrology imaging techniques. Project fringes of light at multiple angles on the package (left), and capture with a camera. Changes in height (z) create a phase shift in the resulting image (center). Height information can be revealed in Z-maps by combining multiple images with algorithms (right).

ball bed: their relative heights must be reconciled to ensure that a tilt or mispositioning of the capacitor isn't causing it to prevent optimal contact of solder balls with the printed circuit board (PCB) (**Figure 6**). In order to do these types of measurements, advanced imaging techniques are used to ensure high accuracy and repeatability. In **Figure 7** we see how projection of light fringes and analysis of their phase shift can provide Z-maps of device surfaces, and then to the determination of critical dimensions. Advanced metrology techniques like this can be designed to achieve enhanced accuracy and repeatability, together with large FOV required for fast processing.

Benefits today and tomorrow

Advanced defect inspection supported by innovative deep learning solutions along with high accuracy, high repeatability metrology techniques help to enable component-level reliability and quality control for safety-critical automotive applications. These innovations will help to support the following:

- Wider range of devices (smaller, bigger, thinner, 3D, irregular);
- More complex features with smaller defects;
- Stricter tolerances for modular assembly;
- Higher quality requirements;
- Maximized tool functionality for high-volume manufacturing; and
- High-speed production with high yield.

At the end of the assembly line, an advanced inspection and metrology strategy provides packaging manufacturers with the data required to improve their yield while effectively sorting components so that defective parts are quickly removed (and potentially restored). In the future, similar high-end process control approaches could be applied earlier in the process, i.e., during assembly, to detect critical issues sooner.

When integrating multiple, expensive die in an advanced 3D package, it's naturally beneficial to detect defects as soon as they arise, well before final assembly. In-process inspection will also give a better insight into the package. When performed only at the end of the assembly process, 360-degree inspection merely extends to the outer layer of the assembled package—after all inspection visibility into the assembled package is lost.

In the future, advanced inspection and metrology may not only be, as it is today, for the incoming integrated circuit (IC) substrate and the final packaged chip, but could be expanded to include testing of the "building blocks" of the multi-die devices, i.e., at pre-assembly. Manufacturers would embrace an interim opportunity to, for example, add a die on the IC substrate and then check overall position and tilt, while looking for any issues like cracks induced by the assembly process.

As an industry, we've largely held a siloed view of front-end semiconductor processes, IC substrates and packaging. But as these technologies continue to evolve and overlap, we envision that shared learning will make it possible to implement new process control strategies for semiconductor content at multiple stages of the integration process, in automotive applications and elsewhere.

Summary

Inspection and metrology techniques for advanced packages in the automotive domain are squarely aimed at optimizing yield and preventing defective chips from being missed, in part by enabling accurate classifications so that escapes don't result in safety issues down the road. Mobile and HPC applications taught us a lot in this regard, and stringent automotive applications will teach us even more.

Advancements in optics provide flexible illumination with high-resolution during six-sided inspection for finding and classifying smaller defects. This is complemented with faster, flexible metrology with high accuracy and repeatability.

All of the above combined with deep learning's crucial role in automating process uniformity and accurate binning are coming together to provide packaging manufacturers with what they need to improve yield and reliability. We anticipate that future innovation in "interim inspections" occurring during multi-die assembly could further pave the way for yield improvements and cost optimizations across the automotive domain.

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Biography

Olivier Dupont is Product Marketing Director at KLA Corporation, Leuven, Belgium. With a PhD in engineering, Olivier Dupont began his career in R&D, then shifted to more customer-facing roles. With this move, he developed an understanding of market needs and experience in product management. After working in various industries, Olivier joined KLA in 2018. As product marketing director, he leads the ICOS Component Inspection Tool portfolio and roadmap. Email olivier.dupont@kla.com

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Challenges with self-assembly applied to die-to-wafer hybrid bonding

By Emilie Bourjot, Frank Fournel, Pierre Montméat, Loic Sanchez, Thierry Enot [CEA-Leti]

The quest for smaller components with better performances at a competitive cost has been the driving force for 3D-IC (integrated circuit) technology developments for several decades. Recent advances in bonding techniques have provided particular benefits for applications such as memory, high-performance computing, and photonics, where performance is strongly linked to the density of interconnections. For such applications, hybrid bonding emerged as a key booster to increase 3D interconnection density.

Hybrid bonding is similar to direct bonding except that it is applied to mixed Cu/dielectric surfaces to create an electrical interconnection between two parts. Direct bonding is quite distinct from thermo-compression and adhesive bonding, which require temperature and pressure, or additional materials such as polymer, respectively, to ensure contact between the two surfaces. In contrast, direct bonding is a spontaneous process, and no external loading is required during its thermal annealing step. However, direct bonding does have stringent surface requirements in terms of topography, planarity, roughness, and particulate contamination. If uncontrolled, irregularities in these characteristics can lead to bonding defects. The two critical parameters for successful direct bonding are clean surfaces and an appropriate topography.

Direct hybrid bonding: W2W and D2W

Two assembly configurations are possible with direct hybrid bonding: wafer-to-wafer (W2W) and die-to-wafer (D2W). W2W hybrid bonding was first proposed by Dr. Suga in 2000, then developed at CEA-Leti with hydrophilic bonding in 2009 in a R&D environment, and then Sony brought it to an industrial level in 2016. It is now a mature process in mass production especially for imaging applications. In this approach, bonding is performed at wafer scale. With the latest generation of W2W bonders, suppliers claim alignment capabilities of less than 3σ. The main advantage of the technique is high throughput. However, there is a drawback in terms of design flexibility, which remains low because the bottom and top dies must have the same dimensions.

In contrast to W2W bonding, hybrid D2W bonding should increase design flexibility. This process re-uses the know-how developed for W2W, but adds dicing and cleanliness challenges. When those challenges are managed, it will pave the way for heterogeneous 3D structures by creating the means to mix and match technologies on a single bottom substrate with high-density interconnections. Moreover, the known-good die (KGD) concept can be applied to increase overall product yield by selecting only good dies before assembly. D2W technology is of great interest for many applications, such as edge devices because of the increasing need for real-time computing of large amounts of data with a limited power budget. Other "More than Moore" applications are good candidates, e.g., photonics, imagers and displays, optical transceivers, and radio frequency (RF).

Today, direct placement D2W is performed by pick-and-place (P&P) processes that make it difficult to reconcile high placement accuracy with high throughput. Indeed, to achieve placement accuracy of better than 1µm, P&P tool throughput must be lower than 1,000 dies per hour. Tool suppliers are examining solutions to increase this throughput, for example, by implementing multiple heads on P&P tools. However, breakthrough D2W processes are needed to remain competitive and to reach industrial requirements. In this context, CEA-Leti has been working for several years on the development of a self-assembly process. This promising process has the potential to increase throughput to several thousand dies per hour thanks to self alignment, and it is the subject of this article.

Self assembly driven by the capillary forces of water droplets

The self-assembly process is based on the use of the capillary forces of droplets of liquid to align a die to a target site on a wafer. Capillary forces are exerted as the liquid tries to minimize its surface energy by regulating its surface tension. From a macroscopic point of view, the liquid tends to minimize its interfacial contact area with the surrounding air

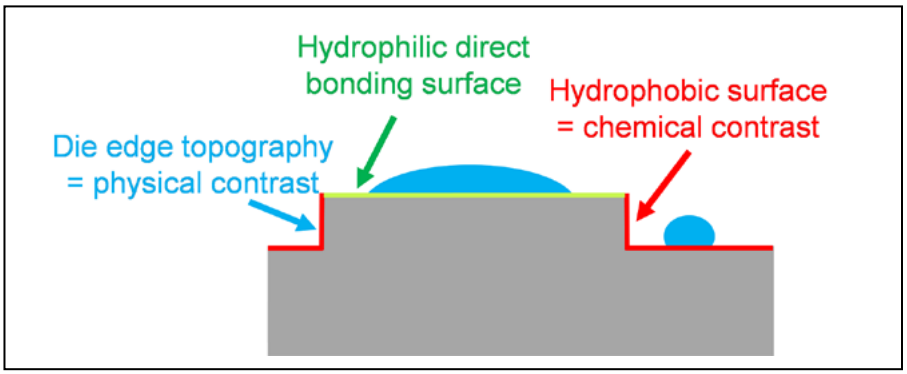

Figure 1: Water containment with both topographic and chemical contrast.

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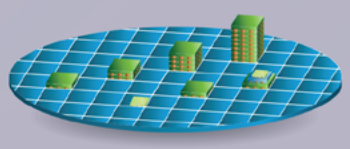

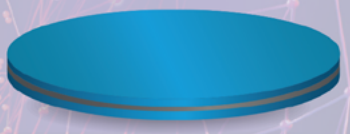

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to reach an equilibrium state with the lowest surface energy. This mechanism results in self alignment of the die with its bonding site. Water was chosen as the working medium because of its high surface tension, which produces strong capillary forces that can be harnessed to drive self alignment. Moreover, water is environmentally friendly and its evaporation is easily controlled in a monitored environment. Finally, water has the additional advantage of being compatible with direct bonding and is already used in hydrophilic bonding mechanisms.

To ensure self alignment, good containment of water on the bonding site is critical (**Figure 1**). The aim of this containment is to prevent liquid overflow outside the bonding area, which would cause misalignment. Containment can be achieved through physical means and/or chemical surface contrast. Physical contrast is achieved by creating a border around the bonding site, whereas chemical contrast is obtained by depositing a hydrophobic material around the periphery of the hydrophilic bonding area. Water containment is maximized by combining both chemical and physical contrasts, resulting in the best possible self-alignment outcome (**Figures 2** and **3**). The extent of alignment is linked to the accuracy of the step and by the definition of the hydrophilic/hydrophobic boundary. Therefore, if the boundary is created by lithographic means, the final alignment will depend on the capabilities of the lithographic process

After self alignment, the water evaporates and direct bonding occurs due to the spontaneous adhesion of the specially-prepared die and wafer surfaces, without requiring any intermediate layer. For good bonding quality, both the die and wafer must meet strict bow, nanotopography and surface roughness requirements. Any organic or particulate contamination of the bonding surfaces may impede bonding. Those parameters, therefore, must be critically controlled to ensure good quality bonding.

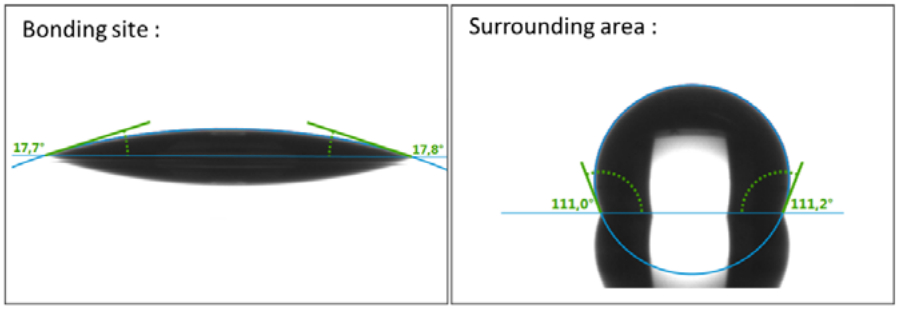

Figure 2: Water contact angle of hydrophilic bonding site and hydrophobic surrounding area.

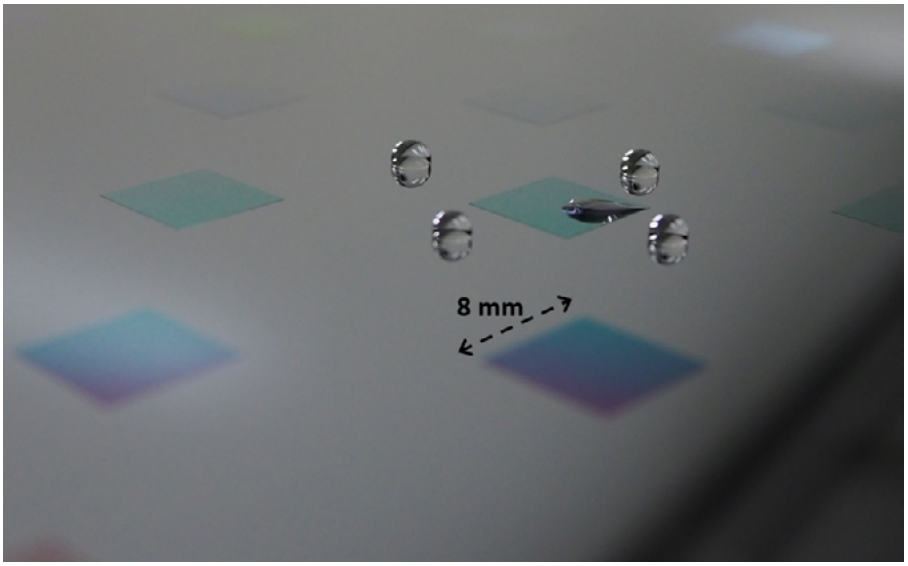

Figure 3: Hydrophilic bonding pad surrounded by hydrophobic area for water containment.

	Die handling	Die alignment	Die assembly	Throughput
Direct placement P&P	Robotics	Optics and robotics	Robotics	→ Low
Self-assembly	High speed robotics	Physics of capillary forces		→ High

Table 1: Impact of self-assembly on the die to wafer process.

Collective vs. direct-placement P&P

Today, direct-placement D2W relies on robotics and optics for the die handling, alignment and bonding steps. A major advantage of our self-assembly process is that it avoids the need for mechanical movements during the alignment and bonding steps by exploiting the physical phenomenon of surface tension, provided by the water droplet, to induce self alignment and bonding with the wafer (**Table 1**). Precise alignment is, therefore, achieved at a high-throughput rate. The handling step can, therefore, be faster because it requires lower accuracy (<200µm) compared to direct-placement P&P. Consequently, the estimated throughput for the overall process should reach more than 2,000 dies per hour.

Another possibility consists in using the direct-placement D2W process for collective assembly (**Figure 4**). All dies, therefore, can be positioned on a holder or a tape with low placement accuracy and at high speed. Then, the dies can be prepared as a group and placed roughly opposite their bonding sites. A technique is then necessary to release the dies onto the water droplets. The water droplet completes the fine alignment of the dies to less than 400nm 3σ. This collective approach to assembly could drastically increase throughput.

A short history of self-assembly development

Self-assembly processes have been investigated by many groups in centers all over the world, such as: Tohoku

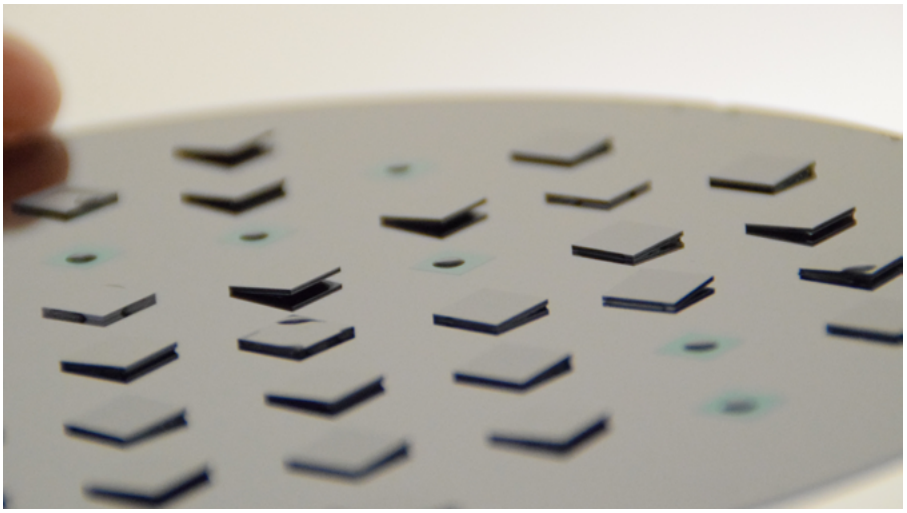

Figure 4: Self-assembly bonding of dies with a water droplet for collective or direct placement D2W bonding.

University [1], Aalto University [2], and imec [3]. Among them, they explored the very good alignment capability for dies with different shapes and sizes (millimeter to micron scales). However, integration with Cu has not been extensively studied for hybrid bonding applications. Moreover, all of the reported results remain at the academic, proof-of-concept, level.

At CEA-Leti, initial investigations into this process were performed as part of two PhD studies in 2010 and 2015 [4-5]. The main results were the demonstration of the alignment capability through experiments and modeling, and the first successful integration of Cu with a positive electrical readout. The studies undertaken indicated that the process could be viable as a proof-of-concept. The method was subsequently matured through continuous developments with homemade tools, which were published at IEEE ECTC 2019 [6].

In 2020, CEA-Leti and Intel Components Research launched a collaboration to evaluate the potential of this technology from an industrial perspective. The objectives were to understand the key parameters controlling self alignment and the physics behind the process, but also to compare the potential of this technology to that of direct-placement P&P. To ensure good reproducibility of experiments and go a step further toward industrialization, collaborations with tool suppliers were engaged to embed water dispensing on an industrial die bonder.

Improved alignment and higher throughput

The first outcome of our collaboration was the discussion on the key process parameters driving self alignment, as presented at IEEE ECTC in 2022 [7]. The water-dispensing technique and the surface preparation to tune the surface's hydrophilicity emerged as critical for the behavior of the self-assembly process. After correctly managing the surface energies of both the hydrophilic and hydrophobic areas, excellent alignment performances were achieved on a homemade collective self-assembly bonding bench. The degree of hydrophilicity of the bonding site receiving the droplet was found to play a major role in self-assembly mechanisms. Therefore, it emerged that a weakly hydrophilic surface with a water contact angle (WCA) >60° optimizes the collection and alignment of the dies. With 8x8mm² dies meeting this condition, excellent alignment yield with the mean alignment of x = 46nm and y = 132nm; 3σx = 439nm and 3σy = 341nm, along with a high throughput were obtained.

In comparison, currently available die bonder P&P tools have achieved 1µm 3σ, and the next generation of die bonder should reach 500nm 3σ. In addition to its very good alignment capability, the self-assembly process was demonstrated to behave like a "collective" process. After dicing, all dies were placed in a silicon holder for collective handling during cleaning and surface preparation before direct, simultaneous bonding of dies to the target by self assembly. It is interesting to note that the error in placement of the die on the silicon holder was quantified at around +/-200µm, resulting in a final misalignment of 500nm 3σ. Based on these data, the self-assembly technique has a real potential to improve D2W processes in terms of both throughput and alignment. Moreover, the self-assembly process was demonstrated to be compatible with a wide range of die dimensions, since at least 70% of assemblies were completed below 500nm 3σ for the different die sizes tested (8x8mm², 2.7x2.7mm², 1.3x11.8mm² and 2.2x11.8mm²) (**Figure 5**).

Figure 5: Self-assembly process applied to high aspect ratio dies.

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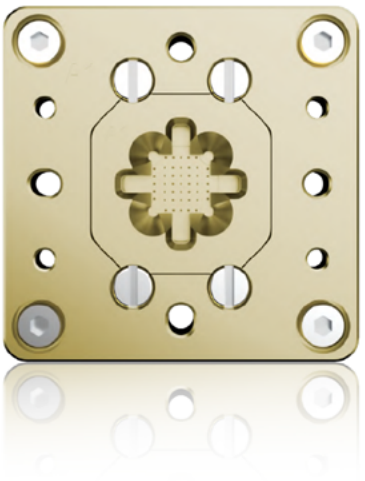

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Self-assembly process and integration challenges

A second paper was presented at IEEE ECTC 2023 [8] that described the latest progress on bonding defectivity, the role of step height and the challenges of Cu integration.

First, bonding quality directly impacts the electrical yield and mechanical stability of the D2W assembly and can be affected by several factors. Surface particles can create bonding defects, whereas organic residuals lead to outgassing during thermal annealing. Pristine surfaces are therefore required before bonding. After reviewing several organic defects, die preparation was carefully optimized to ensure a high quality bonding interface with intact self-alignment capabilities, which means maintaining a good surface-energy contrast between the hydrophilic bonding area and the surrounding hydrophobic material. The results obtained are very good from the perspective of yield.

Second, step height plays an important role in the self-assembly process. Step creation is necessary for water containment, with taller steps correlated with better containment. In our previous work, the step height was set at 15µm, which produced sufficient containment, but may be too tall for full integration. Indeed, after self assembly, other processes such as the creation of through-silicon vias (TSVs) or other routing or bonding layers, may be needed. Those processes are easier to integrate when die and wafer surfaces have shallower steps. To optimize compatibility with these future applications, we experimented to determine the minimum step height compatible with successful self assembly. Investigation of a range of step heights from 10µm to 0µm revealed that step heights of 1µm or less are suitable for use with the self-assembly technique. This smaller step size should facilitate the integration of any subsequent process steps required to obtain the final product. The results confirmed the need for both chemically-induced WCA contrast and a physical step to contain the water droplet and ensure accurate self alignment.

Because self assembly involves hybrid bonding, it is essential to investigate the compatibility of this process with Cu. The following two aspects were studied: 1) the impact of the process steps photolithography, etching and stripping, on the integrity of the Cu, and 2) how water affects the Cu. Among our major findings, we demonstrated a proof-of-concept integration of Cu pad fabrication using the self-assembly process. Some nanotopography degradation was observed on the Cu surface because of the stripping chemistry, but no significant oxidation due to contact with water was visible. These results are encouraging, paving the way toward the commercialization of self assembly in high-volume manufacturing applications. We will now focus on improving the Cu nanotopography and the electrical characterization of the process.

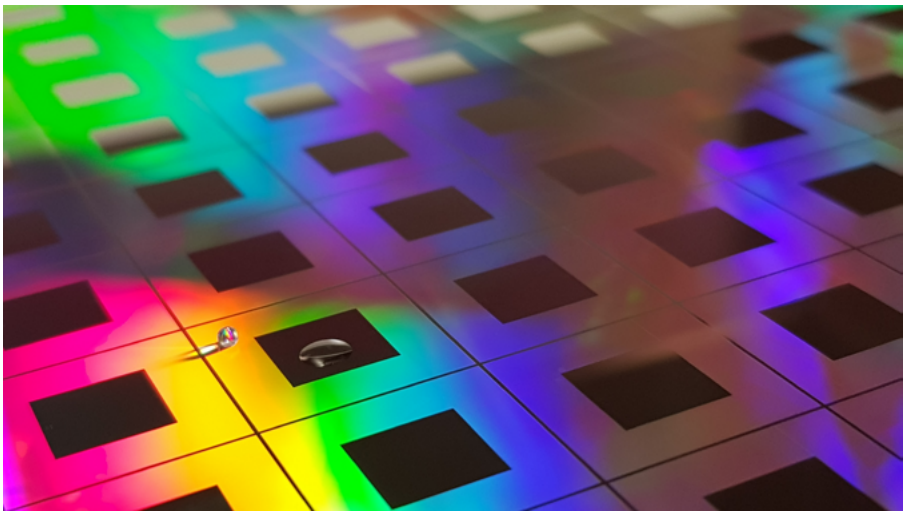

Figure 6: Super-hydrophobic surface integrated with a hydrophilic area.

Hydrophobic and super-hydrophobic surface fabrication

As part of investigations into self-assembly processes, some academic groups have reported on the use of superhydrophobic surfaces. Superhydrophobicity is defined as a WCA exceeding 120°C. At CEA-Leti, we are also investigating these types of surfaces and their integration to assess how they affect alignment capability. We have integrated a superhydrophobic area, with a water contact angle of 150°C, next to a hydrophilic surface (WCA <15°C). Tests will now be performed on the alignment capability of this area (**Figure 6**).

Another topic linked to hydrophobic surfaces is the use of organofluorinated hydrocarbon compounds. This year, the European Chemical Agency is debating the restriction of such fluorinated compounds, which are persistent substances that accumulate in the environment and in the human body. Those materials are very widely used in industry for their hydrophobic properties. CEA-Leti and Intel Components Research have worked on the integration of an alternative F-free material to comply with future Registration, Evaluation, Authorisation and Restriction of Chemicals (REACH) restrictions [9].

Summary

The capillary force of a water droplet can be exploited to quickly align dies and produce self assembly. It could be a good option to increase both throughput and alignment capabilities compared to direct placement D2W. In-depth work to integrate this process has been undertaken jointly by CEA-Leti and Intel Components Research, with results so far revealing good compatibility with the fabrication of microelectronics assemblies. The next steps for the development of this technology are electrical validation of the assemblies, and the development of an industrial assembly tool. To continue the exploration of the fabrication of hydrophobic areas, CEA-Leti is investigating the integration of superhydrophobic surfaces and fluorine-free materials to preempt future chemical restrictions.

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Biographies

Emilie Bourjot is a Project Manager at CEA-Leti, Grenoble, France. Her current activities involve developing advanced hybrid bonding schemes for 3D integration. Prior to joining CEA-Leti, she worked with GlobalFoundries (Germany, USA) and within the IBM Alliance (USA) on the development of advanced FDSOI technologies and sub-3nm nodes. She holds a Masters in Materials Physics from INSA Lyon, France, and a PhD from Aix-Marseille U., France. Email emilie.bourjot@cea.fr

Frank Fournel is the head of wafer bonding technology engineering at CEA-Leti, Grenoble, France. He is also a board member of the international ECS Wafer Bonding Symposium conference, the International Wafer Bond conference, and the Low Temperature Bonding 3D conference. He has more than 180 international publications, 120 deposited patents. He graduated from the "Ecole Supérieure de Physique et de Chimie Industrielle" de la ville de Paris (ESPCI) with a masters in Materials Science, and received his PhD in 2001.

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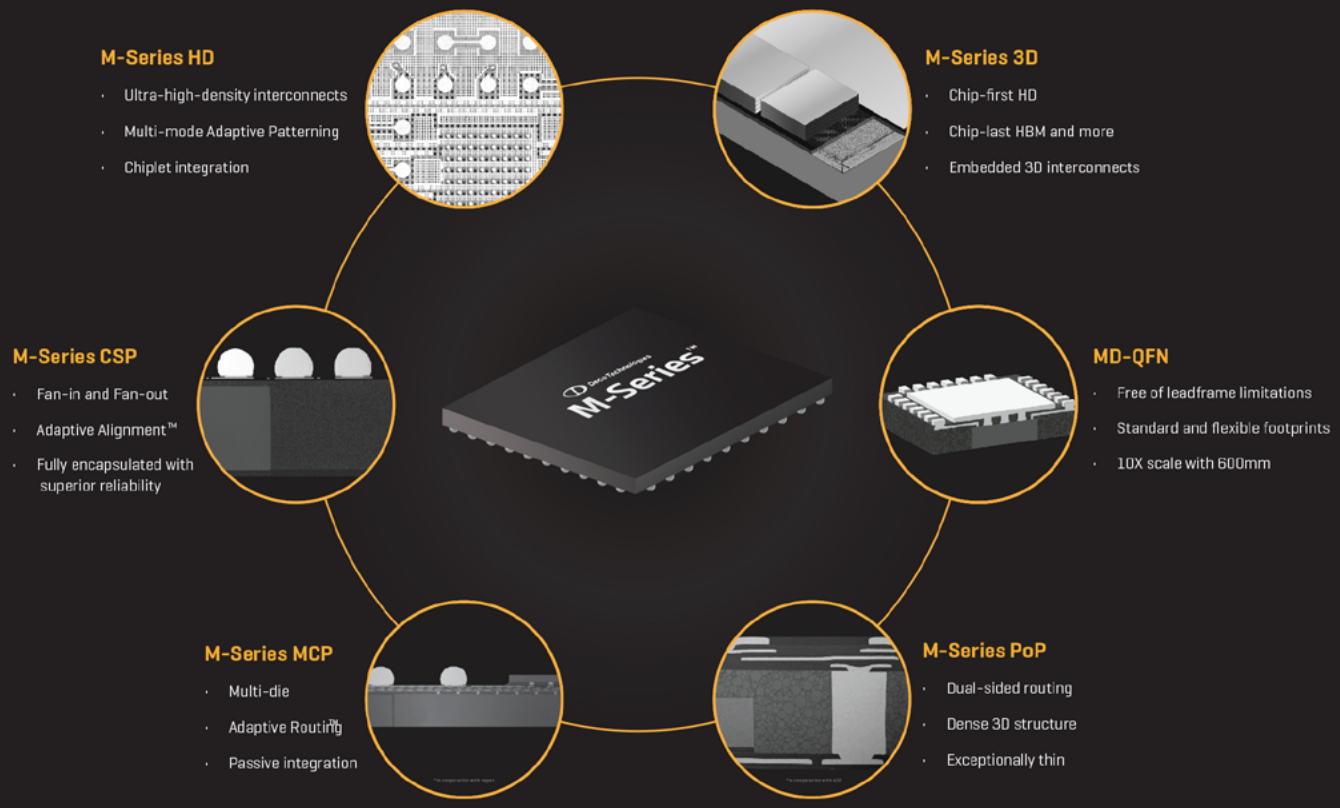

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INTERNATIONAL DIRECTORY OF BONDING EQUIPMENT FOR 2.5D AND 3D ASSEMBLY

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COMPANY HEADQUARTERS Street Address City, State, Zip Country Telephone Fax Website	BONDING TOOLS	WHAT ELSE THEY MAKE
Finetech GmbH & Co. KG Boxberger Str. 14 12681 Berlin Germany Tel: +49 30 936681-0 www.finetech.de	Die Bonders Flip Chip Bonders Manual Bonders/Semi-automated Bonders Fully-automated Bonders	Thermo-compression Bonders Thermo-sonic Bonders Opto-Bonders, Eutectic die Bonders Epoxy die Bonders Rework Systems
Hanmi Semiconductor Co. Ltd. 14, Gawja-ro 30 beon-gil Incheon, South Korea Tel: +82 32 571 9100 www.hanmisemi.com	Die Bonders Flip Chip Bonders	Sawing & Placement, Punch Singulation, Compression Auto Molding, Cam Press Trimming, Laser Marking, 3D Vision Inspection, Pick & Place and Coverlay Attach/Detach, Glass Attach
Hybond Inc. 330 State Place Escondido, CA 92029 USA Tel: +1-760-746-7105 www.hybond.com	Eutectic Die Bonder Epoxy Die Bonder Epoxy/Silver Glass Die Bonder	Wire Bonders Wedge/ Peg and Bar Lead Bonders Diode Bonders Wire Bonder Test System
Kulicke & Soffa Pte Ltd K&S Corporate Headquarters 23A Serangoon North Ave 5 #01-01 Singapore 554369 Tel: +65-6880-9600 www.kns.com	Flip Chip Bonders Thermo Compression Bonders Wafer Level Bonders	Ball Bonders Wedge Bonders Manual Wire Bonders Bonding Tools Wedge Bond Consumables Dicing Blades, Micro/Mini LED
MicroAssembly Technologies, Ltd. Beit Rimon, Ofer Industrial Park Yokneam Illit 2069200 Israel Tel: +(972) 4 959-2225 www.mat-ltd.com	Die Bonders Multi Module Attach Bonders Flip ChipDie Bonders Eutectic Die Bonders	Dispensing & Stamping System (adhesives, flux, other materials)
MRSI Systems 554 Clark Road Tewksbury, MA 01876 USA Tel: +1-978-667-9449 www.mrsisystems.com	Eutectic Die Bonders Epoxy Die bonders Dispensing Bonders (Including UV) Flip Chip Bonders (TCB)	Epoxy Dispensers
Orion System Integration Pte Ltd 2 Woodlands Spectrum #03-10 Woodlands Sector 1 Singapore 738068 Tel: +65.6507.0353 www.orionsi.com	Flip Chip Bonders	
Palomar Technologies, Inc. 6305 El Camino Real Carlsbad, CA 92009 USA Tel: +1-760-931-3600 www.palomartechnologies.com	Die Bonders Epoxy Die Bonders Eutectic Die Bonders Flip Chip Bonders	Fine Wire Bonders Wedge Bonders Ball Bonders Stud bumpers Contract Manufacturing SST Vacuum Reflow Systems (Manual and Automated)
Panasonic Corporation of North America Process Automation 1701 Golf Road, Suite 3-1200 Rolling Meadows, IL 60008 USA Tel: +1.847.637.9600 www.na.panasonic.com/us/factory-equipment-solutions/electronics-assembly-manufacturing-technologies/microelectronics	Die Bonders Flip Chip Bonders	Plasma Cleaner, Plasma Dicer, Profilometers

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COMPANY HEADQUARTERS Street Address City, State, Zip Country Telephone Fax Website	BONDING TOOLS	WHAT ELSE THEY MAKE
Protec Co. Ltd Pnuematic Business Group 11-14 Simin-daero 327beon-gil Dongan-gu, Anyang-si Gyeonggi-do South Korea Tel: +82-32-822-9183 www.protec21.co.kr/eng	Eutectic Die Bonder Epoxy Die Bonder Hybrid Die Bonder	Flip Chip Attach Lid Attach System
Semiconductor Equipment Corp. 5154 Goldman Avenue Moorpark, CA 93021 USA Tel: +1-805-529-2293 www.semicorp.com	Flip Chip Bonder	Pick & Place Systems, Cleaning Systems for: FOUPS, SMIF Pods, Cassettes, FOSBS & EUV Pods
SET Corporation SA Smart Equipment Technology 131, Impasse Barteudet 74490 Saint Jeoire France Tel: +33 (0) 450 35 83 92 www.set-sas.fr/en	Flip Chip Bonders	Lid Attach System Large Device Bonders Non-imprint Nanoimprint Lithography
Shibaura Mechatronics Corporation 2-5-1, Kasama, Sakae-ku, Yokohama, Kanagawa Pref. 247-8610 Japan Tel: +81-45-897-2421 www.shibaura.co.jp/e	Die Bonders Flip Chip Bonders	FEOL products (etching, stripping, coating, jetting) and BEOL
Shibuya Corporation Ko-58 Mameda-Honmachi, Kanazawa, Ishikawa 920-8681 Japan Tel: +81 (76) 262-2201 www.shibuya.co.jp	High Precision Thermo Compression Flip Chip Bonders Semi-auto Thermo Compression Flip Chip Bonders	Micro Solder Ball Mount LED Bonding Photonics Bonding Film Application Chip-on-Glass
Shinkawa Ltd. 2-51-1 Inadaira, Musashimurayama-shi Tokyo 208-8585 Japan Tel: +81-42-560-1231 www.yamaha-robotics.com/en/products/ manufacturer/?maker=SHINKAWA LTD.	Die Bonders Flip Chip Bonders Thermo Compression Bonders (C2S and C2W)	Bump Bonders Wire Bonders
SUSS MicroTec SE Schleißheimer Straße 90 85748 Garching Germany Tel: +49 89 32007 0 www.suss.com	Permanent Wafer Bonders Temporary Wafer Bonders Debonders	Mask Aligner Coater/Developer Inkjet Printer Nanoimprint Equipment, Photomask Cleaning Equipment
Tresky GmbH Neuendorfstrasse 19 B 16761 Hennigsdorf Germany Tel: +49 (0)3302 866 92-0 www.tresky.de	Die Bonders Flip Chip Bonders	Dispensing Attachments, Heating Plates Handlers

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TFE

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Thermal

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Change Kit

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+82-70-7093-8028

Efficiency and cost implications of multi-die heterogeneous integration

By Glenn Farris [Universal Instruments]

The semiconductor industry is actively working towards achieving widespread integration of diverse semiconductor die types through a technique known as heterogeneous integration (HI). These die can originate from various wafer sizes and are produced using different technological processes. This emerging packaging method presents fresh challenges related to the efficiency of assembly and the overall yield.

Historically, the process of flip-chip assembly has employed a single tool to position a singular die type onto the intended substrate. In cases involving multiple die types, manufacturing lines have been configured with a sequence of placement tools, each designated for a specific die type. This article delves into the implications of such an approach in the context of the HI era. The effects on product yield, production speed, manufacturing efficiency, and the comprehensive cost of assembly are investigated across a wide array of HI die setups.

An innovative strategy is proposed for optimizing the comprehensive economic aspects of the assembly. This strategy is based on a sensitivity analysis encompassing the expected range of die types applicable in these scenarios. The viability of this new approach is examined for various packaging solutions, including flip-chip, 2.5D, 3D, and fan-out technologies.

Introduction

While transistor scaling continues, the economic improvements derived from this scaling, typically referred to as Moore's Law, have been diminishing. For example, over the past decade, at nodes below 22nm, the associated costs to design and introduce new products have increased by a factor of 7.75. (**Figure 1**) [1]. The prevailing packaging solution to address this challenge is called heterogeneous integration (HI). Many studies have focused on a chip-to-chip signaling, power distribution, materials, thermals, bonding metallurgy, and design methodologies. Interface open standards such as UCI Express (UCIe™) [2] attempt to establish a common specification for HI implementation.

The economic implications for various placement tool process flows have not been assessed. Placement tool costs can be subdivided into five major categories: yield, equipment depreciation, operators, floor space, and equipment utilization.

The pick-and-place assembly of multiple disparate die in a HI package traditionally uses multiple placement tools. Each unique tool is dedicated to placing a specific die type and/or wafer type. A new approach is to execute the complete placement of all die types for a given heterogeneously-integrated package within a single tool. A sensitivity analysis for a broad range of die configurations can be assessed by modeling the impact on the five major cost categories for multiple dedicated placement tools versus a single-tool solution.

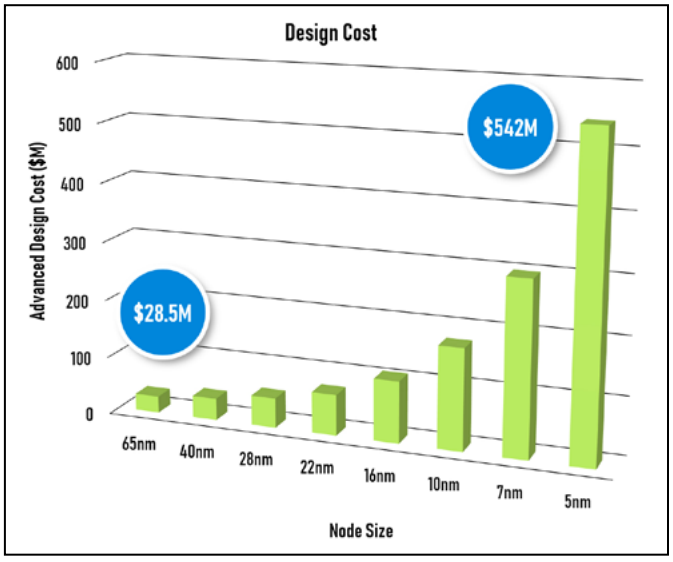

Figure 1: Design cost by node.

HI circuit characteristics

The following sections discuss various HI circuit characteristics.

Device types and quantity per substrate. The number of devices per HI circuit ranges from a minimum of two device types and may be as high as 8 unique devices. These die typically range in size from 0.5 x 0.5mm up to 20 x 20mm. The quantity of each die per substrate can range from one to as many as 8. Each die has a specific function, ranging from processor to memory, to sensing, to data transmission. A typical configuration with four die types and a maximum of 8 die for one die type is shown in **Figure 2**.

Substrate size and quantity. Substrates upon which devices are mounted can range from traditional singulated high-density interconnect (HDI) organic, to singulated silicon interposers, to a substrate-less wafer or panel fan-out. In the case of singulated organic substrates, these are typically presented to the pick and place assembly tool via a JEDEC standard tray (or Gen2 JEDEC tray in the future). At substrate dimensions up to 31 x 44mm, up to 28 circuit substrates can be loaded in one JEDEC tray (**Figure 3**). Future Gen2 JEDEC trays can hold up to 56 of these sized circuit substrates.

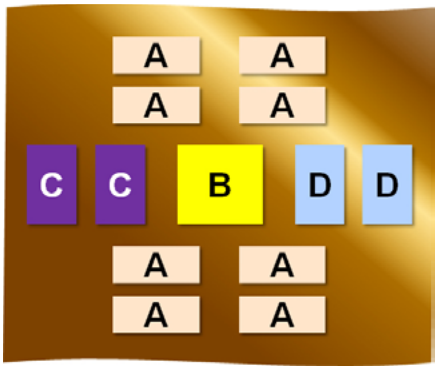

Figure 2: Typical HI device configuration.

A substrate-less wafer-level fan-out carrier offers an assembly area for approximately 38 of this sized circuit. In contrast, a JEDEC standard panel fan-out carrier with a 600mm x 600mm assembly area supports up to 247 of this sized circuit. The number of circuits per carrier significantly impacts the throughput of a single-cell placement solution because wafer exchange time is amortized over a much larger number of placements for a specific die type (**Table 1**).

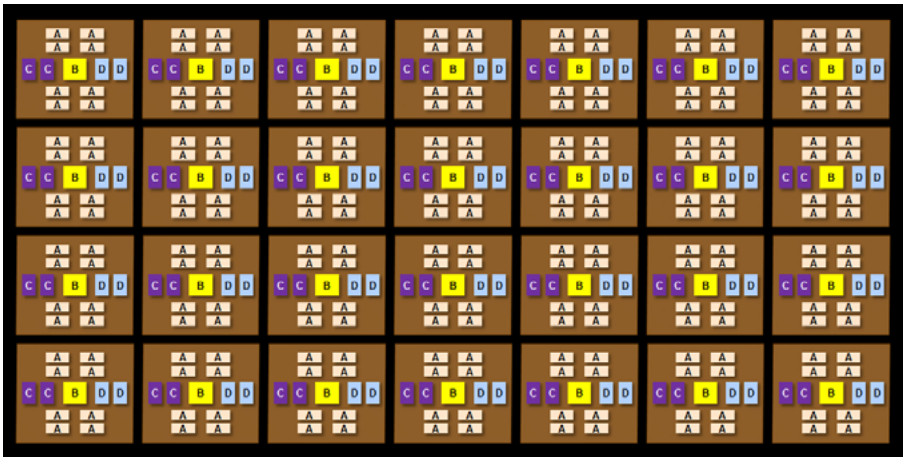

Figure 3: JEDEC tray with 28 substrates.

Carrier Type	Circuits per Carrier
JEDEC Tray	28
Wafer Level Fan-Out Carrier	38
Gen2 JEDEC Tray (future)	56
Semi-Standard Panel	247

Table 1: 31mm x 44mm circuit capacity by carrier type.

Pick-and-place tool characteristics

Traditional die pick-and-place line solutions have been optimized based on the premise that a single die will be placed on a single substrate. This is the typical flip-chip application, which is the dominant advanced packaging application in the market today.

In the case of HI devices, the solution has been to configure multiple systems in series with each other. Each system is tooled and dedicated to a specific wafer type and die type. There are several challenges with this approach. The first challenge is that the line is unbalanced because some systems may be placing 8 or more devices, while some could be placing only one die (or even zero devices if there are more systems than die types to be placed). This results in an overall "effective throughput" per system that is as low as 13% of a single-system solution. Constant rearranging of the line would be required to optimize the assembly flow for different HI circuit configurations, which is impractical in a production environment (**Figure 4**).

The second challenge is that the constant flattening and then flexing of the substrate can cause die float, as can movement out of and into

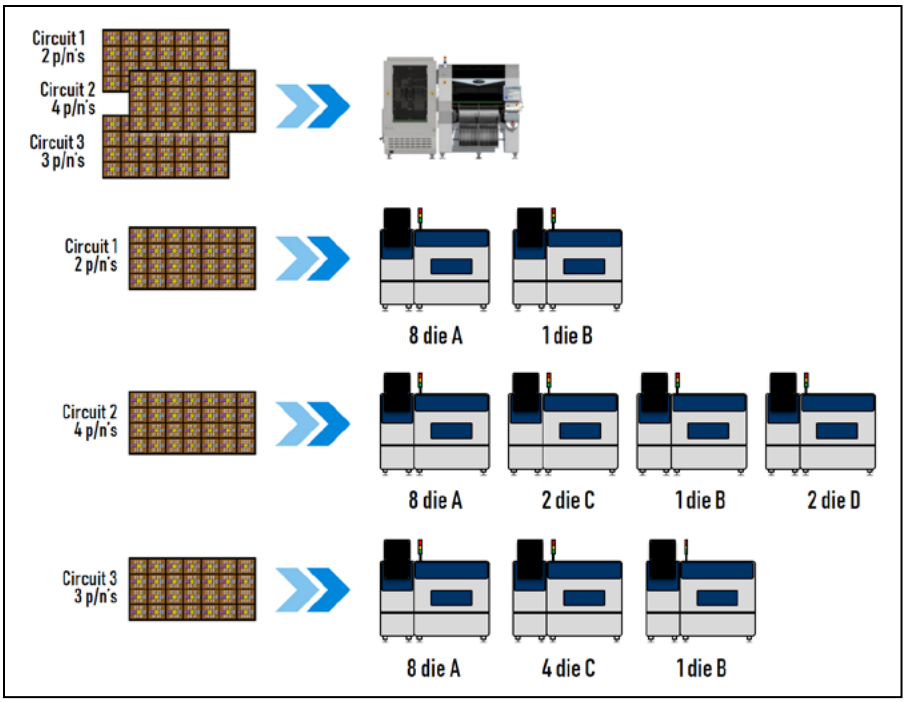

Figure 4: Single system vs. a multiple dedicated system line.

multiple systems, impacting placement accuracy. Finally, moving substrates between 8 dedicated systems in a line increases placement, fiducial find, and potentially, temperature variability, further degrading placement accuracy. Based on typical system variability data, it is estimated that all these factors will increase the defective placement ppm per device from a typical value of 100ppm to 400ppm for a 4-die HI device.

The third challenge is that increased operator attention will be required per line with up to 8 machines in a line, as will increased floor space. This will increase the overall operational expense (OPEX) cost for the line proportional to the number of systems in the line.

The fourth challenge is utilization. Creating a dedicated lines per circuit configuration versus a single cell that can handle any circuit will reduce typical utilization. In addition, material scheduling and downtime typically reduce a single-system solution to 85% utilization. With a 4-system solution, these multi-system factors are expected to reduce utilization further to, at best, 60%.

Throughput sensitivity analysis

To better understand the overall impact of the parameters noted above on HI assembly economics, a mathematical model was created to allow for a comprehensive sensitivity analysis. As mentioned, the most critical factors are the time it takes to automatically change wafers and change associated end effector tooling to support a new die type, the number of circuits to be assembled per carrier, and the number of unique die types to be assembled per circuit.

The sections below discuss the impacts that a number of parameters have on HI assembly economics.

Impact of circuits per carrier and wafer and tooling change time. Table 2 summarizes the relative throughput of assembled circuits for a single system per circuit solution vs. a single die per system solution. The comparison is made for a single-system solution configured with a single-wafer table and a single-system solution configured with dual-wafer tables. The time to exchange unique wafers and end effector tooling for unique die types was varied from 15 seconds to 60 seconds. For this example, it was assumed the circuit had four unique die types, with the quantity of die per die type of 8, 4, 2, and 1, respectively.

Table 2 shows that over the full range of scenarios for circuits per carrier and wafer + tooling exchange time, a single system per circuit solution delivers superior throughput. This advantage ranges from 12% in the corner case of only 4 circuits per carrier and 60-second wafer + tooling exchange time on a single-wafer table system up to a 93% advantage when there are 1,024 circuits on a carrier and an exchange time of only 15 seconds.

Impact of the number of die types and counts per circuit. The impact of the number of unique die types per circuit and the quantity of each die type on the relative throughput of each solution type was also analyzed. This analysis was done for a fixed number of 28 circuits per carrier and a 30-second wafer + tooling exchange time.

As shown in Table 2, a dual-table system, on average, doubles the relative throughput of a single cell per circuit solution. Generally, the placement speed doubles, and the time spent exchanging wafers + tooling is cut in half, resulting in this improvement. The single- and dual-table single system per circuit solutions exhibit a 60% to 90% improvement in throughput in this example. Secondly, the overall variation from 2 to 4 to 8 unique device types has much less impact than the number of circuits per carrier noted in Table 1. Finally, the relative quantity of each unique die type has a more significant impact than the number of unique die types, mainly due to a greater impact on the total number of dies on the circuit (Figure 5).

Economic model summary

An economic model was created to assess the economic impacts of yield, depreciation per circuit, OPEX, and utilization. Pricing for a single-wafer table single system per circuit solution was arbitrarily set to $1mil. The price per machine for the single dedicated system per die type solution was set at $500k. A key observation from the economic model is that, while depreciation cost per assembled circuit is the typical factor used for solution comparison, the assembly yield has a much more significant impact on the overall manufacturing cost (Table 3).

For the single-bay single system per circuit solution, the depreciation cost is only 30.7% of the total assembly cost. Two other factors heavily influence total assembly cost: total scrap per unit produced and operator cost. Operator cost is assumed to be directly proportional to the number of systems. Based on an estimated increase in defective placements from 100ppm to 400ppm for

Circuits per Carrier	Wafer Exchange Time, Single Wafer Table System (sec)									
	15	20	25	30	35	40	45	50	55	60
4	31%	37%	43%	49%	56%	61%	68%	74%	81%	88%
8	22%	25%	28%	31%	35%	38%	41%	44%	47%	51%
16	17%	19%	21%	22%	24%	25%	27%	29%	30%	32%
32	15%	16%	17%	17%	18%	19%	20%	21%	22%	22%
64	14%	15%	15%	15%	15%	16%	16%	17%	17%	17%
128	14%	14%	14%	14%	14%	15%	15%	15%	15%	15%
256	14%	14%	14%	14%	14%	14%	14%	14%	14%	14%
512	13%	13%	14%	14%	14%	14%	14%	14%	14%	14%
1024	13%	13%	13%	13%	13%	13%	13%	14%	14%	14%

Relative Throughput per Circuit: Single System Solution compared to System per Die Type Solution

Circuits per Carrier	Wafer Exchange Time, Dual Wafer Table System (sec)									
	15	20	25	30	35	40	45	50	55	60
4	16%	19%	22%	25%	28%	31%	34%	37%	41%	43%
8	11%	13%	15%	16%	18%	19%	21%	22%	24%	26%
16	9%	10%	11%	11%	12%	13%	14%	15%	16%	16%
32	8%	8%	9%	9%	10%	10%	10%	11%	11%	12%
64	8%	8%	8%	8%	8%	8%	9%	9%	9%	9%
128	8%	8%	8%	8%	8%	8%	8%	8%	8%	8%
256	7%	8%	8%	8%	8%	8%	8%	8%	8%	8%
512	7%	7%	7%	7%	7%	7%	8%	8%	8%	8%
1024	7%	7%	7%	7%	7%	7%	7%	7%	7%	7%

Relative throughput per Circuit: Single System Solution compared to System per Die Type Solution

Table 2: Relative throughput as a function of circuits per carrier and wafer exchange time. (See also **Figure 6**.)

	Single Cell Single Bay	Multi Cell Alternative	Comment
"Per Cell" Throughput efficiency	100%	24%	Throughput efficiency of single cell vs multi-cell
Circuits per Year	1273799	1214458	Input number of Assemblies / year
Solution Price	$1,000,000	$2,000,000	Input solution price to meet Assemblies/ year need
Depreciation Years	5	5	Input # of years to depreciate asset Note: a more flexible tool may justify longer depreciation cycle)
Base Depreciation per Unit	$0.157	$0.329	Calculation based on depreciation time interval
COGS of each Assembly	$50.00	$50.00	Input total COGS of all devices being picked and placed + substrate
Throw Rate %	0.13%	0.13%	Input expected device scrap (throw) rate due to mispick
Circuit Yield Loss	0.17%	0.68%	Input expected assembly yield due to misplacements
Total Scrap Cost per Unit produced	$0.150	$0.405	Calculated based on COGS and scrap %
Utilization	85%	60%	Input expected Solution Utilization
Utilization Cost per unit produced	$0.0236	$0.1334	Calculated based on increased depreciation per actual Unit assembled
Operators Required per Shift	1	4	Input # of Operators (1 per system)
Fully Burdened Cost/Oper	$30.00	$30.00	Input Operator Hourly Rate (Fully Burdened)
Operator Cost per Assembly	$0.1413	$0.5929	Calculated based on total operator cost
Floor Space Required	5	20	Input floor area (m2)
Annual Floor Space Cost (Incl power, Insurance, etc)	$10,000	$10,000	Input total cost per area
Factory Cost per Assembly	$0.0393	$0.1647	Calculated based on total floor space cost
Total Cost per Unit	$0.511	$1.625	
Total Cost if Alternative Solution is free	$0.511	$1.296	

Table 3: Economic model for HI assembly. (See also **Figure 7**.)

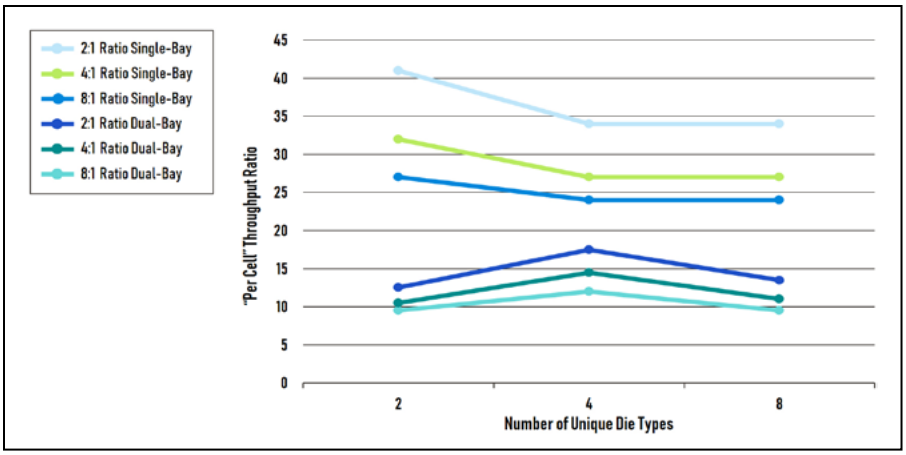

Figure 5: Relative throughput as a function of the number of unique die types and quantity per die type.

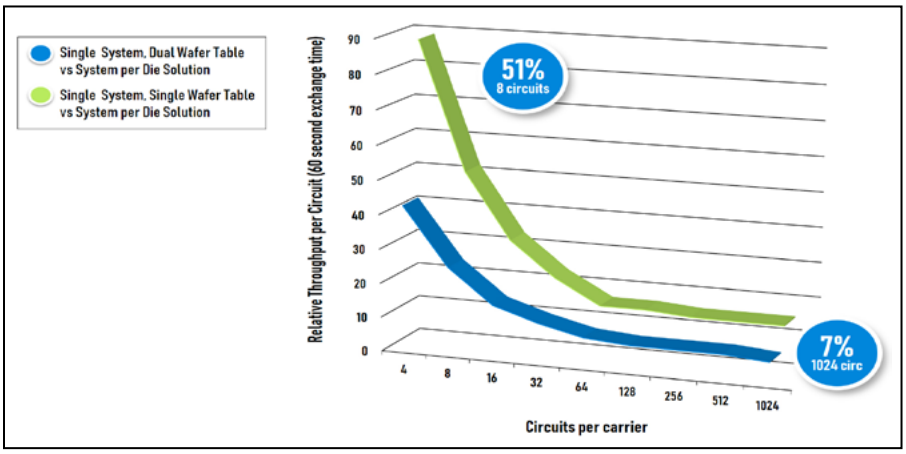

Figure 6: Relative throughput as a function of circuits per carrier and wafer exchange time.

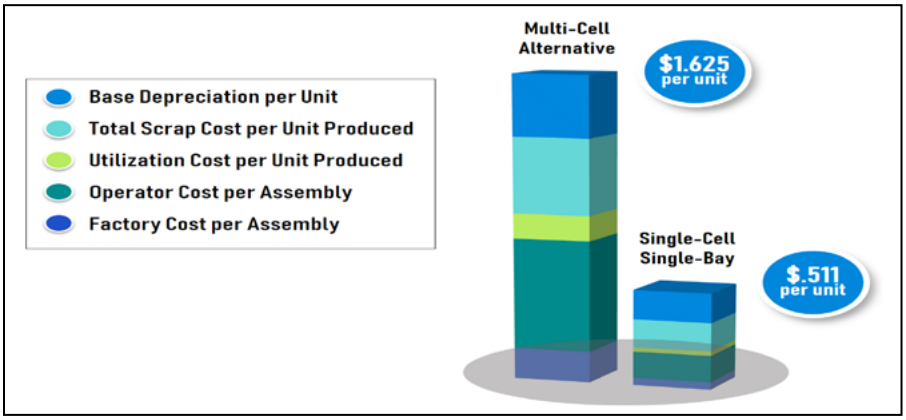

Figure 7: Economic model for HI assembly.

a four-die HI device, the increased scrap cost for the multi-system solution is more than the depreciation cost for the single system per circuit solution. The economic model shows that even if the multi-system solution is free, the increased scrap, operator, and utilization costs result in the single-system solution delivering a 60% lower overall assembly cost.

Summary

In conclusion, with the advent of high-volume HI circuits, efficient advanced packaging assembly solutions are critical to optimizing the overall economics. A comparison of traditional assembly processes, which require a dedicated assembly system per die type, to a novel solution utilizing a single-assembly system for all die, demonstrates a 60% cost of assembly advantage for the single-system solution.

Acknowledgment

The author wishes to acknowledge the solution's inventors and patent holders: Mike Yingling, Sean Adams, David Lyndaker, and Scott Proctor—all employees of Universal Instruments [3].

References

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2. UCIe™ 1.0 Specification is an open industry standard developed to establish a ubiquitous interconnect at the package level; https://www.uciexpress.org/specification
3. "Modular Die Handling System," U.S. Patent No. 11164765 Issue date: 11/2/2021.

Biography

Glenn Farris is VP of Strategic Marketing at Universal Instruments, Conklin, NY. In his 30+ year career in the electronics industry, he has transitioned from being a Research Engineer at NASA to leading marketing organizations for multiple technology companies, including Teradyne and Formfactor. He holds an MBA in Marketing and Finance from Santa Clara U., an MS in Digital Control Engineering from Stanford U., and a BS in Aeronautical Engineering from Purdue U. Email glenn.farris@uic.com.

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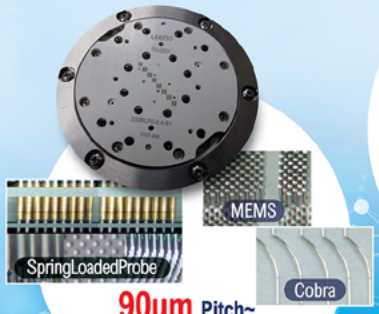
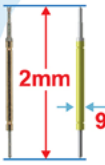
90um Pitch~

Spring Contact Probe



90um Pitch~ Probe Head

Tip Type

Specification
Pitch : Min.120um
Spring Force : 8.0g@ 250um
Current Rating : 1.0A
Inductance : 0.38nH

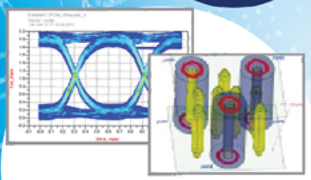
RF Probe for Fine Pitch Probe Head


0.18mm Pitch~
RF Coaxial Spring Probe & Impedance Controlled


Logic Test Socket


High Speed
Frequency : >20GHz
VSWR : < 1.2
Automatic Coaxial Probe


5G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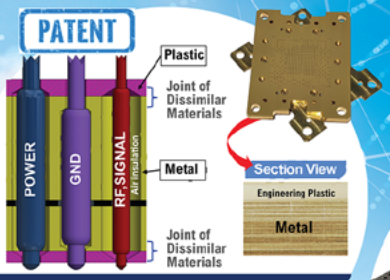
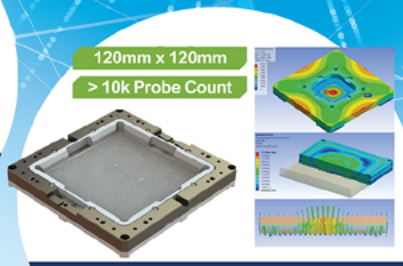
CCC Test, HFSS, TDR
Eye Diagram
4 Port VNA Test



MP Socket



Large Device Socket

Specification
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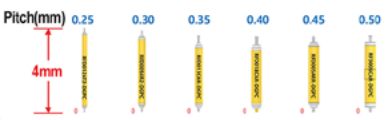
100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%



Coaxial Probe 100GHz

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10 105beon-gil MieumSandan-ro Gangseo-gu, Busan, Korea

CONTACT
USA: hskang@leeno.co.kr / +1 408 313 2964 / +82 10 8737 6561
Korea: sales-leeno@leeno.co.kr / +82 51 792 5639

Mitigating the thermal bottleneck in advanced interconnects

By Zsolt Tőkei, Herman Oprins, Melina Lofrano, Xinyue Chang [imec]

The back-end-of-line (BEOL) is a complex wiring scheme that distributes clock and other signals, provides power and ground, and transfers electrical signals from one transistor to another. It is organized in different metal layers containing local (M_x), intermediate (M_y), and (semi-)global interconnect wires (M_z). The total number of layers can be as many as 15, while the typical number of M_x layers ranges between 3 and 6. Each layer contains unidirectional metal lines, organized in regular tracks and surrounded by intermetal dielectrics. They are interconnected vertically using via structures that are filled with metal.

As dimensional scaling in the front-end-of-line (FEOL) continues, BEOL dimensions are also being reduced – leading to ever smaller metal pitches and reduced cross-sectional areas of the wires. Routing congestion and growing RC delay (resulting from an increased resistance-capacitance product (RC)) have become well-known bottlenecks for further interconnect scaling.

The chip industry, however, has for some time been concerned about another phenomenon: an increase in the BEOL's thermal resistance and, with it, the heating up of the metal lines. This temperature increase can dramatically affect the reliability of the integrated circuits because the reliability degradation of both the BEOL (related to electromigration and stress migration) and the FEOL (related to, e.g., negative bias temperature instability) is accelerated at high temperatures.

The main sources for heating are the active parts in the FEOL, the transistors, which dissipate energy during their operation. Nowadays, logic cells dissipate around 10W/mm^2, and some of the generated heat is dissipated towards the neighboring BEOL [1,2]. On top of that, the currents that run through the interconnects for either power delivery or signal distribution also warm up the conductors, a phenomenon known as Joule heating. This worsens with each technology node due to a scaling-induced rise in the electrical resistivity of the interconnect metal lines and vias. The requirements for ever higher current densities and the poor thermal conductivity of the low-k dielectrics add to the problem.

The need for an accurate predictive framework

Traditionally, thermal analysis of FEOL and BEOL is performed separately using simplified models, and only the impact of the transistor on the first metal layer (M1) is considered. But this approach is becoming too narrow. The concern is fueled by emerging innovations that are expected to go against thermal improvement. Think about the introduction of air gaps as alternative dielectrics to improve RC delay or a further increase in the number of BEOL layers. Also, for 3D technologies, the BEOL might become the dominant contributor to the

overall thermal resistance in advanced packages. The introduction of backside power delivery schemes (moving the entire power distribution network to the chip's backside) and novel transistor architectures (such as gate-all-around nanosheets) in the logic roadmap may impact the temperature of the metal lines as well—in a good or bad sense.

A more comprehensive modeling framework is needed to capture the impact of these innovations on heat propagation and to enhance our fundamental understanding of how heat propagates in narrow BEOL structures. This framework should allow us to identify the biggest contributors to the warming up, predict how the BEOL's thermal resistance evolves with newer technology nodes, and make recommendations for thermal-aware interconnect design.

A multi-step approach using calibrated models

We have taken a modular approach to assess the thermal properties of the BEOL and developed different types of models that capture the thermal properties of the materials at different dimensional scales and levels of detail. Each model can be used by itself, depending on the use case of interest. The output of each of the models can also be used as input for the next, enabling a complete analysis of a full BEOL stack. The modeling work is combined with experimental data obtained on test vehicles with industry-relevant materials and dimensions. The measured data are fed into the models, allowing for accurate calibration and prediction of future scenarios.

An overview of the different (sub-) models

In the first step, the researchers investigate the materials at the atomic level using the density-functional theory (DFT) (**Figure 1a**). With this model, they derive fundamental properties of electrons and phonons, i.e., the heat carriers that move the energy inside the material.

In the next step, the heat conduction within the materials is modeled for varying material dimensions, from µm to nm scale. An in-house developed modeling tool is used that is based on the Boltzmann transport equation (BTE) (**Figure 1b**). The model additionally captures thermal effects at the nanoscale. The material properties of metals and dielectrics, as characterized on dedicated test structures, are used as an input for the model. For the dielectrics, for example, the so-called 3ω method was used to experimentally extract the thermal conductivity of relevant dielectric materials very precisely, revealing a value of 1.15W/mK for SiO_2 and 0.3W/mK for OSG3.0 (an organosilicate glass with 3.0 dielectric constant).

In the third step, the researchers zoom out to a larger part of the BEOL layout. A full BEOL stack's thermal properties are modeled using a 3D finite element modeling (FEM) approach, calibrated with self-heating measurements (**Figure 1c**). This final step gives a thermal conductivity/resistance mapping of the BEOL stack and its individual layers, allowing for a fast evaluation of the temperature rise in the interconnect structure.

To fully estimate how the heat propagates in the BEOL, the model must also accurately account for the heat exchange between the FEOL and BEOL. We have developed a methodology for estimating this heat exchange. This thermal coupling is added as an extra "layer" to the FEM model.

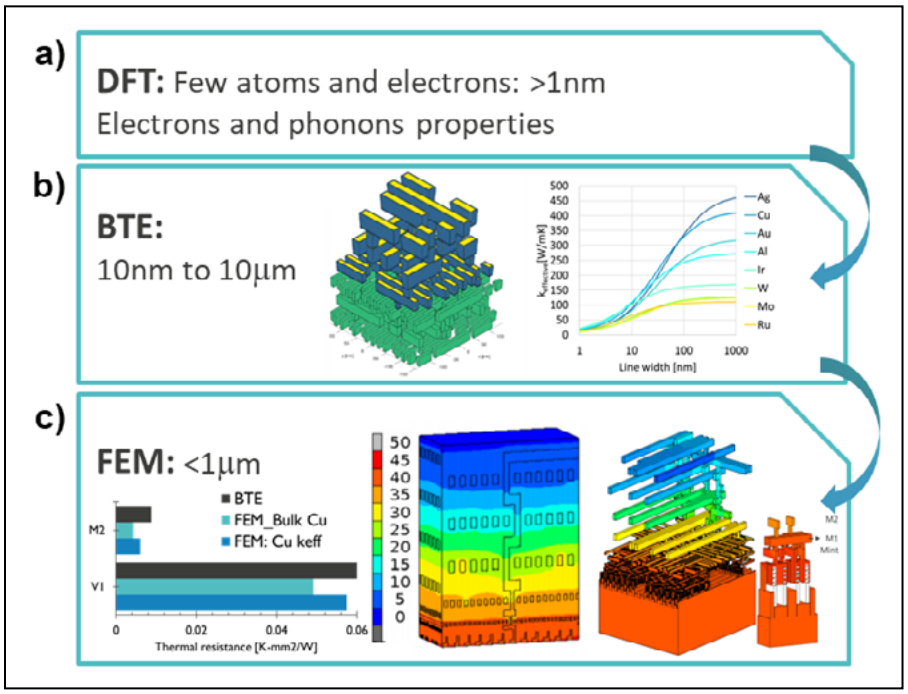

Figure 1: Schematic representation of the proposed hybrid thermal modeling approach: a) (top) Density-functional theory (DFT), b) (middle) Boltzmann transport equation (BTE), and c) (bottom) finite element modeling (FEM) based models capture thermal properties at different dimensional scales.

Applying the models to different use cases: trends and useful insights

The next sections discuss various use cases when applying the models shown in **Figure 1**.

The thermal conductivity of elemental metals drops at <10nm line width. A typical outcome of the BTE modeling work is an evolution of the thermal conductivity of the materials with decreasing line widths. For all evaluated elemental metals, the thermal conductivity significantly drops when line widths scale into the 10nm region, which is relevant for the local level of interconnects at advanced technology nodes. This is illustrated in the graph in **Figure 1b**.

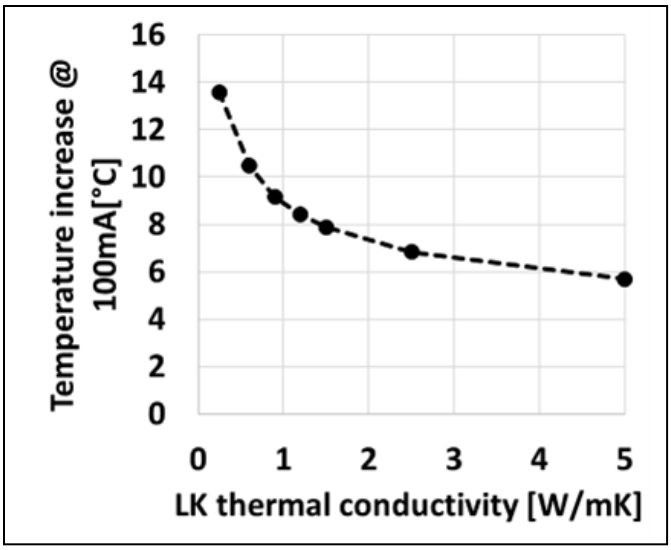

Figure 2: Effect of intermetal dielectric thermal conductivity on the temperature increase of the BEOL structure.

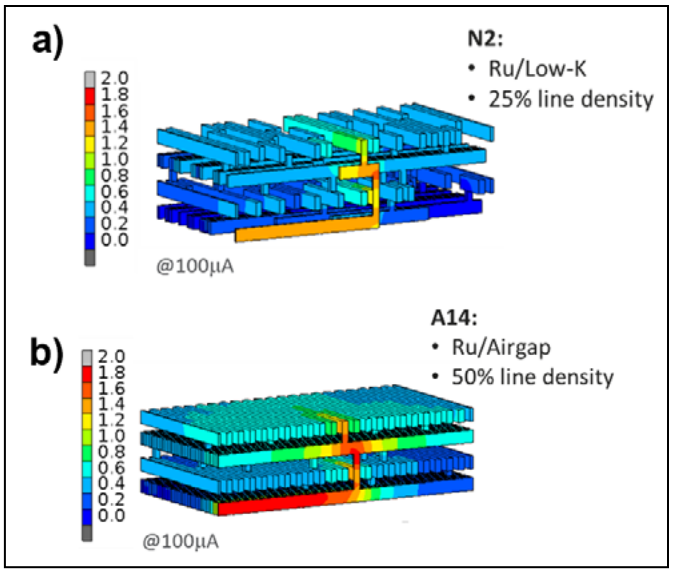

Figure 3: Effect of air gaps on the self-heating of the BEOL structure.

Low-k dielectrics, via layers and the M_y stack, dominate the thermal behavior of a 14-layer BEOL stack. The multi-step modeling framework was used to assess the thermal behavior of a complete, 14-layer BEOL stack in an advanced technology node. The work revealed interesting insights into the way the design and technology options for the BEOL impact the temperature rise.

The contribution of the intermetal dielectric is significant (Figure 2). A fast temperature increase in the BEOL is observed when the thermal conductivity of the intermetal dielectric drops below 1W/mK. This is in the thermal conductivity range of most currently used dielectric materials such as OSG3.0. The impact worsens when air gaps are introduced (e.g., in the A14 technology node) due to the very poor thermal conductivity of the air gap: simulations show an increase of 30 percent for the metal line self-heating (Figure 3). The (choice of the) metal, on the contrary, has a minimal impact on thermal dissipation.

The impact of the via density and configuration cannot be ignored. A larger via density is found to favor thermal dissipation between interconnect layers. The same applies to a stacked via configuration, where vias between different layers are nicely aligned (Figure 4). Such a configuration is typically applied in the global

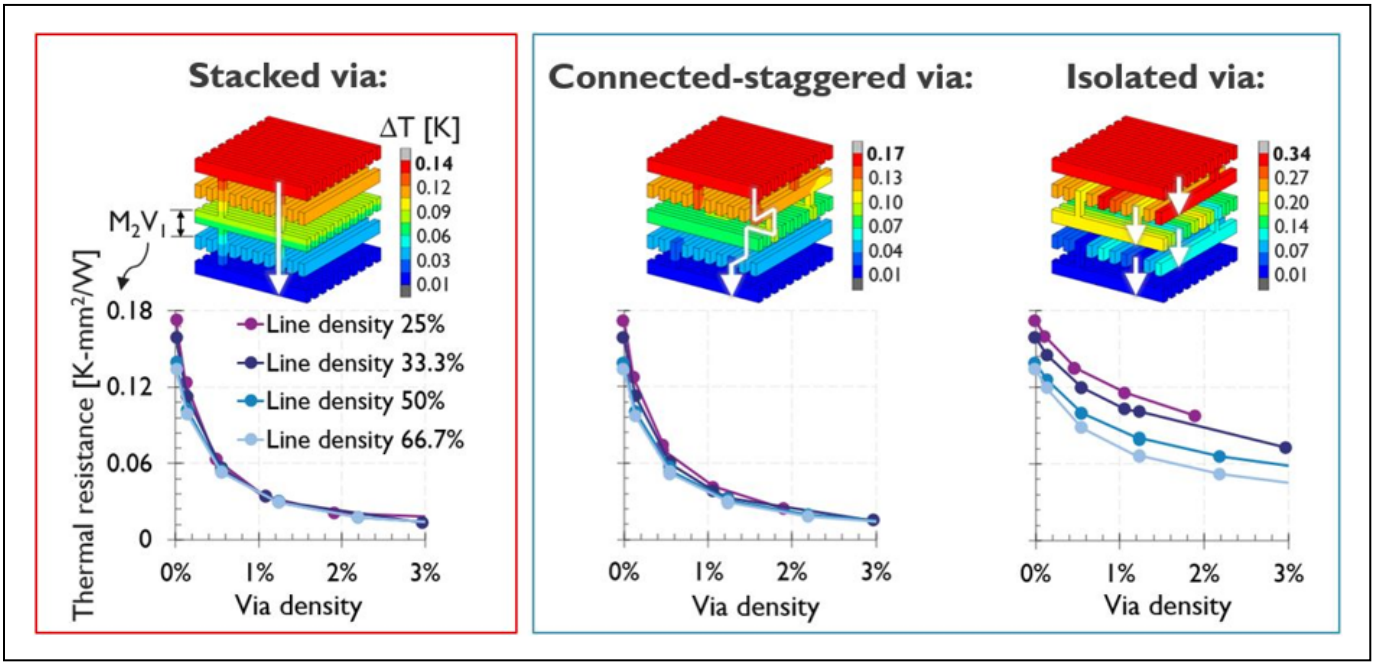

Figure 4: 3D FEM modeling on a simplified BEOL stack, with three different types of via connectivity configurations: a) stacked via, b) connected-staggered via, and c) isolated via.

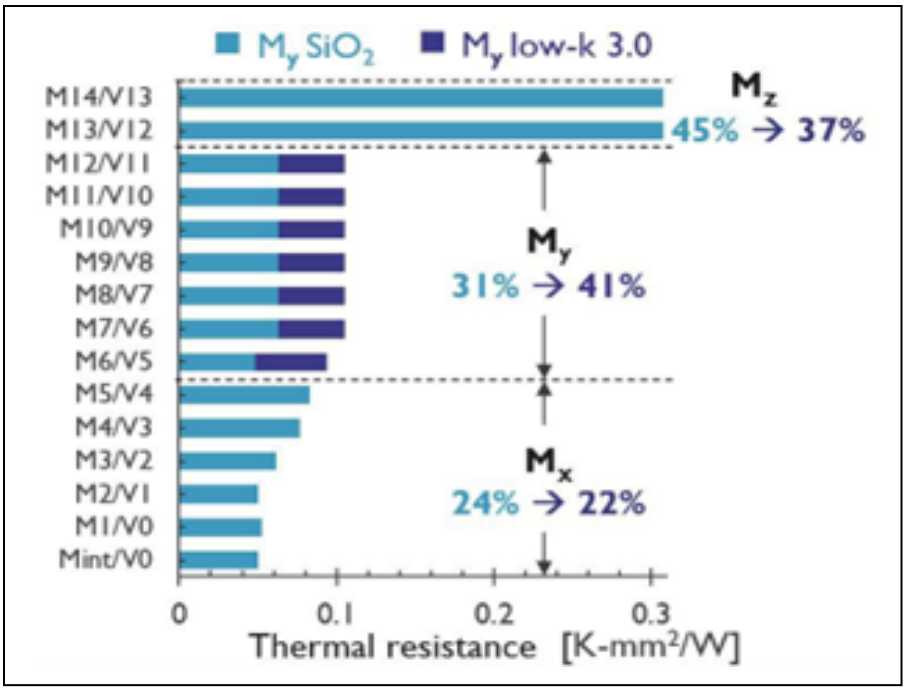

Figure 5: Thermal resistance contribution of each layer. When using SiO2 as the intermetal dielectric in all layers, the highest thermal resistance is ascribed to the Mz layers due to their high thickness—despite the good vertical connectivity for the vias. However, when applying low-k 3.0 as the dielectric in the My layers, the My stack dominates the thermal conductivity of the stack.

interconnect layers (M_z) used for power delivery. A more randomized configuration, commonly used for signal routing in M_x and M_y layers, contributes to increased heating of the interconnect layers.

Finally, when low-k materials are used as intermetal dielectrics in the M_y layers, the M_y stack dominates the thermal resistance of the full BEOL stack (**Figure 5**). Consequently, the M_y part of the BEOL stack provides the most significant opportunity for thermal optimization. The analysis also confirms the impact of the via layers: for the 14-layer stack, they contribute to 86 percent of the total thermal resistance of the BEOL stack, while the line layers only give 14 percent. Note that the thermal resistance of a layer is defined as its thickness divided by the thermal conductivity.

Heat exchange between FEOL and BEOL strongly depends on the package and cooling solution. The metal line temperature is a combination of the line self-heating in the BEOL stack and the heating in the FEOL. The heat exchanged between FEOL and BEOL highly depends on how the chip is packaged and on the solution provided for cooling the package—hence, on the application. Our model was evaluated on three flip-chip packages having different cooling scenarios (**Figure 6**).

In the first scenario (**Figure 6a**), an over-molded flip-chip package is cooled via natural convection from the top of the package, which is closest to the FEOL. In a second scenario (**Figure 6b**), a metal lid frame is added to improve the heat conduction to the upper part. In a third case (**Figure 6c**), forced cooling is applied on the top. While the first and second scenarios resemble a mobile application, forced cooling is typically used in high-performance computer applications.

For the first scenario, most of the heat generated in the FEOL is removed via the BEOL towards the laminate on which the flip-chip package is attached. In other

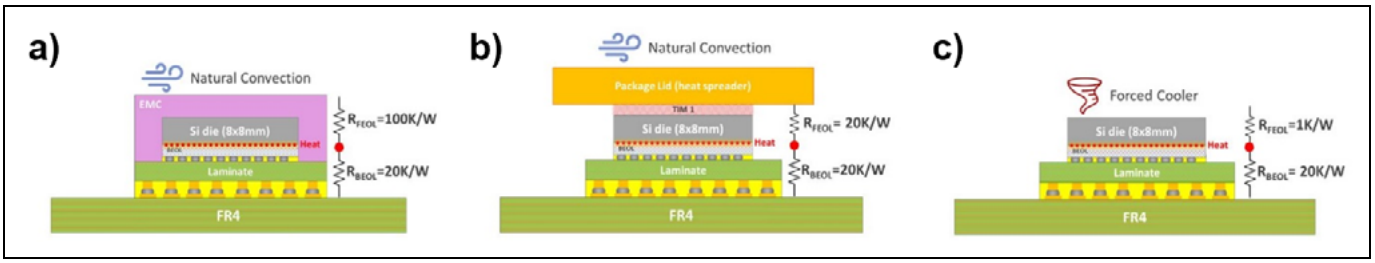

Figure 6: Three IC package options: a) over-molded package with natural convection; b) over-molded with metal lid frame package with natural convection; and c) bare die package with forced cooling. Thermal resistances obtained from experimental characterization are added.

words, this cooling solution results in a large thermal resistance for the FEOL and the BEOL self-heating. The second and third scenarios improve the thermal path towards the top resulting in a 40 percent and 90 percent temperature reduction, respectively, for the same FEOL power, while the BEOL self-heating only reduces slightly.

A valuable tool for STCO

As explained above, each presented model can be deployed for specific use cases, depending on the dimensional scale of interest. For example, the FEM model can be applied to simplified BEOL stacks to investigate thermal aspects of more advanced metallization schemes at the local level, such as semi-damascene. Also, alternative routing and power delivery schemes—such as backside power delivery—can be assessed by feeding in different package configurations in the package model.

Ultimately, mitigating the thermal bottleneck in the chip's BEOL will bring system performance benefits for targeted applications. As such, the models proposed in this work will help identify the right technology ingredients that can unlock major system scaling bottlenecks. They will provide valuable input for imec's 3D and design-technology co-optimization (DTCO) work and, eventually, for the system-technology co-optimization (STCO) that starts from system application needs.

Summary

As dimensional scaling continues, the heating of the interconnects in the chip's back-end-of-line (BEOL) has become a growing concern because it can compromise the chip's reliability. However, accurate models with satisfactory spatial resolution and, at the same time, reasonable computation time are scarce. We have presented a modeling framework that accurately predicts heat dissipation in advanced BEOL structures, considering the coupling with the logic cells in the front-end-of-line (FEOL) and boundary conditions from packaging technologies. We discussed the model and its added value. Valuable insights were presented, such as the dominant contribution of low-k dielectrics and via layers to the BEOL's thermal resistance.

Acknowledgment

The results presented in this article are described in more detail in the following papers. Those interested in receiving a copy should go to the following link and complete the contact form: https://www.imec-int.com/en/connect-with-us

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Biographies

Zsolt Tőkei is an imec Fellow and Program Director of nano-interconnects at imec, Leuven, Belgium. He joined imec in 1999 and has held various technical positions in the organization. He earned an MS in Physics from the U. Kossuth in Debrecen, Hungary. In the framework of a co-directed thesis between the Hungarian U. Kossuth and the French U. Aix Marseille-III, he obtained his PhD in Physics and Materials Science. Email: Zsolt.Tokei@imec.be

Herman Oprins is a Principal Member of technical staff and R&D Team Leader at imec, Leuven, Belgium, where he leads the thermal modeling and characterization team. He joined imec in 2003, where he has been involved in thermal experimental characterization, thermal modeling, and thermal management solutions ranging from device level, over chip level, to the system level. He holds a MSc and PhD in Mechanical Engineering from the KU Leuven, Belgium.

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