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The Future of Semiconductor Packaging

Volume 27, Number 4

July • August 2023

CELEBRATING 25 YEARS

A new generation of e-beam lithography to enable packaging at the leading edge

- Transitioning from 3D packaging to 3DHI
- Foundry 2.0: A renaissance in innovation
- An academic/industry model for integrated systems packaging
- HI of chiplets technology enabled by AP architectures, first-level interconnect
- Parallel validation strategies minimize debug time and ensure sufficient test coverage

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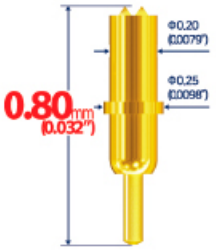
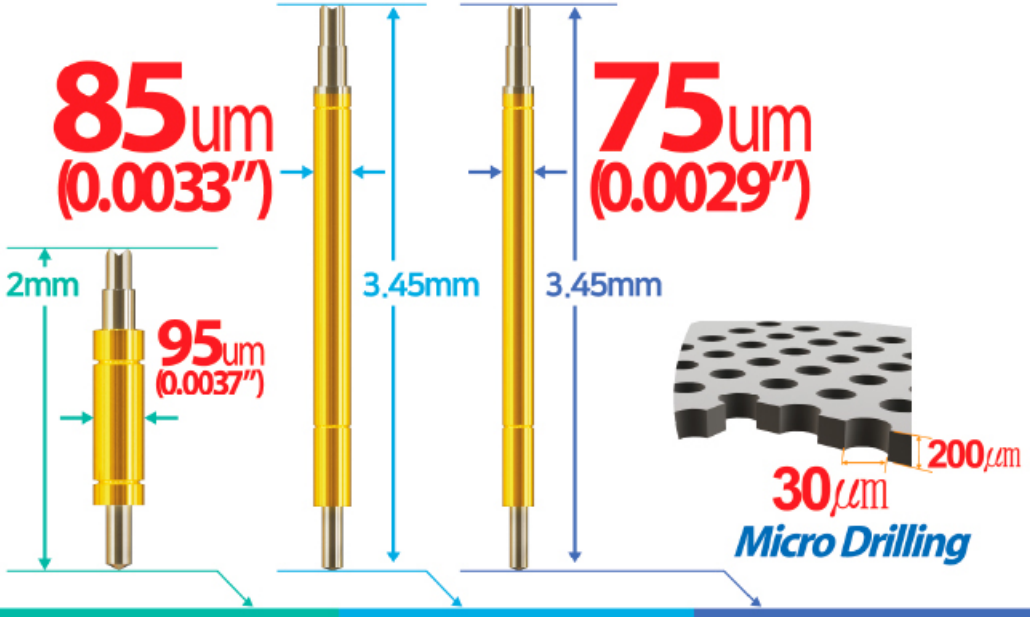
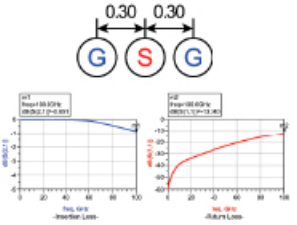
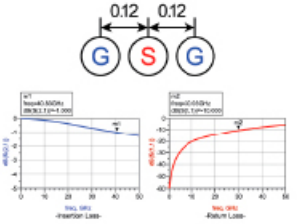
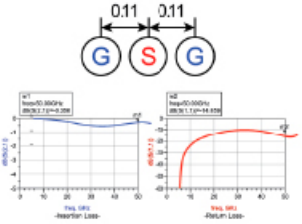
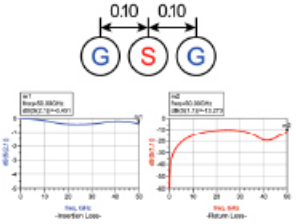




RF-300μm Pitch	120μm Pitch	110μm Pitch	100μm Pitch
Mechanical Spec. • Spring Force : 0.212oz (12.0g) @ .0079 (0.20mm) • Recommended Travel : .0079 (0.20mm) • Full Travel : .0098 (0.25mm) • Current Rating : 2.0A Material Barrel - Alloy / Au plated Plunger - Hardened BeCu / Au plated Spring - Music Wire / Au plated	**Mechanical Spec.** • Spring Force : 0.281oz (8.0g) @ .0098 (0.25mm) • Recommended Travel : .0098 (0.25mm) • Full Travel : .0118 (0.30mm) • Material : Terminal – Pd Alloy / No plated Plunger – Pd Alloy / No plated Barrel – Ni-Au Alloy / Au plated Spring – Music Wire / Au plated	**Mechanical Spec.** • Spring Force : 0.212oz (6.0g) @ .0118 (0.30mm) • Recommended Travel : .0118 (0.30mm) • Full Travel : .0138 (0.35mm) • Material : Terminal – Pd Alloy / No plated Plunger – Pd Alloy / No plated Barrel – Ni-Au Alloy / Au plated Spring – Music Wire / Au plated	**Mechanical Spec.** • Spring Force : 0.247oz (7.0g) @ .0118 (0.30mm) • Recommended Travel : .0118 (0.30mm) • Full Travel : .0138 (0.35mm) • Material : Terminal – Pd Alloy / No plated Plunger – Pd Alloy / No plated Barrel – Ni-Au Alloy / Au plated Spring – Music Wire / Au plated
Electrical Spec. (Simulation data) • Propagation Delay : 7.68ps • Capacitance : 0.05pF • Inductance : 0.25nH • Insertion Loss : > 100GHz @ -1dB • Return Loss : > 100GHz @ -10dB (Dielectric material : MDS100)	**Electrical Spec.** (Simulation data) • Current Rating : 1.0A • Propagation Delay : 20.80ps • Capacitance : 0.21pF • Inductance : 0.38nH • Insertion Loss : 40.83GHz @ -1.000dB • Return Loss : 30.03GHz @ -10.000dB (Dielectric material : CERAMIC)	**Electrical Spec.** (Simulation data) • Current Rating : 0.9A • Propagation Delay : 38.25ps • Capacitance : 0.47pF • Inductance : 0.63nH • Insertion Loss : > 50.00GHz @ -1.000dB • Return Loss : > 50.00GHz @ -10.000dB (Dielectric material : CERAMIC)	**Electrical Spec.** (Simulation data) • Current Rating : 0.8A • Propagation Delay : 35.55ps • Capacitance : 0.44pF • Inductance : 0.66nH • Insertion Loss : > 50.00GHz @ -1.000dB • Return Loss : > 50.00GHz @ -10.000dB (Dielectric material : CERAMIC)
			

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Advanced packaging technologies fuel today's most exciting new applications, but are limited in I/O density, bandwidth, and scale. Novel trends toward adaptable direct-write lithography are emerging to enable a new generation of leading-edge advanced packaging, yielding more connectivity, higher density, and faster speeds between chips.

Cover image courtesy of Multibeam Corporation

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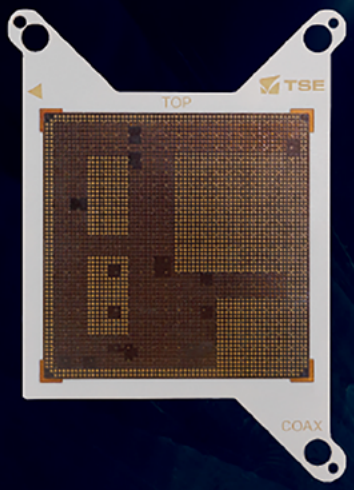
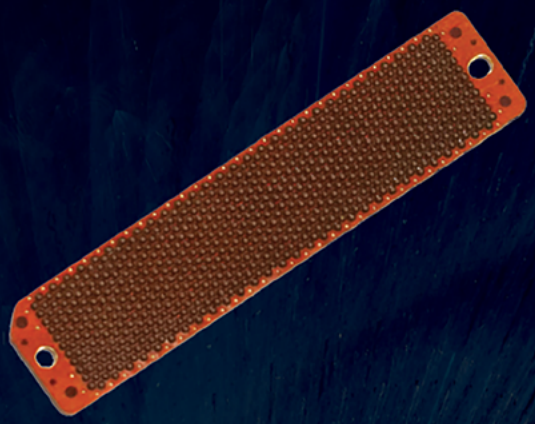


Semiconductor Package Test



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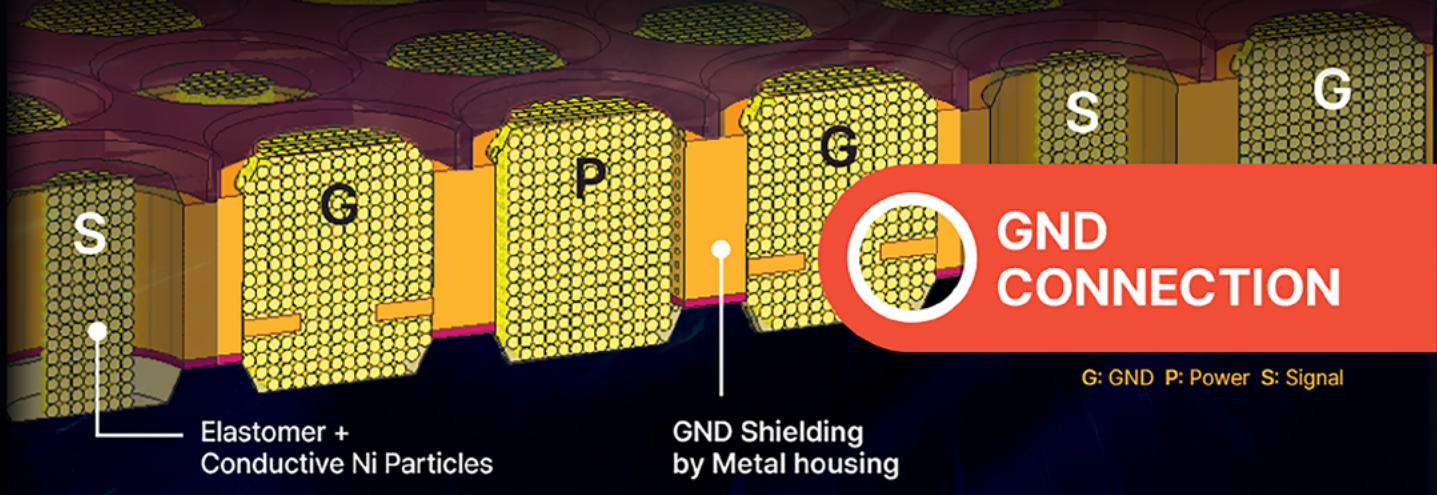

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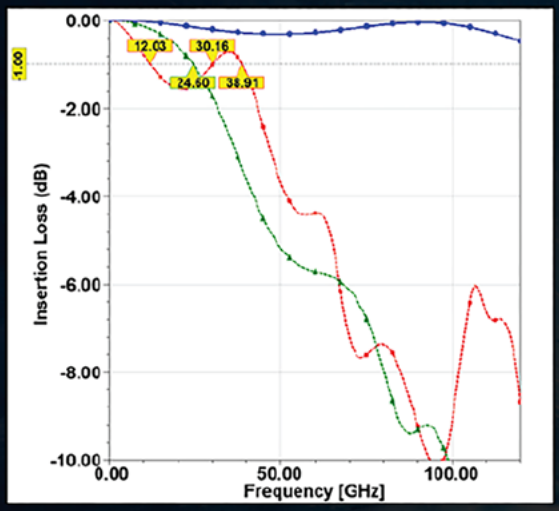
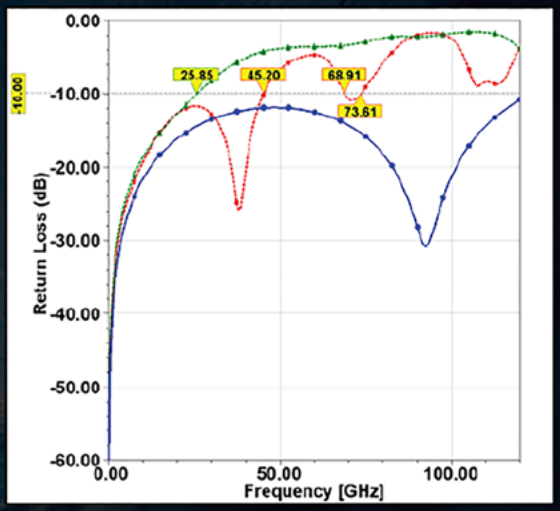
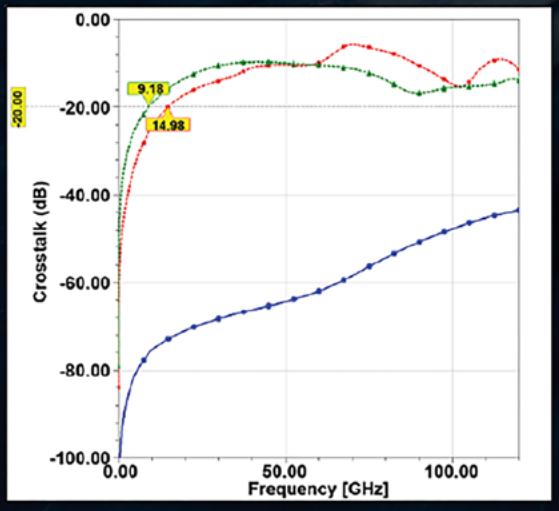
Return Loss (S11) @-10dB	45.20	25.85	>100
Crosstalk (S31) @-20dB	14.98	9.18	>100



Insertion Loss



Return Loss



Crosstalk

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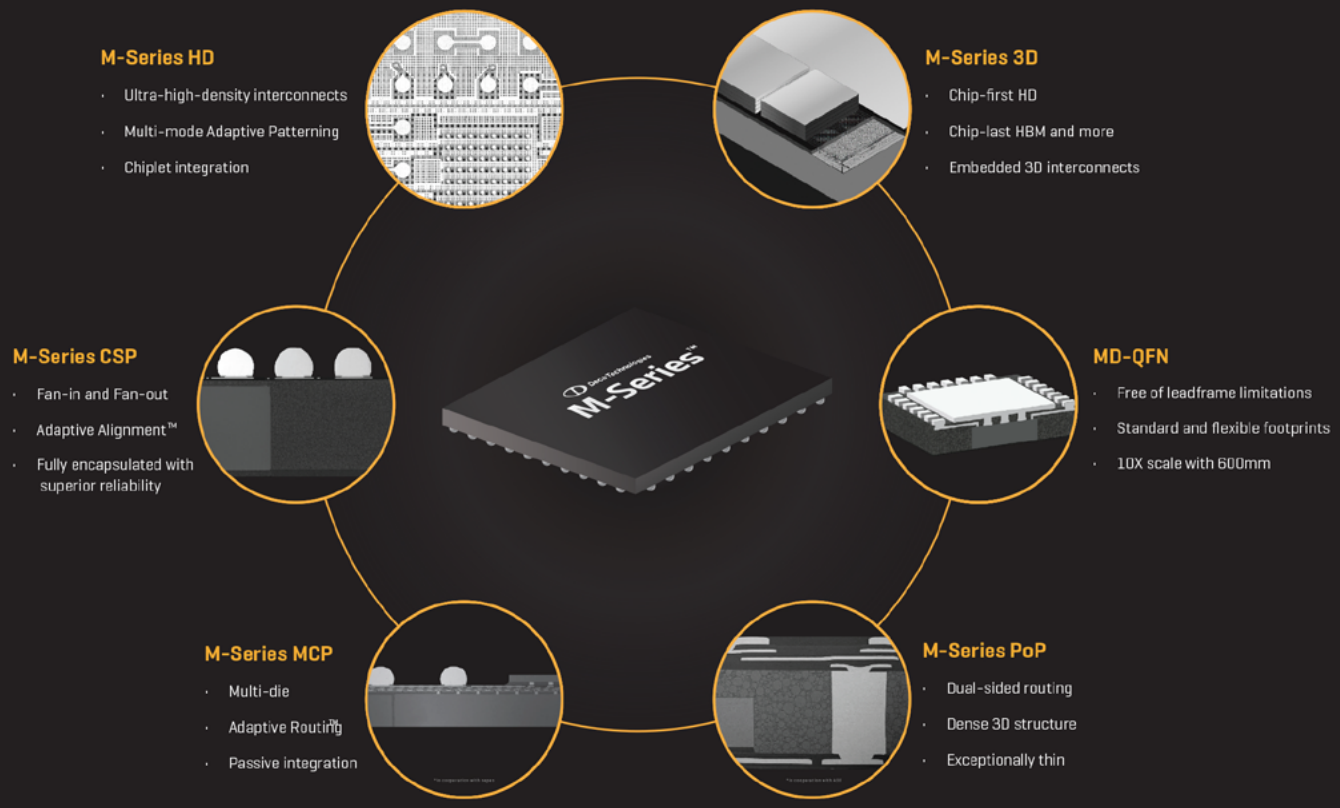

DECA

Expand what's possible

A new generation of e-beam lithography to enable packaging at the leading edge

By David K. Lam, Ken MacWilliams [Multibeam Corporation]

Advanced packaging technologies are enabling hardware improvements in artificial intelligence (AI), 5G, high-performance computing (HPC), smart cars, and other applications that will power continuous growth for the semiconductor industry. Over the years, the packaging industry has relentlessly transitioned to enabling technologies. First with flip-chip, then wafer-level packaging, and now 2.5D and 3D packaging technologies. Today, however, these technologies are being stretched to their limits by certain constraints of conventional back-end lithography tools. Take edge computing, for example. Already on a growth trajectory, this application requires large storage and high I/O to meet aggressive new demands in data analysis, inference, and decision making at the edge of the network. The new requirements are driving new technical imperatives for back-end lithography tools.

The rising prominence of advanced packaging was noted by TSMC chairman, Mark Liu, as he recently remarked that, "Demand for advanced packaging far exceeds the current production capacity [1]." Liu further noted that the company is, "accelerating the increase in production capacity," to match demand for advanced packaging and, "support the next generation of HPC, AI, mobile applications…to help customers achieve product success and seize market opportunities [1]."

Conventional flip-chip packaging (still used today) has a minimum pitch of about 150µm and advanced microbumps have pushed minimum pitches to below 50µm, yet there remains a critical bottleneck. To overcome the limitations, some "big tech" companies are employing in-house custom processors, accelerators, and networking silicon. But it's clear that next-gen devices will inevitably need more chiplets and higher bandwidth in package. Indeed, demands for larger interposers, more I/O, greater bandwidth, more processing power, lower latency, and lower power usage are converging to drive the need for a new generation of lithography technology engineered to enable back-end imperatives.

We have developed Multicolumn Electron-Beam Litho (MEBL) systems that perform maskless patterning to meet current and projected back-end requirements, as discussed in the sections below.

Edge computing. Edge computing eliminates the bottleneck of data-transfer between the edge device and data center. MEBL's fine-resolution and direct-write capabilities enable higher interconnectivity and higher bandwidth between chiplets. Dense interconnects and I/O can be integrated without the need for large, power-hungry SERDES circuits presently required for high-bandwidth communication between chips. All this helps speed in-package data analysis, inference, and decision making, thereby optimizing overall smart computing of edge devices.

Large interposers. Today's interposers are limited to the size of one optical field of view, or a few optical reticle fields, stitched together. In contrast, MEBL's auto-stitch capability enables very large-scale interposers, spanning up to full-wafer. Such large interposers enable a unique flexibility to integrate additional powerful processors for HPC, graphics processing units (GPUs), and AI engines. Furthermore, MEBL is capable of patterning fine-interconnect pitches with more than 10 times higher resolution. This finer resolution creates much greater chip-to-chip bandwidth and reduces the SERDES overhead requirements.

High productivity. EBL has been valued for decades as an enabling tool for research and pilot purposes. However, it has never met the throughput standards required for fab production. In contrast, MEBL is fully automated and employs multiple miniature e-beam columns operating in concert to pattern full wafers while the wafer stage is in motion—an architecture also known as "parallel writing on the fly." This allows MEBL to yield 20x to 100x higher productivity than single-beam lithography systems found in research labs. Incidentally, in e-beam mask-making (an adjacent market of MEBL), single-beam writing systems are being replaced by multi-beam writing systems for the same reason – higher productivity.

Large depth of focus (DoF). In advanced systems-in-package, the substrate may be stressed and warped by processes such as through-silicon via (TSV) or bonding, resulting in an uneven surface. This poses challenges to optical lithography, which is known for its shallow DoF. The problem intensifies at finer resolutions because optics capable of higher resolution have correspondingly smaller DoF. By using a 100x larger DoF than advanced optical systems [4], we were able to overcome this limitation at finer resolutions. This DoF advantage enables patterning of high-resolution interconnects with relaxed requirements for substrate flatness, bow, and warpage. It helps to overcome patterning challenges associated with non-flat surfaces in advanced packaging.

Rapid cycles of learning. New applications have ever-increasing requirements for system integration and performance, and, "Increasing complexity continues to create new challenges for package design," as noted in [5]. Cycles of learning are crucial to successful development of new systems-in-package devices. Our system enables rapid testing of early concepts by writing layouts directly onto substrates with no

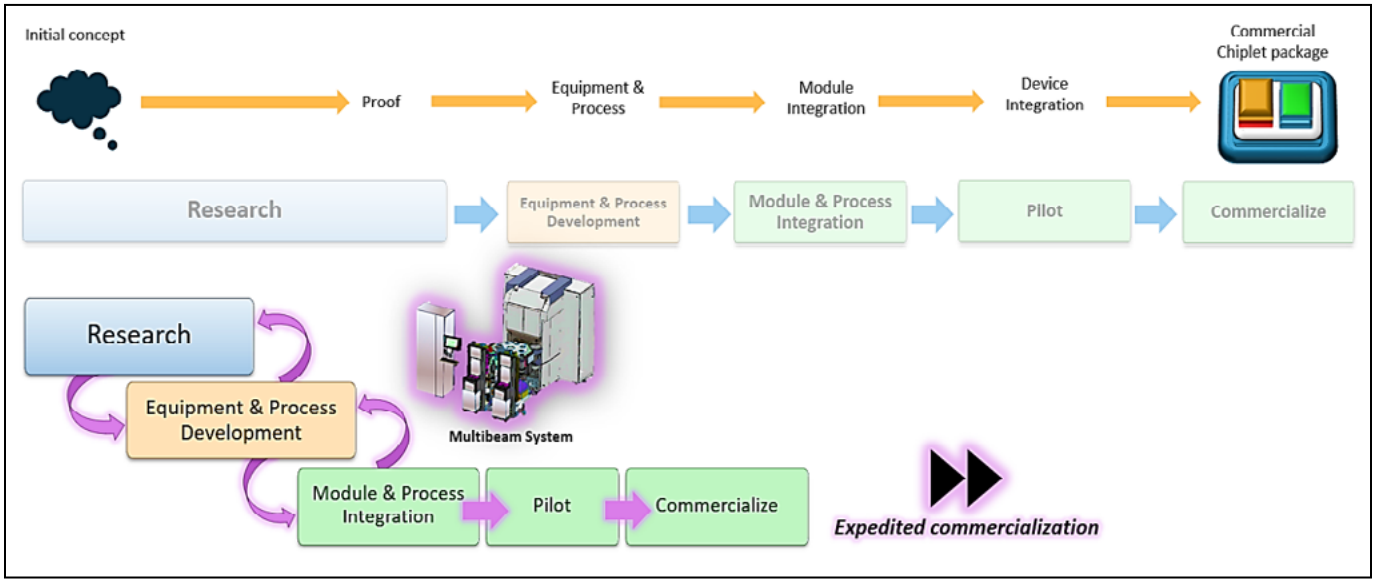

Figure 1: Enabling co-optimization with rapid cycles of learning to accelerate time to market. SOURCE: Multibeam Corporation

masks (Figure 1). Layout changes can be quickly implemented using MEBL's data prep computer, increasing the speed of learning cycles, and reducing time-to-market for new products.

Industry trends driving a new generation of e-beam lithography

Aside from the need for greater fab productivity in EBL technology, there are two major semiconductor industry trends that need to be addressed as discussed below.

Purpose-built devices. Tightly integrated processing, memory, communications, and other functions, can be optimized to meet the needs of specific applications. Dense interconnects between chiplets will eliminate the need for large SERDES circuits previously needed for high-bandwidth chip-to-chip communication. The MEBL solution addresses this need.

Mass customization. Customized devices' compute throughput is distinctly higher than that of general-purpose devices. This has led to an industry-wide shift toward mass customization—a trend that aligns very well with advanced packaging. Advanced packaging allows designers to develop purpose-built devices from individual chiplets, thereby optimizing performance and power efficiency. Data shows that "purpose-built silicon," optimized to accelerate specific tasks, performs significantly better than general-purpose CPUs. This means advanced applications requiring high computation, such as 5G, intelligent edge devices, smart cars, and AI, will all benefit from the trend toward mass customization and purpose-built silicon. With purpose-built silicon and mass customization on the rise, the demand for advanced packaging is soaring (Figure 2).

Extendible very large-scale interposers will allow manufacturers to maximize

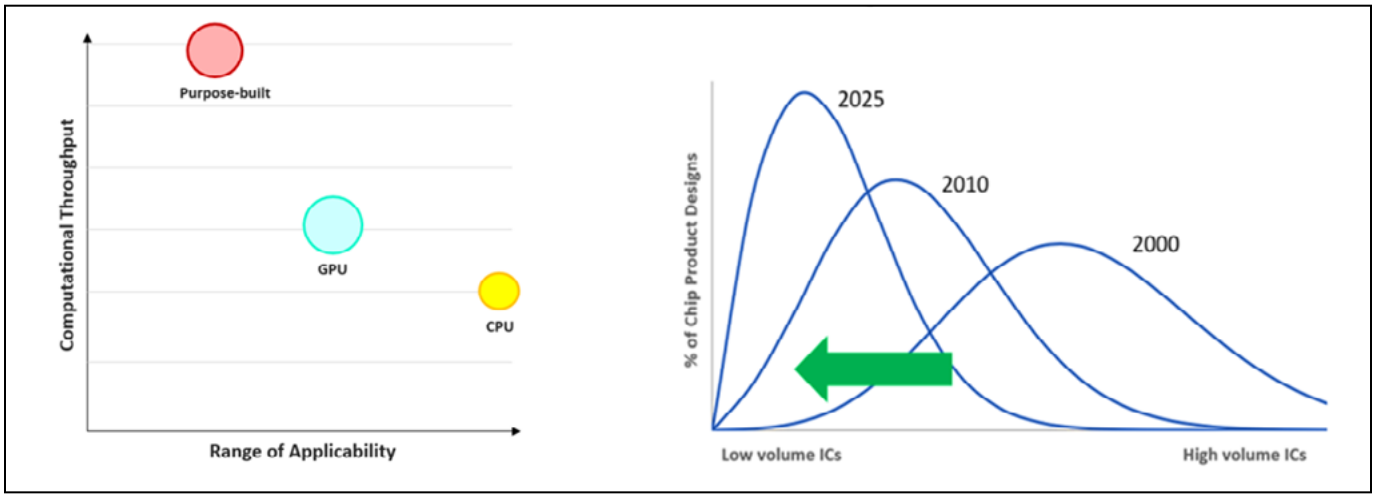

Figure 2: Optimizing performance and power efficiency of advanced packaging by facilitating high-throughput purpose-built silicon and shifting to mass customized designs. SOURCES: Multibeam Corporation, SkyWater Technology

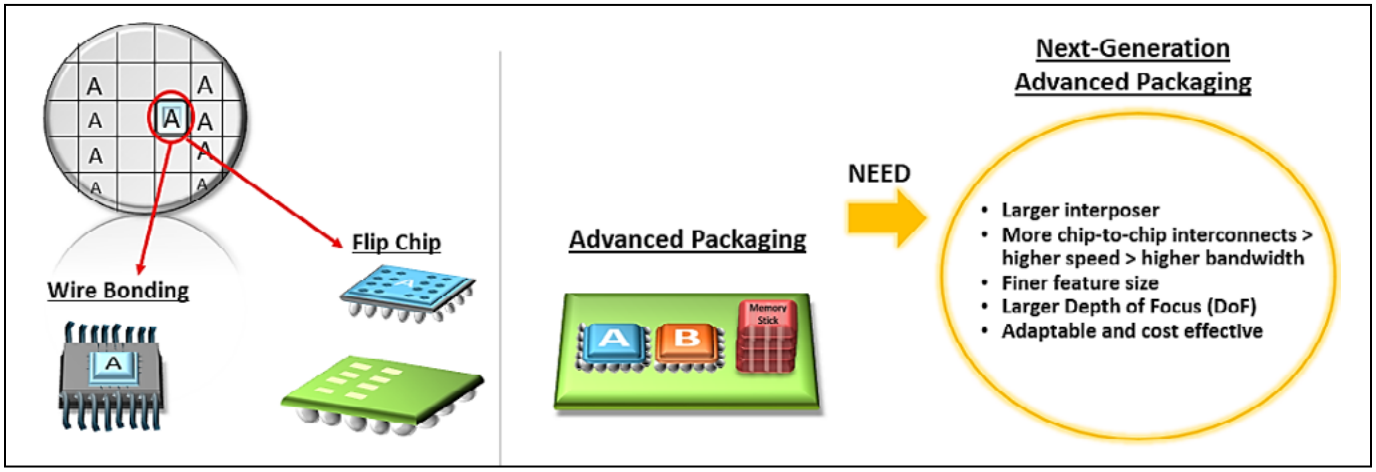

Figure 3: The evolution of advanced packaging to next-generation advanced packaging. SOURCE: Multibeam Corporation

performance by enabling more connections between larger numbers of chiplets in compact, low-power packages.

As packaging evolves and these industry shifts accelerate, back-end lithography will evolve as well. Mask-based optical lithography is a natural fit for high-volume manufacturing and has played an integral role in the chip industry's success. However, device costs rise when fabricating small batches of customized wafers with mask-based lithography technology. Further, mask-based lithography is hindered by die shift that can significantly reduce yield. Such limitations make mask-based lithography less practical for the next-generation of advanced packaging applications. In contrast, maskless e-beam direct writing has inherent advantages in writing fine resolutions across large areas, tying together disparate chiplets into high-performing integrated packages. The maskless MEBL system makes it possible to adjust for die shift, enabling denser interconnects between varied chiplets. This adaptability is crucial in integrating heterogeneous chips into new purpose-built devices (Figure 3).

Summary

System and packaging development cycles can take years. With a high-productivity direct-write MEBL system, the development cycle can be reduced significantly. Moreover, this new generation of direct-write EBL is well-suited to support the shift toward purpose-built edge devices. As AI and edge computing converge to drive growth in the semiconductor industry, a next-generation direct-write lithography system will eliminate in-package bottlenecks and enable larger-scale integration of compact, low-power/high-functionality chiplets. In addition to enabling greater latitude to innovate, the new generation of direct-write EBL gives developers of new devices a faster, cost-effective route to market.

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Biographies

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Ken MacWilliams is President and board member of Multibeam Corporation, Santa Clara, CA. He has helped develop and commercialize novel equipment platforms and processes for the world's leading semiconductor manufacturers, and held senior management positions at Applied Materials, Novellus Systems (acquired by Lam Research), Veeco, and Yield Engineering Systems (YES). He holds PhD and MS Electrical Engineering degrees from Stanford U.

Transitioning from 3D packaging to 3D heterogeneous integration (3DHI)

By John Park, Vinod Kumar Khera [Cadence Design Systems]

The semiconductor industry has been using scaling to keep up with the increasing demands of more functionality, higher integration, improved performance, and smaller footprints. With Moore's Law slowing down at advanced nodes, the industry is transitioning from "More Moore" to "More Than Moore" for the lower cost, larger design sizes and modularity benefits. Advanced packaging technologies and 3D heterogeneous integration (3DHI) are becoming more critical for enabling this transition; these technologies are evolving as the primary alternative to the traditional monolithic system-on-chip (SoC).

As the two worlds of system design and integrated circuit (IC) design are beginning to merge, new challenges for the complete ecosystem are being introduced—from electronic design automation (EDA) tool providers to package substrate designers and application-specific integrated circuit (ASIC)/SoC designers. This paper discusses some of these challenges and the EDA tool provider's perspective on this transition.

Introduction

As nonrecurring engineering (NRE) costs climb for advanced nodes, manufacturing size limitations are reached, and more I/O, analog/radio frequency (RF) designs are required. As a result, new form factors emerge, and solely relying on process shrink (Moore's Law) is no longer the best technical and economical path forward as shown in Figure 1.

It could be argued that reticle size limitations and the emergence of through-silicon vias (TSVs) allowed semiconductor foundries to enter the world of multi-die packaging leading to the Moore-than-Moore era. A decade later, designers and manufacturers are beginning to realize the benefits of integrating some of the die in a vertical stack rather than building a single large monolithic SoC. This approach of 3D stacking can include dies, cores, memory, and more, to meet the needs of their next product. This technology, called 3D-IC, 3D heterogeneous integration (3DHI) or silicon stacking, promises many advantages over traditional single-die planar designs, such as lower costs and more modularity,

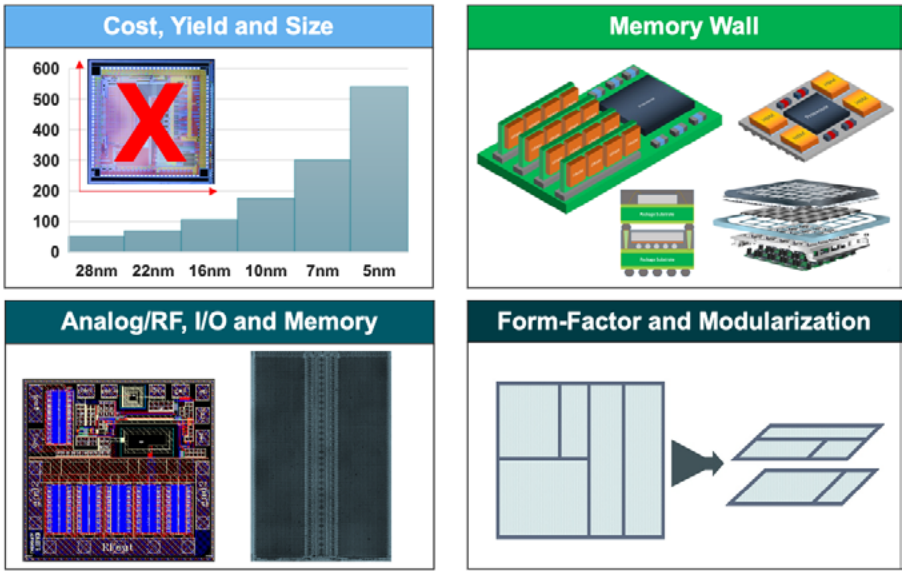

Figure 1: Moore's Law: economic and technical viability.

Integration in the vertical dimension/silicon stacking technologies allows designers to potentially cram more functionality into smaller form factors while improving performance and reducing costs. Silicon stacking architectures can integrate multiple homogeneous and heterogeneous die/chiplets, such as logic, memory, analog, and RF, into a single design. These heterogeneous, multi-chiplet architectures can provide a much lower-cost alternative to using advanced nodes (scaling).

Trends in advanced semiconductor packaging

Semiconductor packaging engineers have been heterogeneously integrating die and designing 3D stacks for multiple decades. Typical examples are stacked and wire-bonded dynamic random access memories (DRAM) and package-on-package (PoP) solutions. The industry used the terms multi-chip module (MCM) and a system in a package (SiP) to describe these architectures. Today, dozens of new packaging technologies support higher interconnect density and better electrical and thermal performance. Before discussing some of the newer packaging technologies, let's go back 30 years to the beginning of advanced packaging.

Advanced packaging started with single and multiple wire-bond and flip-chip die on a printed circuit board (PCB)-like laminate substrate called the ball-grid array (BGA). Build-up substrates came later, allowing smaller interconnect geometries. Interconnect bridges followed sometime near 2012. About the same time, TSV technology emerged, enabling silicon to be used as a high-density multi-chip(let) packaging platform. This technology is commonly referred to as 2.5D-IC packaging and is considered modern-day advanced packaging. This was when the semiconductor foundries began to offer "back-end" services, which

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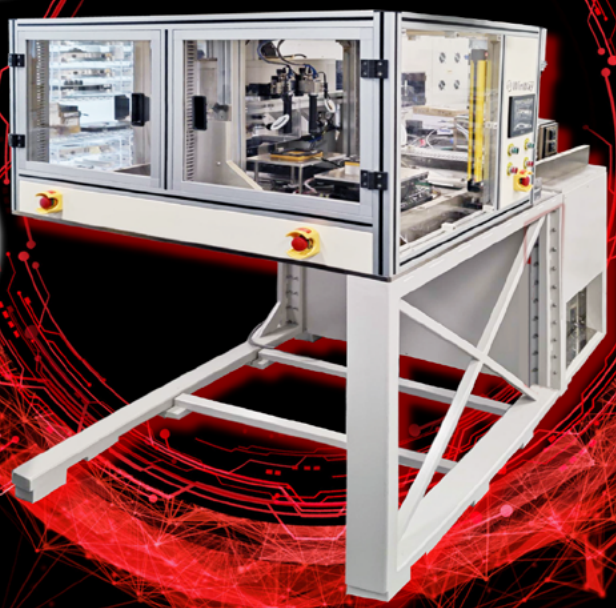

Probing System for Co-Packaged Optics

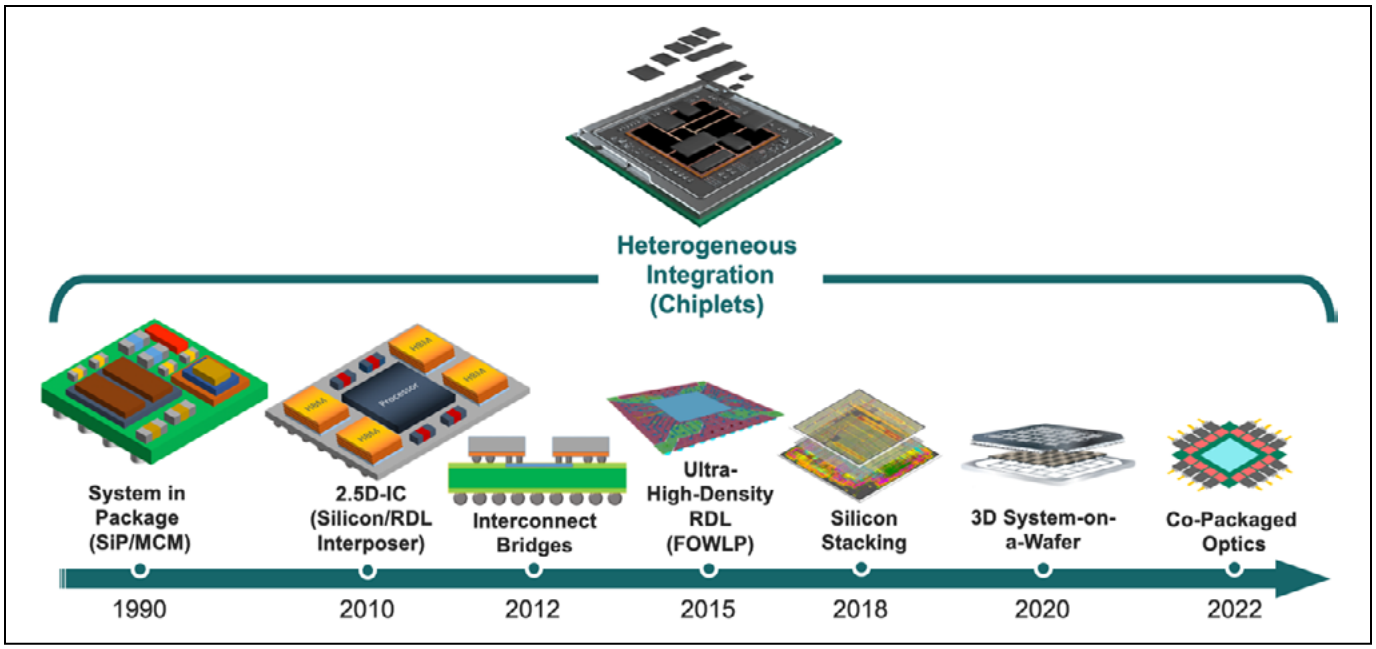

Figure 2: Heterogeneous integration leverages multiple packaging technologies.

were multi-die packaging using foundry-based manufacturing techniques. A few years later, foundries also started offering higher-density single-die packaging solutions ideally suited for the mobile communications market. Fan-out wafer-level packaging (FOWLP) wasn't new, but the ultra-high-density fan-out redistribution layer (RDL) provided smaller interconnect geometries than previous FOWLP solutions. These new foundry-based technologies created healthy competition and collaboration with the outsourced semiconductor assembly and test (OSAT) companies that had dominated packaging for 25 years.

Over the past few years, a new vernacular has emerged based on a new set of acronyms – 3DHI, 3D-IC, and chiplets. This new vernacular primarily comes from semiconductor foundries and IC designers as they pivot from More Moore to the world of More-Than-Moore (3DHI). The sections below discuss specific challenges with 3DHI.

3D heterogeneous integration (3DHI). Heterogeneous integration is about the disaggregation of a chip into smaller building blocks, commonly called chiplets. It offers many benefits, such as: 1) Lower nonrecurring engineering (NRE) costs; 2) Shorter time to market (TTM); and 3) Flexibility and modularization benefits.

Heterogeneous integration is a term used to describe the disaggregation of an ASIC/SoC into smaller building blocks, each of which can be fabricated at whatever node or technology makes the most sense. Advanced packaging then becomes the process of aggregating all the building blocks (chiplets). And, of course, designers get to choose from dozens of packaging technologies (Figure 2). As discussed previously, semiconductor foundries started extending the back-end design services into silicon-based advanced packaging solutions a decade ago. The foundry-based approach of high-density interconnect geometries combined with TSVs paved the way for silicon interposers to emerge as the leading technology to aggregate and integrate multiple chiplets. But other packaging technologies might be starting to catch up. Most notable are RDL interposers, which don't require TSVs, thus lowering the cost.

With advanced packaging as the primary technology for the next generation of electronic product design, it's crucial to understand the nuances between different packaging technologies. Packaging engineers have been designing organic/laminate substrates for three decades. The design flows and methodologies are well established. However, some interesting facts about today's foundry-based packaging technologies include:

- Convergence of the die design flows with the system design flows leads to questions about the expertise needed (die design or system design).
- While using bumpless stacking technology, in many cases, true chip-on-wafer and wafer-on-wafer applications are not packaging at all. Instead, it's die design except with the ability to now design in the vertical direction. This silicon stacking approach best suits the die designer with enhanced 3D capabilities in their place and route tool. In most cases, silicon stacking doesn't use chiplets in the traditional sense. Instead, a single register transfer level (RTL) gets partitioned in the third dimension, and in the case of face-to-face stacking, small 1-2µm pads are used to connect the two levels. This differs from most chiplet-based applications, which connect devices with micro I/O buffers, RDL, and micro-bumps using a die-to-die (D2D) communication interface such as Unified Chiplet Interconnect Express (UCIe™) or bunch of wires (BoW).
- Finally, the combination of these two worlds is the hybrid scheme. Hybrid packaging technologies combine these two worlds (3D packaging and silicon stacking). 2.5D silicon interposer or ultra-high-density FOWLP requires tools and expertise spanning IC and

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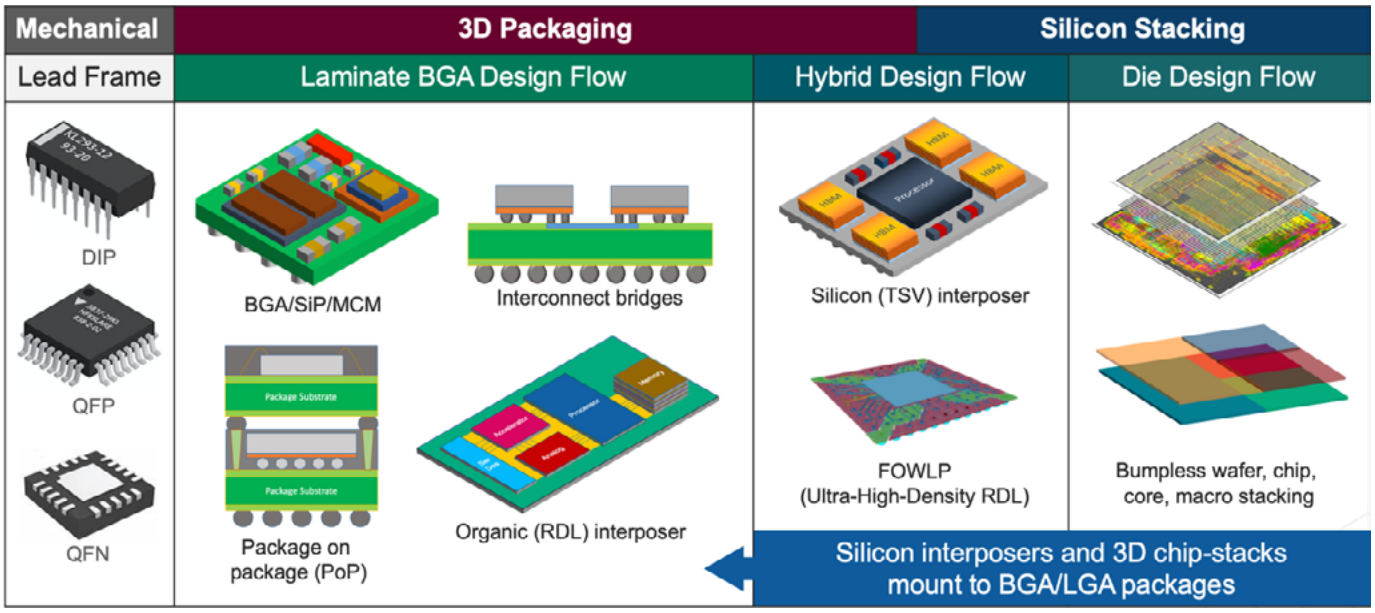

Figure 3: Packaging technologies.

system design. Figure 3 illustrates the different categories of multi-chip(let) packaging technologies.

Bottom line, 3DHI has its caveats, such as: 1) The design does not get easier with heterogeneous integration and gets more complicated; 2) Moving from a single monolithic SoC to a system-level architecture reintroduces considerations that SoCs effectively counteracted, such as thermal, electrical, and mechanical stresses; and 3) The correct tools, methodologies, and team collaboration approaches must be implemented before designing a heterogeneous integration chip.

Challenges for 3DHI

As discussed above, 3DHI offers many benefits over monolithic IC design. However, as with most emerging technologies, several challenges must be overcome—starting with the minimal availability of assembly design kits (ADKs) (Figure 4). Some of the primary design challenges for 3DHI are discussed in the sections below.

Lack of package ADKs. PDKs provide the necessary information to start the design in ASIC/SoCs, but there is a lack of such data to start the package design as we transition to the world of 3DHI. Existing ADKs are focused on the rule deck and lack the design libraries for packaging. Starting a new design without a PDK is another hurdle for IC designs to jump.

Commercialization and standardization. Commercialization and standardization of chiplets are two more major challenges. This is because most chiplet-based designs today are in a closed ecosystem of vertically-integrated companies. While much progress has been made with standards such as UCIe™, BoW, chiplet design exchange (CDX) and TSMCs 3Dblox™, we have ways to define a business model that makes sense for turning silicon intellectual property (IP) into chiplet form for the general market.

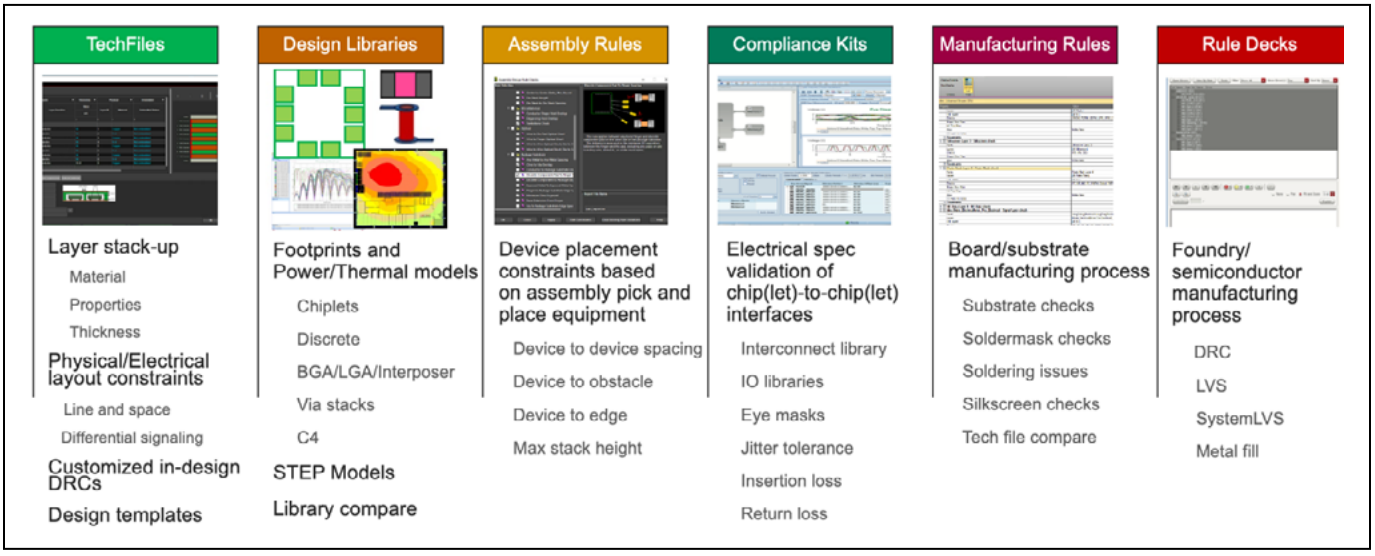

Figure 4: Package assembly design kits (ADKs).

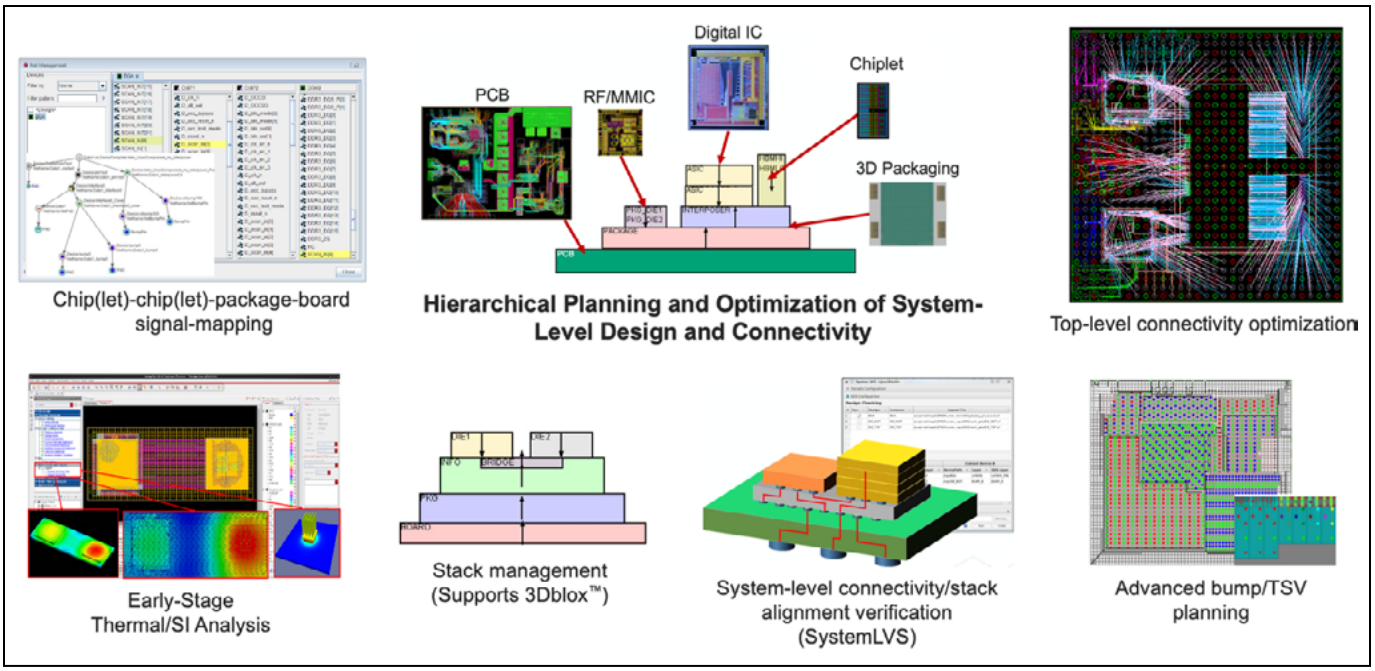

Figure 5: Requirements for EDA tools.

It may be 3-5 more years before we have a catalog of known-good chiplets from which to choose like what is available to printed circuit board (PCB) designers.

3DHI challenges for the package designers

Package designers face new challenges while pivoting to ultra-high-density foundry-based packaging technologies. A massive change for most package designs is the design verification step. Further, they face many other challenges, such as:

- Sign-off design rule check (DRC) and layout vs. schematic (LVS) are standard practices when designing something for a foundry-based manufacturing process. Today, most package substrate designers use a much less formal process of validating their design from a DRC, LVS and assembly perspective (see previous discussion re: ADK).
- Lack of a formal SystemLVS methodology to validate the alignment and connectivity through the multiple levels of a 3D heterogeneously-integrated package.
- Pre- and post-route chiplet-to-chiplet signal integrity and compliance issues have become a new requirement for most substrate designers focused on single-die packaging. In single-die packages, electromagnetic (EM) extraction tools are used to generate the pin parasitics of a package. In multi-chip(let) designs, the electrical compliance between the devices requires signal integrity expertise.

3DHI challenges for ASIC/SoC designers

There are a number of 3DHI challenges that face ASIC/SoC designers such as:

- A top-level planning methodology needs to be established for planning and optimizing the interconnect (netlist) for the system-level design across multiple chiplets and packaging tiers.
- Robust co-design with the package substrate design team is paramount. The over-the-wall approach of the past may lead to increased final product cost, or worse.
- Pre-place and route thermal analysis capabilities to determine the best 2D and 3D chiplet placement to meet thermal budgets long before detailed implementation.
- On-the-fly die splitting and repartitioning in the third dimension, potentially across different design nodes, requires a design tool that works concurrently with multiple PDKs or tech library exchange formats (LEFs) in a single layout session.

EDA tools perspective

From the EDA tool provider's perspective, it is essential to develop cross-domain design flows that provide a platform to the user for designing multi-chiplet-based packages from a single logical hierarchical representation to a multi-chiplet-design (from the transistor level to the full system level) (Figure 5). The existing die design tools need extensive enhancements to support 3DHI architectures and help design and analyze from the system perspective. The increasing complexity because of the rising number of design tools as we transition from monolithic SoC to 3D-IC demand EDA tools with capabilities such as:

- Place and route tools must be extended to support multiple PDKs;
- The tool database must also be extended to support structures such as silicon vias, TSVs, bumps, backside metal, and more;
- Scalability to handle increasing instances and routing interconnect styles;
- Pre-place and route and heat/thermal analysis;
- Automated optimized TSV placement solutions and routers to connect multi-die in a stack;
- Additional capability for digital signoffs, such as:

- Static timing analysis (STA) with automated corner reduction; and
- Rule-deck-free SystemLVS for 3D package-level alignment and connectivity checking.

- Comprehensive thermal stress and design for manufacturability (DFM) tools for chemical mechanical polishing (CMP) planarity checks across the dies.

These tools should allow the designer to aggregate the chiplets and packaging technologies to plan and optimize the top-level design. Apart from this, the tools should have the ability to work at very abstract levels of the design to make designers capable of performing early-stage analysis of the 3DHI.

Additionally, next-generation design flows need to move more analysis further upstream in the design process. EDA technologists have used the term "shift-left" to describe moving electrical analysis into the layout tools, but for 3DHI, the analysis tools need to be shifted further left into the design planning stage. Thermal analysis, for example, must be performed as early as possible when considering stacking silicon.

Summary

As we advance with 3DHI, design methodologies are becoming even more complex. Companies willing to invest in their design flows will have a competitive edge. As the domains of die and system design converge, many new challenges await ASIC and package designers entering the world of "Moore-than-Moore." An integrated design methodology across IC, package, and board design, along with analysis and verification moved further upstream in the flow, will be vital in enabling designers to focus on design work, not design tools. Seamless integration across the tools will significantly reduce design cycle times and enable co-design and co-analysis across IC, package, and PCB domains.

Biographies

John Park is Product Management Group Director for Advanced Semiconductor Packaging at Cadence Design Systems, Louisville, CO, where he leads a team responsible for defining cross-domain solutions and methodologies for IC, package, and PCB co-design and analysis. His team is especially focused on developing tools and flows for chiplet-based 3D designs. He has over 40 years of experience in the EDA field and is regarded as an international expert on chiplets, packaging, and heterogeneous integration. Email jpark@cadence.com

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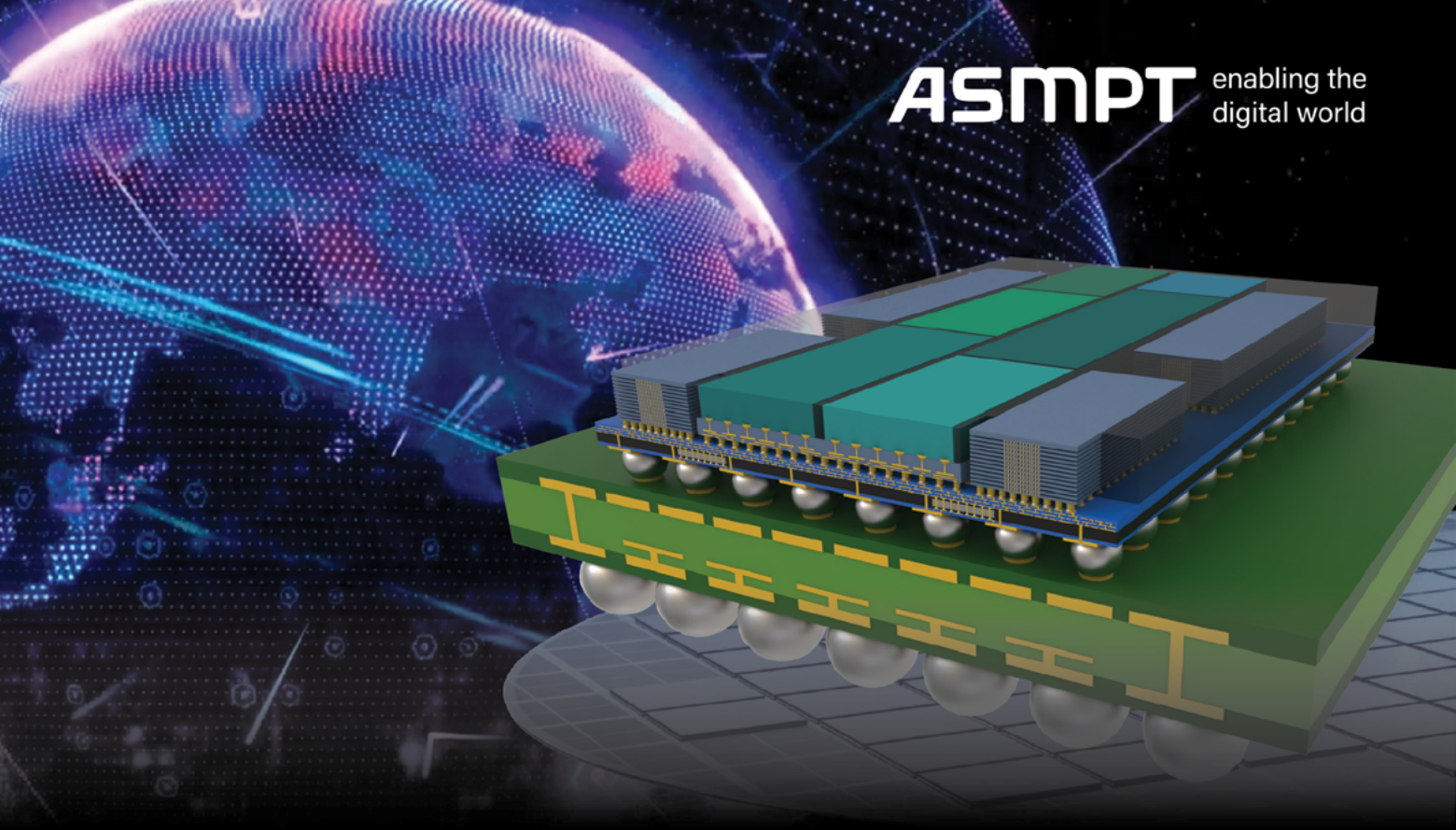

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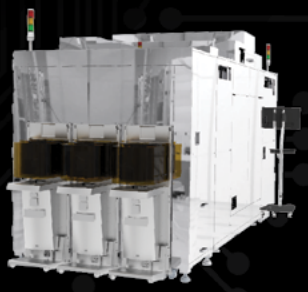

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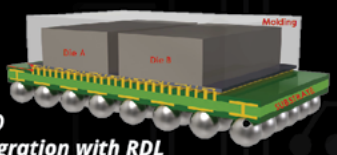

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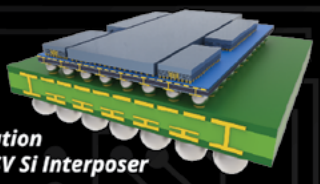

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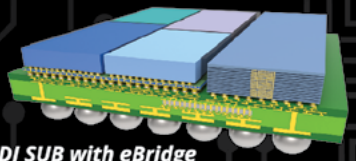

HDI SUB with eBridge

Integration with
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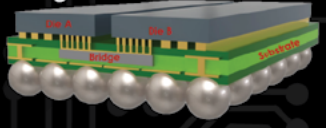

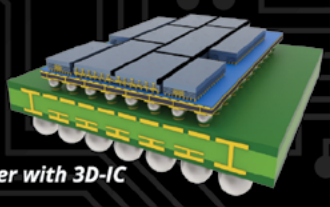

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Heterogeneous integration of chiplets technology enabled by advanced package architectures, first-level interconnect

By Nelson Fan, Eric Ng [ASMPT Limited]

While leading semiconductor companies continue to develop complementary metal-oxide semiconductor (CMOS) scaling under the driving forces of high-performance computing (HPC) and artificial intelligence (AI) applications, "More than Moore" has been successfully demonstrated through the heterogeneous integration of chiplets (HIC) in various advanced package architectures, together with advanced first-level interconnect (FLI) technologies (**Figure 1**). The objective of developing advanced package architecture is to deliver the same or even better device performance as a system-on-chip (SoC) format while achieving the best cost of production.

FLI process mapping

Although CMOS scaling is continuing to progress at a slower pace, the focus is now on creating chiplets with higher density and I/O counts at a finer pitch (down to sub-micron pitch level) resulting in smaller bump sizes, rather than using SoCs. The HIC approach is being deployed to mitigate the economic effects of expensive nodes. To achieve the required performance, a very high degree of chiplets placement accuracy in a heterogeneously-integrated (HI) device is being scaled up, and more advanced FLI interconnect processes are being developed. From traditional mass reflow flip chip (MR-FC) and thermal compression bonding (TCB) at 5µm and 2µm placement accuracy respectively, the technology is now evolving towards fluxless thermal compression bonding with bond accuracy of less than 1µm to handle the very high bump density with pitches less than 10µm. Although the ultimate device performance can be enabled by the copper-to-copper connection through the hybrid bonding process, the cost of ownership can currently only be borne by devices with a very high average selling price (ASP). That being said, hybrid bond technology is continuously being developed to target devices with higher density, better yield, and an affordable cost of ownership for high-volume manufacturing (HVM) in the near future.

Various HI package architectures

Over the last decade, various HI package architectures have been developed by the technology frontrunners including wafer foundries, integrated device manufacturers (IDMs), outsourced semiconductor assembly and test suppliers (OSATs), and advanced substrate houses (**Figure 2**). These HI package architectures can be classified into three major basic categories: 1) with a through-silicon via (TSV) interposer; 2) with a redistribution layer (RDL) interposer; and 3) with single and/or multiple embedded silicon bridges (e-bridge) inside the high-density build-up interconnect (HDI) substrate.

Among the three categories mentioned above, the TSV interposer offers the best routing capability with the finest line width and spacing at the sub-micron scale of wafer fabrication feature size. However, it is the most expensive type and is also limited by its 300mm diameter manufacturing format. The number of interposers will be very much limited per 300mm diameter format,

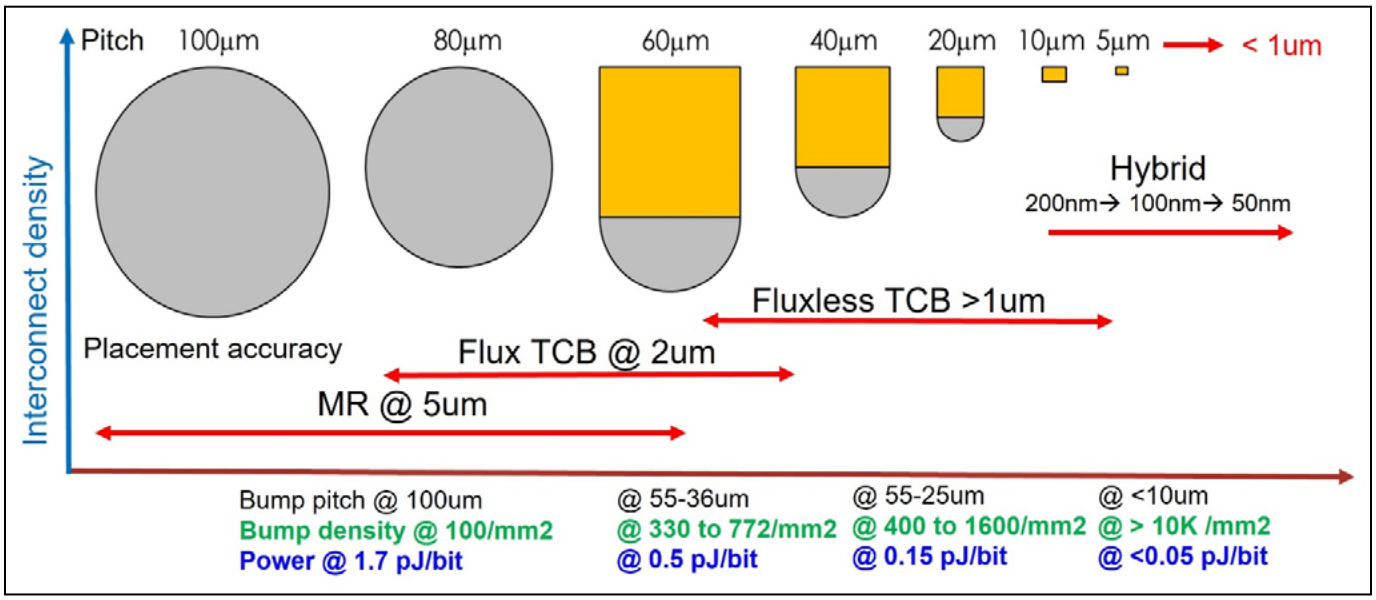

Figure 1: First-level interconnect (FLI) process mapping.

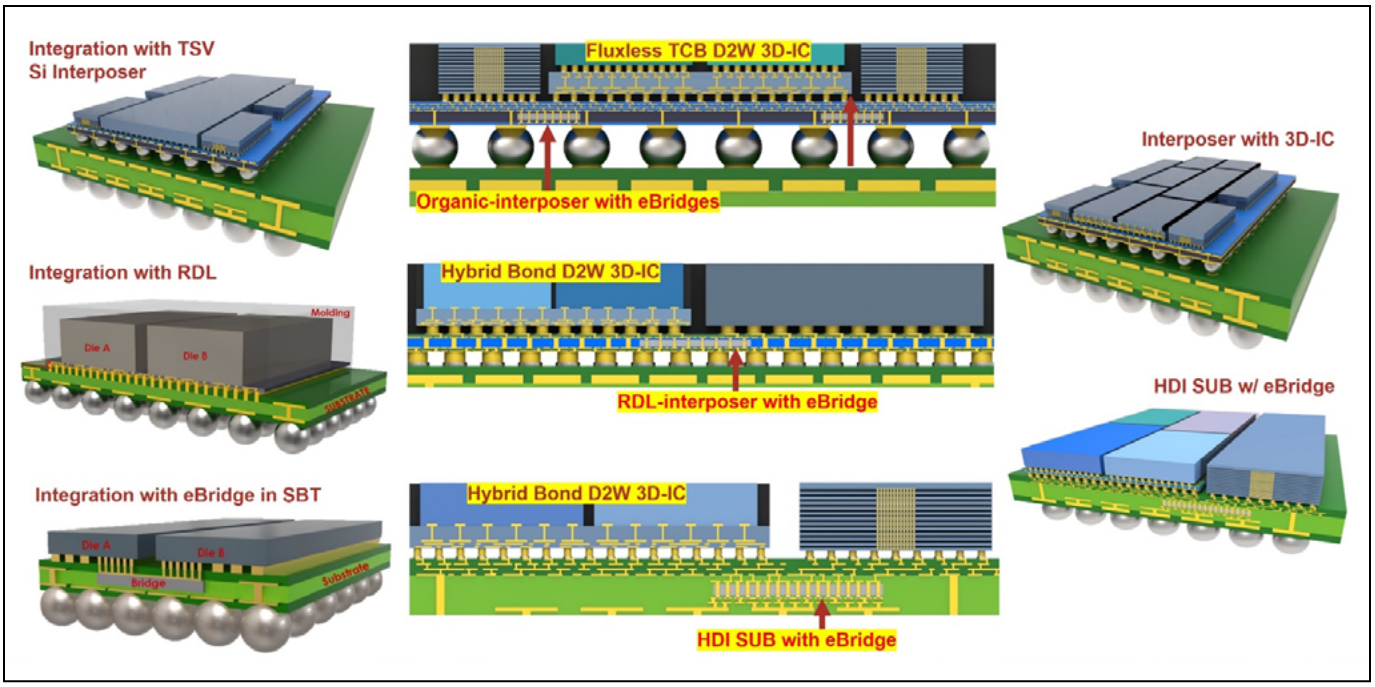

Figure 2: Various heterogeneous integration (HI) package architectures at a glance. SOURCE: ASMPT

particularly if the interposer size is continuously growing (said to be more than 4 reticle sizes to support a larger degree of integration).

A HDI substrate with e-bridge has been developed as another way to integrate multiple chiplets without facing the interposer manufacturing format size limitation. It makes use of single or multiple pieces of a smaller Si bridge fabricated with fine line width and spacing capability to partially connect two chiplets at the location designed for die-to-die communication. Because the e-bridge is embedded precisely onto the target location of the high-density build-up (HDBU) substrate as part of the manufacturing process, the associated challenges are the final substrate yield related to the induced top substrate top surface planarity, open/short continuity, and warpage, among others.

The RDL interposer has been developed to provide the most cost-effective way for integration. Various versions can support a die-first or die-last approach depending on the process capability and device performance requirement. Recently, silicon bridges have been embedded into the RDL interposer to further improve the integration capability and to enhance the power and signal integrity of integrated device performance requirements.

Continuous advancement of the TCB process

TCB is one of the most advanced FLI methods. Although it has been developed and deployed for more than a decade, it is continuously being adopted for new applications (**Figure 3**). The most recent adoption is for the next-generation high-bandwidth memory (HBM). Flux-TCB has been qualified for HBM as the HVM process up to 12 layers, with proven capability to maintain the tight control die-to-die gap height for all the layers (**Figures 4-6**). The next-generation HBM is required by the latest HPC and AI devices to meet the performance requirements.

Another example of new HVM deployment of the TCB process is for extra-large HI die interconnection to the HDI substrate (**Figure 7**). As the HI die is becoming larger (larger than 6 reticles in the area), with reduced bump pitch and complicated die layout, coupled with the extra-large HDI substrate (easily 2x larger in the area), the traditional mass reflow flip-chip (MR-FC) process becomes impossible. The next-generation TCB bonder, with extra-large HI die handling capability, as well as the sophisticated bond head heater and bond stage design, enables dynamic warpage control for both HI die and HDI substrate during solder joint formation, and is now the new process of record (POR).

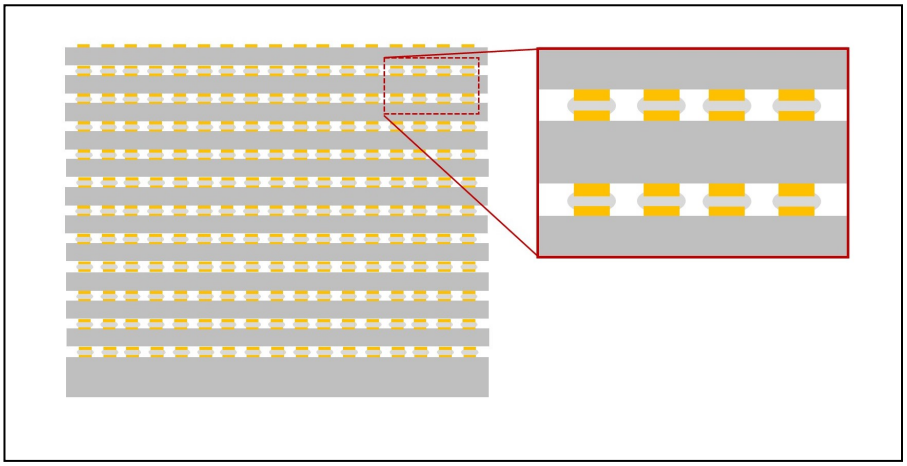

Figure 3: Cross-section of the next-generation HBM with flux-TCB.

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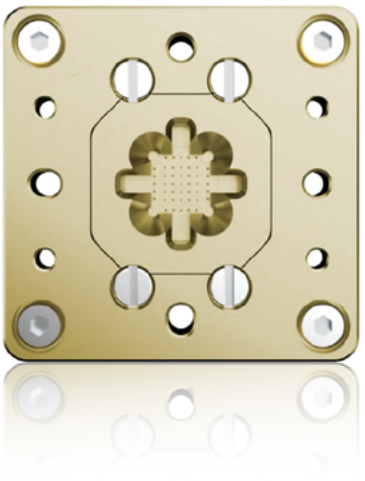

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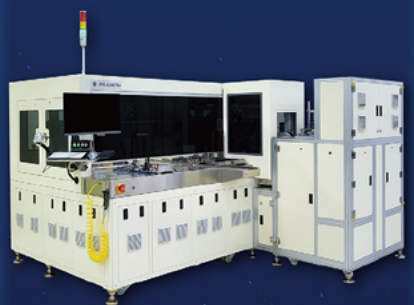

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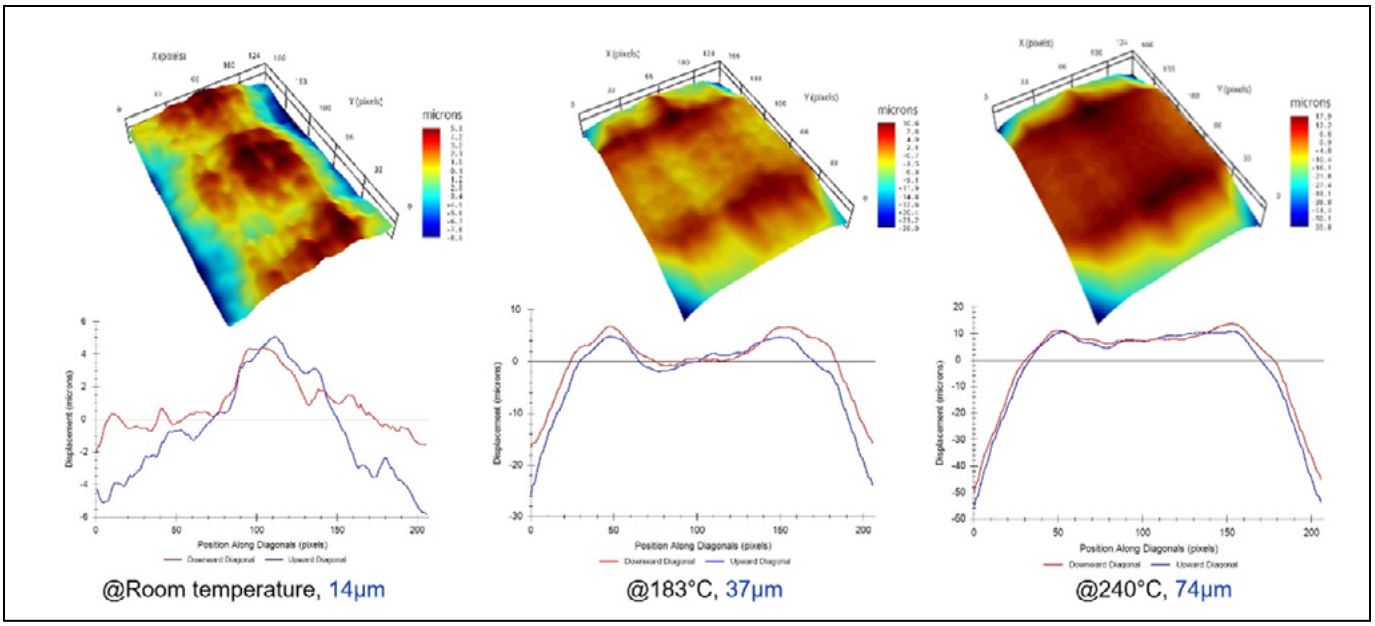


Figure 4: HI die warpage characterization. An example of warpage in large compound HI dies from room temperature to reflow temperature. SOURCE: ASMPT

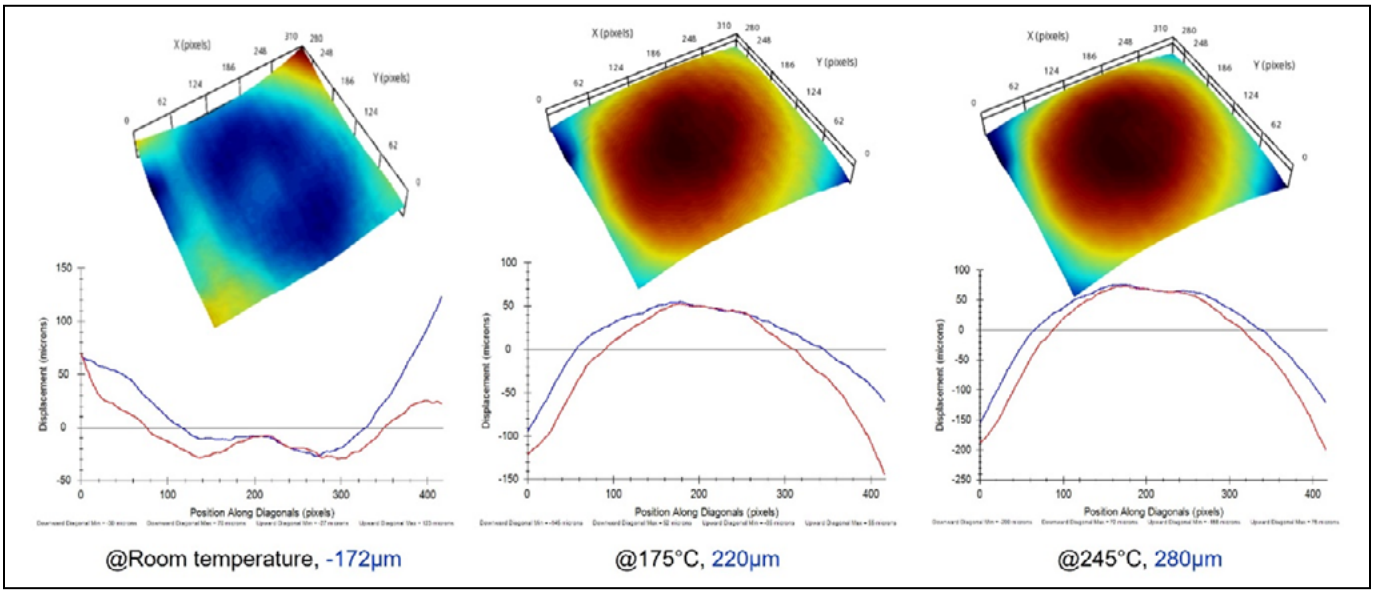


Figure 5: HDI substrate warpage characterization. An example of warpage in a large HDI substrate from room temperature to reflow temperature. SOURCE: ASMPT

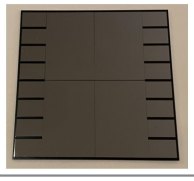
Substrate Size/mm	55x55 to 110x110 (continuously increasing)	
Bump Pitch/µm	120, 90, 80 (continuously reducing)	
Compound Die Layout	• Square to rectangular shape • Rectangle shape with a high aspect ratio • Both symmetric & asymmetric design	

Figure 6: HI packaging architecture associated challenges and solutions with ASMPT home-built TV with 70 x 70 integrated die size.

TCB bonder manufacturers continue their development efforts to enable the emerging fluxless-TCB process, which is an alternative process to very expensive and yet HVM immature hybrid bonding (HB) technology. Recent development work has shown robust bonding capability for micro bump devices with fine bump pitch at less than 15µm (**Figure 8**). The test vehicle, in the form of a 3D structure bonded by the fluxless-TCB process, has also passed the reliability stress test up to 1000 cycles of thermal cycling, as well as 1000 hours of

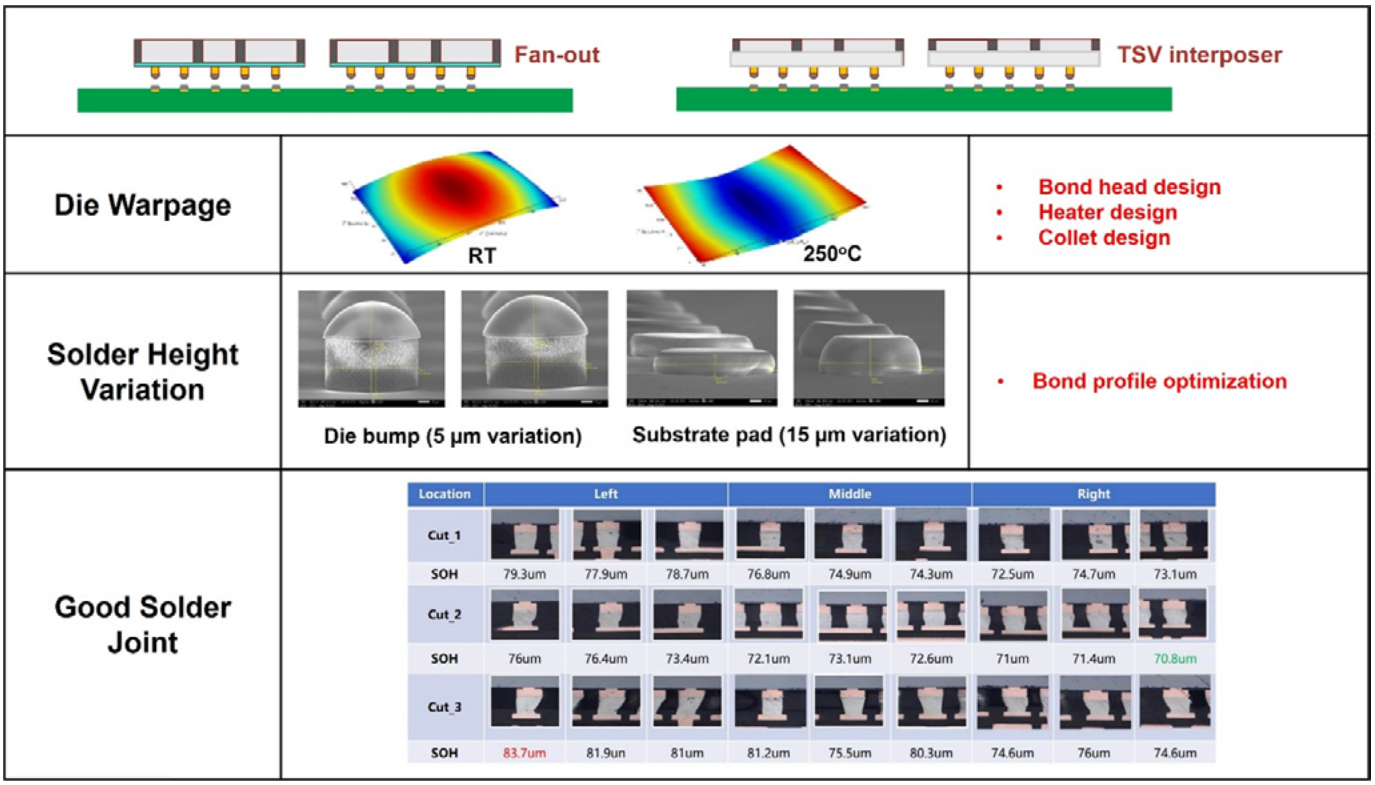


Figure 7: Challenges for extra-large HI die bonding. SOURCE: ASMPT

This figure has been removed per author's request to avoid potential disclosure of proprietary details

Figure 8: Fine-pitch micro bumps with fluxless-TCB. SOURCE: ASMPT

high-temperature and humidity testing per JEDEC standard (**Figure 9**). It is believed that the fluxless-TCB process, with the appropriate TCB bonder design equipped with a robust oxide removal process, will enable the HVM interconnection process for chiplets integration with a micron bump pitch of less than 10µm.

The emerging hybrid bonding technology

What if the chiplets' I/O pitch is to be less than 1µm? The solder volume of micro-bumps at this small pitch makes

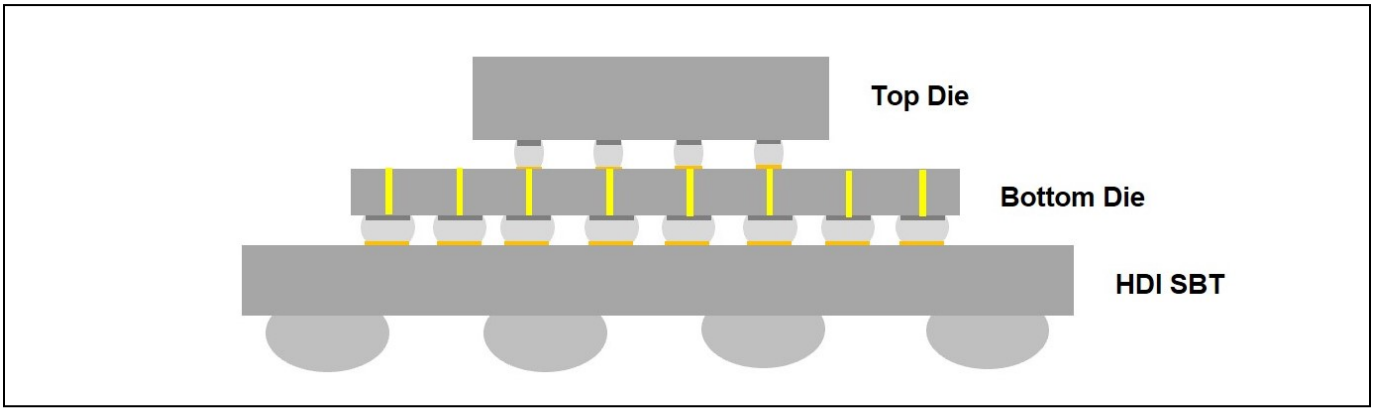


Figure 9: Fluxless bonding for 2-layer stack packages. SOURCE: ASMPT

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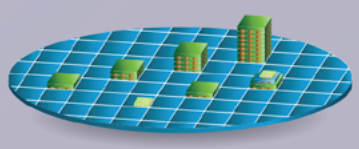

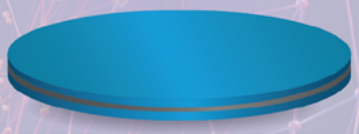

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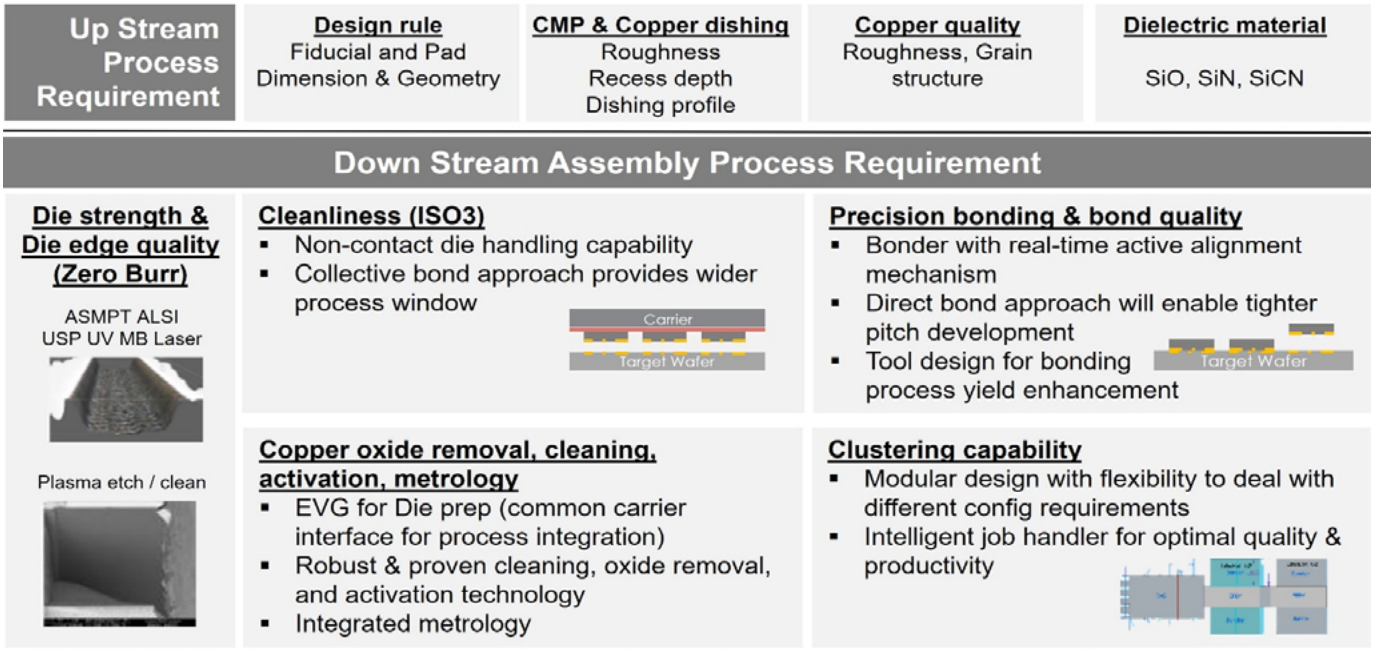

Figure 10: Key challenges and solutions in D2W hybrid bonding.

the resultant solder joint not reliable under stress conditions. A copper-to-copper joint is likely the way to go. While the I/O pad pitch is getting so small, the die gap-filling process will be impossible if it follows the approach of conducting a post-bond underfill process. Bonding the dielectric simultaneously together with the copper-to-copper I/O bonding that makes a hybrid bonding process is the most probable way.

Hybrid bonding (HB) for HI devices with chiplets integration is an emerging FLI process that requires very different upstream design and process requirements such as chiplets design rules, choice of dielectric material, copper I/O pad plating chemistry, as well as chemical mechanical polishing (CMP) and copper pad dishing (**Figure 10**). It is targeted for devices with I/O pitch at the sub-micron level. Tool makers have already made HB bonders to meet the high-precision alignment accuracy at 200nm (**Figure 11**). Besides high-precision alignment, a very clean environment to enable a die-to-wafer face-to-face bonding process is also required, with almost zero tolerance for foreign particles. Therefore, bonder cleanliness capability is required to meet ISO 3 specifications, the same as for front-end

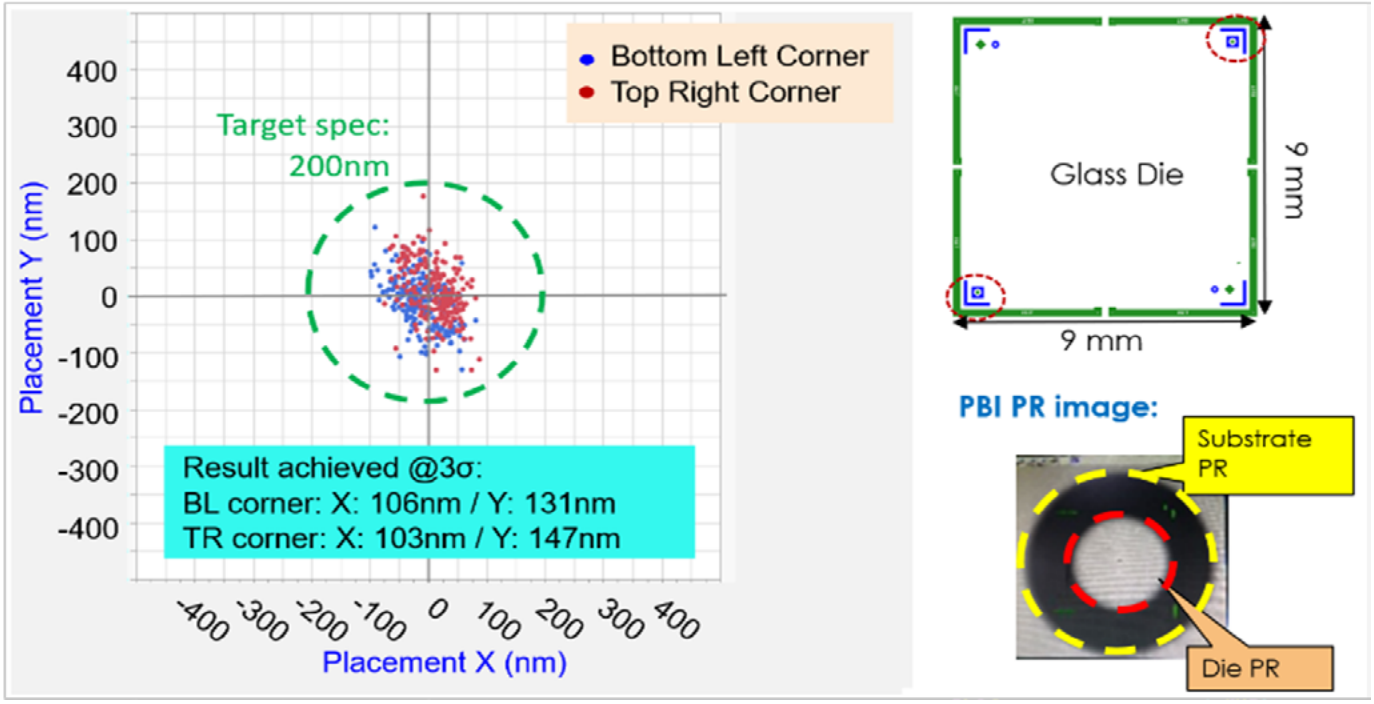

Figure 11: Alignment accuracy verification test based on COG (chip-on-glass) done on an ASMPT LithoBolt Bonder showed that a ≤200nm result has been achieved.

equipment. The bonder is also being put inside the front-end condition to ensure cleanliness. This is a very costly operation compared to running in a traditional back-end assembly clean room. To ensure a successful bond with good yield, not only are cleaning and activation of the chiplets and target wafer needed to be done by the material preparation tool critical, but queue time control and cleanliness are also vital. Integration of the material preparation tool and multiple bonders is being advocated, which will induce a "line balancing" issue. The situation will be further complicated if the number of chiplet types increases. All these issues incur additional costs compared with other devices running in HVM mode with TCB and mass reflow (MR) processes.

To fully bring up the merit of HB technology for next-generation chiplets-integrated HI devices in a much more cost-effective way, and enable it for more applications than just very high-end devices, new development efforts are being undertaken.

Summary

The rise of the HPC and AI era exerts increasing demand for performance advancement of computational devices. With front-end node technology continuing to evolve, advanced packaging technology is making corresponding progressive developments. Both advanced TCB and HB are promising FLI processes to enable heterogeneous integration and chiplets applications for our industry. Reaching HVM at a reasonable cost of ownership for advanced packaging technology requires not only the effort of equipment manufacturers to develop equipment capabilities, but also close collaboration with the user to fully understand design requirements, associated material technology, as well as manufacturing conditions.

Biographies

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Parallel validation strategies minimize debug time and ensure sufficient test coverage

By Adir Zonta [Advantest]

Test data volumes are exploding as the number of transistors per chip increases along with the number of test vectors needed to test each transistor. A recent article [1] provided an overview of how the device validation and characterization, structural and functional test at automated test equipment (ATE), and system-level test have evolved over the years to deal with ever-increasing complexity. The author [1] described how traditional methods no longer suffice and introduced innovations in pre-silicon verification, first silicon bring-up, and post-silicon validation (PSV) that are necessary to meet today's challenges. This article provides more details on these recent innovations and the systems necessary to implement them, including information on how to equip an engineering lab with automated parallel test stations to speed up test engineering tasks such as pattern validation. In addition, it describes how a new standard helps bridge the gap between the electronic design automation (EDA) and ATE domains and how an EDA company and an ATE maker have collaborated on an initiative to put the standard into practice.

Test-pattern validation

One of the challenges that the explosion in test data imposes on test engineering is the ever-lengthening time required for test-pattern validation, which is impacting time to market. Test-pattern validation determines whether the patterns are generated correctly, that the expected responses are accurate, and that they have enough margin to account for parameter variations (for example, in voltage and frequency) in production.

Generating test patterns

The test patterns include structural scan patterns generated by automatic test-pattern generators or functional test patterns generated manually from a test specification or automatically using random or constraint-based test-generation methods or other techniques linked with EDA tools. Test patterns from the EDA tools are generally in a standard format such as STIL (Standard Test Interface Language) or WGL (Waveform Generation Language). Structural test patterns target specific fault models, such as "stuck at" faults or timing faults, whereas functional test patterns aim to come closer to confirming the device under test's (DUT) performance in its end use. The need for functional test vectors is particularly important in automotive and other industries where performance and safety are critical. The following sections discuss aspects of generating test patterns.

Cyclized test vectors. The patterns in STIL or WGL from the EDA tools must be converted to cyclized test vectors for the target ATE system. The cyclization process involves adding timing and control information to synchronize the patterns with a specific ATE system's clock and control signals, which can require extensive development time.

Error causes. Inevitably, errors will appear in the cyclized test vectors. These errors could result from design defects that percolated through the cyclization process, or they may have resulted from the cyclization process itself, or they may result from corner cases that the original design did not take into account. Whatever the reason, the PSV process must identify them and correct any errors.

Correcting test-pattern errors. When errors are detected during the pattern validation process, they must be corrected through manual or a combination of manual and automated methods. Engineers can manually review test patterns to identify errors, analyze failing test patterns, examine response traces, perform debugging and diagnosis, and modify the stimulus pattern, the expected response pattern, or both. Alternatively, automated tools can analyze failing test patterns and generate reports making recommendations for correcting errors based on predefined rules.

Using automated parallel test stations to speed up the process

With or without automation, the process discussed above is time-consuming. Speeding up the process requires a test lab with the equipment necessary to run parallel pattern validation, thereby minimizing the time spent on pattern debugging while assuring sufficient test coverage. A solution such as the Advantest V93000 EXA Scale EX Test Station, an engineering platform for complex device bring-up that supports structural and functional test, provides such parallel test capability without requiring a lot of floor space because it is designed to fit under the company's single-site M4171 automated handler. Complete with integrated active thermal control (ATC) over a -45 to +125°C range, the handler brings automated device loading, unloading, and binning into the laboratory environment. As shown in **Figure 1**, six test cells can fit within a 5m by 5.5m laboratory space.

Bridging pre-silicon verification and post-silicon

An engineering lab with automated, parallel test stations can significantly enhance the test engineering process where the typical test content is dominated by structural test. However, while the structural test is the foundation for systematic test coverage according to targeted fault models, there is a growing need for functional tests to reach high-volume readiness.

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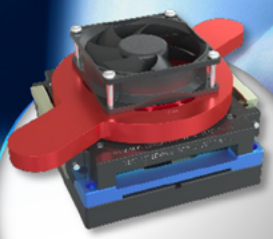

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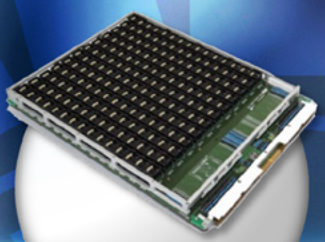

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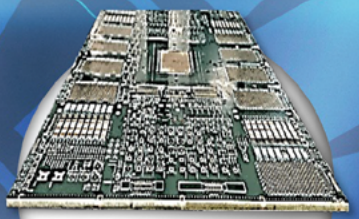

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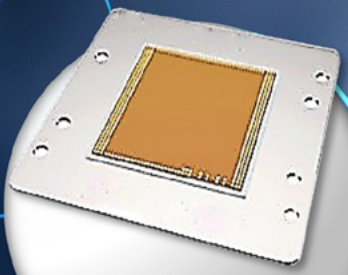

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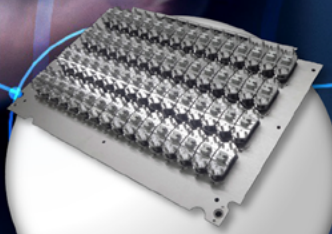

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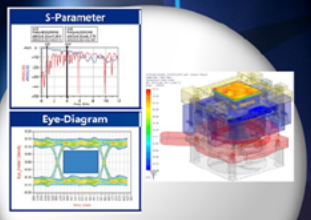

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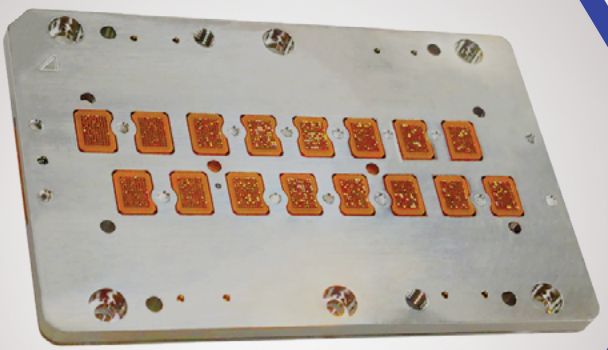

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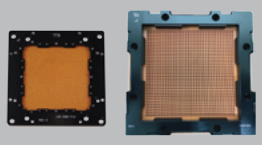

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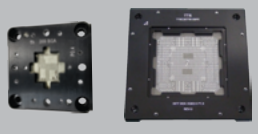

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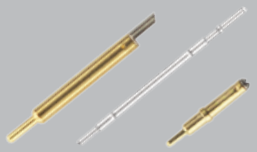

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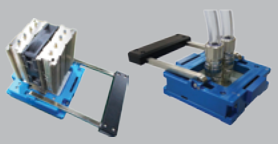

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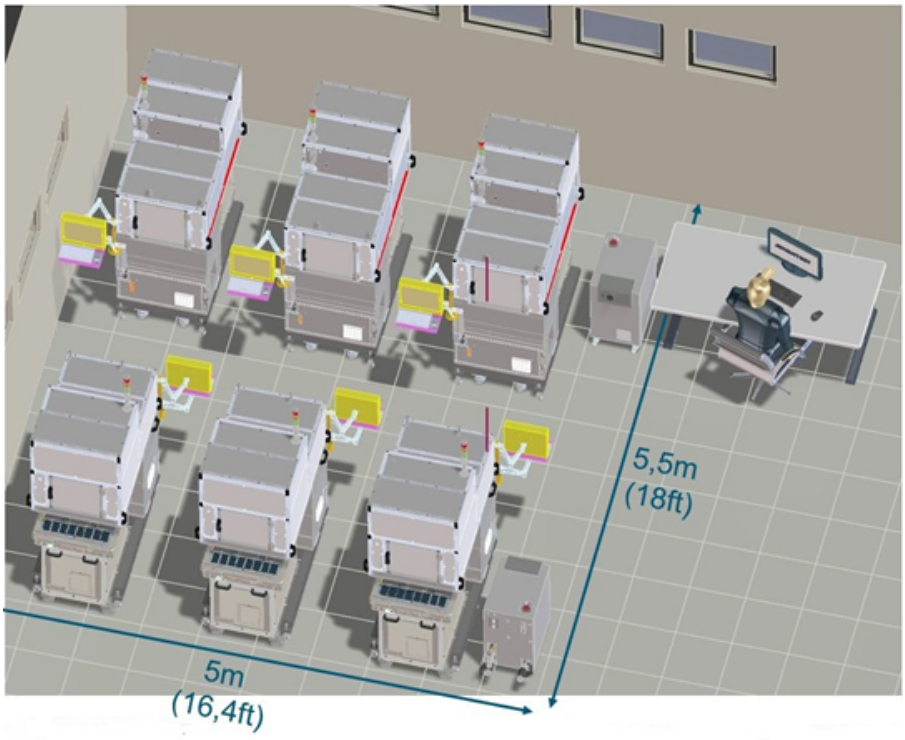

Figure 1: Six EX Test Stations with M4127 handlers fitting within a 5m by 5.5m laboratory space to speed up test-pattern validation and other engineering tasks.

Accordingly, there is a trend for an increasing amount of functional tests.

The challenges involved in creating functional test on ATE can be summarized in two major categories. First, the need to convert the functional test content into a production test vector pattern requires tooling and extensive development time. Second, on a typical ATE, there is no native software debugging environment, making it very difficult for the test case developer to debug any issues in support of the test engineer. Excessively long, unpredictable debug cycles are inevitable. That is where pre-silicon methodologies and an ATE instrument can work together to seamlessly and interactively validate the functional test content to help to meet these challenges.

Introducing the PSS standard

The transition from the pre-silicon verification stage to first silicon—involving bring-up, bare-metal test execution, and the ATE stage—can be greatly smoothed through the reuse of pre-silicon verification test content. To that end, the Accellera Systems Initiative, an organization focused on the creation and adoption of EDA and intellectual property (IP) standards, has promulgated the Portable Test and Stimulus Standard (PSS), which specifies a single representation of stimulus and test scenarios that span simulation, emulation, and post-silicon [2].

Linking the EDA and ATE communities

A result of PSS is that the once-siloed disciplines of the EDA and ATE communities can work together. Barriers remain, however. Structural test dominates the ATE side, but rising quality expectations are driving a need for more functional test to ensure the chip will perform properly in its end application environment or mission mode. However, as previously mentioned, converting functional test content into production test vectors requires extensive development time, and a typical ATE system lacks a native software debugging environment that could speed up the process [3].

Proposed solutions to handling functional test content

A solution would involve meeting one or more of the following requirements: 1) seamless software-driven execution of unconverted functional test content on the ATE; 2) ATE hardware that supports high-speed I/O (HSIO) communication; 3) enhanced functional coverage closure using constraint random test content; 4) a native software debugging environment instead of vector-pattern compare and error reporting; 5) or an enhanced PSS scenario analysis to observe how varying test conditions impact PSV.

PSS implementation

A joint cooperative initiative between Cadence and Advantest involved a combination of the PSS and HSIO approaches. The companies have developed a solution that involves PSS-based test content creation, an interface to ATE software, the loading of parameterized test content, test execution on ATE hardware, and debug and analysis (**Figure 2**). The solution begins with the Cadence Perspec System Verifier, which automates the process of extending the PSS models used in pre-silicon validation to the ATE environment, reducing the complex use-case scenario development time. A container file labeled FDAT in **Figure 2** provides an efficient interface between Perspec and the Advantest SmarTest 8 software for its V93000 ATE systems.

Interacting natively with DUT with no cyclization

Continuing with the process noted in the previous section, Advantest's new Link Scale ATE instrument interacts natively with the DUT using low pin-count HSIO, such as USB and PCI Express interfaces running in full-protocol mode, without pattern cyclization. Collected test traces can be viewed in a SmarTest viewer or imported into Cadence's Verisium Debug AI-powered debug tool for correlation with the original PSS tests. In addition, Link Scale can host embedded software debuggers such as the Lauterbach TRACE32.

Device validation best practices

The process outlined in **Figure 2** can significantly ease the burden of the post-silicon activities but not eliminate it. Not all DUTs will have HSIO channels for the delivery of test patterns without the necessity of converting them to cyclized test vectors, or not all functions

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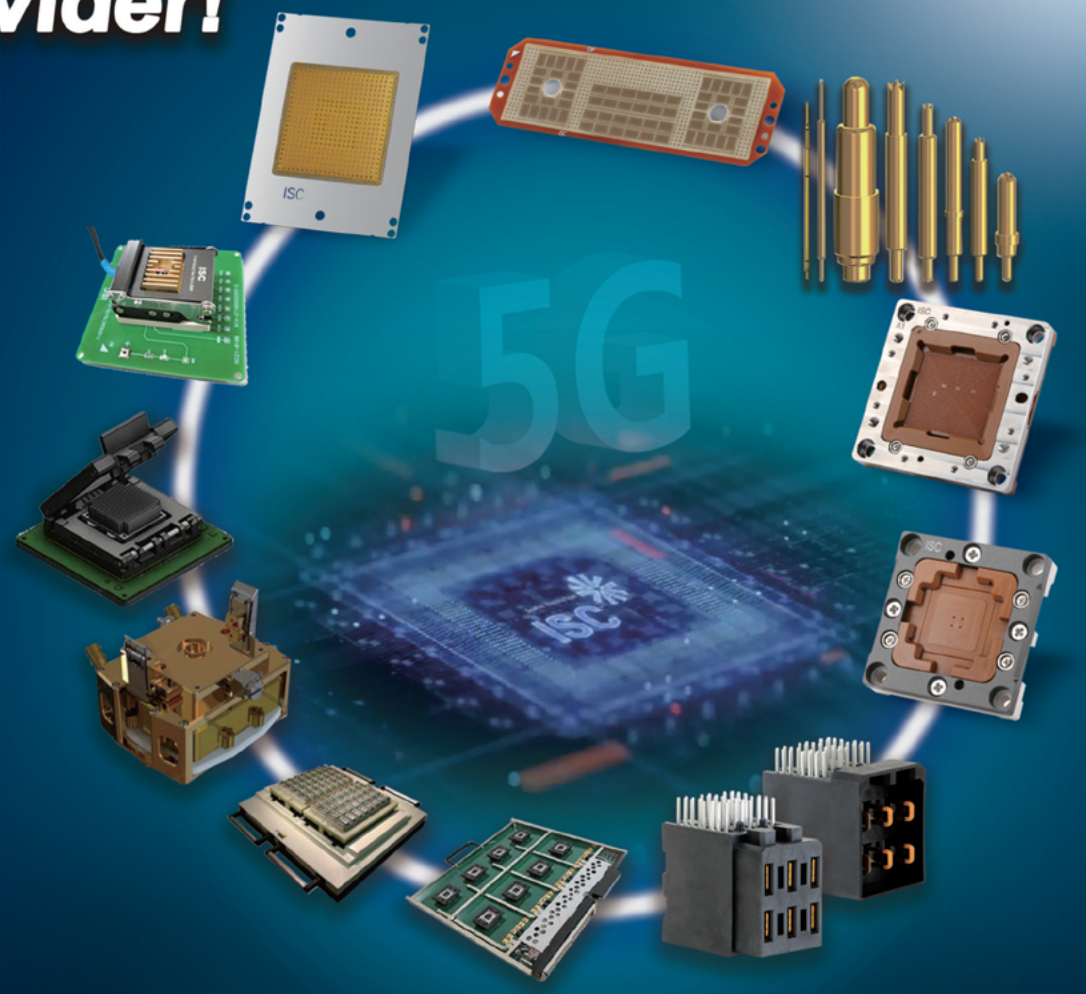

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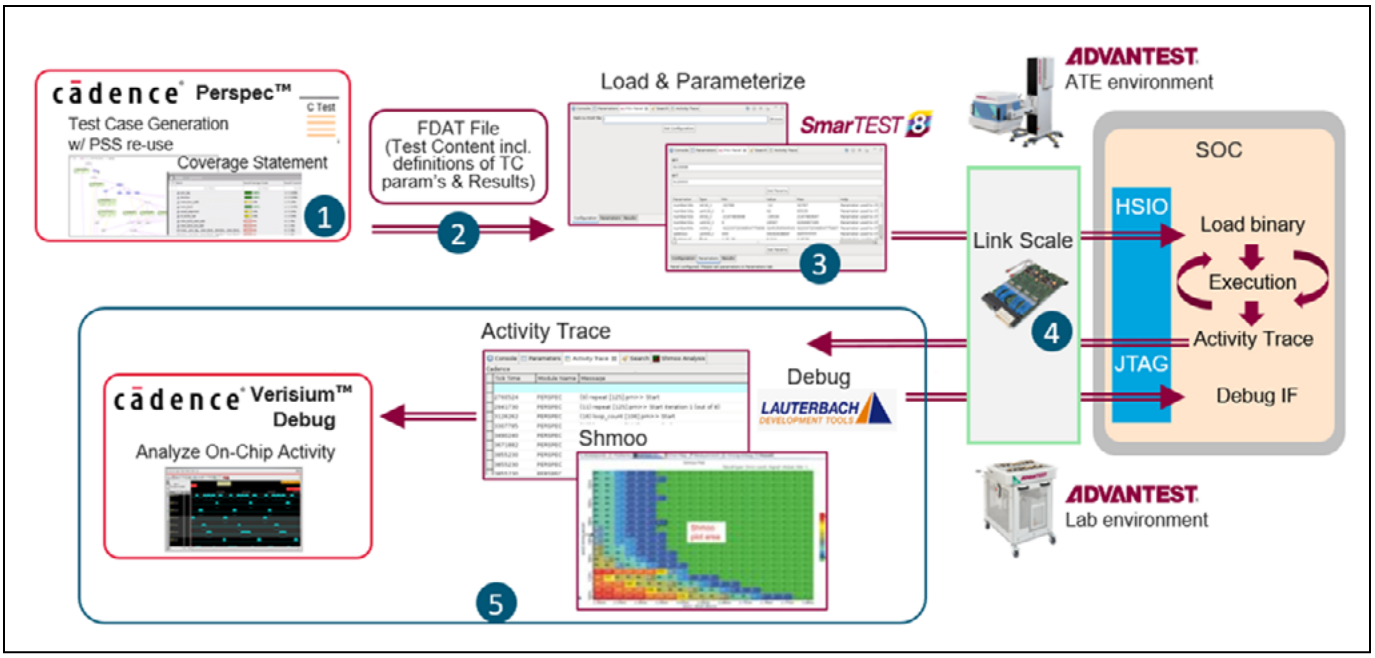

Figure 2: PSS enables the interfacing of EDA and ATE domains.

of a DUT with HSIO will be able to be accessible to test instruments through HSIO ports in mission mode. Consequently, the need will remain and even grow for engineering test laboratories populated by automated, parallel single-site test stations.

Going forward, one key will be smoothing the transition from the lab environment with engineering test stations to the production floor. One example is the single load board strategy, in which a multisite load board for high-volume production can be used in the lab with only a single site enabled, making it unnecessary to develop one board for engineering activities and another for high-volume manufacturing (HVM). The engineering environment should be as close as possible to the HVM environment, and the EX Test Station achieves this goal because it uses our Xtreme Link technology. The station is also suitable for testing initial engineering batches efficiently.

Summary

The semiconductor industry has a long and successful history of testing increasingly complex devices, continually enhancing structural, functional, and system-level test to minimize test escapes. Advances continue as the industry contends with an exploding amount of test data necessary for silicon bring-up, PSV, and other test engineering tasks. A key innovation is a laboratory equipped with engineering workstations that can operate in parallel to speed up tasks such as pattern validation. In addition, EDA and ATE companies are cooperating to leverage standards such as PSS to bridge the pre- and post-silicon verification stages, and they are leveraging HSIO to allow ATE to apply test patterns without cyclization. Finally, engineering workstations are incorporating the load-board, compute, and communications technologies of production ATE systems, thereby speeding the transition from the lab to HVM.

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Biography

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Foundry 2.0: A renaissance in innovation

By Bob Patti [NHanced Semiconductors]

Our society craves customization. We all want clothing, cars, and phones that fit us and our personal usage styles. In semiconductor hardware, however, customization has become prohibitive. How did the industry get here? What can be done to revive innovation in high-end chips? This article discusses a new business model called Foundry 2.0.

Remembering the "Golden Age"

The 1980s and 1990s saw a golden era of custom integrated circuits (ICs). New gate arrays, or even standard cell custom devices, were relatively inexpensive. A startup company could develop a new chip and go to market for 10 or 20 million dollars. New devices and intellectual property (IP) thrived in the market. Individual companies developed and tuned their own semiconductor products. Moore's Law was in full swing and roomfuls of 1970s electronics became desktops, laptops, tablets, and personal digital assistants (PDAs).

The rise of the SoC

Since the "Golden Age," transistors have shrunk from 1µm to 2nm while wafers grew from 200mm to 300mm, providing more dies per wafer and vastly more transistors per die. Cell phones now routinely outperform the personal computers (PCs) of the 1990s. Key to this progression was bundling ever larger groups of functions into system on chip (SoC) devices to reduce cost, power, and size. These improvements were largely enabled by reduction in wire size and length. Cumbersome chip-to-chip wiring and electrostatic discharge (ESD) structures were replaced by elegant on-chip communication. Today's one-size-fits-all SoCs are the result.

However, progress on the path described above has slowed to a crawl. Absorbing more features into an SoC no longer translates reliably into cost, power, and size improvements. Why? Because advances in wiring have fallen far behind advances in transistors.

Wiring limitations are imposed by the limits of process technology and by basic physics. Today's wires are too small to be made with smooth edges; the structures look as if they were drawn with a crayon. Electrons bounce and scatter off these ragged edges, seriously impacting signal speed. At the same time, scaling draws wires closer together and they become more resistive. Wire proximity also adds to capacitance and, therefore, energy consumption. For all of these reasons, wires consume most of the power and most of the delay at very small nodes; transistors take a tiny portion of both budgets. Wires are the root of the problem with continued scaling.

The current business model: Foundry 1.0

As feature sizes have shrunk, development and factory costs have risen to staggering heights. Stark economic realities force today's fabs to echo Henry Ford's famous quote, "Any color the customer wants, as long as it is black." Certainly, software provides a level of customization, but hardware inflexibility

requires that customers shoe-horn big field-programmable gate arrays (FPGAs) or multi-function SoCs into their applications. These one-size-fits-all chips provide workable solutions, but they typically contain millions of transistors that the application doesn't need and never uses. They take up more space, consume more power, and run more slowly than a sleek, well-tuned custom chip.

Today, IC development costs range into the billions. Developers are scarce and are increasingly averse to risks in technology, design, or market. Innovation is always risky, and is therefore highly constrained in this environment. Customization is nearly impossible; diverting precious resources to address a niche customer carries an enormous opportunity cost that no leading-edge fab is willing to accept. We are at the end of the road for the semiconductor business model driven by Moore's Law.

Of course, the existing Foundry 1.0 model is extremely efficient and effective. It runs uniform, well-proven processes and produces vast numbers of identical devices with tremendous economies of scale. It seems highly unlikely that a technology breakthrough will fundamentally alter this model. The best answer is to not change the reliable and successful Foundry 1.0 model, but to build upon it.

Fostering a resurgence: Foundry 2.0

The Foundry 2.0 model aims to stimulate innovation via advanced packaging and additive semiconductor manufacturing, using current semiconductor production as feedstock. Under Foundry 2.0, the existing semiconductor plants will use their formidable production model to build chiplets—disaggregated "LEGO® blocks" of today's existing SoCs—while new, smaller fabs perform additional cleanroom processing on these chiplets to produce low- to mid-volumes of finished devices.

Just as SoC benefits came from eliminating chip-to-chip wiring, Foundry 2.0 will use advanced packaging to reduce chiplet-to-chiplet wiring. Advanced packaging interconnect (wire) is as good as, or even better than, wiring within a modern SoC; this breaks the chip-to-chip wiring barrier. Combining separately manufactured chiplets frees us from the tyranny of forcing everything into one chip and one fabrication flow. The "LEGO® blocks" that were combined in an SoC can be taken apart again and selectively assembled in various advanced packages. New combinations of blocks are possible. Non-essential blocks are simply left out. Lean, swift, single-function chiplets are wired together into flexible, cost-effective solutions. This changes everything—a new era of semiconductors is born.

Foundry 2.0 is best viewed as a toolbox of technologies and processes to integrate chiplets and create customization by adding materials or unique processes on top of Foundry 1.0 produced dies or wafers. One tool in the toolbox is 2.5D assembly—perhaps the worst term the industry ever coined. This is side-by-side chiplet assembly on an interposer. State-of-the-art (SOTA) chiplet assembly permits high-speed pick and place of components with sub-micron accuracy onto interposers—the equivalent of yesterday's circuit boards. Interposers provide micron or sub-micron wiring. Because all the wiring is essentially on-chip, ESD structures drastically shrink or altogether disappear. Similarly, the chiplet-to-chiplet

I/O drivers on the interposer are scaled like those within an SoC. Interposers can be made of either silicon or glass; glass reduces parasitics to achieve even greater returns.

Our toolbox also has 3D assembly. Chips have been stacked for years with cascading waterfalls of wire bonds, but this is nothing like what can be done today. Directly bonding layers of circuitry and integrating them with ultra-short vertical interconnect drastically reduces the wire for faster, lower power devices.

Hybrid bonding is a vital tool in our box for either 2.5D or 3D assembly. This stacking technology allows sturdy physical assembly and seamless vertical interconnect with almost no capacitance. Hybrid bonding provides thousands to millions of ultra-short wires between layers of ultrathin full chips or chiplets, with wiring pitches of just a few microns—rivaling the global interconnect of today's leading SoCs.

A major power tool in the box is heterogeneous integration. 2.5D and 3D assembly allow our "LEGO® blocks" to be built in a vast array of materials, at different nodes, and in dissimilar process flows. The disparate pieces can nonetheless be assembled as tightly as any components in an SoC. What's more, fine-grained wiring allows assembly of completely incompatible semiconductor technologies that could never be combined in an SoC at any cost. Heterogeneous integration allows assemblies to incorporate only best-of-class components, boosting system-level performance 1000x almost instantaneously.

Dozens of other tools crowd our toolbox, including:

- Adding back-end-of-line (BEOL) memory (e.g., magnetoresistive random access memory [MRAM]) through additive semiconductor manufacturing;
- Adding magnetics for local precise high-efficiency power delivery;
- Adding thermal materials, sensor materials, etc.;
- Building optical interconnect into interposers;
- Integrating analog components;
- Incorporating custom chiplets; and
- Applying non-standard processes.

An intriguing possibility is the revival of the Sea of Gates. This concept imagines building vast arrays of undifferentiated transistors. Functionality is not built in with the transistors, but created by the wiring layers in the BEOL. Manufacturing the transistor layers would be extremely efficient, as all dies would be completely identical—only the BEOL would differ. This promising idea fell by the wayside with the dominant rise of the SoC. A Sea of Gates incorporates nothing but

digital transistors; an SoC contains memory, modems, and analog and mixed-signal elements. SoC flexibility overpowered the elegant Sea of Gates approach. But now, in chiplet designs, digital transistors can once again be conveniently separated from all other components. High-volume foundries could manufacture immense numbers of identical Sea of Gates chiplets to be differentiated by wiring.

Let's talk about money

While the gains in power, size, and performance are exciting and may be compelling enough in many applications, the elephant in the room is cost. Foundry 2.0 must provide a fundamental cost benefit to the end consumer.

Today's massive SoCs can cost hundreds of millions to design. The factories that manufacture them are measured in tens of billions. By comparison, Foundry 2.0 technologies generally run in the ~1µm range—a more forgiving node. Development nonrecurring engineering (NRE) costs are likely to be measured in hundreds of thousands of dollars. The leading edge of high-speed, high-volume manufacturing is just now catching up to the chiplet revolution; as it gains traction it will drive costs far down, enabling affordable mass market opportunities for chiplet-based semiconductor devices.

The new opportunity

Foundry 2.0 gives leading-edge fabs a valuable point of entry to niche markets that are currently untapped. By disaggregating their powerful SoCs into chiplets, fabs will create state-of-the-art components that customers will eagerly incorporate into their assemblies. Foundry 1.0 will thereby participate fully in Foundry 2.0, penetrating lucrative custom markets without disrupting the high-volume business model.

A new niche opens for smaller fabs that do not build any transistors, but focus on the value-added technologies discussed here. These factories would be 10-100x less expensive to build and equip than high-volume transistor factories. Their business model would target high-mix, high-touch, low- to mid-volume manufacturing. Importantly, they would not compete with the industry giants at all. A modest BEOL and advanced packaging fab could cooperate under nondisclosure agreements (NDAs) with big foundries that compete fiercely with one another. As an utterly neutral party, the smaller fab would enable assemblies that are truly heterogeneous in every sense, assembling chips or chiplets from multiple sources.

Summary

In summary, innovation has been stifled by the high cost risk of developing SOTA SoCs. New semiconductor startups have virtually disappeared because a first-try product requires hundreds of millions of dollars. In this high-stakes game, investors are unwilling to fund anything but slam-dunk investment unicorns. Foundry 2.0 changes all of this. With chiplets, advanced packaging, and additive semiconductor manufacturing, it will be economically feasible to develop new devices; risk taking will again become possible and startups will be created for millions, or at most a few tens of millions. Innovation looks bright again under Foundry 2.0. Perhaps a new "Golden Age" is on the horizon.

Biography

Robert (Bob) Patti is President of NHanced Semiconductors in Batavia, Illinois. He helped design over 100 chips at his first semiconductor startup, ASIC Designs, and later founded Tezzaron Semiconductor to develop 3D wafer stacking. His latest company, NHanced Semiconductors, looks to drive the rise of Foundry 2.0. Bob received the 2009 SEMI Award for North America for his pioneering work in 3D IC integration as well as the 2015 3DIncites Individual Achievement Award. Email rpatti@NHanced-semi.com

A pioneering and successful academic-industry model in integrated systems packaging at Georgia Tech

By Rao R. Tummala [Georgia Tech]

Many industry-university models have been developed globally in electronics over the last five decades to improve the effectiveness of the academic community, to serve the needs of the local industry, and to contribute to the competitiveness of the applicable country. Academic universities are known to perform highly-innovative research—but that research hardly ever ends up in products. Industry, therefore, performs its own R&D, independent of academic R&D, to address the so called "valley of death" between academic R&D and the industry's manufacturing needs.

Asian and European countries created national industrial institutes like the Industrial Technology Research Institute (ITRI) in Taiwan, the Institute of Microelectronics (IME) in Singapore, and the Fraunhofer-Gesellschaft in Berlin, Germany to address the valley of death. Except for imec (Belgium), most industrial institutes focus on short-term technology development in partnership with industry to transfer developed-technologies into manufacturing. In the U.S., no such institutes exist as bridges. Companies work directly with universities, mostly for purposes of training an educated workforce. The National Science Foundation Engineering Research Center (NSF ERC) is the best example of all government-funded programs in the U.S. that attempts to close the gap between academic institutions and industry—it starts with the basic research and tries to couple to the industry. The Semiconductor Research Corporation (SRC) was created in the USA, but its focus is more strategic R&D, funded by the industry, and the R&D takes place at universities.

Georgia Tech Packaging Research Center (GT PRC) is an example of how universities can perform leading-edge next-generation strategic R&D, educate massive numbers of students, and co-develop all the technologies necessary for the next-generation of computing, communication, automotive and consumer systems, and ready them for commercialization. This paper is about how we created an innovative and successful academic/industry model while developing glass-panel packaging from concept to commercialization. The result was leading-edge packaging for high-performance computing and artificial intelligence (AI), 6G and beyond communications, and automotive and consumer electronics. How this was accomplished is the basis of the new model described in this article.

Setting-up the Packaging Research Center

The model we set up is very different from the other models used by the organizations listed above. The GT PRC started as an NSF ERC with a system-on-package (SoP) vision I defined, which was in contrast to the system-on-chip (SoC) vision widely practiced in the industry.

Georgia Tech is top ranked and the largest academic engineering institute in the U.S. As such, it has a very large group of faculty and many, if not all, engineering departments, have state-of-the-art facilities. In semiconductors, it has an extensive facility called IEN, Institute for Electronics and Nanoelectronics. Within that, it has many centers including the Packaging Research Center (PRC) created by me when I joined Georgia Tech in 1993, after 25 years at IBM where I developed leading-edge packaging, now called chiplet or 2.5D. This technology integrated up to 144 small chips including logic, memory and capacitor devices, on very large, 127mm substrates. The substrate was the industry's first low-temperature co-fired ceramic (LTCC), now an industry standard that is used in all radio-frequency (RF) applications.

The NSF ERC I started is the flagship program that funds transformational technology concepts, such as the exploration and development of three major programs simultaneously, described below.

Explore and demonstrate SoP. This program was in contrast to the use of SoC packaging, which was being pursued by the industry at the time.

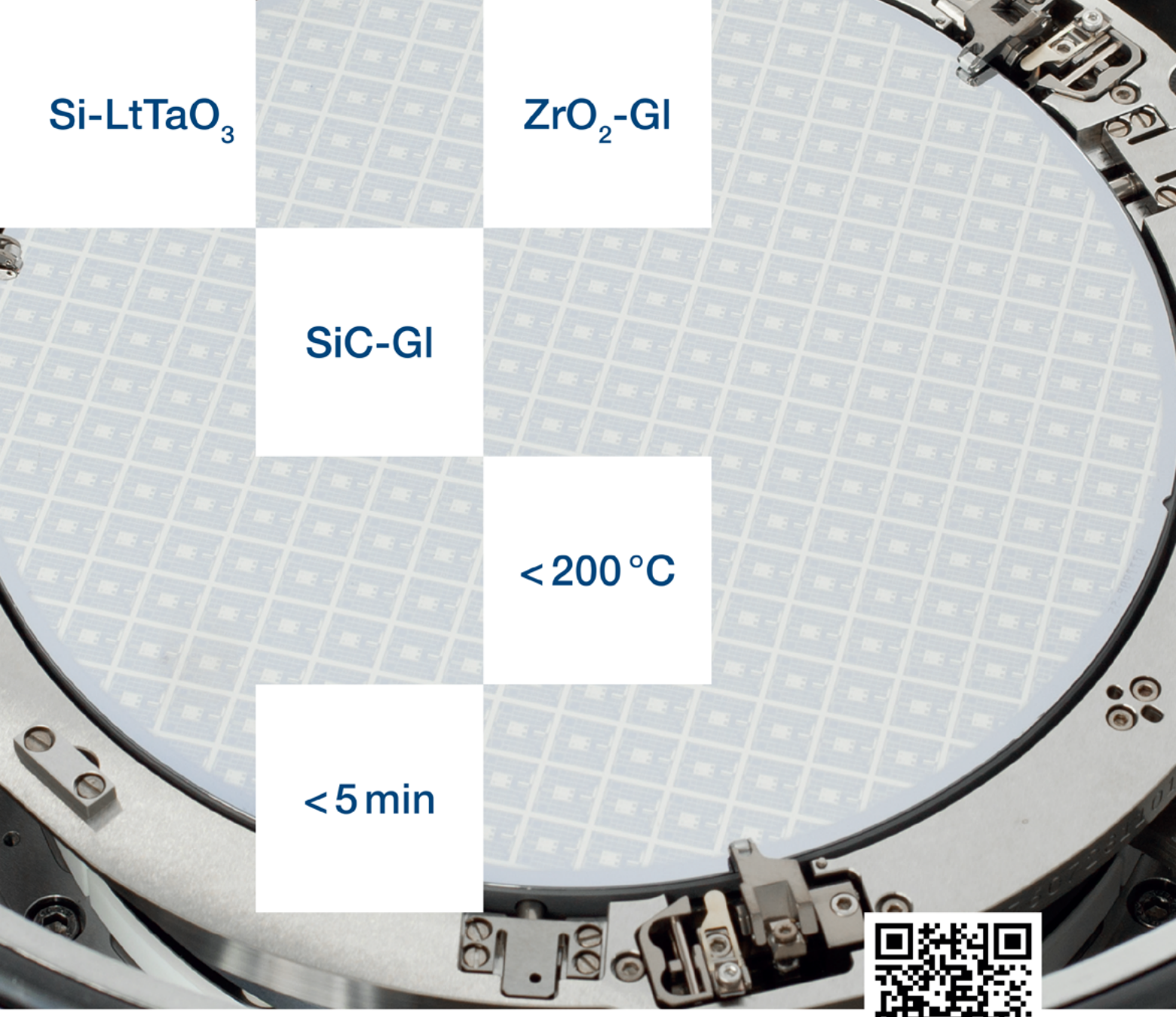
Develop educational programs. A large number of educational programs, including both classroom and hands-on courses, were developed along with curricula and textbooks. A large number of interdisciplinary students participated at the BS, MS and PhD levels.

Set up and demonstrate a large global industry consortium. It was essential to gather a large number of researchers, developers, manufacturers and users, all working together to co-develop next-generation systems technology, ready for manufacturing in an accelerated mode.

Two-part R&D strategy with two R&D teams

U.S. universities are viewed as the best and most innovative in the world for leading-edge R&D. But their impact on developing and transferring technologies ready for commercialization has been minimal. In Asian and European countries, this problem has been addressed by universities performing research and industrial institutes performing technology development in partnership with, and funding from, the industry, thereby building upon academic advances.

Georgia Tech PRC divided R&D into two parts described in the sections below.



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Advancing individual core technologies by faculty and students. Very much like other universities, we focused on advancing core technologies. However, we placed the focus on next-generation strategic technologies for the industry. We identified and developed 12 core strategic technologies.

Integration of core technology advances into sub-system prototypes. We refer to sub-system prototypes as design and demonstrate (D&D) system prototypes—these prototypes integrate advances in each of the 12 core technologies, using pilot line facilities. Typical universities cannot achieve this level of integration. The reasons for this are many and include faculty expertise in one discipline, lack of pilot line facilities, lack of program management experience, and a lack of motivation for industry projects. Faculty, typically, are single-disciplined and within that they are experts in one area, but with phenomenal depth. A leading-edge system prototype requires knowledge in many, many areas in electrical, mechanical, chemical and materials engineering.

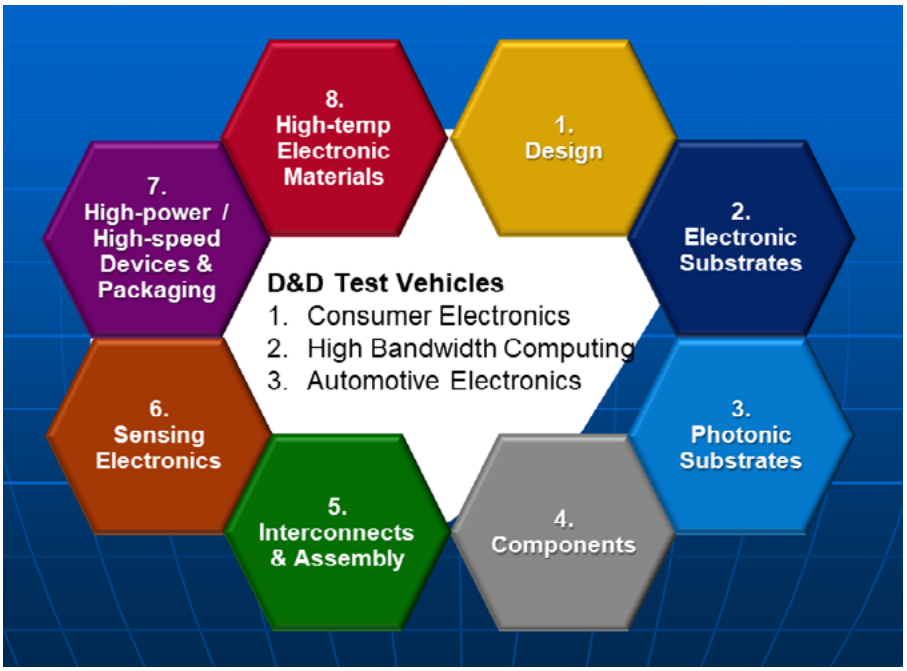

Figure 1: Two parts to R&D: academic and industry.

We addressed the challenges noted above by creating a global industry consortium consisting of all supply-chain companies from users to developers to material, process, and tool manufacturing companies, and users. Each of these companies paid a membership fee and, in addition, assigned one or more of their engineers to work with Georgia Tech PRC either on campus or off campus for up to three years. GT PRC quickly learned the need for industry-like system-level engineers, just like in manufacturing companies, to work as the program managers to manage D&D prototypes. Such program managers take advances developed by faculty and students, and then by using on-campus industry engineers as project managers, they develop synergy with other global industry partners. The D&Ds, therefore, included not only faculty and their students, but also industry engineers and full-time research faculty. Figure 1 conveys this two-part strategy.

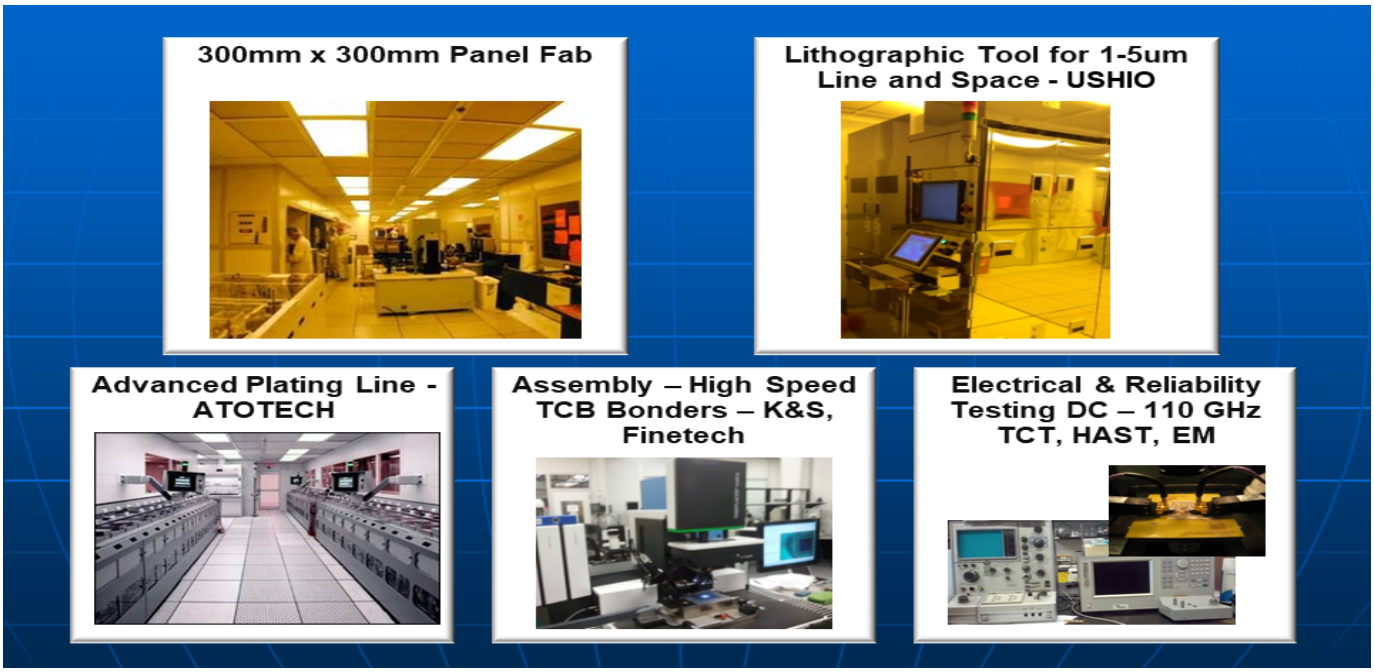

Figure 2: State-of-the-art 300mm panel pilot line cleanroom facility.

Cleanroom 300mm panel pilot-line facilities

Traditionally, universities buy and set up individual pieces of table-top equipment to perform experiments. The results from these experiments are not scalable to manufacturing, therefore, further technology development and qualification are required.

Using 300mm panel tools and facilities, we set up an entire pilot line from design to substrate fabrication, to assembly, test, reliability and metrology (see Figure 2). These facilities are designed to be used in such a way as to function both as basic R&D and system demonstration test vehicles, and to educate students in inter-disciplinary system-level R&D as well as in the industry's culture.

Interdisciplinary-individual education

In contrast to traditional education in a single discipline, I accepted incoming students into the GT PRC program from either electrical, mechanical, materials or chemical engineering disciplines, but the outgoing students are system-level interdisciplinary engineers. This is enabled by the

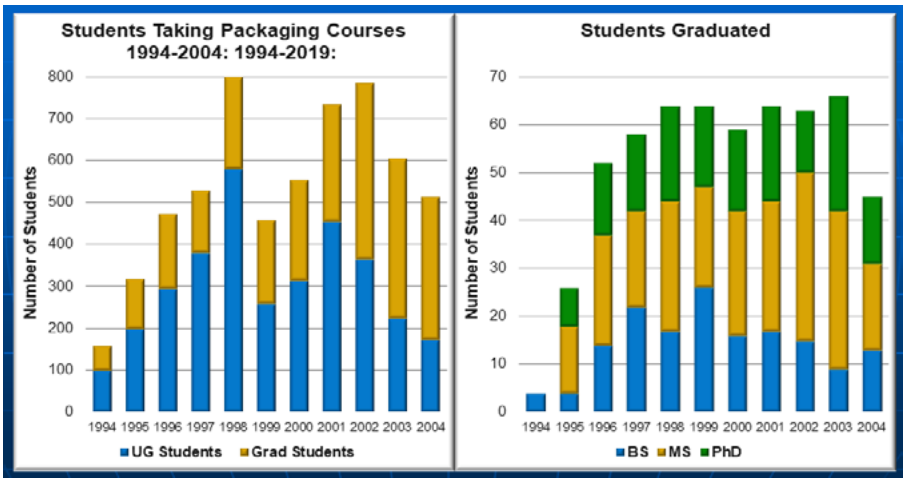

Figure 3: Students educated in the classroom: 5,870 (1994-2004); total: 10,600. Total students educated with degrees: 560 (1994-2004); total: 1,020 (1994-2019).

D&D program, described above, requiring that each student design, fabricate, assemble and characterize their prototypes and in so doing, the students became interdisciplinary students. Each student, in addition, took many courses including system courses and hands-on courses.

Over a 30-year period, GT PRC produced approximately 1,000 PhD, MS and BS students. The breakout is as follows: 560 students between 1994-2004 during the NSF ERC period, and approximately, another 450 between 2004 and 2019. The Center also produced more than 10,000 engineers who took one or more of 20+courses in systems packaging courses taught by more than 20 faculty at Georgia Tech (see Figure 3). Additionally, GT PRC published three textbooks, including one that introduced the concept of SoP.

Global industry consortium

All major universities have industry projects. They tend to be individual company projects. Some universities go beyond and have multiple companies fund and be involved in a single project, typically in a thrust area. Our approach is very different. Knowledge

Figure 4: Large-scale global industry consortium at Georgia Tech.

of any next-generation technology requires researchers, developers, manufacturing supply-chain companies for materials, and tools (both hardware and software), manufacturers and users. So we developed an industry consortium that spanned all of these areas globally—companies from the U.S., Europe, Japan, Korea and Taiwan are involved.

In addition to the above approach that is different from other universities, we focus on next-generation system technologies from design and architectures to materials and processes for substrates, design for reliability, design and development of thermal technologies, assembly, reliability, metrology, and all others required to make a system. This is very much like what companies do in developing their next-generation technologies. As can be seen in Figure 4, the industry consortium comprises researchers, developers, supply chain companies, manufacturers, and users from the U.S., Europe, Japan, Korea and Taiwan.

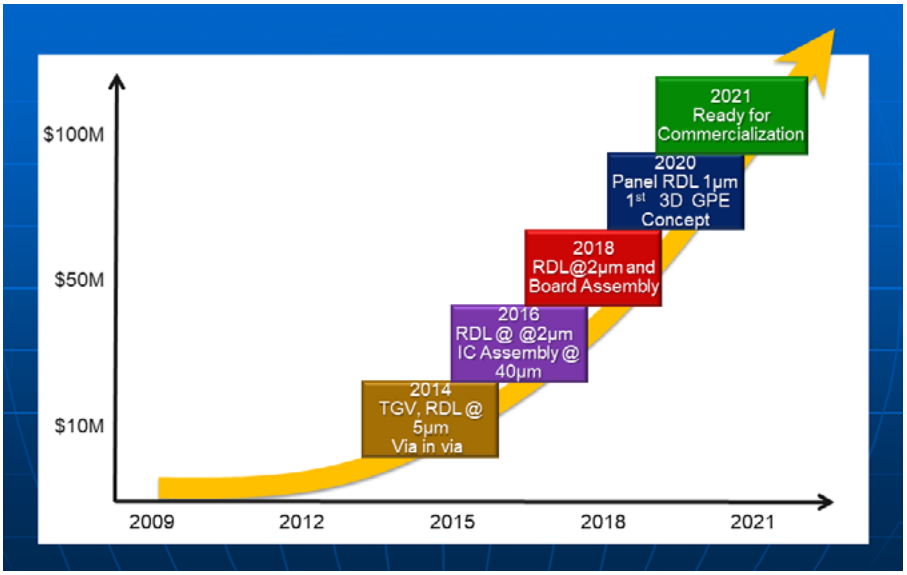

Figure 5: Georgia Tech and its partners invested $100M in glass packaging R&D to commercialization.

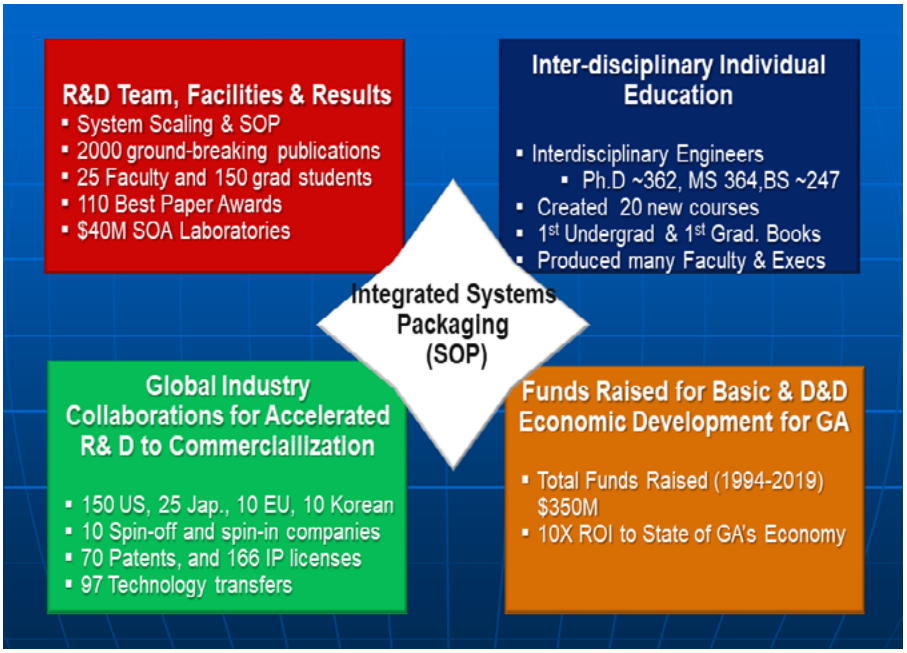

Figure 6: Impact of GT PRC in 25 years.

Results using the model

Since its inception, there have been many pioneering advances in designs and architectures, materials, processes, components and their integration into system prototypes at GT PRC. The best example that verifies the success of our model is the development of glass packaging from concept in 2009, to commercialization in 2023. Four global companies announced their plans to manufacture. They are Absolics in the U.S., DNP in Japan, Unimicron in Taiwan, and Intel, most recently.

Figure 5 shows how GT and its industry partners invested $100M and developed all the building block technologies over a 10-year period. The investments encompassed design and architectures, through-via technologies, thin-film redistribution layers (RDL), integrated circuit (IC) and board assembly, and many others. Figure 6 summarizes the impact of the Georgia Tech model in research, education, infrastructure, funds raised, and in the industry consortium.

Acknowledgments

I wish to thank all my faculty colleagues, all GT PRC students, and global industry partners who contributed to the creation and success of the Georgia Packaging Research Center and its model.

Biography

Rao R. Tummala is the founding Director and Distinguished Emeritus Professor at the Georgia Institute of Technology, Atlanta, GA. Prior to that, he was an IBM Fellow and Director of the Advanced Packaging Technology Lab at IBM. He received his PhD in Materials Science and Engineering at the U. of Illinois. Email rtummala@ece.gatech.edu

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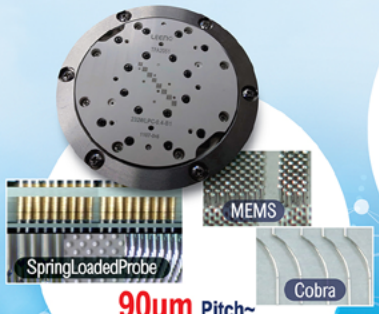
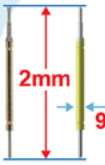


90um Pitch~ Probe Head

Tip Type

Specification
Pitch : Min.120um
Spring Force : 8.0g@ 250um
Current Rating : 1.0A
Inductance : 0.38nH

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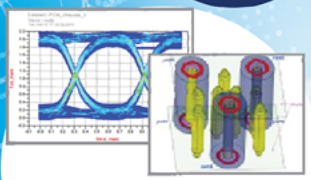
Frequency : >20GHz
VSWR : < 1.2
Automatic Coaxial Probe


5G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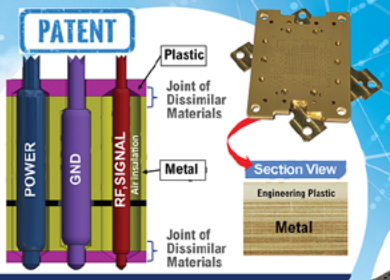
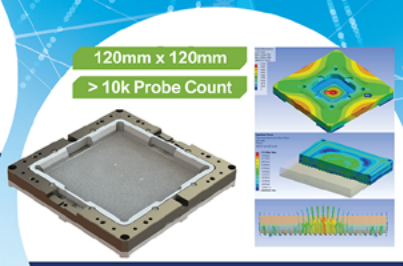
CCC Test, HFSS, TDR
Eye Diagram
4 Port VNA Test



MP Socket



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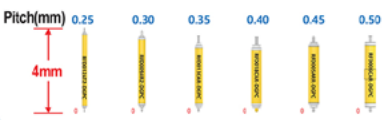

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CHIPS Act, Si-photonics among topics featured at 2023 IEEE 73rd ECTC

By Ibrahim Guven [General Chair, 2023 IEEE 73rd Electronic Components and Technology Conference and Virginia Commonwealth University]

ECTC is the premier international microelectronic packaging, components, and systems technology conference. The 73rd edition of the ECTC was held at JW Marriott Grande Lakes in Orlando, Florida, USA, from May 30 to June 2, 2023, and it was a resounding success. We had 1,619 attendees from 28 countries, the second-highest attendance in the 73 years of ECTC.

Preparation for ECTC 2023 started one year ago and was strongly supported by over 250 experts from 15 countries—members of 10 technical committees. The technical committees critically reviewed 618 submitted abstracts from industry (56.1%) and academia (43.9%), resulting in 369 technical papers. The papers, organized in 41 sessions, included five interactive presentation sessions – one of which was dedicated to students – were presented by speakers from 22 countries.

The most attended topics reflected interests in wafer/panel-level and advanced substrate technologies, large form factor dense system integration by fan out, and advancements in copper/silicon-oxide hybrid chip-to-wafer bonding. The three CHIPS Act special sessions also attracted many of our attendees. Special emphasis was also given to Si-photonics with two regular sessions and one special session. There were six talks with more than 400 attendees, ten with more than 300 attendees, and fifteen with more than 200. The most attended session averaged a whopping 417 attendees across seven talks. These attendance numbers unmistakably communicate the importance of ECTC in the packaging industry and the criticality of packaging in the overall electronics industry. Supplementing the technical program and co-located with the IEEE ITherm Conference, ECTC offered 13 CEU-approved professional development courses (PDCs).

Figure 1: Prof. Michael Manfra, Purdue University, delivering Keynote Speech and subsequent Q&A.

We were honored to have Michael Manfra, Bill and Dee O'Brien Distinguished Professor of Physics and Astronomy at Purdue University, and Scientific Director of Microsoft Quantum Lab West Lafayette, as our Keynote Speaker. Prof. Manfra (**Figure 1**) described the current state of quantum computing from a hardware perspective, listing the challenges and opportunities ranging from the basic choice of qubit platform, through scalable control and readout, to system architecture. He focused on what the packaging community can now innovate to make this revolutionary technology a reality. Following the keynote speech, a substantial Q&A session was held. Prof. Manfra's talk was captivating, inspirational, and intellectually stimulating.

This year the conference included nine special sessions and panel discussions that were very well attended and with international participation of experts and executives across the supply chain. These events (see list below) featured deep-dive discussions on technology developments, emerging applications, different perspectives, business and industry insights, and trends, as well as career, diversity and workforce development topics:

- IEEE EPS President's Panel
  - Co-chaired by IEEE EPS President Kitty Pearsall of Boss Precision, US and David McCann of Lyte, and moderated by Amr Helmy of University of Toronto on "How can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP;"
- ECTC Plenary Session
  - Co-chaired by Kevin Gu of Metawave Corp. and Ivan Ndip of Fraunhofer IZM/Brandenburg University of Technology on "Digital Transformation – The Cornerstone of Future Semiconductor and Advanced Packaging Growth;"
- IEEE EPS Seminar
  - Co-chaired by Takashi Hisada of IBM and Yasumitsu Orii of Rapidus, Japan, on "The Future of High-density Substrates – Towards Submicron Technology;"
- ECTC Materials & Processing and Thermal/Mechanical Simulation & Characterization Technical Sub-Committees Special Session
  - Co-chaired by Tanja Braun of Fraunhofer IZM, Germany, and Przemyslaw Gromala of Bosch, Germany on "Advanced Packaging and HIR for Harsh Environment – Current Status and Opportunities;"
- ECTC Interconnections Technical Sub-Committee Special Session

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TRACK 1: SiP/Design/ Manufacturing Optimization	TRACK 2: Wafer Level/Panel Level (Advanced RDL)	TRACK 3: High Performance / High Reliability	TRACK 4: Advanced Package (Flip Chip, 2.5D, 3D, Optical…)	TRACK 5: Advanced Process & Materials (Enabling Tech.)
PLANNED SESSIONS: • System Architecture, Design, & Integration • Embedded / High Voltage/ High Density • Optical • Automotive Microelectronics • Wearable Electronics • Internet of Things (IoT) • EMI Shielding • Computing & Networking Package • CPI & Modeling • Design for Reliablity/ Manufacturing • PDK Development for Packaging • System Optimization	**PLANNED SESSIONS:** • Wafer-level Fan Out / WLCSP • Advanced Fan Out & Heterogeneous Integration • Panel-level Fan Out • MEMS & Sensors • Edge Protection • Carrier Technologies • Reliability & Test • Df/Dk Loss Tangent of Dielectrics	**PLANNED SESSIONS:** • High Reliability in Defense and Aerospace • High Reliability in Automotive • MM Wave / High-speed Packaging • RF / Wireless Components • HiRel in Bio/Medical •HiRel in Extreme Environments	**PLANNED SESSIONS:** • Large Body / Small Body FC • 2.5D/3D Technologies • Optical Co-Packaging/ Photonics / Waveguides / Lasers • BUMP & Interconnect • 3D Technologies • Advanced Flip Chip • Heterogeneous Integration	**PLANNED SESSIONS:** • Substrate Technology • Polymer Materials & Processes • Novel Materials & Processes • Advanced Wirebond • Advanced Equipment for Additive Manufacturing • Flexible & Wearable Electronics
TRACK 6: **INTERACTIVE POSTER SESSION - *"Posters & Pizza Lunch"***				

Technical sessions are being planned for these tracks, and abstracts will be considered on the session topic listed below. Abstracts are rated by the technical committee members and are selected into the sessions by the session chairs appointed by the technical committee. Authors should identify their preferred session (topical area) when submitting their abstracts. Abstracts should highlight the major contributions of the work in one or more of these areas. **All abstracts submitted must represent original, previously unpublished work.**

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Figure 2: ECTC/ITHERM Diversity Panel.

Figure 3: Great networking events—never too early to start attending ECTC!

Figure 4: We are looking forward to seeing you at the Gaylord Rockies Resort and Convention Center in Denver, Colorado, USA for 2024 ECTC.

- Co-chaired by Thomas Gregorich (Infinera) and Chaoqi Zhang (Qualcomm), and moderated by Jan Vardaman of TechSearch International on "Copper Hybrid Bond Interconnections for Chip-On-Wafer Applications;"
- ECTC Photonics Technical Sub-Committee Special Session
  - Co-chaired by Stéphane Bernabé of CEA Leti, France, and Hiren Thacker of Cisco that covered "Photonic Integrated Circuit Packaging: Challenges, Pathfinding and Technology Adoption;"
- ECTC CHIPS Act Special Session
  - Co-chaired by Nancy Stoffel of GE Research, Jan Vardaman of TechSearch International, and William Chen of ASE on "Advanced Packaging Manufacturing in North America: Building the Ecosystem;"
- ECTC/ITHERM Diversity Panel
  - Co-chaired by Kim Yess of Brewer Science, Nancy Stoffel of GE Research, and Cristina Amon of University of Toronto, Canada, on "Diversifying our Technical Workforce to meet National Needs including the CHIPS Act Initiative" (**Figure 2**);
- ECTC Young Professionals Networking Panel
  - Chaired by Yan Liu of Medtronic, Inc., a networking panel focusing on career development for young professionals with the participation of IEEE EPS Board of Governors (**Figure 3**); and
- Heterogeneous Integration Roadmap (HIR) Workshop
  - o Sponsored by the IEEE EPS and chaired by William Chen of ASE, Bill Bottoms of MTS, US, and Ravi Mahajan of Intel, took place at our conference with another packed audience this year as well. Thank you to the HIR committee for bringing another excellent workshop to ECTC.

This year the ECTC hosted a sold-out lineup of 117 exhibitors in the Technology Corner and attracted a record level of industry support with 49 sponsorships and 13 media partners. This level of support significantly indicates the growing interest in advanced packaging and the vital role ECTC plays in this industry. This year's event delivered even more diversified content. Besides the highly technical content of this conference and several opportunities to learn and get insights into the latest developments and trends in microelectronics packaging, ECTC is also well known for its excellent networking events. ECTC 2023 offered over 10 receptions, gala, luncheons, and networking events.

The feedback was overwhelmingly positive, and on behalf of the entire Executive Committee, we would like to thank all our participants and contributors for their strong and continued support. Special thanks go to the Executive Committee and IEEE EPS sponsoring organization for their commitment and support in making this year a fantastic event.

Looking forward, the 74th ECTC will be held at the Gaylord Rockies Resort and Convention Center in Denver (**Figure 4**), Colorado, between May 28 and 31, 2024. The Call for Papers can be found at www.ectc.net. Abstract submission will close on October 9, 2023. Plan to attend in-person sessions, get to know new people, learn where this industry is going, and network with your colleagues!

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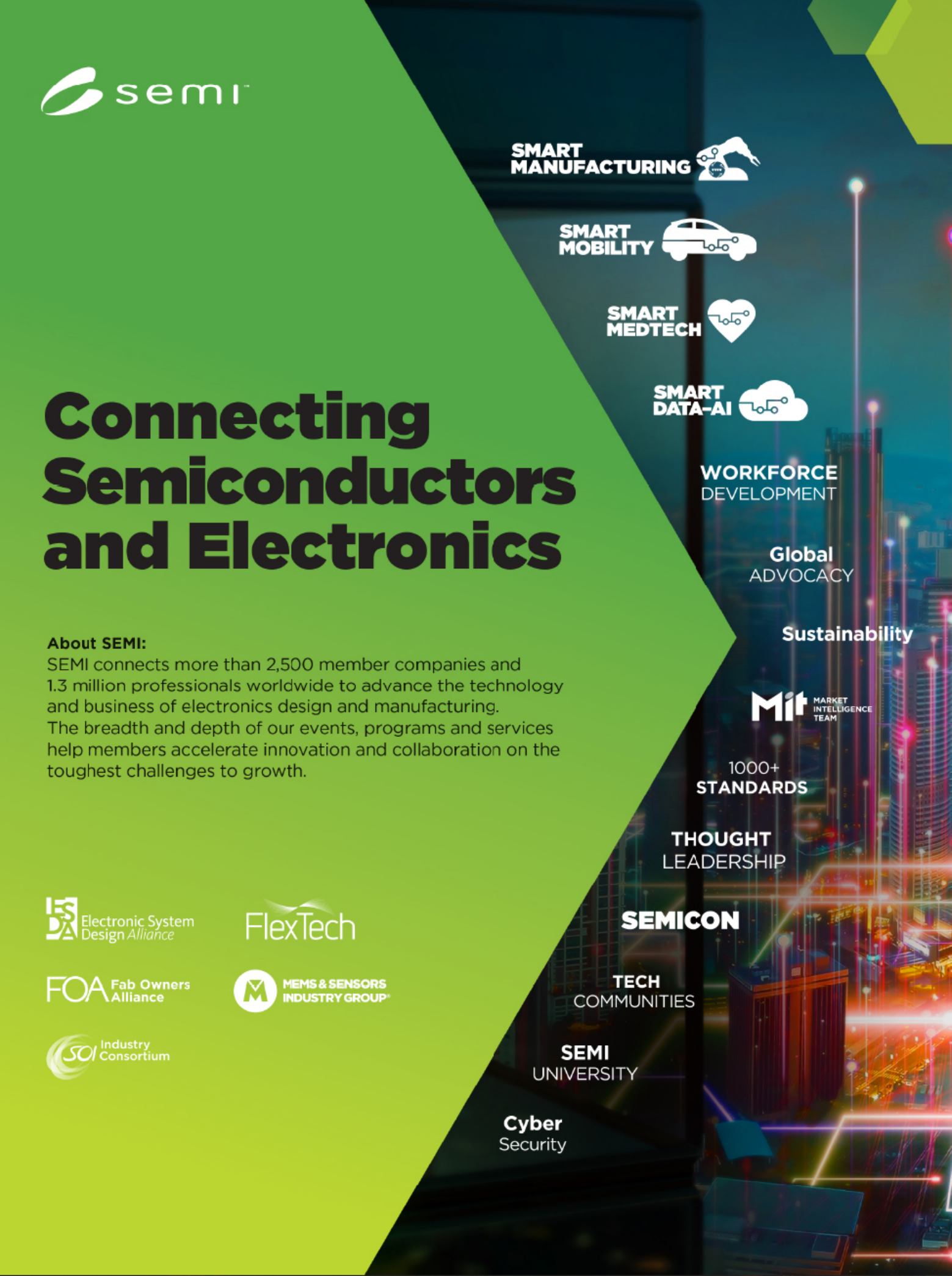
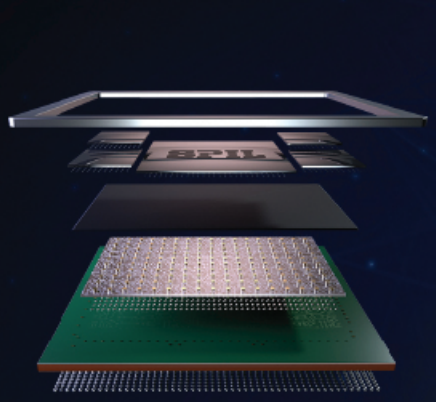
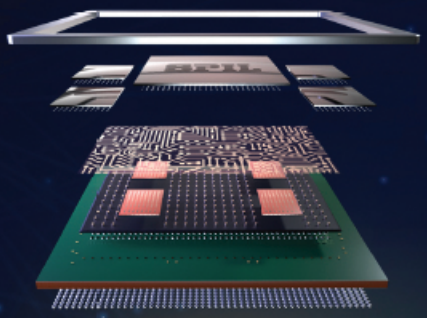


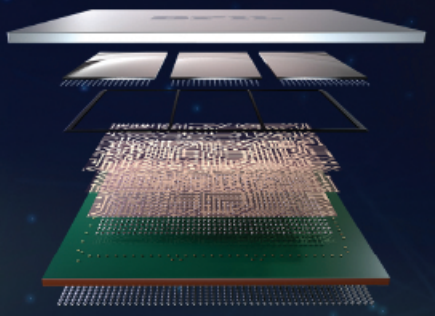
SPIL



2.5D IC



FO-EB



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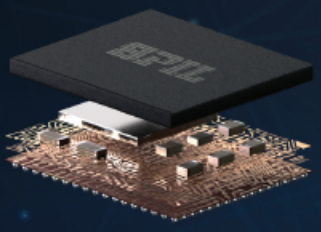

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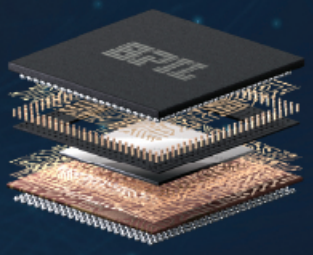

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