Chip Scale Review®

ChipScaleReview.com

The Future of Semiconductor Packaging

Volume 27, Number 3

May • June 2023

Illumination inspection technology for defect detection on advanced IC substrates

INTERNATIONAL DIRECTORY OF DEFECT INSPECTION SYSTEMS

- Slipping IC package design schedules and what to do about it
- TSV oxide etch-back optimization for the via-last integration scheme
- Achieving automated shmoo results analysis with a deep learning method
- High-performance, multi-chip leadframe package with internal connections

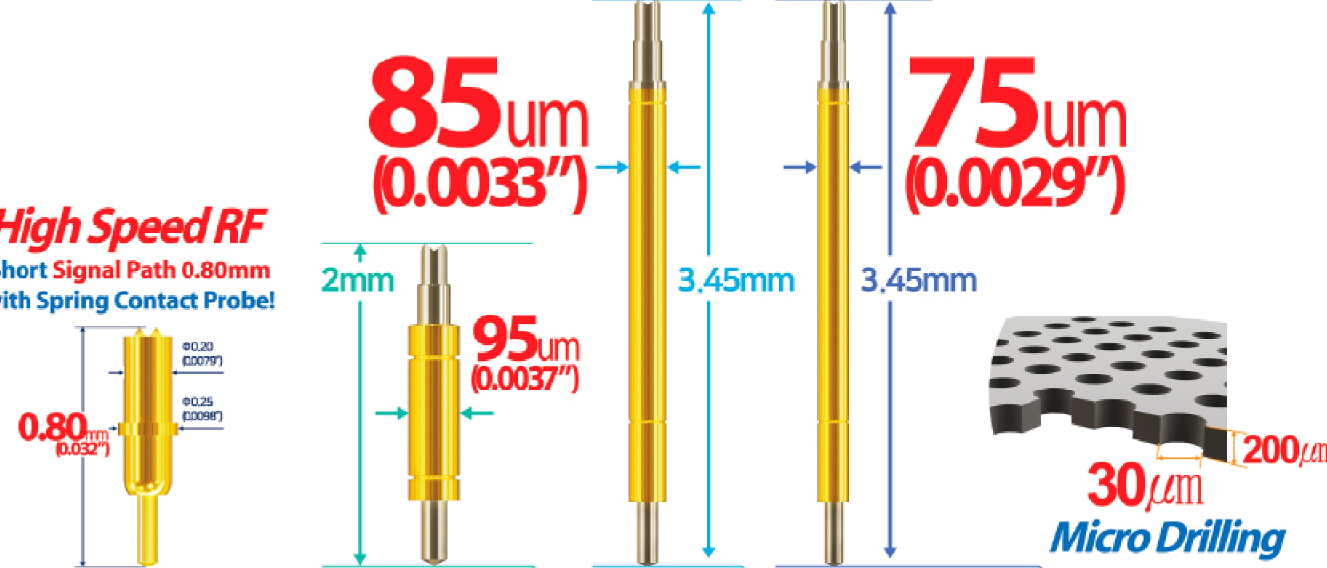
LEENO

www.leeno.com

Fine Pitch Probe & Probe Head

Continuous Non-stop Innovation!

Proven Mass Production Capability



RF-300㎛ Pitch	120㎛ Pitch	110㎛ Pitch	100㎛ Pitch

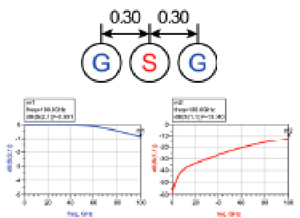
RF-300㎛ Pitch

Mechanical Spec.

- Spring Force : 0.212oz (12.0g) @ .0079 (0.20mm)
- Recommended Travel : .0079 (0.20mm)
- Full Travel : .0098 (0.25mm)
- Current Rating : 2.0A
  Material
  Barrel - Alloy / Au plated
  Plunger - Hardened BeCu / Au plated
  Spring - Music Wire / Au plated

Electrical Spec. (Simulation data)

- Propagation Delay : 7.68ps
- Capacitance : 0.05pF
- Inductance : 0.25nH
- Insertion Loss : > 100GHz @ -1dB
- Return Loss : > 100GHz @ -10dB
  (Dielectric material : MDS100)



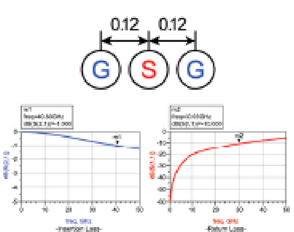
120㎛ Pitch

Mechanical Spec.

- Spring Force : 0.281oz (8.0g) @ .0098 (0.25mm)
- Recommended Travel : .0098 (0.25mm)
- Full Travel : .0118 (0.30mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation data)

- Current Rating : 1.0A
- Propagation Delay : 20.80ps
- Capacitance : 0.21pF
- Inductance : 0.38nH
- Insertion Loss : 40.83GHz @ -1.000dB
- Return Loss : 30.03GHz @ -10.000dB
  (Dielectric material : CERAMIC)



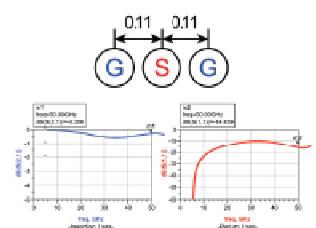
110㎛ Pitch

Mechanical Spec.

- Spring Force : 0.212oz (6.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation data)

- Current Rating : 0.9A
- Propagation Delay : 38.25ps
- Capacitance : 0.47pF
- Inductance : 0.63nH
- Insertion Loss : > 50.00GHz @ -1.000dB
- Return Loss : > 50.00GHz @ -10.000dB
  (Dielectric material : CERAMIC)



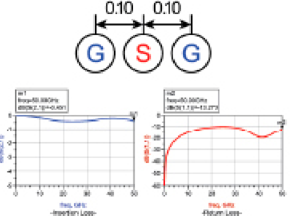
100㎛ Pitch

Mechanical Spec.

- Spring Force : 0.247oz (7.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation data)

- Current Rating : 0.8A
- Propagation Delay : 35.55ps
- Capacitance : 0.44pF
- Inductance : 0.66nH
- Insertion Loss : > 50.00GHz @ -1.000dB
- Return Loss : > 50.00GHz @ -10.000dB
  (Dielectric material : CERAMIC)



GLOBAL LEADER LEENO

HEAD OFFICE
10 105beon-gil, Mieumsandan-ro Gangseo-gu, Busan, Korea

CONTACT
USA : hskang@leeno.co.kr / +1 408 313 2964 / +82 10 8737 6561
korea : sales-leeno@leeno.co.kr / +82 51 792 5639

May • June 2023
Volume 27, Number 3

The drivers of semiconductor packaging technologies include meeting the packaging performance requirements for applications related to artificial intelligence (AI) processors, high-performance computing (HPC) and high-bandwidth memory (HBM), datacenter devices, network processors, and virtual reality devices. Related to the demand for AI and HPC are supply chain issues for advanced IC substrates. Articles in this issue offer solutions to some of these challenges.

Cover image courtesy of iStockphoto/jiefeng jiang

CONTENTS

FEATURE ARTICLES

7 **High-performance, multi-chip leadframe package with internal connections**
By DaeYoung Park, HyeongIl Jeon, GiJeong Kim, JiYeon Yang, KwangSoo Sang, ByongJin Kim, JinYoung Khim
[Amkor Technology Korea, Inc.]

15 **TSV oxide etch-back optimization for the via-last integration scheme**
By Bhesetti S. S. Chandra Rao, Hemanth K. Cheemalamarri, Darshini Senthilkumar
*[Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR)]*

23 **Illumination inspection technology for defect detection on advanced IC substrates**
By Cheolkyu Kim, Burhan Ali, JungHyun Kim
[Onto Innovation]
Jong Eun Park, Misun Hwang, Chan Jin Park
[Samsung Electro-Mechanics (SEMCO)]

Amkor Technology®
Enabling the Future

Enabling **solutions** to keep you going.

Amkor's MEMS and optical sensors offer highly scalable, small footprint packaging solutions for diverse applications enabling a smarter connected world.

amkor.com ▶ sales@amkor.com
© 2023 Amkor Technology, Inc. All Rights Reserved.

ACCELERATING 3D AND HETEROGENEOUS INTEGRATION

- Revolutionary NanoCleave™ technology enables release and transfer of ultra-thin layers with nanometer precision
- Fusion and hybrid bonding for next-generation 3D and heterogeneous integration (W2W and D2W)
- Innovative lithography and wafer bonding solutions for advanced packaging and photonics integration
- Integration Competence Centers serving as leading-edge incubation centers for customers and partners

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

Chip Scale Review®
ChipScaleReview.com The Future of Semiconductor Packaging

STAFF
Kim Newman
Publisher
knewman@chipscalereview.com

Lawrence Michaels
Managing Director/Editor
lmichaels@chipscalereview.com

Debra Vogler
Senior Technical Editor
dvogler@chipscalereview.com

SUBSCRIPTION—INQUIRIES
Chip Scale Review
All subscription changes, additions, deletions to any and all subscriptions should be made by email only to
subs@chipscalereview.com

Advertising Production Inquiries:
Lawrence Michaels
lmichaels@chipscalereview.com

Copyright © 2023 Haley Publishing Inc.
Chip Scale Review (ISSN 1526-1344) is a registered trademark of Haley Publishing Inc. All rights reserved.

Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry.
Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December.

P.O. Box 2165
Morgan Hill, CA 95038
Tel: +1-408-846-8580
E-Mail: subs@chipscalereview.com

Printed in the United States

Volume 27, Number 3
May • June 2023

FEATURE ARTICLES [continued]

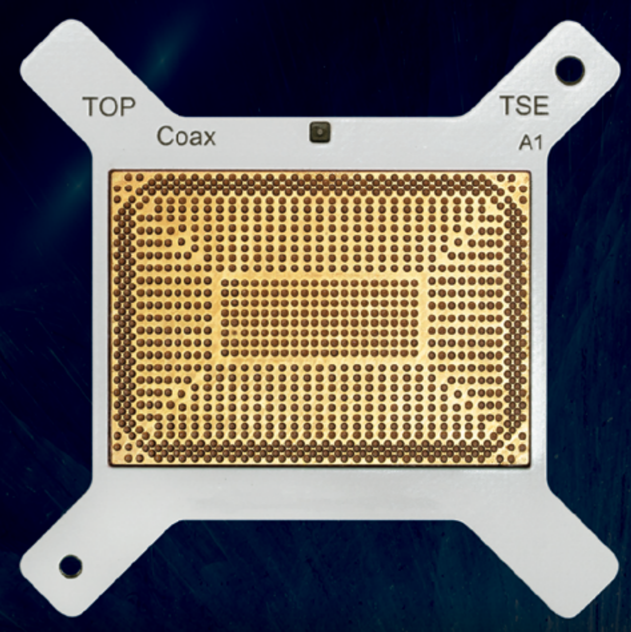
29 **INTERNATIONAL DIRECTORY DEFECT INSPECTION SYSTEMS**
By Chip Scale Review Staff

37 **Slipping IC package design schedules and what to do about it**
By Keith Felton
[Siemens Digital Industries Software]

42 **Achieving automated shmoo results analysis with a deep learning method**
By Chao Zhou
[Teradyne Inc.]

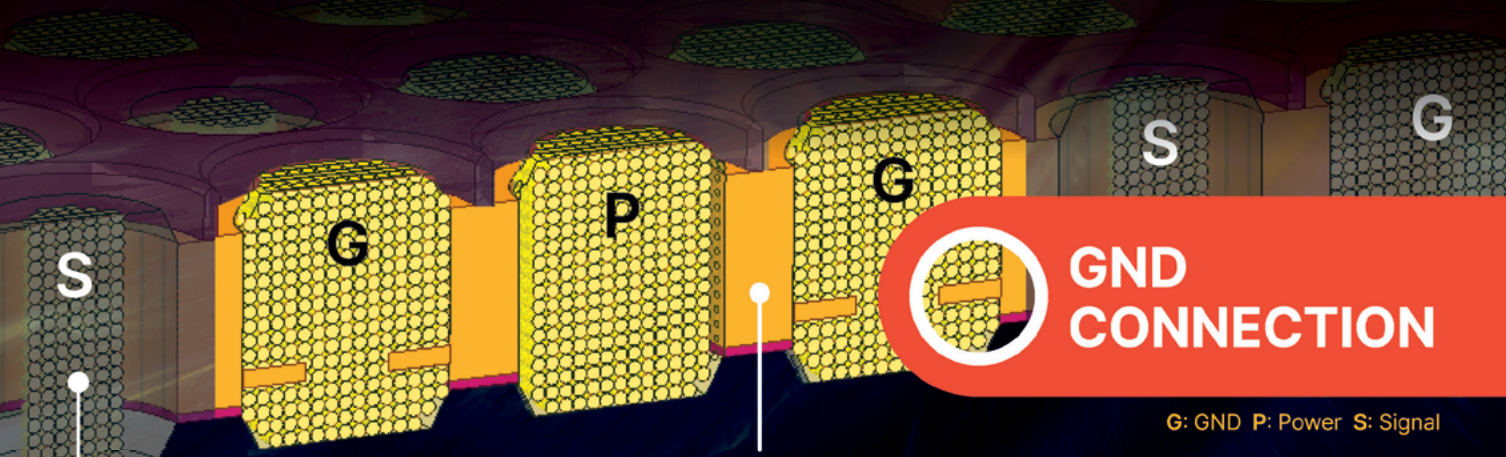
COAXIAL ELASTOMER SOCKET

for >64Gbps ATE/SLT Test
for Crosstalk free Board to Board Connector



ELTUNE-coax™

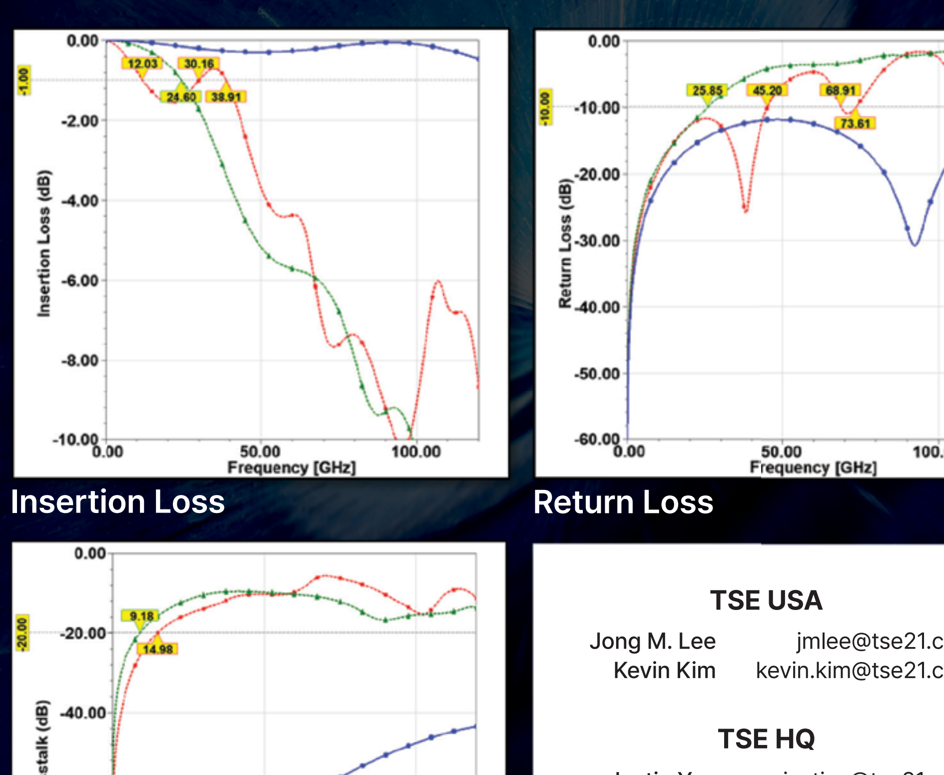
Metal GND Structure
Extremely Low Crosstalk >100Ghz@-20dB
Inductance <0.1nH
Min. pitch 0.6mm



COAXIAL ELASTOMER SOCKET

for >64Gbps ATE/SLT Test
for Crosstalk free Board to Board Connector

Electrical Specifications (unit: GHz)			
50Ω, 0.80mm pitch	Spring pin	Elastomer	ELTUNE-coax™
Electrical Length(mm)	3.05	0.60	0.60
Insertion Loss(S21) @-1dB	12.03	24.60	>100
Return Loss (S11) @-10dB	45.20	25.85	>100
Crosstalk (S31) @-20dB	14.98	9.18	>100



Insertion Loss

Return Loss

Crosstalk

TSE USA

Jong M. Lee jmlee@tse21.com
Kevin Kim kevin.kim@tse21.com

TSE HQ

Justin Yun justice@tse21.com
Jimmy Hwang jimmyhwang@tse21.com

- ELTUNE-coax™
- Elastomer
- Spring Pin

www.tse21.com
189, Gunsu 1-gil, Jiksan-eup, Seobuk-gu,
Cheonan-si, Chungnam, 31032, Korea

Throughput got you down?

Speed things up with Deca's 600mm panel technology!

Offering a 5X increase in usable area as compared to a standard wafer, increasing efficiency by upwards of 20% for large designs, eliminating pesky reticle limitations, and increasing the speed of die placement by solving die shift problems using Deca's patented Adaptive Patterning®.

WE CLEAN IT UP. ADAPTIVE PATTERNING® FROM DECA

thinkdeca.com

High-performance, multi-chip leadframe package with internal connections

By DaeYoung Park, HyeongIl Jeon, GiJeong Kim, JiYeon Yang, KwangSoo Sang, ByongJin Kim, JinYoung Khim
[Amkor Technology Korea, Inc.]

This paper discusses a highly-integrated multi-chip module (MCM) routable (thin) *Micro*LeadFrame® (rtMLF®) packaging for multi-functional high-performance applications. This package includes internal routing leads to connect die to die within the package. These routing leads let the package enhance the small form factor and, for reference, can be compared to a structure with two single quad flat no-lead (QFN) packages where the dice were connected by board traces. Feasibility of the MCM rtMLF package was confirmed using a conventional QFN process—and it passed the Automotive Electronics Council Q006 (AEC-Q006) reliability test. Die-to-die interconnections through routing leads showed better electric performance in terms of resistance, inductance, and capacitance parasitics and insertion loss than the on-board interconnections of the two single QFN packages. Lastly, thermal resistances of the MCM rtMLF package measured by thermal simulation were lower than those of MCM two-layer chip-scale packages (CSPs).

Introduction

For high-performance applications, demand for highly-integrated packages has increased. This is due to the highly-integrated package's electrical performance advantages of reduced interchip distance (delay), high-density I/O counts for multi-function capabilities, and small form factor [1-3]. With the increasing importance of highly-integrated packages, the need for improved thermal management is also increasing. When the high-density I/O signals operate for the highest performance, heat generation increases on the die. The high heat generation without effective heat dissipation has adverse effects on reliability and electrical performance of electronic products [4].

The *Micro*LeadFrame® (MLF®)/quad flat no lead (QFN) package, which is a CSP fabricated from a one-layer leadframe has been used in various applications for many years [5]. The MLF (or QFN) is famous for high reliability and high heat dissipation from a thick copper (Cu) alloy exposed pad that has high thermal conductivity at the bottom of the package. This design supports reduced die temperatures [6]. However, it is hard to apply the QFN in a highly-integrated package with high-density multi-functional I/O counts because of the peripheral leads on the QFN. The QFN leadframe cannot have formed routing leads because of its etching process [7-9].

To overcome the limitations of QFN design, we introduced the rtMLF® package with routable connections. The process flows of QFN and rtMLF substrates are shown in **Figure 1**. Comparing the two substrates, the conventional substrate has top and bottom etching before the surface finish (**Figure 1a**), while the rtMLF substrate has etching performed first at the bottom followed by pre-resin filling and grinding. After top etching, the top pattern remains, including the routable internal leads, without exposing the bottom (**Figure 1b**) [7]. The conventional leadframe substrate may also be configured with internal leads, but their length is limited because they have no stable support at the bottom. In contrast, the new routable substrate can be configured with internal routing leads because the pre-resin supports the bottom of the internal routing leads. Therefore, it is possible to increase design flexibility of rtMLF packaging so it can be applied to various applications. Recently, this new technology has been researched as a wettable flank package with pre-resin that supports the package along with electromagnetic interference (EMI) shielding that uses isolated pads for automotive applications [8,9]. However, a highly-integrated package for multi-functional I/O counts with multiple dice has not been studied with rtMLF technology and its internal routing leads.

In this study, a new package structure that is a multi-chip module (MCM) rtMLF was researched. The MCM rtMLF design layout was proposed according to multi-die interconnections with internal routing leads between two dice with two individual exposed pads. Testing provided verified enhancement of its small form factor compared with two single QFN packages. The designed MCM rtMLF samples were tested for their feasibility. Then, various reliability tests for automotive use were performed to verify the structural rigidity. In addition, electrical simulations were performed comparing two single QFN packages mounted on a board with the MCM rtMLF. Furthermore, thermal simulation with respect to thermal resistance of the MCM rtMLF was conducted to compare it with MCM two-layer chip-scale packages.

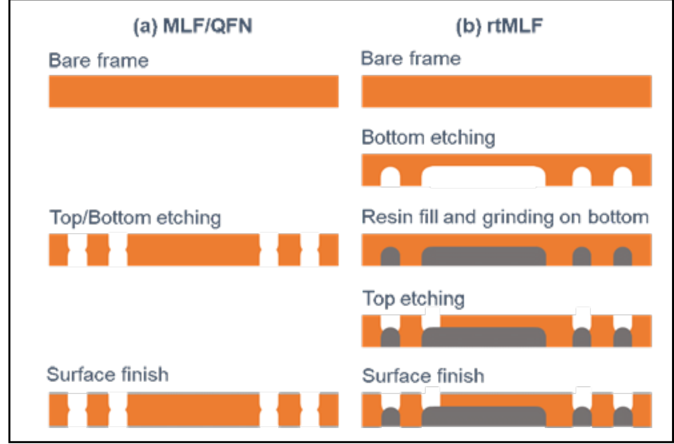


Figure 1: Steps in the fabrication of package substrates.

MCM rtMLF technology

The following sections discuss various aspects of testing performed on the MCM rtMLF technology.

Test vehicle and enhancement of small form factor. Information for the test vehicle is summarized in **Table 1**. Most descriptions are similar to a conventional QFN. Using this test vehicle, layout on the board was compared with two single QFN packages. The layout of two single QFN packages consisted of a 7X7mm^2, 9X9mm^2 body using 8.5mm^2 and 9.1mm^2 sized dice as shown in **Figure 2**. In the former case, the two dice are connected by internal routing leads in the package, so there is no need for additional connections on the board (**Figure 2a**). Whereas, in the latter case, Cu traces must be designed on the board for the connections of two dice with a 3mm distance (**Figure 2b**). The area of two single QFN packages, including board connections, is 211.38mm^2, and that of the MCM rtMLF package is 102mm^2. Therefore, at least 51.75% board space can be saved by using the new package; enhancement of the small form factor was, therefore, confirmed.

Manufacturability. Process flow for the new package described in **Table 1** is shown in **Figure 3**. The left side presents fabrication of a substrate with routable leads. Initially, the Cu alloy leadframe was the same as the QFN substrate. Secondly, the rtMLF substrate was bottom etched leaving exposed pads and leads. During bottom etching, the region of long routable internal leads was also etched, and it remained after the top etching process. Thirdly, pre-resin filling on the bottom etched area was performed to support the remaining top region. Grinding the overfilled pre-resin exposed the package leads. Finally, routing of the internal leads was performed after top etching. As a result, the internal routing leads could be left during fabrication because they were supported by the pre-resin. The right side of **Figure 3** shows the assembly process for the new package, which is the same as for the QFN process. Two dice were attached on separated individual exposed pads and cured at the same time. After this, wire bonding and molding processes were conducted to confirm feasibility of the MCM rtMLF design.

In the assembly process, wire bonding was key to confirm the feasibility of the new design. Internal routing leads for die-to-die interconnections were positioned far from the package pin area and floated from the bottom side. Wire bondability, therefore, was needed essentially for confirming the feasibility of structure and package reliability. After wire bond optimization, the measured stitch pull of the internal routing leads was over 6g, which is above the minimum requirement. The wire bondability and moldability are shown in **Figure 4**. From these results, the feasibility of MCM rtMLF design was confirmed.

Part	Item	Description
Package	Package type	MCM rtMLF
	Package thickness	0.850 mm
	Package size	12 mm X 8.5 mm
Leadframe	Thickness	0.152 mm
	Material	C19400
	Surface finish	PPF (Ni/Pd/Au)
Die	Size	8.5 mm^2, 9.1 mm^2
	Thickness	0.203 mm
Wire	Type / Dia.	AuPCC / 0.8 mil

Table 1: Test vehicle dimensions and description.

Reliability testing. After the assembly process, package-level reliability tests were conducted on the new package. The reliability testing is based on the Automotive Electronics Council Q006 (AEC-Q006) for Gold Flash Palladium Coated Copper (AuPCC) wire packages. Moisture sensitivity level 3, thermal cycle H, unbiased highly accelerated stress testing, and high-temperature storage testing were conducted. During the test, structural failures (e.g., delamination) were checked by scanning acoustic tomography inspection at each reading point. Inspection results showed that all passed. The reliability items, conditions, reading points, quantities and results are summarized in **Table 2**.

Electrical performance. Electrical simulation test vehicles were designed the same as in **Figure 2**. The Ansys Q3D 2022R1 simulation tool was used for the electrical simulation tool to compare resistance, inductance and capacitance (RLC) parasitics between the two test vehicles under 1GHz frequency conditions. The measured nets were composed of die-lead-die connections

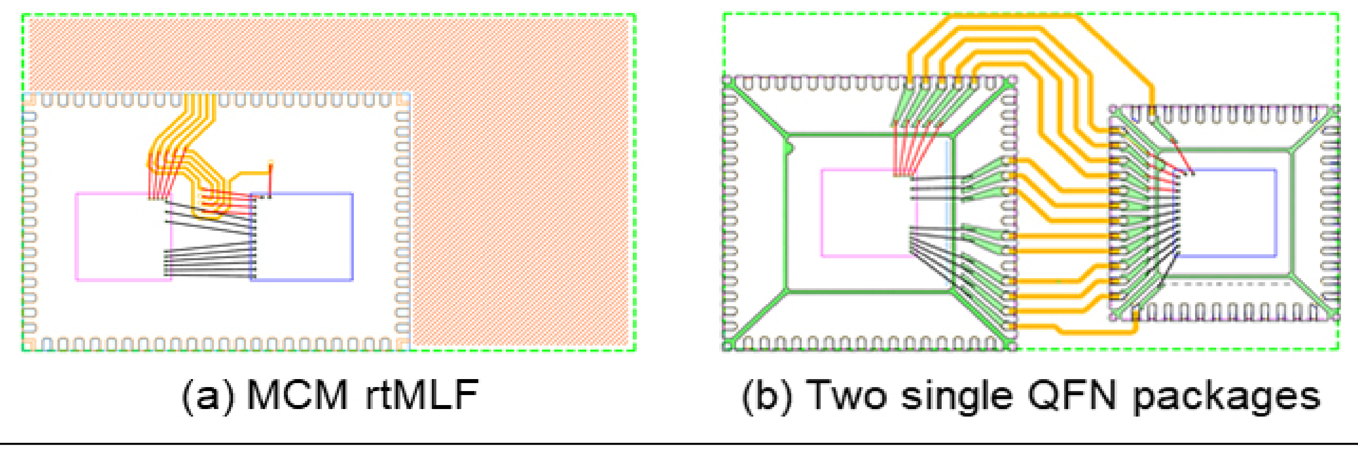


Figure 2: Package layout on the printed circuit board.

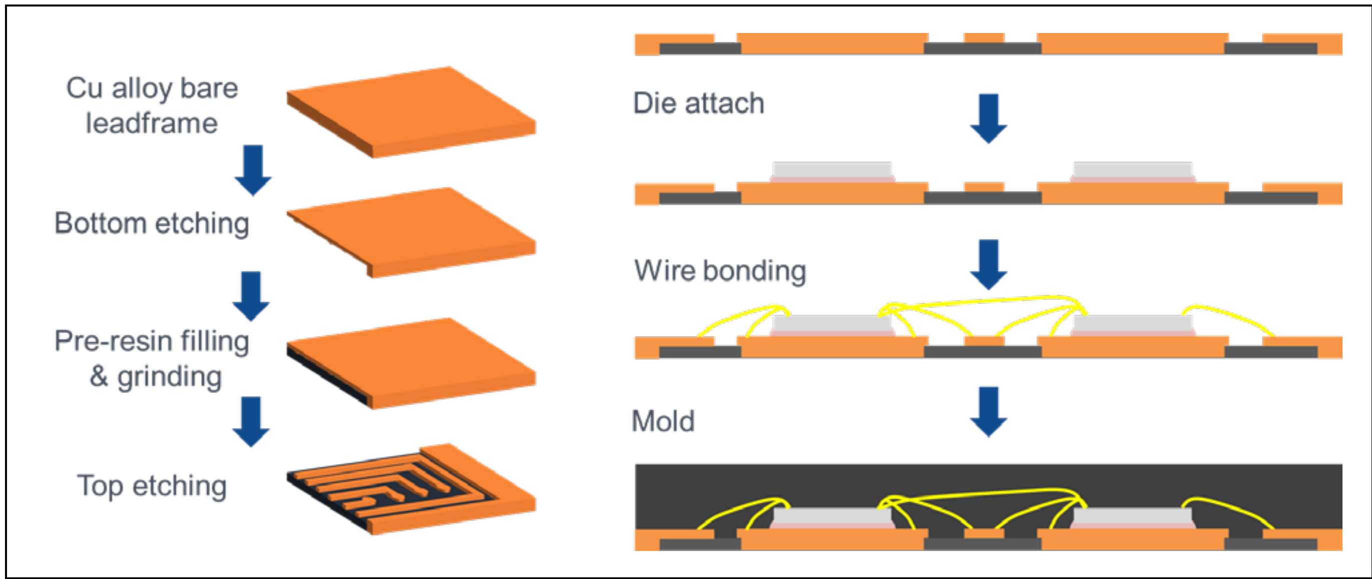


Figure 3: Process flow for the MCM rtMLF package.

Test item	Test condition	Reading point	Qty.	Result
Moisture sensitivity level 3	30 °C / 60%RH	260 °C 3X	231	Pass
Thermal cycle 'H'	-55 °C to +150 °C	500 cycle	77	Pass
		1000 cycle	77	Pass
Unbiased highly accelerated stress test	130 °C / 85%RH	96 hours	77	Pass
High temperature storage test	175 °C	250 hours	77	Pass
		500 hours	77	Pass

Table 2: Results of reliability (AEC-Q006) tests.

in package or die-Cu trace-die on the board (net #1, #2), and die-die connections in packages or die-Cu trace-die on the board (net #3, #4) as shown in **Figure 5**. Also, the scattering parameter (S-parameter) of nets #1 and #2 were measured by an Ansys HFSS 2022 R1 simulation tool at frequencies from 10MHz~1GHz.

The RLC parasitic values for MCM rtMLF and those of two single QFN packages are summarized in **Table 3**. The measured values of MCM rtMLF are drastically decreased compared with two single QFN packages with about 35% of resistivity and 40~50% of inductance. Furthermore, the decrease in capacitance was about 35% and 54% in each die-lead-die connection (net #1, #2), and 85% in die-die interconnections (net #3, #4). These RLC reductions occurred because of shorter interconnection lengths.

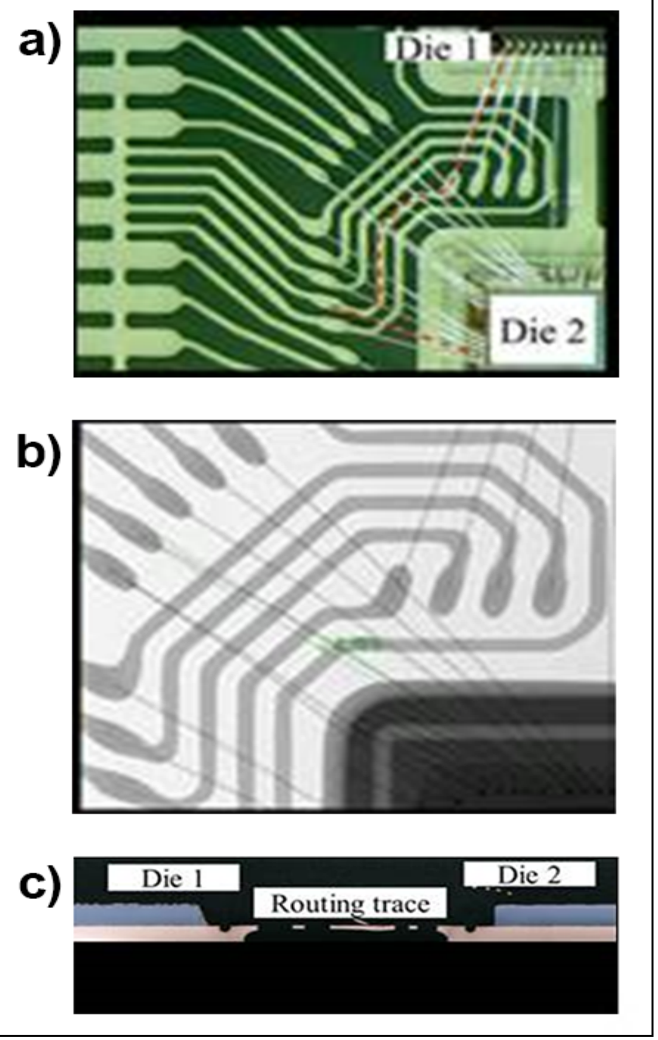


Figure 4: Feasibility of MCM rtMLF packaging: a) after wire bonding; b) after molding; and c) cross-sectional image after the MCM rtMLF process.

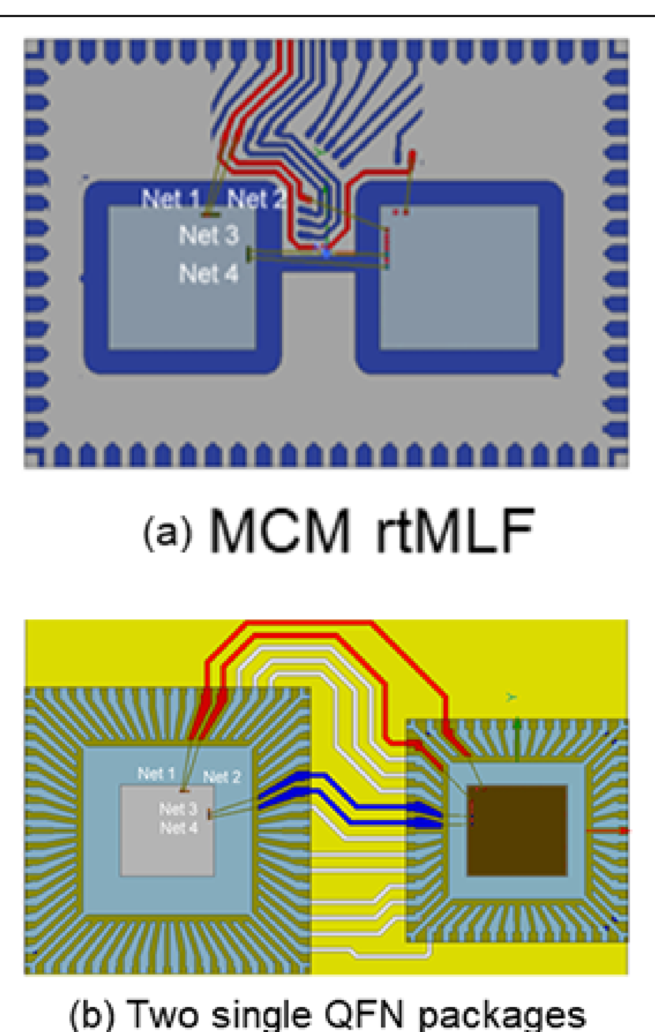


Figure 5: Test vehicles for electrical simulation.

Net #	Item	Two single QFNs	MCM rtMLF	Δ (%)
1	Resistance (mOhm)	1053.15	688.88	↓34.59
	Inductance (nH)	9.28	5.40	↓41.81
	Capacitance (pF)	2.06	1.31	↓36.41
2	Resistance (mOhm)	1038.88	676.18	↓34.91
	Inductance (nH)	8.95	4.64	↓48.16
	Capacitance (pF)	1.92	0.88	↓54.47
3	Resistance (mOhm)	704.65	457.28	↓35.11
	Inductance (nH)	6.35	3.13	↓50.71
	Capacitance (pF)	1.16	0.18	↓84.48
4	Resistance (mOhm)	694.01	457.44	↓34.09
	Inductance (nH)	6.25	3.14	↓49.76
	Capacitance (pF)	1.15	0.18	↓84.35

Table 3: RLC parasitics after electrical simulation.

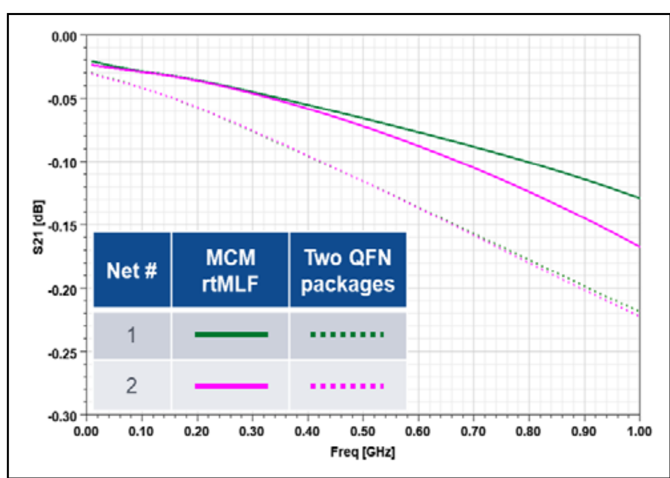


Figure 6: Insertion loss of test vehicles.

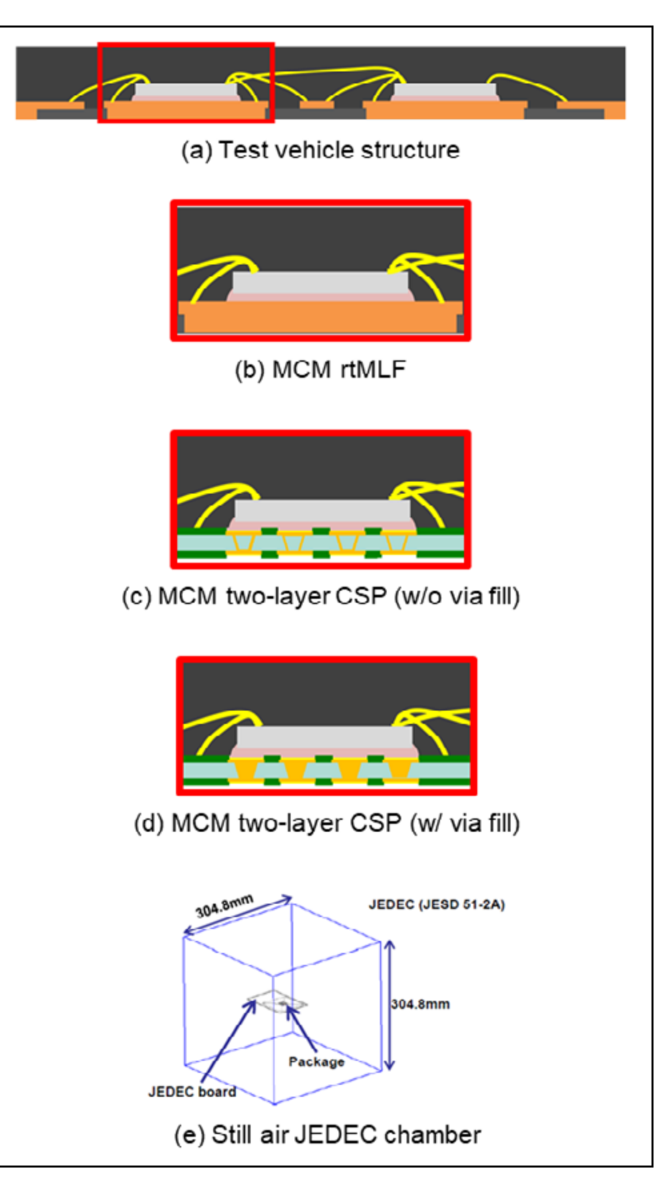


Figure 7: Thermal simulation set up: a) test vehicle structure; b) MCM rtMLF; c) MCM two-layer CSP (without via fill); d) MCM two-layer CSP (with via fill); and e) still-air JEDEC chamber.

Insertion loss comparison of the test vehicles is shown in **Figure 6**. At 1GHz, insertion losses of MCM rtMLF (shown by two solid lines) are lower than those of two single QFN packages, which are shown by dotted lines. In conclusion, the electrical performance of MCM rtMLF is better than two single QFN packages.

Thermal dissipation performance. Usually, most of the heat generated from the die is dissipated through the board [10]. A thermal simulation was done to evaluate and compare thermal performance for MCM rtMLF and MCM two-layer CSP structures at different power levels. **Figure 7** shows schematics of the thermal simulation test vehicles. The schematics of the simulation structures were shown in **Figure 7a-d**. In this simulation, the package outline of the thermal simulation structure was the same except for the die pad structure. For the MCM rtMLF, exposed pads for heat dissipation were composed of thick Cu alloy (**Figure 7b**). However, those of the MCM two-layer CSP packages were composed of thermal vias (without via fill, and with via fill) as shown in **Figure 7c-d**. The thermal simulation followed the JEDEC (JESD 51-2A) set up for a still-air environment (**Figure 7e**).

Table 4 summarized the result of thermal simulation comparison between MCM rtMLF and MCM two-layer CSP structures. Theta JA (θ_{JA}), the thermal resistance, is a parameter for showing heat dissipation performance. Based on the thermal simulation result, the θ_{JA} of MCM two-layer CSP packages is about 20% higher than that of the MCM rtMLF package for each value of power applied to the die.

Item	Power per die	MCM rtMLF	MCM CSP (w/o via fill)	MCM CSP (w/o via fill)
Die 1 Temp. (℃)	1 W	65.29	72.68 (↑11.3%)	72.34 (↑10.8%)
	2 W	103.09	118.36 (↑14.8%)	117.71 (↑14.2%)
Die 2 Temp. (℃)	1 W	65.08	71.24 (↑9.4%)	70.91 (↑9.0%)
	2 W	102.66	115.05 (↑12.1%)	114.45 (↑11.5%)
Theta JA (℃/W)	1 W	19.277	22.975 (↑19.2%)	22.801 (↑18.3%)
	2 W	18.657	22.474 (↑20.5%)	22.314 (↑19.6%)

Table 4: Results of thermal simulation.

Figure 8 shows the temperature distribution on the package surface when the power per die is 1W. The temperature of dice used in MCM two-layer CSP packages is about 10% higher than that of the MCM rtMLF package. Consequently, the MCM rtMLF package shows higher heat dissipation performance than that of MCM two-layer CSP packages.

Die Sorting Solutions

Syagrus Systems®

(651) 209.6515
4370 West Round Lake Road
Arden Hills, MN 55112
syagrussystems.com

New DTS1 and DTS2 Die Sorter Sales and Manufacturing (up to 300mm)
- Highly flexible with quick changeover
- Medium- to high-volume systems capable of 4k to 16k UPH
- Die sizes down to .150mm
- Invert and vision inspection capable

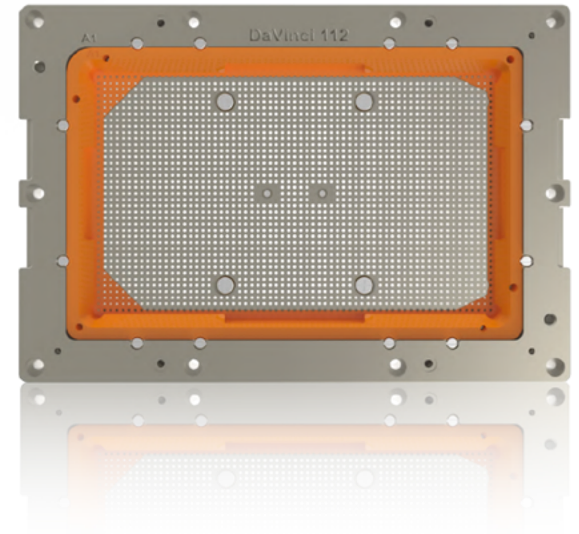
We also provide service and support for legacy Laurier DS4000 and DS9000 systems
- Service, spare parts and software support
- “Modernization Upgrades” bringing your existing systems up-to-date by refurbishing both hardware and software.

©2023, Syagrus Systems, LLC

Cutting-edge Connectivity

DaVinci 112 Test Socket

The coaxial structure of the DaVinci 112 test socket is designed to meet the high-speed interface requirements of next generation ASICs up to 112 Gb/s. This allows high-speed functional testing of your integrated circuits.



- Controlled impedance interface
- Protection against solder build-up and longer probe life thanks to homogeneous alloy spring probe technology
- Optimized ground connection to reduce crosstalk during testing
- Unrivalled mechanical strength thanks to patented insulated metal housing
- Designed for large ASIC device footprints

High Performance Compute | High Speed Digital | Data Center

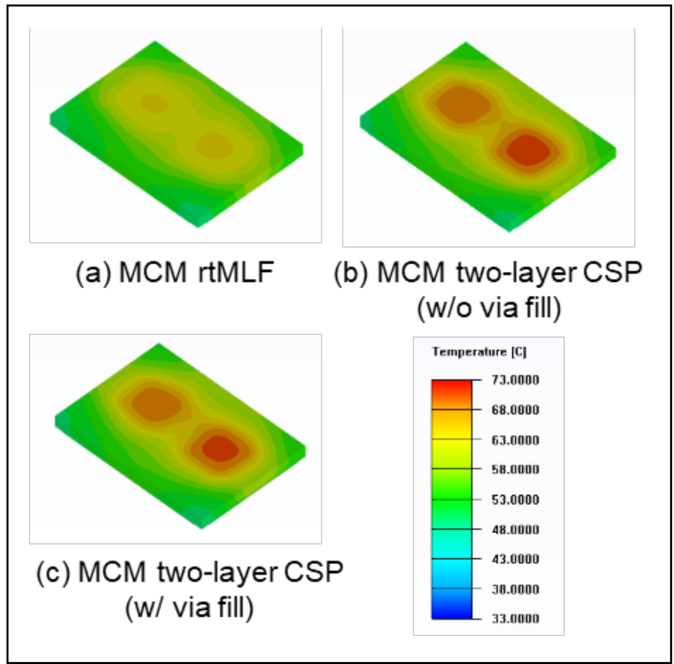


Figure 8: Temperature distribution of the package surface (1W).

Summary

Highly-integrated packaging is one of the driving forces for high-performance and small form factor packages. As multi-functional I/O density increases, the importance of thermal management also increases. In this study, MCM rtMLF is suggested for highly-integrated packaging with internal routing that connects die to die and provides high heat dissipation. Internal routing leads are supported by a pre-resin that is filled during substrate fabrication. It can overcome the limitations of a conventional QFN design.

From this research, the feasibility of the MCM rtMLF with internal routing leads was checked. The new structure passed AEC-Q006 reliability testing. Through electrical simulation comparison, the better electrical performance of MCM rtMLF over two single QFN packages was verified. In addition, the high heat dissipation property of the MCM rtMLF package was checked by comparing it with MCM two-layer CSP designs. The routable molded leadframe can provide a highly-integrated solution with high heat dissipation and will enable application of this platform to be expanded in various markets.

Acknowledgements

*Micro*LeadFrame, MLF and rtMLF are registered trademarks of Amkor Technology, Inc. This article was originally presented at the 2022 IEEE 24th Electronics Packaging Technology Conference (EPTC) and has been edited for publication in *Chip Scale Review*.

References

1. L. L. W. Leung, M. L. Sham, W. Ma, Y. C. Chen, J. R. Lin, T. Chung, "System-in-package (SiP) Design: issues, approaches and solutions," 2006 Inter. Conf. on Electronic Materials and Packaging, Kowloon, China, Dec. 2006, pp. 1-5.
2. B. J. Kim, S. H. Lee, J. B. Shim, N. H. Cho, J. Y. Khim, "Design constraints and scale down evolution in advanced semiconductor packages," 2021 54th Inter. Symp. on Microelectronics (IMAPS), San Diego, USA, Oct. 2021.
3. L. He, S. Elassaad, Y. Shi, Y. Hu, W. Yao, "System-in-package: electrical and layout perspectives," Found. Trends Electron. Des. Autom, Vol. 4, No. 4 (2011), pp. 223-306.
4. J. Liu, Z. Yang, Q. Zeng, "Research on thermal performance of single chip based on SiP technology," 2020 21st Inter. Conf. on Electronic Packaging Tech. (ICEPT), Guangzhou, China, Aug. 2020, pp. 1-3.
5. A. R. Moreno, F. R. I. Gomez, E. M. Graycochea, "Enhanced loop height optimization for complex configuration on QFN device," 2020 IEEE 22nd Electronics Packaging Tech. Conf. (EPTC), Singapore, Dec. 2020, pp. 182-184.
6. K. Hollstein, L. Yang, Y. Gao, K. Weide-Zaage, "Identification of influencing PCB design parameters on thermal performance of a QFN package," 2020 21st Inter. Conf. on Thermal, Mech. and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), Kracow, Poland, July 2020, pp. 1-5.
7. B. J. Kim, W. B. Bang, G. J. Kim, J. Y. Jung, J. H. Yoon, "Introduction of routable molded lead frame and its application," Jour. of the Microelectronics and Packaging Soc., Vol. 22, No. 2 (2015), pp. 41-45.
8. B. J. Kim, H. I. Jeon, G. J. Kim, N. H. Cho, J. Y. Khim, Y. K. Kim, "Wettable flank routable thin MicroLeadFrame for automotive applications," Microelectron Reliab, Vol. 135 (2022).
9. B. J. Kim, H. I. Jeon, D. Y. Park, G. J. Kim, N. H. Cho, J. Y. Khim, "EMI shielding leadless package solution for automotive," Jour. of Advanced Joining Processes, Vol. 5 (2022).
10. C. C. Hsieh, C. H. Wu, D. Yu, "Analysis and comparison of thermal performance of advanced packaging technologies for state-of-the-art mobile applications", 2016 IEEE 66th Electronic Comp. and Tech. Conf. (ECTC), Las Vegas, USA, May 2016, pp. 1430-1438.

Biographies

DaeYoung Park is a Researcher, Advanced Maintstream Development, R&D, at Amkor Technology Korea, Inc., Incheon, Republic of Korea. Email daeyoung.park@amkor.co.kr;

HyeongIl Jeon is Senior Director, Advanced MS Development Project Leader at Amkor Technology Korea, Inc., Incheon, Republic of Korea.

adeia™

Adeia turns ideas into innovations

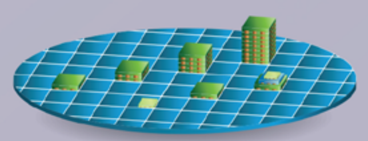
Our name may be new, but our roots run deep with decades of continued innovation. We invent, develop and license innovations that advance how we live, work and play.

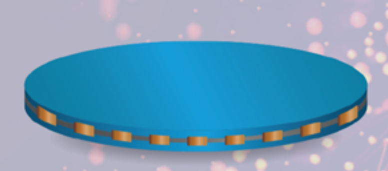
Adeia invented and pioneered Direct and Hybrid Bonding

DBI® Ultra
Die-to-Wafer
Hybrid Bonding

DBI®
Wafer-to-Wafer
Hybrid Bonding

ZiBond®
Wafer-to-Wafer
Direct Bonding





Better Ideas.
Better Entertainment.

adeia.com

TSV oxide etch-back optimization for the via-last integration scheme

By Bhesetti S. S. Chandra Rao, Hemanth K. Cheemalamarri, Darshini Senthilkumar
*[Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR)]*

Through-silicon via (TSV) technology has become the key driver for advanced electronic packages such as those used in 3D stacking and backside illuminated image (BSI) sensor applications. Among the various possible methods of integrating TSVs such as via first, via middle and via last, the via-last method has gained much attention. The via-last method helps reduce the impact on back-end-of-line (BEOL) processing and does not require a TSV-reveal process flow. However, the via-last process scheme requires a more reliable TSV bottom-oxide etch-back process for making contact with the underneath interconnect layer. One potential challenge with respect to the oxide etch-back process is in protecting the top corner of the TSV liner oxide to ensure better electrical reliability. This challenge arises because the etch rate (ER) at the bottom of the via is much lower than at the top corner of the TSV. This work focuses on process methodology to increase the bottom-oxide ER while reducing the TSV's top-corner oxide.

The oxide etch-back process has been optimized with a fluorine-deficient regime with the addition of O_2. The optimized process suggests that adding a slight amount of O_2 with argon-diluted C_4F_8 plasma helps in protecting the top corner oxide more effectively and the optimized process shows that the bottom-oxide ER is 20 to 30% higher than the TSV top-corner erosion.

Introduction

Three-dimensional (3D) integration has become more prominent and is a credible alternative to Moore's Law-inspired interconnect advances in recent years [1]. It also overcomes the constraints of system-on-chip (SoC) technology in terms of performance, cost, and time to market [2]. It becomes more and more evident that 3D integration works in conjunction with semiconductor scaling to enable higher integration densities along with the integration of heterogeneous technologies [3,4].

The use of TSVs has become a prominent interconnect technology for signal integrity through vertical stacking [5-6]. There are several approaches for TSV formation. The via-first approach creates the TSVs before the front-end-of-line (FEOL) and BEOL processes. The via-middle approach carries out FEOL fabrication, followed by TSV and BEOL fabrications. The via-last approach [6] forms the TSVs after FEOL and BEOL fabrications. In the via-after bonding approach, vias are formed after bonding either chip-to-wafer (C2W) schemes or wafer-to-wafer (W2W) schemes. Depending on the integration scheme, the via-last or via-after bonding is selected for heterogeneous integration applications [7], like complementary metal-oxide semiconductor microelectromechanical systems (CMOS-MEMS). In the via-last approach, the oxide liner is deposited on the Si TSV immediately after TSV dry etching and wet cleaning.

The **Figure 1a** schematic shows the typical post-oxide liner deposition. This liner not only acts as electrical isolation for the TSV in terms of electrical leakage, but will also help as a contamination barrier for the Si substrate in terms of re-sputtered metal underneath while landing on the metal pad (aluminum or copper). During the etch-back process, there is a potential issue of losing oxide at the TSV's corner (as shown in **Figure 1b**) because of the high plasma sheath potential at the corner, which receives the highest ion bombardment. If the etch-back process is not controlled, it results in an electrical leakage path and becomes a significant yield loss [9-11].

The oxide etch process has been well understood by using fluorine-based etch chemistries; ionized fluorine radicals react with the Si-broken bonds of silicon oxide to form volatile compounds [8].

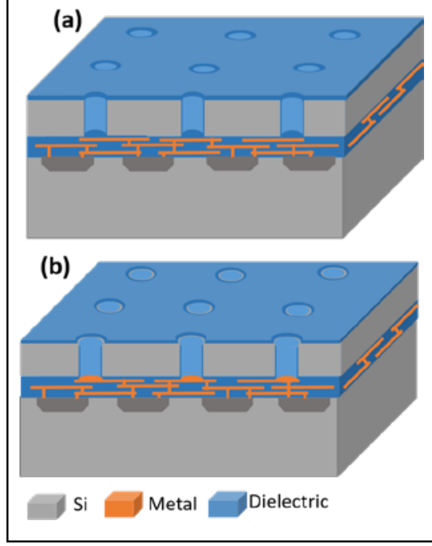


Figure 1: a) Schematic of the oxide liner for the via-last integration approach; b) Effect on the TSV's top-corner oxide, after oxide etch.

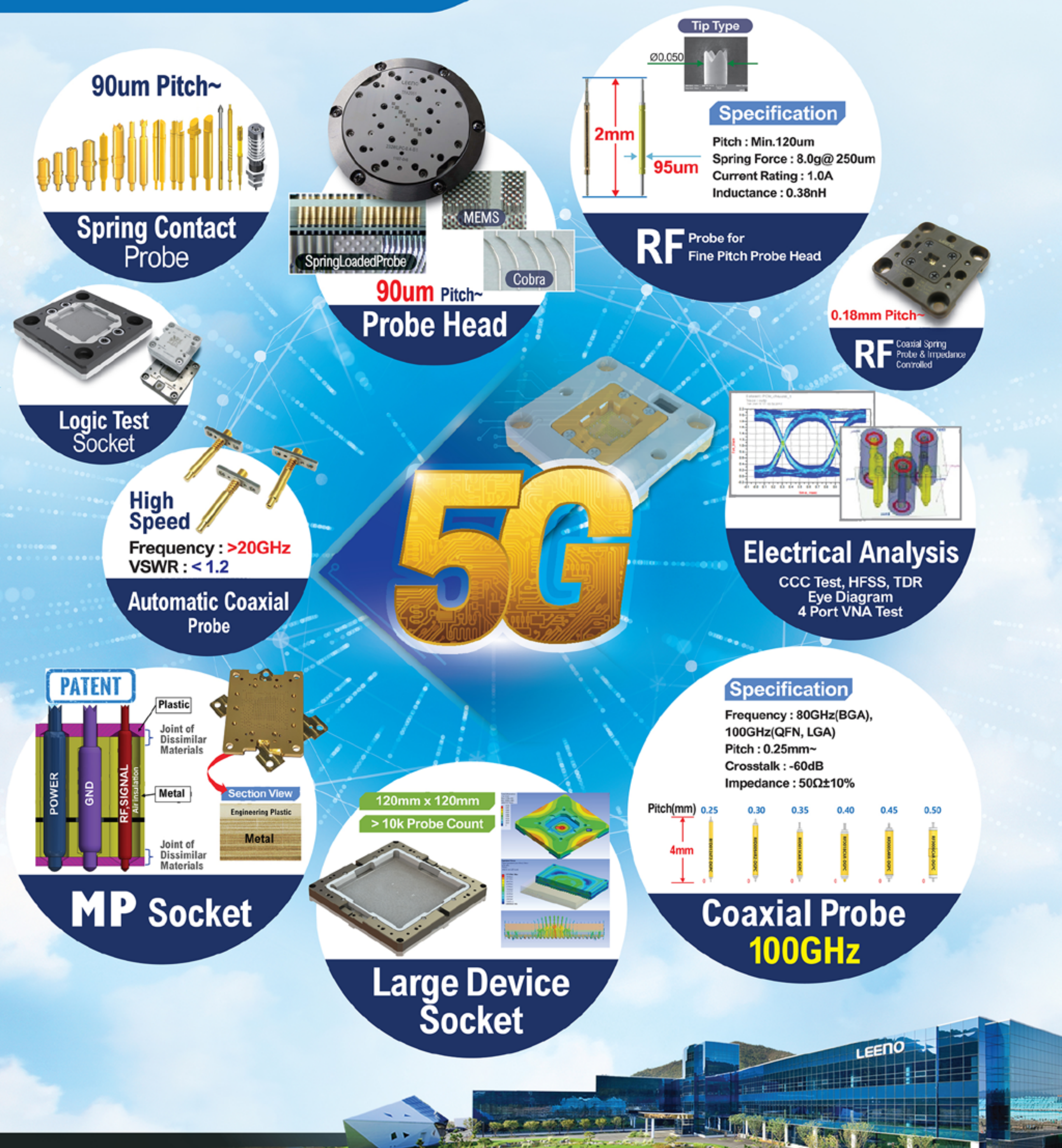
However, the bottom-oxide etch back in the TSV is more challenging and requires a better-optimized process to obtain higher ER at the bottom of the TSV compared to the top-corner oxide. Therefore, this requirement drives more attention to the bottom-oxide etch-back process for a smooth landing on the underneath contact prior to the electroplating of copper in the via-last TSV integration approaches.`

There are a few reports in the literature that propose protecting the TSV's top corner using an additional protection layer such as SiN over the liner oxide along with optimized etching [9-11]. There is another integration approach to mitigate top-corner oxide loss is by depositing a thick hard-mask oxide deposition (>1.5µm) before TSV etch. However, this additional process step incurs a higher cost of TSV fabrication and is less attractive for integration adoption.

This study focuses on TSV oxide liner etch-back process optimization

LEENO

www.leeno.com



LEENO
LEENO INDUSTRIAL INC.

GLOBAL LEADER LEENO

HEAD OFFICE
10 105beon-gil MieumSandan-ro Gangseo-gu, Busan, Korea

CONTACT
USA: hskang@leeno.co.kr / +1 408 313 2964 / +82 10 8737 6561
Korea: sales-leeno@leeno.co.kr / +82 51 792 5639

on improving the bottom oxide ERs while simultaneously minimizing the top-corner oxide ER. The design of experiments (DOE) is designed by considering the variables that help in thicker passivation and minimizing the free radicals for silicon etching. C_4F_8 gas is known for a higher passivation deposition rate when mixed with argon. Argon addition helps in increasing the electron temperature, which, in turn, increases the plasma density and results in the faster passivation rate. The addition of O_2 to the C_4F_8 increases passivation and thereafter further increases in O_2 lowers the passivation rate. Because of the high aspect ratio, the passivation deposition rate varies from the top to the bottom of the TSV—as the depth progresses, the passivation transport mechanism changes from convective flow to diffusional flow, which results in more deposition at the TSV top than at the bottom. The process DOE targets minimizing the ratio of the oxide ERs between the TSV's top corner and the bottom of the TSV.

Materials and methods

The wafer sample fabrication process flow is shown in the schematic (**Figure 2**). Wafer substrates of 300mm p-type (100) Si have been used for the current study. These wafers are spin coated using a negative photoresist (PR) and pattern-transferred using a EUV stepper. A TSV pattern of 10µm (critical dimension [CD]) is etched to a depth of ~45µm using a standard multiplexed time etch process in an inductively-coupled plasma (ICP) chamber. After the TSV etch, the remaining PR is stripped using a high-temperature O_2 plasma. Subsequently, the wafer was wet cleaned to remove the post-etch residues.

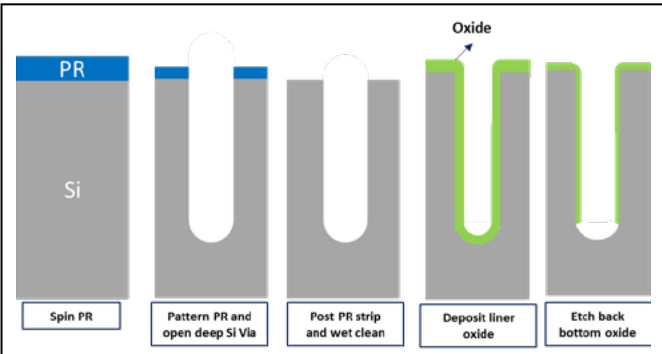


Figure 2: Schematic of the process flow.

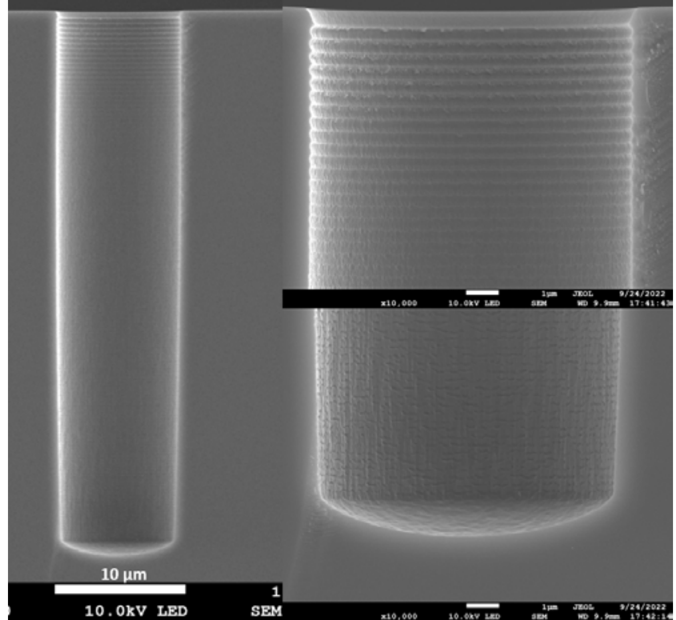


Figure 3: TSV structure prior to oxide liner deposition.

Figure 3 shows the post-etch and wet-cleaned TSV structure with <40nm scallops and a near-vertical profile. The TSV wafers are deposited with a liner oxide of ~1µm using a plasma-enhanced CVD (PE-CVD) process. **Figure 4** shows the TSV with liner oxide. The initial oxide thickness of the field (top), top corner, and bottom of the TSV are measured at ~1.31µm, ~0.86µm, and ~0.85µm, respectively. The step coverage ratio

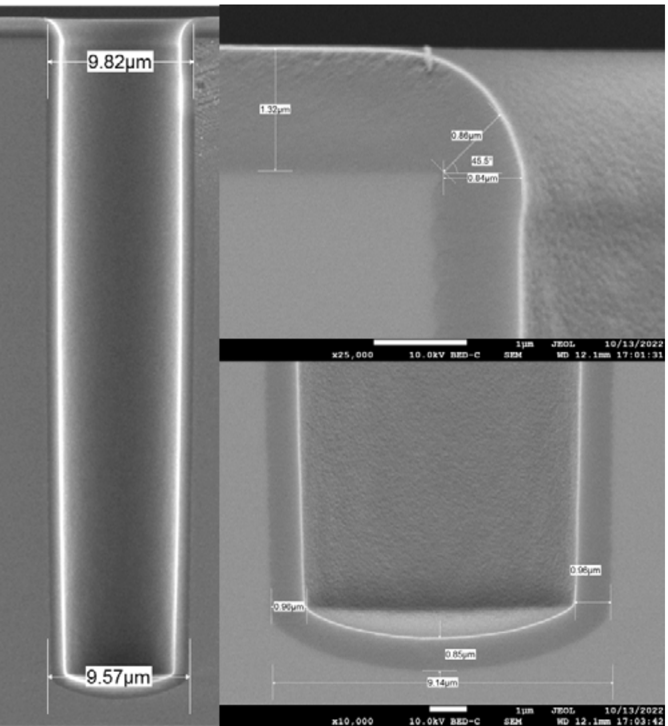


Figure 4: TSV structure after oxide liner deposition.

of the TSV top corner to the bottom is 1:1. This scenario makes the process challenging if the ERs are similar or faster at the TSV top corner. The DOE is conducted to determine the optimum process conditions to minimize the top-corner ER while enhancing the bottom-oxide ER. Process parameters (argon, O_2, C_4F_8, and pressure) are used to generate a full-factorial DOE with the three center points. After etching, these wafers were inspected using cross-sectional field-emission scanning electron microscopy (FE-SEM) for post-etch liner oxide thickness measurement.

Results and discussions

Fluorine radicals are responsible for the etching of the Si in the dry etch process by forming volatile SiF_4 at even low ion energies. However, in the case of SiO_2, due to the stronger energy threshold (an energy threshold of 799KJ/mol for the Si-O bond, and 552KJ/mol for the Si-F bond [12]), the reaction can't

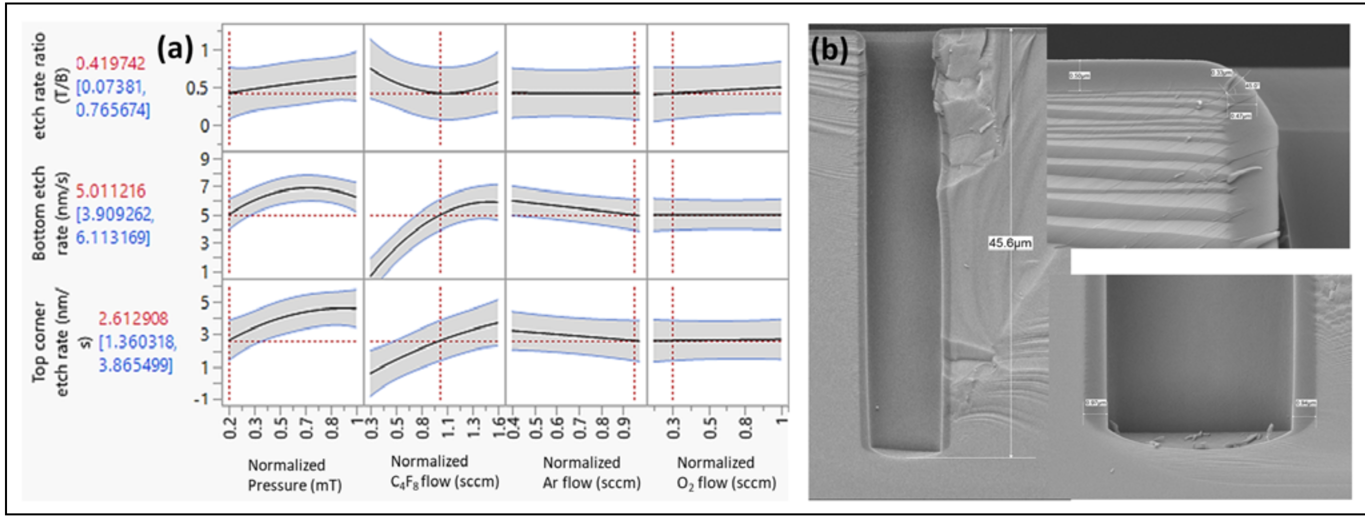


Figure 5: The JMP predictive model for determining the best possible condition for a greater bottom-oxide etch rate than for the top-corner oxide.

be spontaneous. The chemical etching of SiO_2 occurs after Si-O bond breakage under the ion bombardment and, therefore, Si in the broken bonds is scavenged by fluorine radicals. Therefore, a combination of high-energy ion bombardment and chemical etching are needed for oxide etching.

ER process DOE trends are shown in **Figure 5a**, e.g, C_4F_8 with the addition of argon results in bottom-oxide ERs being lower than ERs for the top corner of the TSV. Without O_2 flow addition, it is observed that nearly a 30% faster ER is at the top corner. As the O_2 flow increases, the top-corner oxide ER slowly drops and achieves the lowest reduction in ER observed at 30% of its normalized O_2.

At optimized DOE conditions, passivation film deposition is thicker at the top of the TSV than at the TSV bottom. Passivation deposition variation is caused because of the transport mechanism of polymer radicals, i.e., the convective flow of constituent species controls the passivation film (silicon-oxy-fluorocarbon) deposition at the top of the TSV, whereas the diffusion flow controls the bottom of the TSV when the TSV aspect ratio >3. The reduction in the top TSV corner ER is attributed to the formation of the thick-passivation film. **Figure 6** shows the typical passivation film in the absence of the bias power. The results show that there was a thicker passivation film at the top than at the bottom of the TSV. However, this thicker passivation film (silicon-fluorine carbon) is not strong enough to withstand argon bombardment and results in ineffective protection of the TSV top-corner oxide because of the low bond-breaking energy (~4.4eV) of C-F bonds in the film [13].

When O_2 is added to the etch chemistry, the formation of thick silicon-oxy-fluoride (Si-O-F) film results in a reduction of the oxide ER at the TSV's top corner. The ER drops with an increase in O_2 and achieves a maximum when O_2 flow reaches 30% of the total C_4F_8 gas flow. In addition to the thick passivation film, addition of O_2 also forms a volatile COF_2 resulting in a reduced fluorine-free radical concentration.

Figure 6: Passivation deposition at the TSV top corner.

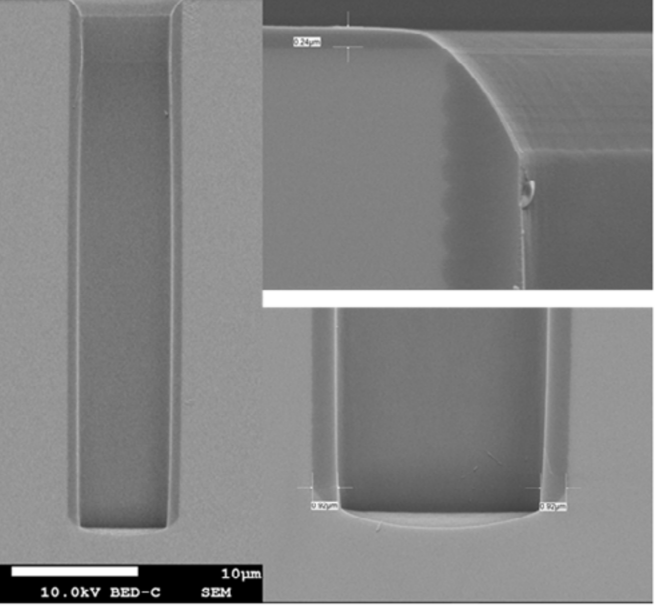


Figure 7: A non-optimized run resulted in a higher top-corner oxide etch rate than for the bottom oxide.

Sustainable Excellence
TFE
Total Solution Provider
Burn-In
Thermal
ATE
PCR Elastomer Socket
Change Kit
Pick & Place
S-Parameter
Eye-Diagram
Analysis
Enhanced Technology
World's Best Test Solution Provider
TFE
Align & Smart Contact
JMT
www.tfe.co.kr
TFE USA : fred@tfe.co.kr / matt@tfe.co.kr
+1-480-326-8028 / +1-408-202-7153
TFE Korea (H.Q) : g.m@tfe.co.kr
+82-70-7093-8028

Increasing passivation and reducing the fluorine-free radical concentration helps in the reduction of ER of the oxide at the top corner. However, because of lower passivation at the bottom of the TSV, the oxide is continuously sputtered to the sidewalls and results in a higher ER.

To understand the optimized process window for the DOE, JMP software is used to generate the predictive profile as shown in **Figure 5a**. The dependent variable (bottom ER, top corner ER and ratio of ERs) and independent variables (O_2, argon, C_4F_8, and pressure) are analyzed using the least squares fit model. The top-oxide to bottom-oxide ER ratio is lowest at the lower pressure and at 60% of normalized C_4F_8 flow. At high pressure and higher flow, the ER ratio is higher, and the TSV top-corner oxide ER dominates, resulting in complete loss of top-corner oxide during the bottom-oxide etch back, as shown in **Figure 7**.

Summary

The etch-back process of the liner oxide at the TSV bottom – achieved while protecting the top-corner oxide – has been demonstrated. An optimized O_2 flow in fluorine-deficient regimes helps in minimizing the oxide ER of the TSV top corner. At the same time, a higher oxide ER is observed in the TSV bottom. The JMP statistical analysis was used to optimize process conditions. The predicted process window is observed at lower pressure (<40mT), with an O_2 flow of <20sccm, a higher argon flow (>10 times that of the C_4F_8 flow), and a lower C_4F_8 flow of <100sccm. The optimized process conditions achieved a 20% higher oxide ER at the TSV bottom than that at the TSV top. This optimized process helps enable the highly reliable TSV etch-back process for the via-last integration scheme.

Acknowledgements

This work was supported by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research), Singapore, under Grant No. 12101E0008. Portions of this article were originally presented at the 2022 IEEE 24th Electronics Packaging Technology Conference (EPTC) and has been edited for publication in *Chip Scale Review*.

References

1. B. Hoefflinger, "ITRS: The international technology roadmap for semiconductors," Chips 2020; Springer, Berlin, Heidelberg (2011) pp. 161-174.
2. P. Ancey, "3D-SOC to 3D heterogeneous systems: technology and applications," 2011 IEEE Symp. on VLSI Technology-Digest of Technical Papers, pp. 180-181.
3. S. Zhang, et al., "Recent prospectives and challenges of 3D heterogeneous integration," e-Prime-Advances in Electrical Engineering, Electronics and Energy (2022): 100052.
4. A. A.Elsherbini, S. M. Liff, J. M. Swan, "Heterogeneous integration using omni-directional interconnect packaging," 2019 IEEE Inter. Electron Devices Meeting (IEDM) 2019.
5. Z. Xu, J-Q. Lu, "Through-silicon-via fabrication technologies, passives extraction, and electrical modeling for 3-D integration/packaging," IEEE Trans. on Semiconductor Manufacturing 26.1 (2012): 23-34.
6. K-J. Chui, W-L. Loh, Q. Ren, W. Sunil, M. Yu, "A cost-effective, CMP-less, via-last TSV process for high-density RDL applications," 2016 IEEE 66th Elec. Comp. and Tech. Conf (ECTC).
7. M. Puech, J. M. Thevenoud, J. M. Gruffat, N. Launay, N. Arnal, P. Godinat, "Fabrication of 3D packaging TSV using DRIE," 2008 Symp. on Design, Test, Integration and Packaging of MEMS/MOEMS, Nice, France, 2008, pp. 109-114, doi: 10.1109/DTIP.2008.4752963.
8. V. M. Donnelly, "Reactions of fluorine atoms with silicon, revisited, again," Jour. of Vacuum Science & Tech. A: Vacuum, Surfaces, and Films 35.5 (2017): 05C202.
9. Y. Li, M. Stucchi, S. Van Huylenbroeck, G. Van Der Plas, G. Beyer, E. Beyne, K. Croes, "TSV process-induced MOS reliability degradation," 2018 IEEE Inter. Reliability Physics Symp. (IRPS) (pp. 5B-5).
10. N. Tutunjyan, S. Sardo, J. De Vos, S. Van Huylenbroeck, A. Jourdain, L. Peng, et al., "Etch process modules development and integration in 3D-SOC applications," Microelectronic Eng., 196, 38-48 (2018).
11. S. Van Huylenbroeck, J. De Vos, Z. El-Mekki, G. Jamieson, N. Tutunjyan, K. Muga, et al., "A highly reliable 1.4µm pitch via-last TSV module for wafer-to-wafer hybrid bonded 3D-SOC systems," IEEE 69th ECTC (2019) (pp. 1035-1040).
12. Bond Dissociation Energies (Online source: 11---bonddissociationenergy.pdf (ucsb.edu), section 4, p. 50).
13. M. Zhang, P. Watson, "Reactive ion etching selectivity of Si/SiO_2: Comparing of two fluorocarbon gases CHF_3 and CF_4," (2019); https://repository.upenn.edu/cgi/viewcontent.cgi?article=1055&context=scn_protocols

Biographies

Bhesetti S. S. Chandra Rao is a Senior Scientist at the Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore. His research interests are 3D-IC, C2W and W2W bonding and dry etch process technologies. He received a PhD from the NUS Singapore, a Master's degree from the IISc, Bangalore, and a Bachelors degree from the NIT, Warangal, India. Prior to this, he worked for 9 years at Lam Research and Applied Materials in dry etch technology. He has served EPTC2021 as a Technical Chair and General Chair for IEEE-EPTC 2022. Email Bhesetti_Chandra_Rao@ime.a-star.edu.sg

Hemanth Kumar Cheemalamarri is a Scientist at the Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore. He completed his PhD from IIT Hyderabad, India, 2021. He is currently working as a research scientist in W2W bonding technology for heterogeneous integration and MEMS applications.

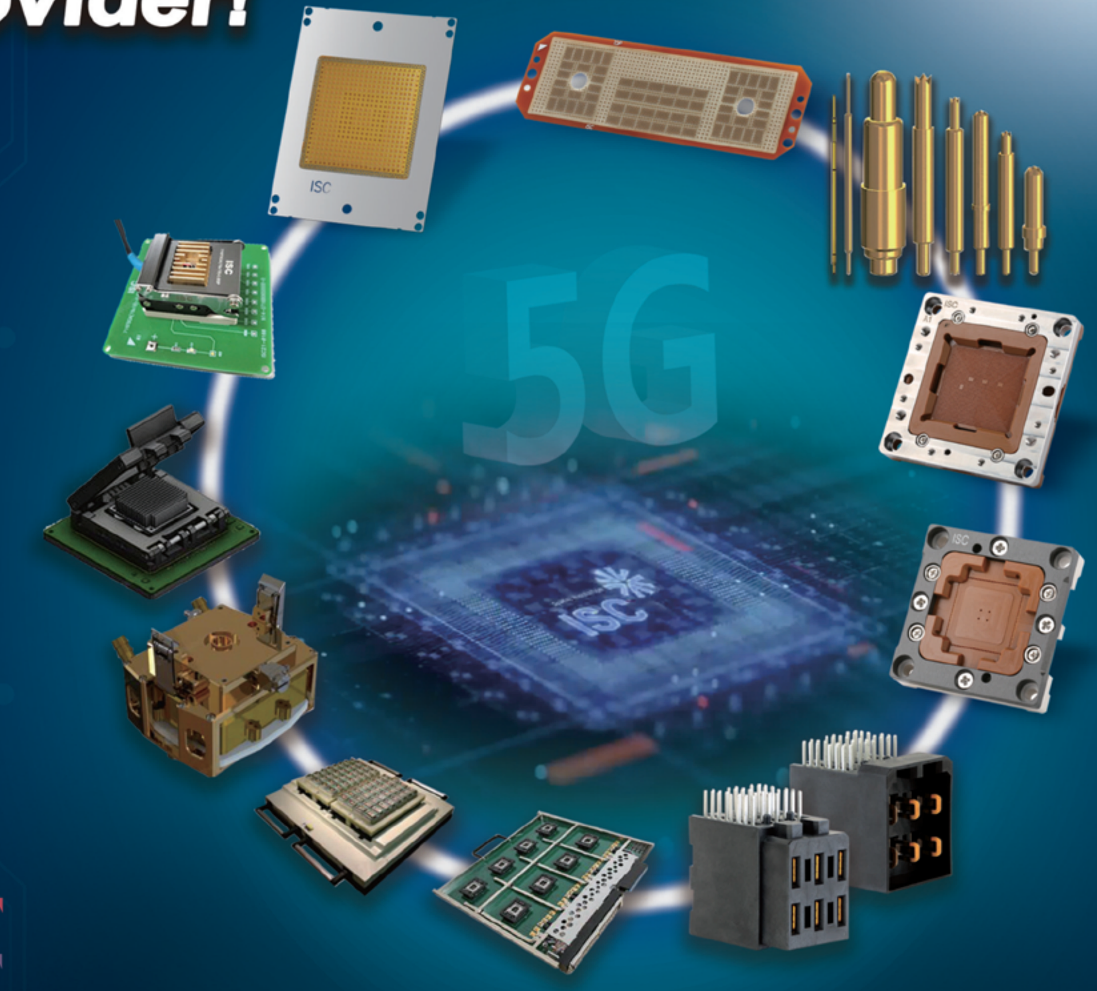
The Best Solution Provider !

200mm/300mm | Bumping | RDL
FIWLP | FOWLP | Probe-test | Back-end

Based in Pyeongtaek, South Korea, LB Semicon provides bumping, probe test, back-end, and WLCSP services for DDI, CIS, AP and PMIC used in electronic devices such as TVs, monitors, and mobile phones. We have continuously developed and evolved our technology since the company's founding in 2000.

Website www.lbsemicon.com
Facebook www.facebook.com/lbsemicon
LinkedIn www.linkedin.com/company/lbsemicon
Youtube www.youtube.com/@lbsemicon

Global No.1! Total Test Solution Provider!



BURN-IN SOCKET SOLUTIONS
iSB
- No ball damage
- Direct inserting on Burn In Board without soldering
- No damage on Burn In Board land
- Simple structure without sub PCB & easy maintenance

POGO SOCKET SOLUTIONS
iSP
- Various design available
- Excellent gap control & long lifespan
- High bandwidth & low contact resistance
- Adjustable Impedance
- Fully Metal Shielding

Hi-fix & Burn In Board
iSTCU
- High performance and competitive price
- Test fine pitch, high speed device at hot & cold temperature
- Customized design to meet individual requirements

ELASTOMER SOCKETS & INTERPOSERS
iSC
- High performance and competitive prices
- High speed & RF device capability
- No load board pad damage & no contact trace on the ball
- Customized design to meet challenging budget constraints
- Full thermal and electrical simulation

ISC Connector
iSCON
- ISC Connector Solutions solve many problems across a wide range of circuit sizes, configurations, pitch, and PCB-attach terminations.
- Designed to have the strong resistance against torque forces on mating area to achieve the high reliability in the natural fall shock.

THERMAL CONTROL UNIT
iSTIU
- Extreme active temperature control
- Customized design to meet challenging requirements
- Price competitiveness through self designing and fabrication
- Safety auto shut down temperature monitoring of the device & thermal control unit
- Full FEA analysis for strength, deflection, air flow and any other critical requirements

CONTACT	ISC HQ	ISC International	Tel: +82 31 777 7675 / Fax : +82 31 777 7699
ISC CO., LTD	Seong-nam, Korea	Siliconvalley, CA	Email:sales@isc21.kr / Website: www.isc21.kr

Illumination inspection technology for defect detection on advanced IC substrates

By Cheolkyu Kim, Burhan Ali, JungHyun Kim [Onto Innovation]
Jong Eun Park, Misun Hwang, Chan Jin Park, [Samsung Electro-Mechanics (SEMCO)]

Across the semiconductor industry, advanced integrated circuit (IC) substrate (AICS) supplies are low. The causes vary, from a limited number of suppliers who can meet performance requirements, to constrained production capacities, and increased demand resulting from the adoption of high-performance mobile devices, as well as advanced technologies like artificial intelligence (AI) and high-performance computing (HPC). And without question, the ongoing shortage of Ajinomoto build-up film (ABF), a necessary component of many AICS, plays a significant role as well. One area where this shortage of ABF and AICS is having a significant impact is in the manufacturing of flip-chip ball-grid array (FC-BGA) packages—the most advanced substrates to meet the electrical and thermal requirements for IC chips with high numbers of I/Os.

To address the substrate shortage, suppliers of FC-BGA substrates are ramping up capacity. However, that acceleration comes with high costs due to the fact that the AICS process is burdened by low yields resulting from the presence of defects that are left undetected by many macro inspection systems. Furthermore, that inability to detect certain defects is potentially magnified as each new layer of ABF on the FC-BGA substrate is built up. In some cases, the number of layers of build-up may reach 20. With each additional layer, the potential for killer defects increases, whether the cause is ABF residue in laser-drilled vias, poor dry-film resist development, or the under- and over-etching of Cu seed.

For advanced packaging houses, addressing this issue is a matter of considerable interest. After all, few businesses are not interested in reducing waste and cost, while more efficiently utilizing an in-demand resource in short-supply, like ABF. Fortunately, optical inspection technologies are available that can discover these difficult-to-detect defects. In this article we will discuss a proven macro inspection technology that is uniquely capable of finding defects and errors in AICS.

Inspection challenges

Before we move forward, let's reexamine why ABF has become an important component in manufacturing AICS. In an AICS, specifically those made for FC-BGA, Cu is used for electrical connections and ABF is used for insulation (**Figure 1**). ABF is a compound material of epoxy polymer matrixes and inorganic fillers. The chemical and electrical properties of epoxy polymer can be easily tailored by changing chemical components to meet various material requirements [1]. Another advantage of ABF is that it facilitates the formation of fine-pitch lines/spaces because its surface is receptive to laser processing and direct copper plating. This advantage, in part, makes ABF an ideal material for devices where miniaturization is a driving force for innovation. For pattern formation on the build-up layers of IC substrate, dry film is commonly used together with a semi-additive process to achieve copper lines down to 5µm/5µm or smaller lines/spaces in laminated substrates.

Because the main function of an IC substrate is to create an electrical connection between the IC and circuit board, the most serious process issues are shorts or open circuits, both of which require inspection tools to find defects. For example, poor dry-film development leads to bad patterning, which, in turn, leads to poor or bad signal integrity. Meanwhile, during the curing process, particles or bubbles under laminated ABF can cause pattern distortions. Left after the formation of vias through the ABF by laser ablation,

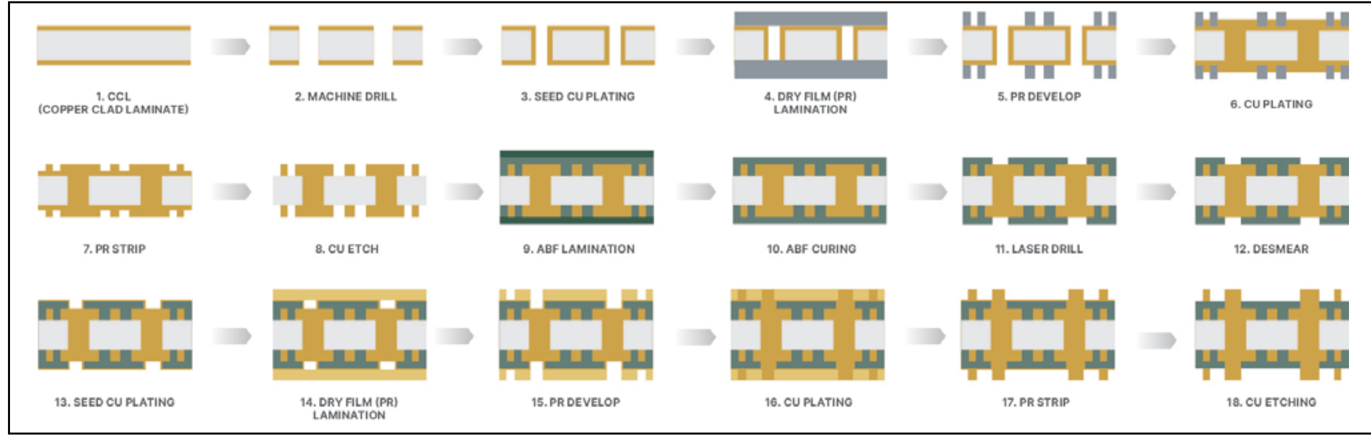


Figure 1: Typical flow of an advanced substrate process. Steps 9 through 18 are repeated for multi-layer buildup.

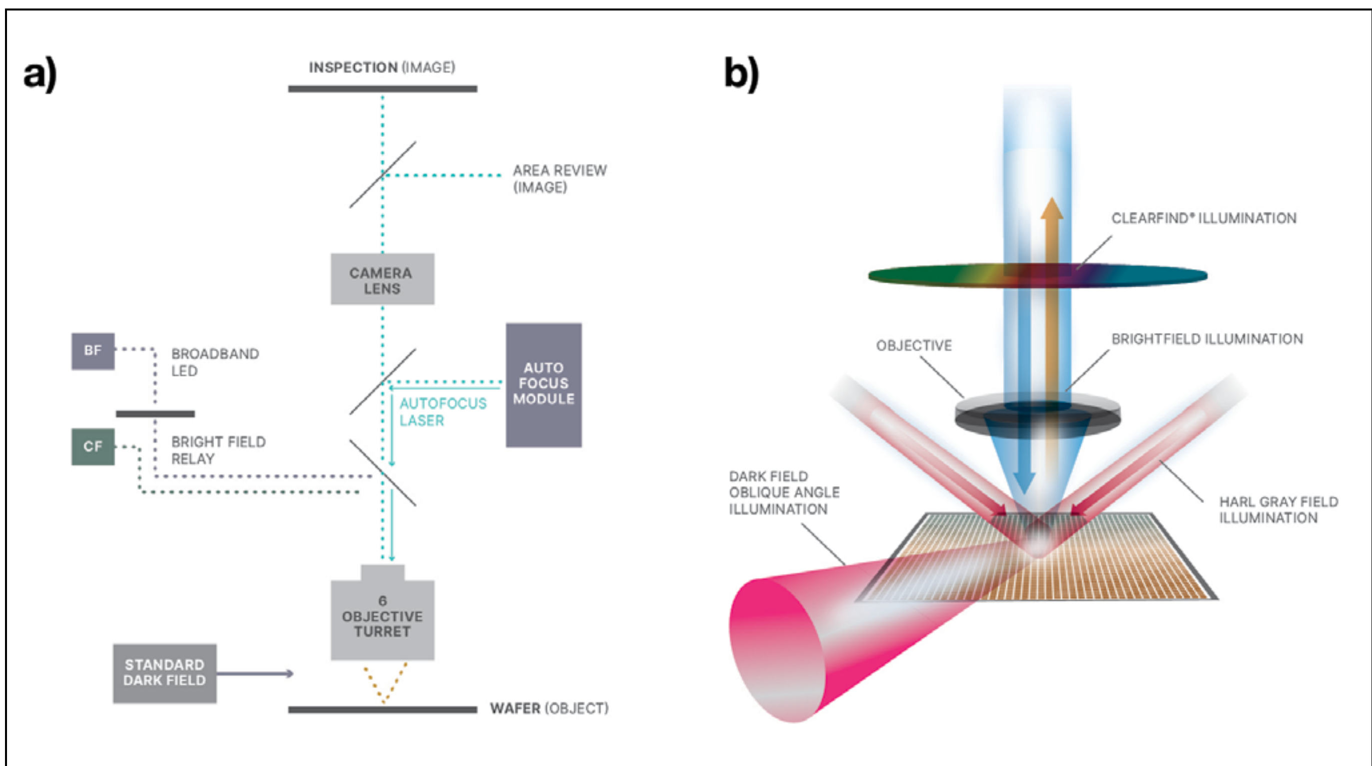


Figure 2: Schematic of inspection optics: a) Conventional macro inspection setup; and b) CF inspection setup.

residual ABF can also affect the integrity of the electrical signal. Etching the Cu seed layer is the final process step of each build-up layer; this step defines the routing of Cu trace lines. Under- or over-etching the Cu seed layer can lead to shorts and open circuits. Preventing shorts and open circuits is a critical issue when addressing decreases in yield.

Conventional macro inspection is typically done using one of two techniques: bright-field (BF) and dark-field (DF) illumination (Figure 2a). Both BF and DF techniques use light-emitting diode (LED) sources that cover the visible wavelength region. In BF illumination, the camera objective and illumination source are positioned on a common axis perpendicular to the surface of the substrate so that the camera sees the specular reflection of the source illumination. Therefore, the BF image is formed by the reflected light from the sample and is therefore a strong function of light attenuation and reflection between differing materials on the sample. In DF illumination, the camera is positioned away from the direction of the specular reflection of the illumination source. On a flat, mirror-like surface, the specular reflection from the substrate is directed away from the camera, and the field becomes dark. But any particle or surface irregularity that

scatters light out of the specular beam will make the field bright. This characteristic makes DF illumination particularly good at identifying small particles and defects on a flat specular surface.

We also used another inspection illumination technology, Clearfind® (CF). The optical path of this technology is also shown in **Figure 2b**, but **Figure 3** illustrates in more detail how this technology works. The light source for this new illumination technology is a monochromatic blue laser with a stable wavelength and output power. The laser beam is collimated and expanded into a horizontal line at the sample and then scanned over the surface. Stimulated by illumination, the sample either reflects the light from the source, or emits secondary photons of lower energy, depending on the types of materials involved. Metals have continuous energy bands in the visible wavelength regions and will either absorb or reflect incident photons. Organic materials, such as polymers, exhibit distinctive optical properties that are not present in the metals or common inorganic materials used in IC substrate manufacturing. These properties tend to be unique to organic molecules displaying a high degree of conjugation, such as polycyclic aromatic hydrocarbons, and in linear or branched chain organic polymers with multiple regularly interspersed pi bonds [2]. The emission from the organic surface tends to be anisotropic and, therefore, less sensitive to surface topography that could potentially direct most ordinary BF- or DF-reflected light away from the detector. Moreover, photons of the same energy are blocked by the filter; as a result, any reflection or scattering from the metal surface cannot be collected by the imaging camera. This results in increased sensitivity to organic residue and reduced sensitivity to interference from the surrounding features.

The method described above has the additional advantage of being relatively insensitive to signal variations caused by metal grains. The new technology has been found to be very effective in detecting invisible defects on fan-out wafer-level packaging (FOWLP) and fan-out panel-level packaging (FOPLP) [3,4]. In our investigation, we employed a high-speed, near-infrared laser-triangulation autofocus system that maintains a constant distance between the imaging optics and the area being scanned to keep the image focused. Imaging is accomplished using a high-resolution line scan camera. The image pixel size corresponds to 0.7µm at 10X, which provides the highest level of magnification for inspection.

Via inspection

ABF is a widely-used insulating dielectric in advanced IC substrates used for FC-BGA. To make electrical connections between layers, vias are formed by high-energy ultraviolet (UV) lasers. Occasionally, ABF is not completely removed from the via, which results in a poor electrical connection through the via and, in turn, negatively affects signal integrity. Therefore, inspecting the via after laser ablation is necessary to find such defects (Step 12

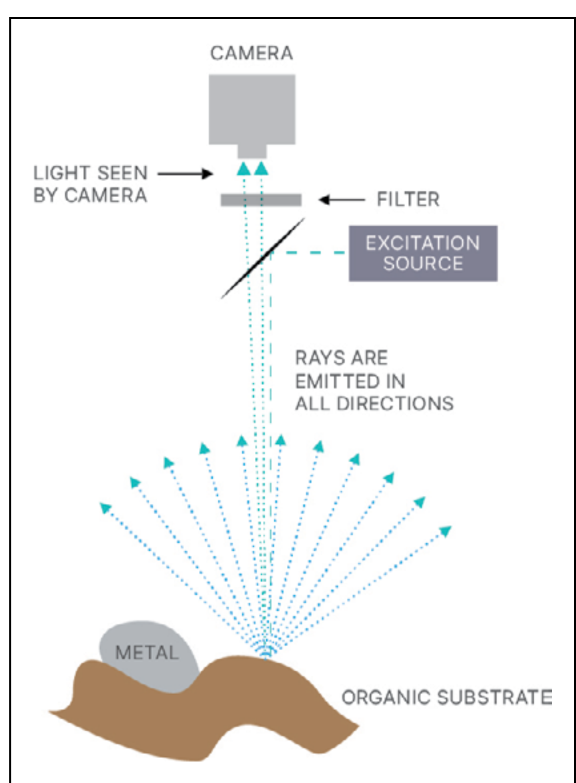


Figure 3: Illustration of CF technology.

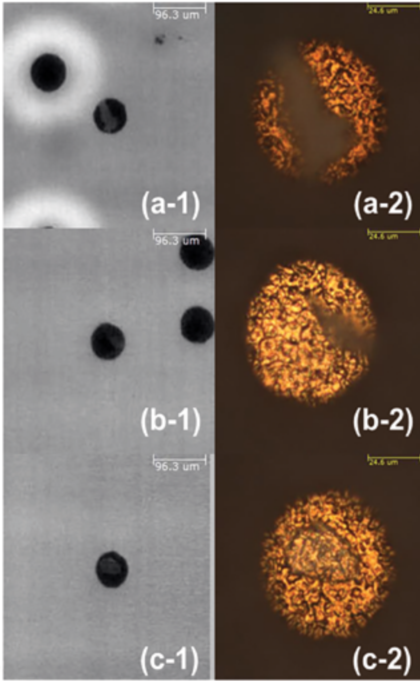


Figure 4: Images of vias with ABF residue. The left three images are those using CF illumination, while the right three images are corresponding images, but with BF color illuminations at higher magnification.

in Figure 1). Figure 4 shows example images of vias with ABF residue. The left three images are those using Clearfind® illumination, while the right three images are corresponding images but with BF color illuminations at higher magnification.

For examples (a-1) and (a-2) shown in Figure 4, the residue is detectable using either CF or BF technology. For the CF image examples of (b-1) and (c-1), residual ABF inside the vias is easily detectable because secondary photons from the residual ABF are brighter than the rest of the Cu, which does not emit secondary photons. However, in the case of the corresponding BF images of (b-2) and (c-2), the area of residue in the image can be easily confused with the via bottom. This is because the surface of the bottom of the via is rough Cu—and because of the grainy structure of the Cu, this image is very similar to images of ABF residue. These example images clearly demonstrate that the new illumination technology is more robust for leftover ABF residue in vias.

Visit us on our website
www.e-tec.com
NEW
in the Test Socket World:
E-tec
Interconnect
E-tec Interconnect is pleased to present its new Clamshell Open Top Socket
• **High reliability** up to 500k insertion cycles
• **High frequency** up to 27 GHz in pogo pin (up to 40GHz validated, with Elastomeric contact technology)
• Thru-hole technology, SMT, Solderless Type
Also pluggable into adapter MiniGridSocket series (see E-tec catalog TS01)
• All kinds of packages, even your latest special custom packages
Flat Pack PGA LGA Ceramic spatial LCC BGA QFN / Power QFN Custom
E-Tec Interconnect AG, Mr. Pablo Rodriguez, Lengnau Switzerland
Phone : +41 32 654 15 50, E-mail: p.rodriguez@e-tec.com
EP Patents 0897655, 1385011, 0829188, US Patents 6249440, 6190181, 6390826 and Patents in other countries

After-development inspection: dry resist film

To create circuit patterns on each build-up layer of the IC substrate, a dry-film resist is laminated and developed on a Cu seed layer, as shown in process steps 14 and 15 in Figure 1. Any process excursion during development will lead to poor circuit patterning. Figure 5 shows an image of an organic defect after dry-film resist development. All four images show defects at the same site but with different illuminations. The BF image does not show any defects, while the DF and Clearfind® images do. It should be noted that not all the defects found with DF are seen in the CF image. This is because DF illumination is sensitive to scattering from various particles, while CF illumination is sensitive to organic defects only. The DF image shows vias because of a difference in scattered light intensity, while CF cannot identify the difference between vias and the Cu seed layer because neither of these emits secondary photons, causing both regions to appear dark. Therefore, the best illumination technique to find defects after dry-film resist development is to use both DF and CF illumination simultaneously, as shown on the bottom right of Figure 5.

Figure 6 shows another defect example after dry-film resist development. All four images show defects at the same site but with different illuminations. In this case, Clearfind® technology images do not indicate defects. This is an indication that these defects are either metallic or inorganic dielectrics. Considering the stage in the process flow in which these defects are identified, it is very likely that these are metallic defects. The BF image indicates some defects, but with relatively low contrast, while the DF image clearly shows all defects. As we have seen, CF illumination is very effective in finding organic defects, and we believe a combination of it and DF illumination together offers the best illumination tool for the inspection of dry-film resist after development.

After-etch inspection: Cu seed

After the dry-film resist is developed, the substrate goes through Cu plating to form Cu trace lines for the circuit, and then the dry-film resist is removed by stripping. At this stage, all Cu trace lines are connected by a Cu seed layer that needs to be etched to complete circuits as designed. During the process, under-etching may cause shorts, while over-etching may cause open circuits.

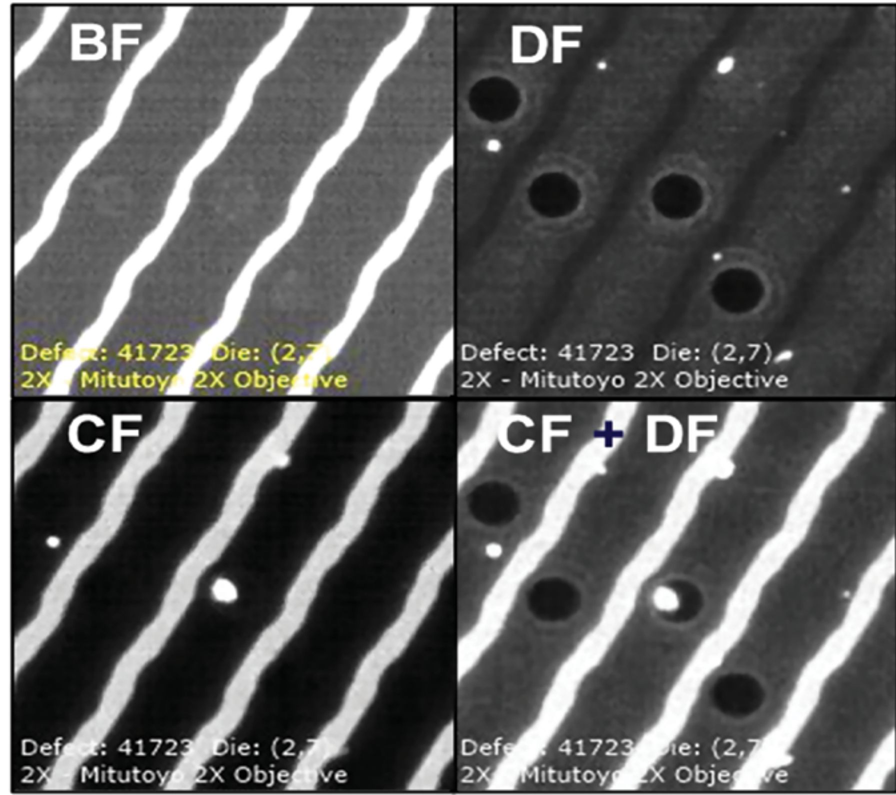


Figure 5: Organic defects after dry-film resist development inspection. All four images show defects at the same site but with different illuminations, as indicated in the panels.

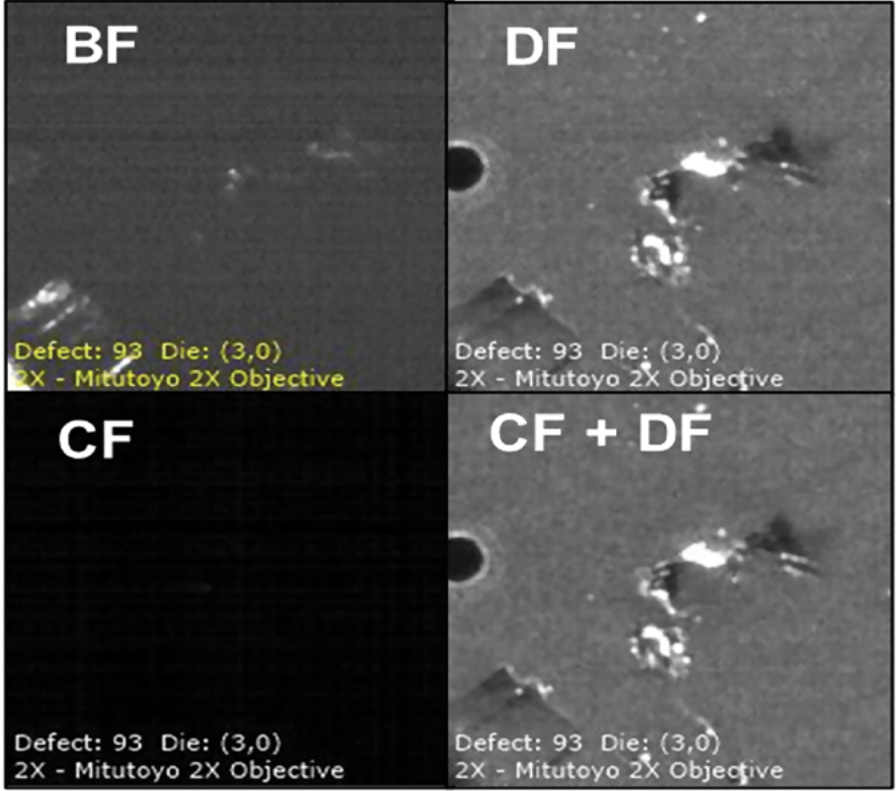


Figure 6: Inorganic defects after dry-film resist development inspection. All four images show defects at the same site but with different illuminations, as indicated in the panels.

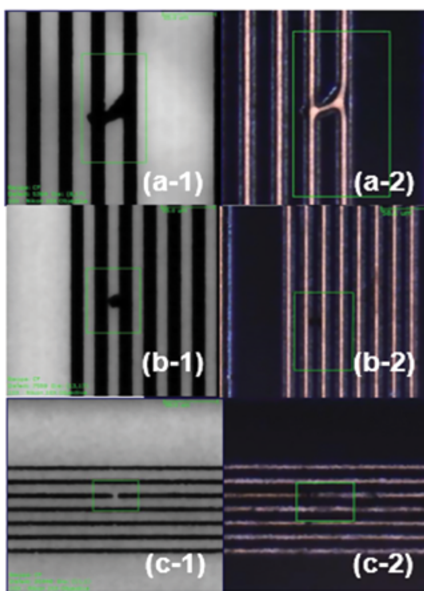


Figure 7: Three different defects for after-etch inspection of the Cu seed layer. The three images on the left are from using CF inspection, while the three images on the right are corresponding images captured with a BF color camera at higher magnification.

For residual Cu seed, if the residual Cu seed extends to 30% or more into the space between the Cu trace lines, it is considered to be a critical defect.

Figure 7 shows three different defects for after-etch inspection of the Cu seed layer. The three images on the left are from using CF inspection, while the three images on the right are corresponding images captured with a BF color camera at higher magnification. The two top images, (a-1) and (a-2), show a short circuit defect that could be easily detected with either CF or BF illumination. For the two images in the middle, (b-1) and (b-2), the defect was very clear in CF, but was not seen in BF. This is because the top flat surface of the Cu trace line only reflects light to the detector, making the area bright, while the reflection is very weak from Cu in the sloped area or from the thin and rough surface of the Cu residue. The CF technology image (c-1) clearly shows an open circuit, while an open circuit is not obvious in the corresponding BF color image (c-2). This is because the surface of Cu trace lines tend to become very rough and grainy after the etching process, making any brightness variation of the Cu line significant. In addition, any dark regions of the Cu lines can be easily mistaken for open circuits. Because the CF image is insensitive to the rough or grainy surface of metal, it is the most robust inspection technology for the after-etch inspection of Cu.

DL TECHNOLOGY
Precision Dispensing Accessories

LEADERS IN MICRO DISPENSING TECHNOLOGY

SMALL REPEATABLE VOLUMES ARE A CHALLENGE, BUT NOT IMPOSSIBLE IF YOU HAVE BEEN CREATING THEM AS LONG AS WE HAVE.

TO DO IT WELL, WE PROVIDE THREE THINGS:

Dispensing Expertise in a variety of microelectronic packaging applications.

Feasibility Testing & Process Verification based on years of product engineering, material flow testing and software control.

Product Development for patented valves, dispensing cartridges, needles, and accessories.

Our Micro Dispensing product line is proven and trusted by manufacturers in semiconductor, electronics assembly, medical device and electro-mechanical assembly the world over.

www.dltechnology.com.

216 River Street, Haverhill, MA 01832 • P: 978.374.6451 • F: 978.372.4889 • info@dltechnology.com

Summary

In this article, we have compared inspection images with various illumination techniques for the inspection of ABF via residue, dry-film resist after development, and Cu seed after etching. For the inspection of via residue following the laser ablation of ABF, Clearfind® technology was found to be the most effective tool for identifying residue. For the inspection of dry-film resist after development, the simultaneous use of CF and DF illumination was the best choice because the former technology could easily find under-developed dry-film resist or residue inside the via, and DF could find metallic defects in the Cu area. Regarding inspection after the Cu seed etching process, CF illumination was the most efficient inspection technology because it clearly shows open or short defects without showing false defects that may come from rough and grainy surfaces when inspected by BF or DF.

Acknowledgments

The authors wish to express their sincere thanks to Dong-Heon Kang at Samsung Electro-Mechanics, and Wesley Chou and Kazuko Jochi at Onto Innovation, for their valuable discussions.

References

1. H. Hichri, et al., "Fine line routing and micro via patterning in ABF enabled by excimer laser ablation," IMAPS, Oct. 2017, pp. 113-119.
2. D. C. Harris, M. D. Bertolucci, *Symmetry and Spectroscopy*, Dover Publications, New York, 1978, pp. 307-418.
3. G. Singh, "Reveal previously invisible defects and contaminants in advanced packaging applications," *Solid State Technology*, Nov./Dec. 2017, pp. 11-15.
4. W. Young Han, "Reveal invisible defects on large 600mm panels," *Chip Scale Review*, Jan./Feb. 2021, pp. 39-43.

Biography

Dr. Cheolkyu Kim is a Senior Director of Applications at Onto Innovation, Wilmington, MA USA. Prior to joining Onto, Kim was a postdoctoral research associate in the Physics Department of Brown U. He received a PhD in Physics from the U. of Rhode Island and a Master's degree in Physics Education from Seoul National U., Seoul, Korea. His research has been published in various scientific journals. Email Cheolkyu.Kim@ontoinnovation.com

INTERNATIONAL DIRECTORY OF DEFECT INSPECTION SYSTEMS

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication

COMPANY HEADQUARTERS	OPTICAL INSPECTION	X-RAY INSPECTION	ACOUSTIC INSPECTION
Company Street Address City, State, Country Telephone Website *Advertisers within the calendar year are indicated by listings in bold text*	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) BP - Broadband Plasma LS - Laser Scanning PR - Programmable NP - Non-Programmable MP - Max Product Size PL - Panel CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board
Akrometrix, LLC 2700 NE Expressway Bldg. B, Ste. 500 Atlanta, GA 30345 USA Tel: +1-404-486-0880 www.akrometrix.com	3D (TherMoire) PR MP - 600+ mm WFR, PKG, SUB, PCB		
ASC International, Inc. 830 Tower Drive, Suite 200 Medina, MN 55340 USA Tel: 1-763-479-6210 www.ascinternational.com	3D PR, NP MP - 450+ mm SDP, SUB, PCB		
Bruker Corporation 40 Manning Road Billerica, Massachusetts 01821 USA www.bruker.com/en/products-and-solutions/semiconductor-solutions/x-ray-defect-inspection	2D, 3D PR MP - 300+ mm WFR, PKG		
Camtek Ltd. Ramat Gavriel Ind. Zone HaArig St 10 Migdal HaEmek 2309407 Israel Tel: +972-4-604-8100 www.camtek.com	2D, 3D PL PR MP 300mm WFR, PKG, SUB		
Comet Yxlon GmbH Essener Bogen 15 22419 Hamburg Germany Tel: +49 40 52729-0 www.yxlon.comet.tech		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Creative Electron, Inc. 201 Trade Street San Marcos, CA 92078 USA Tel: +1-760-752-1192 www.creativeelectron.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
CyberOptics Corporation **5900 Golden Hills Drive** **Minneapolis, MN 55416 USA** **Tel: +1-763-542-5000** **www.cyberoptics.com**	3D PR MP - 450+ mm SDP, SUB, PCB		
EV Group **DI Erich Thallner Strasse 1** **St. Florian am Inn A-4782, Austria** **Tel: +43-771-253110** **www.evgroup.com**	(X,Y,Z) - CM PR, NP MP - 300 mm WFR (BONDED)		
GE Research 1 Research Circle Niskayuna, NY 12309 USA www.ge.com/research/technology-domains/electronics-sensing/microelectronics		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Glenbrook Technologies, Inc. 11 Emery Avenue Randolph, NJ 07869 USA Tel +1-973-361-8866 www.glenbrooktech.com		2D NP MP - 600+ mm PKG, SUB, PCB	

Compiled by Chip Scale Review • Submit all Directory inquires and updates to directories@chipscalereview.com

INTERNATIONAL DIRECTORY OF DEFECT INSPECTION SYSTEMS

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication

COMPANY HEADQUARTERS	OPTICAL INSPECTION	X-RAY INSPECTION	ACOUSTIC INSPECTION
Company Street Address City, State, Country Telephone Website *Advertisers within the calendar year are indicated by listings in bold text*	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) BP - Broadband Plasma LS - Laser Scanning PR - Programmable NP - Non-Programmable MP - Max Product Size PL - Panel CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board
Göpel Electronic GmbH Göschwitzer Strasse 58/60 Jena D-07745, Germany Tel: +49-0-36-416896-0 www.goepel.com	3D PR MP - CM PKG, SUB, PCB	2D PR MP - CM PKG, SUB, PCB	
HANMI Semiconductor Co., Ltd. 532-2 Gajwa-Dong, Seo-Gu Incheon, 404-250, South Korea Tel: +82-32-571-9100 www.hanmisemi.com	2D, 3D CM MP - CM PKG, SUB, PCB		
Hitachi High-Tech Toranomon Hills Business Tower 1-17-1 Toranomon, Minato-ku Tokyo 105-6409, Japan Tel: +81-029-276-6391 www.hitachi-hightech.com/global/en/products/semiconductor-manufacturing/cd-sem/			3D PR MP - 360 mm WFR, PKG, SUB, PCB
Intekplus Co., Ltd. (Tamnip-dong), 263, Yuseong-gu Daejeon, Korea (34026) Tel: +82-42-930-9900 www.intekplus.com	2D, 3D PR MP - CM SDP, PKG, SUB, PCB		
KLA Corporation Three Technology Drive Milpitas, CA 95035, USA Tel: +1-408-875-3000 www.kla.com	2D, 3D LS, PR, NP MP - CM WFR, PKG, SUB		
Koh Young Technology Inc. 14F Halla Sigma Valley 53 Gasandigital 2-ro, Geumcheon-gu Seoul 08588 Republic of Korea www.kohyoung.com	3D PR MP - 810 mm PKG, SDP, SUB, PCB		
Landrex Technologies Co., Ltd. No.570, Jianguo Rd., Yingge Dist., New Taipei City 239 Taiwan (R.O.C.) Tel: 886-2-26787966 www.landrex.com.tw	CM PR CM WFR, SUB, PCB		
Lloyd Doyle Ltd. Molesey Road, Walton on Thames Surrey KT12 3PI, England Tel: +44-1932-245000 www.lloyd-doyle.com	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB		
Machine Vision Products Inc. 3270 Corporate View, Suite D Vista, CA 92081 USA Tel: +1-760-438-1138 www.visionpro.com	3D PR MP - 600+ mm PKG, SDP, SUB, PCB		
Machvision Inc Co., Ltd. NO. 2-3, Gongye East 2nd Road II, Hsinchu Science Park, Hsinchu 30075, Taiwan (R.O.C) Tell: +886-3-563-8599 www.machvision.com.tw	2D, 3D PR, NP MP - 600+ mm SUB, PCB		

Compiled by Chip Scale Review • Submit all Directory inquires and updates to directories@chipscalereview.com

iPIS-HX Series Realizes the Cutting-Edge Technology Inspection Solution for Heterogeneous Integration

	Budgetary iPIS-140HX	Advanced iPIS-240HX	Flag-Ship iPIS-340HX
Inspection Package	TSOP / LDP / QFP / BGA / BOC / QFN / uSD CARD etc.		
Vision System	2D/3D Bottom, 2D Top, 3D Top(Option), 4 Side(Option)		
Advanced Feature	· High Productivity · Cost Effective	· Solution for Heterogeneous Integration PKG · High Resolution and Wide FOV · Stitching (240+ & 340)	
Option	· Double Device · Multi Pad Technology · AI Deep Learning Solution		

Features

- Prominent Vision Inspection Quality
- Pick & Place Handling Method
- Capability to handle full Coverage Package Size
- Provision for AI Deep Learning Technology
- Applied Multi Pad Technology

INTEKPLUS CO., LTD.

#263, Techno 2-ro, Yuseong-Gu, Daejeon, 34026 Korea
Tel : +82-42-930-9900 Fax : +82-42-930-9999

For more information
www.intekplus.com / sales1@intekplus.com

INTERNATIONAL DIRECTORY OF DEFECT INSPECTION SYSTEMS

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication

COMPANY HEADQUARTERS	OPTICAL INSPECTION	X-RAY INSPECTION	ACOUSTIC INSPECTION
Company Street Address City, State, Country Telephone Website *Advertisers within the calendar year are indicated by listings in bold text*	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) BP - Broadband Plasma LS - Laser Scanning PR - Programmable NP - Non-Programmable MP - Max Product Size PL - Panel CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board
Mars Tohken Solutions Co. Ltd. Shinjuku-gyoen Muromachi Bldg 1-8-5, Shinjuku, Shinjuku-ku Tokyo 160-0022, Japan Tel: +81 3 3352 8537 www.mars-tohken.co.jp/en		2D, 3D PR MP - 400 mm WFR, PKG, SUB, PCB	
Microtronic Inc. 171 Brady Avenue Hawthorne, NY 10532 USA Tel: 1-877-642-7687 www.microtronic.com	2D PR, NP MP - 300 mm WFR		
MIRTEC USA 3 Morse Road Oxford, CT 06478 USA Tel: +1 203-881-5559 www.mirtecusa.com	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB		
Nanotronics Imaging Inc. New Lab – Building 128 63 Flushing Ave, Unit 241 Brooklyn, NY 11205 USA www.nanotronics.co	2D, 3D PR MP – 200 WFR		
Nikon Precision Europe GmbH Robert-Bosch-Str. 11 63225 Langen Germany Tel. +49 61 03 9 73-0 www.nikonprecision.com/products-and-technology/semiconductor-inspection-systems	2D, 3D PR, NP MP - 600+ mm WFR, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Nordson Test and Inspection 28601 Clemens Road Westlake, OH 44145-4551 USA Phone: +1 440.892.1580 www.nordson.com/en/divisions/test-and-inspection	2D, 3D PR, NP MP - 600+ mm SDP, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm WFR, PKG, SUB, PCB	
North Star Imaging Inc. 19875 S Diamond Lake Road Rogers, MN 55374 USA Tel: +1-763-312-8836 www.4nsi.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Onto Innovation 16 Jonspin Road Wilmington, MA 01887 USA Tel: +1 978-253-6200 www.ontoinnovation.com	2D, 3D LS, PR MP - 600+ mm PL WFR, SUB		
PVA TePla Analytical Systems GmbH Deutschordenstrasse 38 73463 Westhausen, Germany Tel: +49-7363-9544 0 www.pvatepla-sam.com			3D PR MP - 420 mm WFR, PKG, SUB, PCB

Compiled by Chip Scale Review • Submit all Directory inquires and updates to directories@chipscalereview.com

INTERNATIONAL DIRECTORY OF DEFECT INSPECTION SYSTEMS

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication

COMPANY HEADQUARTERS	OPTICAL INSPECTION	X-RAY INSPECTION	ACOUSTIC INSPECTION
Company Street Address City, State, Country Telephone Website *Advertisers within the calendar year are indicated by listings in bold text*	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) BP - Broadband Plasma LS - Laser Scanning PR - Programmable NP - Non-Programmable MP - Max Product Size PL - Panel CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board
Quality Vision International, Inc 850 Hudson Avenue Rochester, NY 14621 USA www.viewmm.com	2D, 3D PR, NP MP - 300+ mm SDP, PKG, SUB, PCB		
Saki Corporation DMG MORI Tokyo Digital Innovation Center 3-1-4, Edagawa, Koto-ku, Tokyo 135-0051 Japan Tel. +81(0)3-6632-7915 www.sakicorp.com/en/company/ technology/3daxi_tec	CM PR MP - 500 mm SDP, SUB, PCB	2D, 3D PR MP - 510 mm WFR, PKG, SUB, PCB	
ScanCAD International 26437 Conifer Road Conifer, CO 80433 USA Tel: +1-303-697-8888 www.scancad.net	2D PR, NP MP - 600+ mm SDP, PKG, SUB, PCB		
Scienscope International 5751 Schaefer Avenue Chino, CA 91710 USA Tel: +1-909-590-7273 www.scienscope.com		2D, 3D PR MP - 1,375 mm WFR, PKG, SUB, PCB	
SEC Co.,Ltd 111, Saneop-ro 155beon-gil Gwonseon-gu, Suwon-si Gyeonggi-do, Korea, 16648 Tel: 82-31-215-7341-2 www.seceng.co.kr		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Semilab Semiconductor Physics Laboratory Co. Ltd. Address: Prielle Kornélia u. 4/A. H-1117 Budapest, Hungary Tel.: +36 1 505 4690 www.semilab.com/hu			
Sonix Inc. **8700 Morrissette Drive** **Springfield, VA 22152 USA** **Tel: +1-703-440-0222** **www.sonix.com**			3D PR MP - 350 mm WFR, PKG, SUB, PCB
SUSS MicroTec SE **Schleissheimer Str. 90** **85748 Garching** **Germany** **Tel:+49 89 32007-0** **www.suss.com**	2D, 3D PR, NP MP - 300 mm WFR (BONDED)		
Teradyne, Semiconductor Test Division 600 Riverpark Drive North Reading, MA 01864 USA Tel: +1-978-370-2700 www.teradyne.com/products/semiconductor-test		2D, 3D PR, NP MP - 450+ mm PKG, SUB, PCB	

Compiled by Chip Scale Review • Submit all Directory inquires and updates to directories@chipscalereview.com

INTERNATIONAL DIRECTORY OF DEFECT INSPECTION SYSTEMS

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication

COMPANY HEADQUARTERS	OPTICAL INSPECTION	X-RAY INSPECTION	ACOUSTIC INSPECTION
Company Street Address City, State, Country Telephone Website *Advertisers within the calendar year are indicated by listings in bold text*	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) BP - Broadband Plasma LS - Laser Scanning PR - Programmable NP - Non-Programmable MP - Max Product Size PL - Panel CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	2D - 2 Dimension (X,Y) 3D - 3 Dimension (X,Y,Z) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board
Test Research Inc. 7F., No.45, Dexing West Road., Shilin District Taipei City 11158, Taiwan Tel: +886 2 28328918 www.tri.com.tw	2D, 3D PR, NP MP - 600+ mm SDP, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Toray Engineering Co., Ltd 6th Floor, Yaesu Ryumeikan Building 1-3-22 Yaesu, Chuo-ku Tokyo, 103-0028, Japan Tel: +81+3+3241-1541 www.toray-eng.com	3D PR MP - 300 mm WFR		
VI Technology (Mycronic AB) Rue de Rochepleine 38120 Saint Egrève France Tel: +33 4 7675 8565 www.vitechnology.com	2D, 3D PR MP - 600+ mm SDP, PKG, SUB, PCB		
Veeco Instruments Inc. 3050 Zanker Road San Jose, CA 95134 USA Tel: +1 408 321-8835 www.veeco.com	2D, 3D LS, PR, NP MP - CM SDP, PKG, SUB, PCB		
Viscom AG Carl-Buderus-Straße 9 - 15 30455 Hanover Germany Tel: +49 511 94996-0 www.viscom.com	2D, 3D PR, NP MP - 508 mm, 660mm, 750mm (optional 2000mm) PKG, SDP, SUB, PCB	2D, 3D PR, NP MP - 450mm, 610mm, 722mm PKG, PCB, SPD	
Vitrox Corporation Berhad 746, Persiaran Cassia Selatan 3 Batu Kawan Industrial Park 14110 Bandar Cassia Penang, Malaysia Tel: +60-4-545 9988 www.vitrox.com	2D, 3D PR, NP MP - 762 mm SDP, PKG, SUB, PCB	3D PR MP - 609 mm WFR, PKG, SUB, PCB	
VJ Group Inc. 89 Carlough Road Bohemia, NY 11716, USA Tel: +1-631-589 8800 www.vjt.com/industries/electronics		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Zeiss SMT, Inc. 75 Sylvan St., Suite 101 Danvers, MA 01923 USA www.zeiss.com/semiconductormanufacturing-technology	2D, 3D LS, PR, NP MP 300+mm, PL WFR, PKG, SDP, SUB, PCB	2D, 3D PR, NP MP – 600+mm WFR, PKG, SDP, SUB, PCB	
Zygo Corporation Laurel Brook Road Middlefield, CT 06455 USA Tel: +1-860-347-8506 www.zygo.com	2D, 3D PR, NP MP - CM SDP, PKG, SUB, PCB		

Compiled by Chip Scale Review • Submit all Directory inquires and updates to directories@chipscalereview.com

$Si\text{-}LtTaO_3$

$ZrO_2\text{-}Gl$

SiC-Gl

< 200 °C

< 5 min

EXCLUSIVELY OFFERING:
IMPULSE CURRENT BONDING

SUSS MicroTec's manual and automatic wafer bonder systems bring to bear a novel game changing bonding technology. Impulse Current Bonding (ICB) combines the robustness of Anodic Bonding with the material versatility of more complex bonding methods. It allows for the bonding of materials with different coefficients of thermal expansion as well as alkali-free field-assisted bonding. Due to high interatomic diffusion at the material interface a strong and durable bond is achieved at low temperatures.

Contact us for more information!

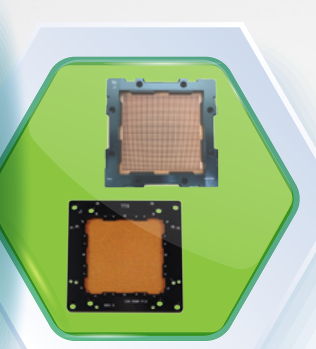
SUSS MicroTec
info@suss.com
www.suss.com

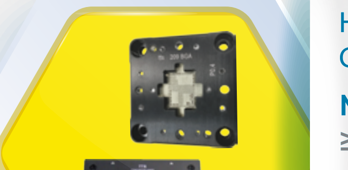
HIGH PIN COUNT SOLUTION

Min. Pitch
≥0.90mm

Pin Count
≤10,000

Coplanarity
<0.35mm





HIGH SPEED COAXIAL

Min. Pitch
≥0.40mm

Insertion Loss
>40GHz@-1dB

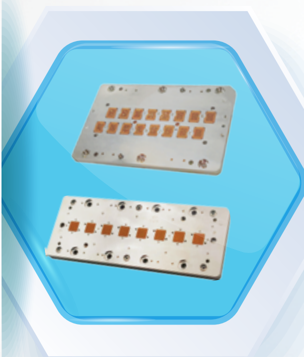
Crosstalk
>35GHz@-52dB

WLCSP SOLUTION

Min. Pitch
≥0.15mm

Pin Count
≤6000

Longevity
>1000K



PROBE PIN

Min. Pitch
≥0.15mm

High Power
≤6.5A

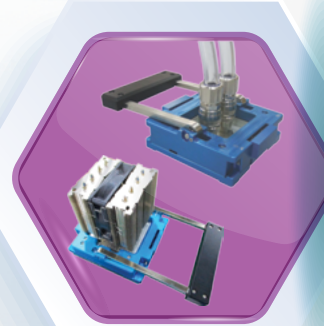
High Frequency
>140GHz

RF & mmWAVE SOLUTION

Min. Pitch
≥0.40mm

Insertion Loss
>60GHz@-1dB

Return Loss
>30GHz@-20dB



HAND SOCKET LID

Heatsink
<100W

Heatpipe
100W - 1000W

Liquid Cooling
300W - 1500W

Slipping IC package design schedules and what to do about it

By Keith Felton [Siemens Digital Industries Software]

Several factors are causing advanced packaging design schedules to slip to a perilous degree. This article enumerates five factors that cause increasing design cycles and presents five workflows to get around them and get IC packaging design work back on track.

Designs are getting more complex

First, as with all semiconductor designs, increasing complexity continues to create new challenges for package design, verification, and modeling. Packages are now heterogeneous integration (HI) platforms and are no longer simply a connector between a chip's IO pads or bumps and a printed circuit board (PCB). The goal of an HI platform is to integrate, connect, and optimize multiple dies together. These could include application-specific integrated circuit (ASIC) logic, chiplets, memory, voltage regulators, and discrete components that can be mounted and interconnected into a single package using high-speed, high-bandwidth chiplet-to-chiplet interfaces. The resulting HI assembly can deliver greater performance at a reduced cost and higher yield, with only a slightly larger footprint than a traditional monolithic system on chip (SoC). There is also an emerging trend to include embedded logic, voltage regulators, and capacitors within the package substrate.

As a result of the above developments, the first problem advanced packaging designers may face in dealing with this complexity lays at the feet of their existing legacy design tools—tools developed for single-die organic laminate ball grid array (BGA) designs. Often companies must consider add-ons or upgrades to new, expensive options.

Advanced substrates come with complex metal planes

Many of today's advanced package substrates require complex, filled metal plane areas to deliver power to the die (**Figure 1**). These metal-filled plane areas are required to pass the exacting fabrication requirements of the substrate supplier and/or outsourced semiconductor assembly and test (OSAT) supplier. Last-generation package design tools struggle with complex filled metal areas, especially those with strict multi-aperture outgassing and area metal balancing rules, so they often apply workarounds such as a "fast" mode to get over their performance issues when creating mask-ready geometries. Of course, such "fast" modes are typically not manufacturing ready/correct and usually must undergo a post-process phase, or "smooth" pass, which takes time, sometimes considerable time, further extending the design cycle.

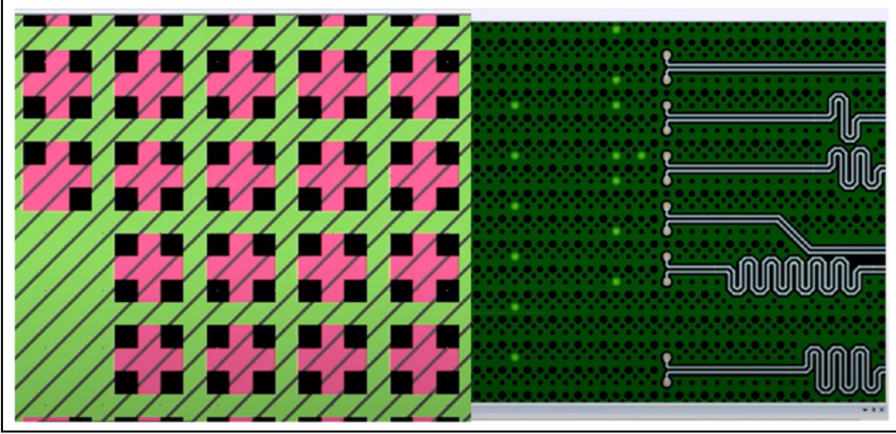


Figure 1: Offset hatched plans and multi-aperture outgassing.

Shifting to high-bandwidth memory

High-bandwidth memory (HBM) is another new challenge when undertaking high-performance computing package design, which includes datacenter devices, artificial intelligence (AI) processors, network processors, and virtual reality devices. HBM has exacting routing rules and requires a massively-parallelized interface, typically implemented as four 4-HI stacks with a total memory bus width of 4,096 bits. Routing such a wide bus and getting it within specification can take a long time unless the design tool is capable of intelligent channel replication, including the ability to update replicated channels due to any post-route edits typically caused by signal integrity performance optimization (**Figure 2**).

Avoiding re-inventing or re-creating design content

Another area that can easily increase design time is lack of support for the reuse of known-good physical design intellectual property (IP). Advanced packaging often has repeated structures, complex via arrays, and areas of fanout/escape routing. Without an efficient way to define and reuse them, such as a library element, designers face hours of manual creation and editing—not just on their own design, but across other designs as well.

Use concurrent multi-designer team design

Because advanced packages contain multiple heterogeneously-integrated dies (aka chiplets), there is a significant increase in overall device size and complexity. These factors demand much

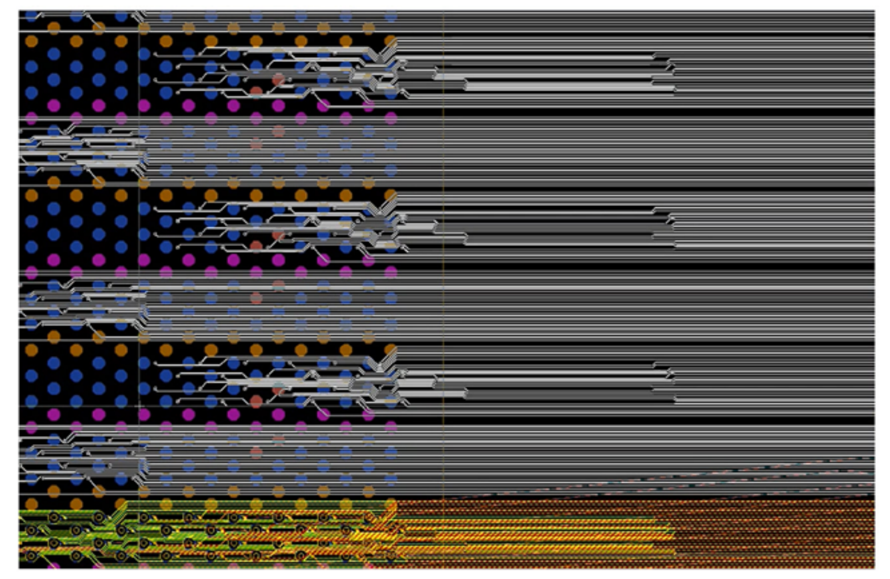


Figure 2: Example of smart HBM channel replication.

greater designer effort and the need to draw upon more specialized expertise, which increases design cycle time. One way to attack this is by deploying multiple designers concurrently on the same design, i.e., team design (Figure 3). The latest generation of semiconductor package design tools come with built-in dynamic team design, where each designer can see in real time what the other designers are creating or editing and where "soft fences" prevent one designer overriding another designer's work.

Clearly, advanced packaging design workflows need to be improved to meet the needs of companies creating HI platforms—ideally in a manner that doesn't require expensive tool add-ons or upgrades. Siemens Digital Industries Software proposes five key workflows that shorten overall design time.

Five HI packaging workflows

There are five areas that deliver the most impact on the successful implementation and design of chiplets:

1. Chiplet design kits (CDK) provide a model of the chiplet for implementation and integration. A CDK can include interface protocols, IO models, automatic test equipment (ATE) test methods, power characteristics, and thermal models such as boundary condition independent reduced order model (BCI-ROM).
2. Heterogeneous planning and co-optimization should use a complete 3D digital model (aka digital twin) of the entire device assembly that drives all downstream aspects of design, analysis, and verification, maintaining a continuous digital thread.
3. Physical verification at every level of 3D assembly, from the substrate layer through design rule checks to assembly-level layout-versus-schematic are important.
4. Multi-domain testing starting with the individual die and continuing with die-to-die and across the entire package assembly is also important.
5. Ecosystem interoperability, including the ability to seamlessly share designs and data with suppliers, partners, foundries, and OSATs, is necessary for success.

Chiplet interface management and design

A standardized interface is a key enabling characteristic of a chiplet. This is how the chiplet, in a predefined manner, communicates with a core design or other chiplets. Therefore, broad adoption of chiplets requires standardized interfaces and protocols, such as those discussed earlier: USR, XSR, BoW, and UCIe serial interfaces and OpenHBI, HBM, and BoW Fine parallel interfaces. All these interfaces bring a new challenge for designers: how to rapidly describe the interfaces for new chiplets while interconnecting commercial off-the-shelf (COTS) or existing chiplets.

Current design approaches, such as graphical schematics or writing thousands of lines of hardware description language (HDL), make it challenging to capture, visualize, manage, and implement chiplet designs. A designer could look up the interface definition for each chiplet interface and manually create the required

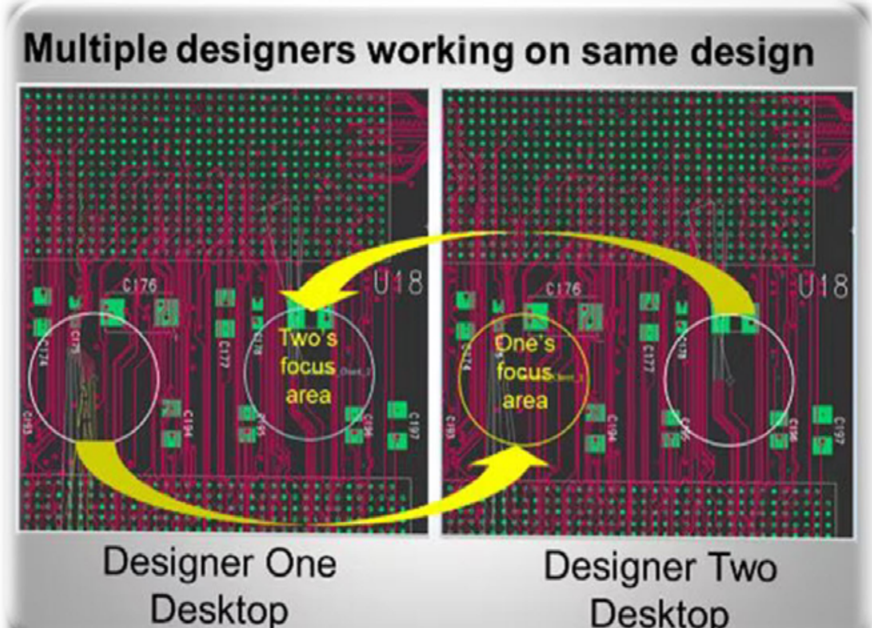


Figure 3: Concurrent design allows multiple designers to work together simultaneously.

connectivity in accordance with the specification, then define electrical constraints to ensure correct package design. But this is a lot of manual work and introduces the risk of human-generated mistakes that might not be easy to catch early in the design process. To avoid this risk, we will introduce a novel concept: interface-based design.

Automating interface-based design

Interface-based design (IBD) is an exciting new approach to capturing, designing, and managing large numbers of complex interfaces that interconnect multiple chiplets. Because the chiplet has a known formal interface, the interface description can become part of the chiplet part model. When a designer places an instance of this chiplet, everything related to the interface is automatically put in place. This way, we take the human out of the equation, ensuring that correct-by-design chiplet connectivity is established (**Figure 4**).

With an interface defined as an IBD object, the designer can focus on a higher level of connectivity abstraction. This facilitates more insightful chiplet floorplanning and chiplet-to-package or chiplet-to-interposer signal assignments, and it allows designers to explore, define, and visualize route planning without having to transition the design into a substrate place-and-route tool. IBD allows the designer to see both "the forest" and "the trees" during the design process by expanding or contracting the interface. As such, IBD provides visualization and manipulation at the appropriate level of interface expansion.

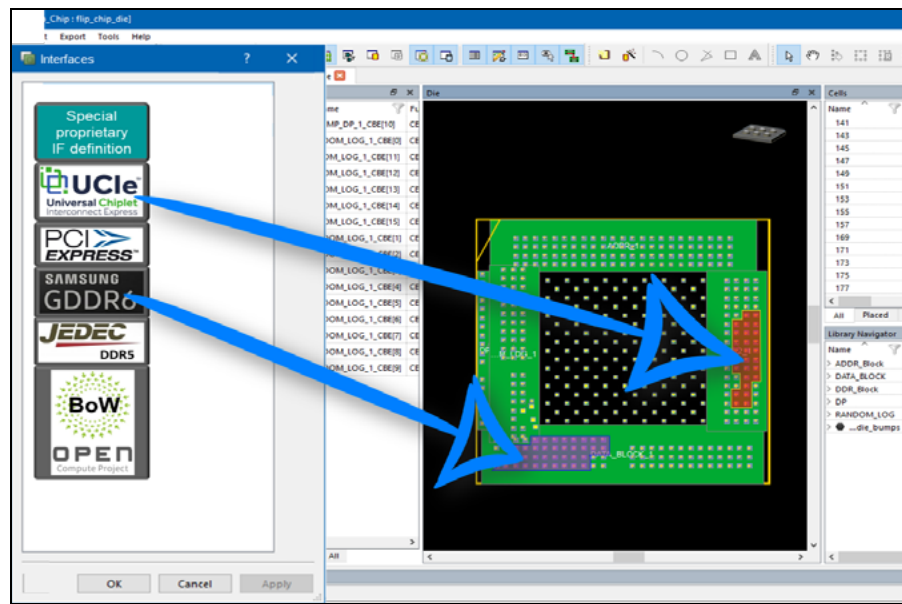


Figure 4: An interface object library could rapidly and accurately construct connectivity.

Thermal, stress, and reliability management

The proximity of devices within heterogeneous packages necessitates understanding the effect they have on one another, also referred to as chip-package interactions. These could be electrical-, thermal-, or stress-related, and are not mutually exclusive.

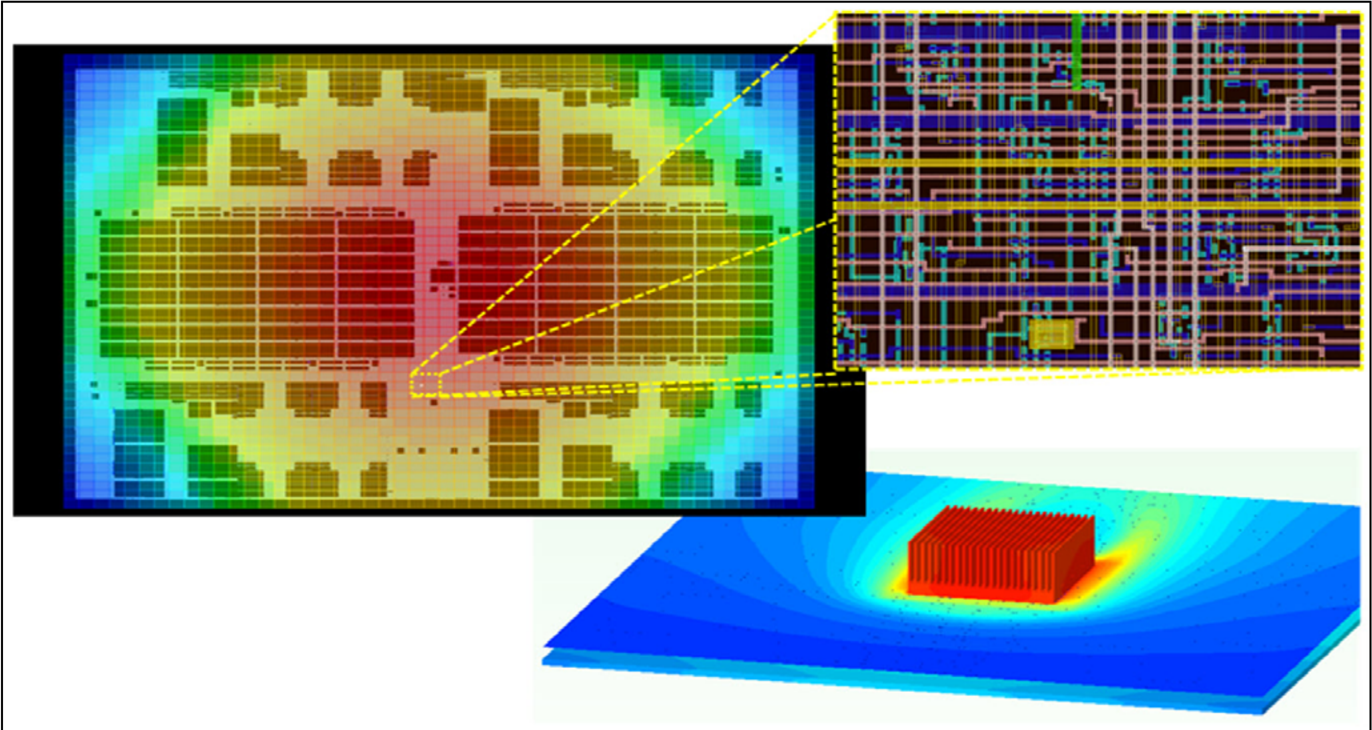


Figure 5: Thermal modeling at the chip-, package-, and system-levels generates power-aware thermal and stress device-level models that provide greater accuracy for thermal and mechanical simulations.

Using a combination of chip-, package-, and system-level thermal modeling, designers can generate power-aware thermal and stress device-level models that provide greater accuracy for thermal and mechanical simulations (**Figure 5**). The models can then be used to perform warpage, stress, and fatigue analysis.

When it comes to material choices, substrate stackup and device or chiplet proximity have considerable impact on thermal and stress performance. So it is very important to not wait until design of the package assemblies is complete. Instead, start with predictive analysis before or during the prototyping/planning phase. Starting analysis as early as possible in the process allows for the most flexibility in making choices and tradeoffs and usually results in the minimum impact on the design.

Grypper
Same Size as Device
• True Zero Footprint
• Pluggable ~100 Insertions
• 0.35mm to 1.27mm Pitch
RoHS
Ironwood ELECTRONICS
1-800-404-0204
www.ironwoodelectronics.com

Test and testability

The production test methodology used in digital, homogeneous designs has been established for many years: deploying structural design-for-test (DFT) logic implemented during the ASIC design process. DFT test tools are run on the inserted test logic to generate the ATE production test programs used for wafer- and package-level production testing. Additionally, boundary scan description language (BSDL) test patterns are generated for the design to be used for PCB-level tests.

Heterogeneous chiplet design requires extensive changes and additions to the traditional, homogeneous design. Because these designs include two or more ASIC/chiplet components, a production test program must be provided for each of the internal components. It is assumed that externally-sourced chiplets will be wafer-sorted and delivered as a known-good-die but will still need to be retested once they are assembled in the system-in-package (SiP) device. Furthermore, these tests need to be run from the external package pins, most of which are not connected directly to the chiplet pins. In addition to the individual die testing, the interfaces between each component need to be functionally tested, preferably at speed for each of the die-to-die interfaces.

IEEE test standards are being developed to accommodate these 2.5D test methods. Different tool vendors may deploy different approaches in implementing these standards, which may cause test compatibility issues of components that use different DFT vendor tools. For board-level testing, a composite BSDL file for each of the internal components is preferred, but not necessarily supported, by all DFT tool vendors, which further complicates the PCB-level testing.

With the introduction of 3D heterogeneous designs, additional challenges are introduced as the die stacked above the base die may not be accessible through traditional BSDL/JTAG interfaces. There are additional emerging IEEE test standards being developed to accommodate 3D test methods as well (**Figure 6**). These methods deploy hierarchical test methods that can only test the stacked die after assembly. Just as with 2.5D, DFT vendor capability issues will likely arise in 3D

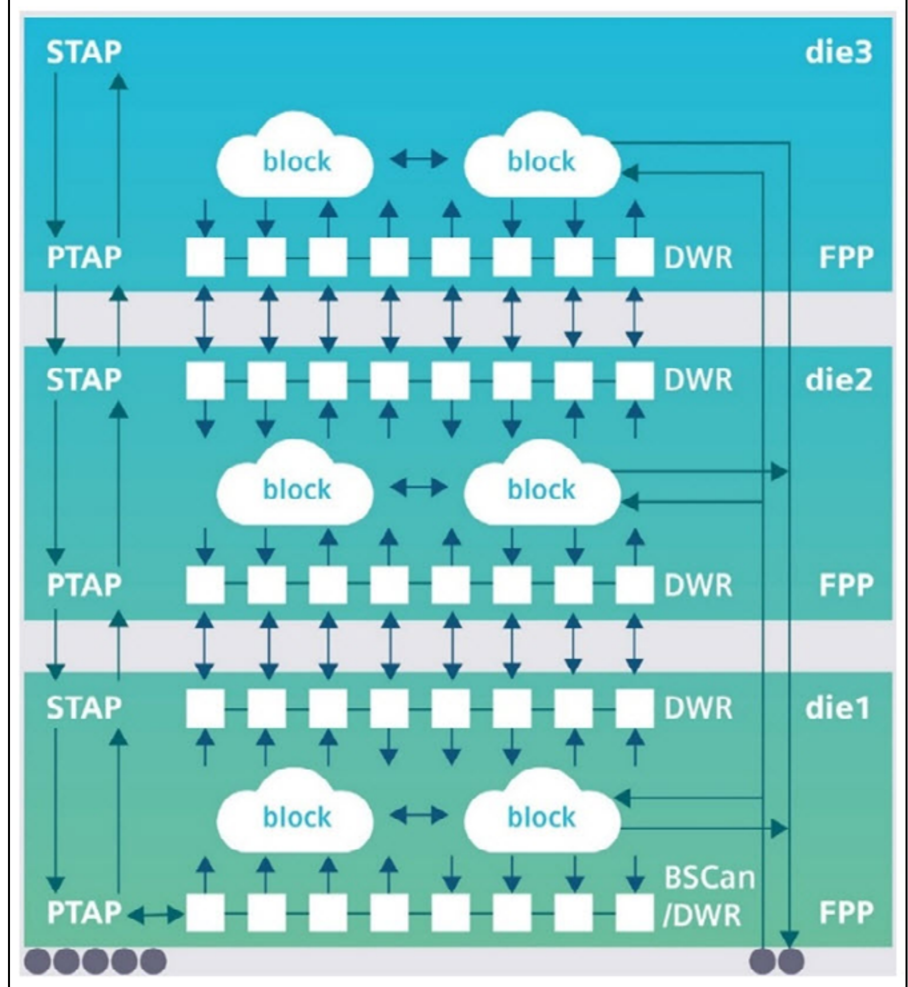


Figure 6: The IEEE 1838 standard provides guidance for 3D multi-die architectures.

stacked dies built with components using different vendor tools.

The inclusion of multi-die in a package may also dramatically increase the production test time and cost. New high-speed scan methods are being developed that will enable the use of very high-speed test interfaces, such as XSR, to replace the traditional slow-speed JTAG approach, which should significantly reduce the SiP-level connectivity as well as reduce test time. Because the test connectivity in 2.5D devices is implemented through an interposer, the package design is required for the planning and routing of the die-to-die test connectivity, which will require new package design and analysis flows.

Driving verification and signoff

It is critical for all verification to start in the planning process and continue throughout the layout process. It starts during initial planning where early assembly validation of device and bump placement can be performed along with IO pad ring validation, ERC checks, and ESD cell insertion determination.

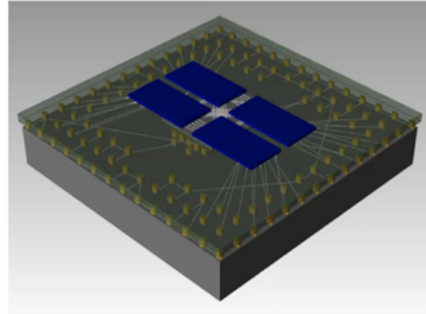


Figure 7: Verification of complete package assemblies including chiplets, interposers, and package substrate.

Such in-design validation provides early identification and resolution of manufacturing issues without running the full sign-off flow – which can be resource and time intensive and usually requires a different department's involvement.

When it comes to final design verification, more than just mask metal layer fabrication checking against the fabricator's rules is involved. It is also very important to analyze various layout enhancements that will improve yield and reliability, such as analysis of thickness variations and planarity issues of the redistribution layer (RDL). It is extremely important to release into manufacturing with confidence that all the devices and substrates work together as expected to avoid costly late-stage errors and delays (Figure 7).

Summary

Several factors are converging and driving the chiplet design revolution. The recommended workflow adoption focus areas presented in this article provide immediate heterogeneous integration capability benefits while establishing a managed methodology adoption and migration process that minimizes disruption, risk, and cost. This will bring heterogeneous integration-based chiplet design within reach of the mainstream, instead of being accessible only to the mega integrated device manufacturers (IDMs) and fabless semiconductor companies.

Biography

Keith Felton is the Marketing Manager for the Xpedition IC Packaging solutions at Siemens Digital Industries Software in Marlborough, MA. Working extensively in IC package design since the late 1980s, Keith drove the launch of the industry's first dedicated system-in-package design solution in the early 2000s and led the team that launched Siemens OSAT Alliance program. His current focus includes driving the strategy and direction for Siemens multi-substrate prototyping, design, and verification solution for high-density advanced packaging. Email keith.felton@siemens.com

Achieving automated shmoo results analysis with a deep learning method

By Chao Zhou [Teradyne Inc.]

The shmoo plot is a widely-used technique in the semiconductor industry for evaluating product specifications and debugging test vectors. It examines the characterization of supply voltage and operating frequency, providing valuable information for improving yield ratios. However, the manual review process of shmoo plot results, particularly during test with automated test equipment (ATE), is time-consuming and can prolong the test period, delaying time to market. To address this challenge, a deep learning based method has been developed and implemented to analyze shmoo results automatically. This method, developed using PyTorch, can accurately analyze shmoo results in a shorter time compared to manual methods, and can be seamlessly integrated into any existing test environment.

In the field of ATE, there are several techniques described in the literature to analyze shmoo data, such as decision tree, logistic regression, support vector machines, and random forest [1-2]. These methods are traditional machine learning techniques, which require the results to be manually reviewed, thereby limiting their application and resulting in poor test accuracy in some cases.

Deep learning, deployed in this new application, is a machine learning method in which a neural network with hidden layers is used to simulate the operation of a human's neural actions, extracting the features of the input signal and executing the classification work without human intervention. Nowadays, deep learning applications in computer vision and natural language processing far exceed those of traditional machine learning methods. In this application, a neural network was adapted to analyze and interpret the characteristics of a shmoo plot, significantly improving test accuracy (**Figure 1**).

Proposed model introduction

The structure of this model is a modified AlexNet, proposed by Alex Krizhevsky [3], which demonstrated that the self-learning features of neural networks can surpass manual capabilities. The neural network structure of this method is shown in **Figure 2**. A total of eight layers of convolutional neural networks (CNNs) are used, including four layers of convolution (feature extraction), one spatial pyramid pooling (SPP) layer [4] to process the variable size of the input, two layers of fully-connected (FC) layers (classification) and one output layer.

The first four convolutional layers are to extract the features of the shmoo plot. The convolution kernel shape of all layers in the network is 3x3, while the shape of the shmoo plots in the training data set are all 11x11, which means that a large convolution kernel to extract the pattern is not necessary. A small 3x3 window to capture a single pixel and its surrounding pixels is sufficient. Padding is used to preserve the pixel information of the shmoo edge to avoid misjudging missing edge pixels. The padding size is set to 1, which, coordinated with the convolution kernel, can make the height and width of each convolutional layer's output equal to 11x11.

To make the tool compatible with shmoos of different sizes, a 3-level (4, 2, 1) SPP layer, which is inserted between the convolutional layers and the FC layers, is introduced in this CNN model (**Figure 3**). The SPP layer is used to convert different shapes of input into a fixed value, which is required as the input size of the subsequent fully-connected layer. The core principle of the SPP layer is to use multiple level pooling of different sizes (4*4, 2*2 and 1*1 pooling windows are used in this method) to process the output of the last convolutional layer. Then, it combines the results to obtain three (16*ch, 4*ch and 1*ch) level feature vectors [4]. Finally, after flattening these feature vectors, they are passed to the next fully-connected layer.

The role of the fully-connected layer is to do the classification. The SPP layer is connected to an FC layer with 84-channels, at which point the extracted features output by the SPP layer pass through two fully-connected layers. A one-dimensional array with six elements is output as the result, with these six elements representing the Fail, Pass, Vol, Freq, Marginal and Hole values, respectively.

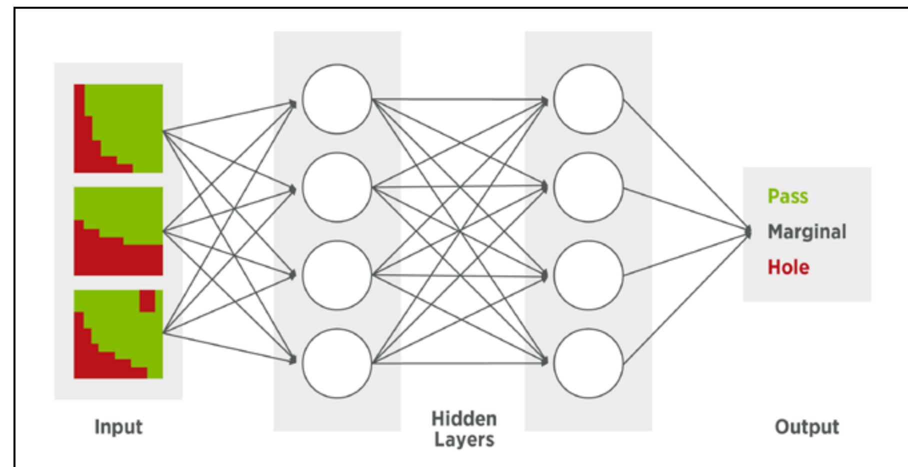


Figure 1: Functional diagram of a deep learning method.

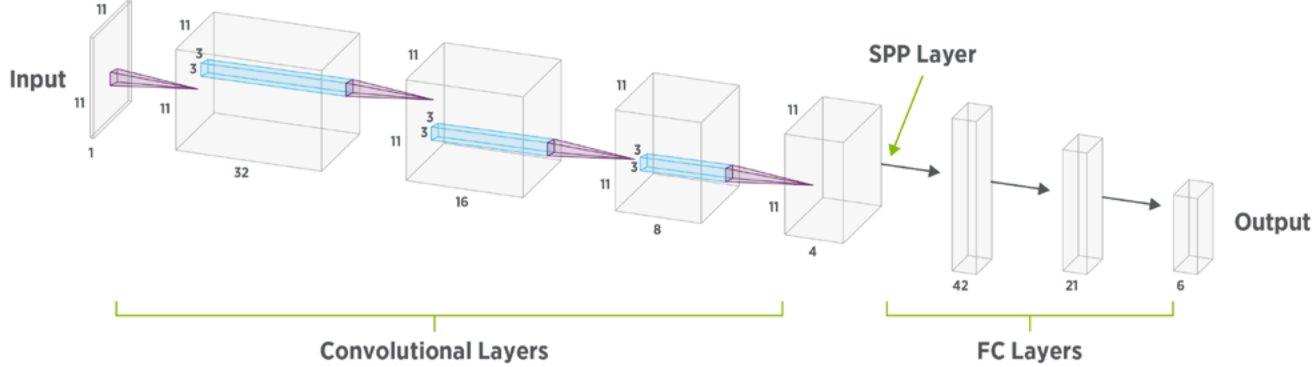


Figure 2: CNN structure of the proposed modified AlexNet neural network. SOURCE: Created using the NN-SVG diagramming tool, (www.github.com/alexlenail/NN-SVG).

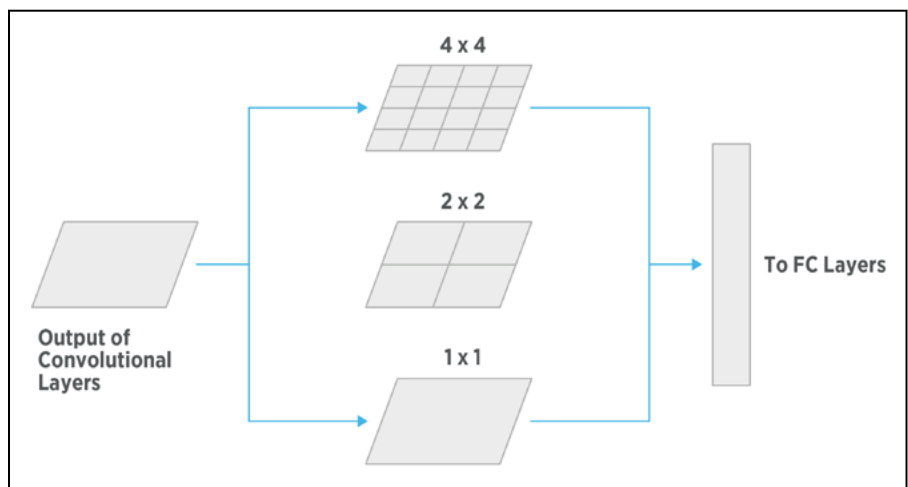


Figure 3: Diagram of a spatial pyramid pooling layer.

A significant difference between AlexNet and this neural network is that all pooling layers except the SPP are removed. This is because each test point is processed as a pixel of the input shmoo image, so the result of the shmoo is sensitive to every test point. The pooling layer takes the maximum value or the average value for a group of adjacent pixels, which causes loss of information, so it is abandoned because it could reduce the test accuracy of the shmoo result types Hole and Marginal.

Additionally, the batch normalization layer is implemented instead of using the dropout method to suppress overfitting. With batch normalization the data is standardized in a mini-batch, with the mean value of the normalized data being 0 and the standard deviation as 1. This process is similar to dropout, as it "discards" a part of the nodes where the output is close to 0 at this layer. It also makes the output of each layer follow the same distribution, and so, as a result, eliminates the potential of "parameter explosion" and "parameter attenuation" in the deep network structure training process. This stabilizes and accelerates the model's training [5].

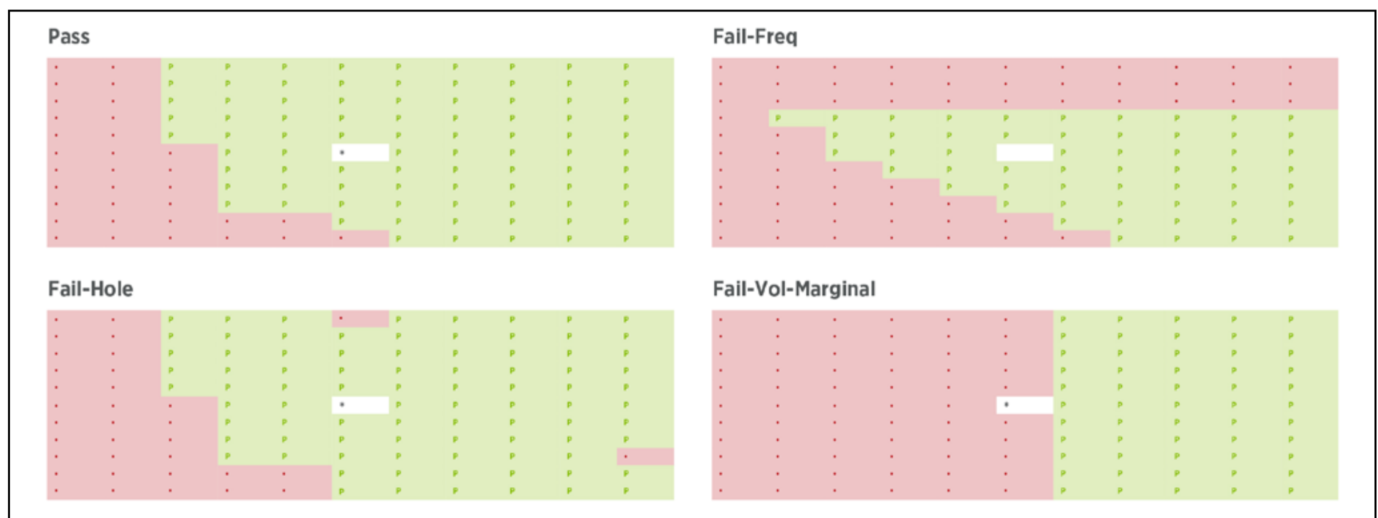
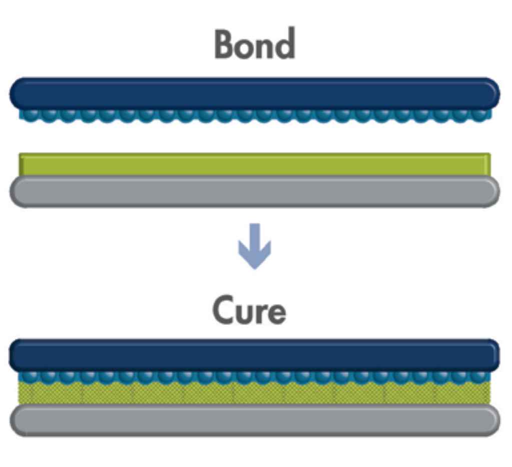


Figure 4: Shmoo samples in the training dataset.

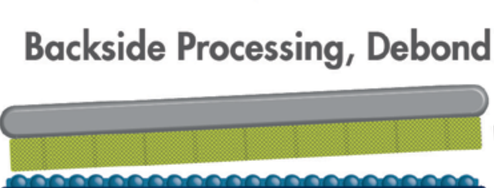
Dual-Layer Solution

A path-changing direction for temporary bonding

Bond



Backside Processing, Debond



Our unique dual-layer solution for high-temperature & high-stress applications found within the semiconductor industry

www.brewerscience.com

©2020 Brewer Science, Inc.

Implementation

The training set is a critical part of the entire method, and defects at this level will directly reflect on the test accuracy of the shmoo results analysis. For now, there are about 650 shmoo diagrams in the training set, including five categories: pass/good, hole, voltage walls, frequency walls and marginal. All samples are chosen from real shmoo testing projects with scaling to an 11x11 dot matrix. Because the shmoo plot size is not very large, the proposed method was implemented using PyTorch 1.8.0, and trained and tested on a computer with an Intel Core i7-10810U central processing unit (CPU), and without a graphics processing unit (GPU). The format of the shmoo samples in the training dataset is shown in **Figure 4**. There are two parts in each training sample: the result information and the shmoo diagram. In this experiment, the X-axis represents the voltage, while the Y-axis is the period.

In addition to the pass/fail indicators, there are four additional indicators used to describe the detailed shmoo results:

1. Vol-Wall result is used for the voltage-wall shmoo, where the count of the pass points changes dramatically along the X-axis (voltage).
2. Freq-Wall result is for the frequency-wall shmoo, where the count of the pass points changes dramatically along the Y-axis (period).
3. Marginal indicator is used to show the shmoo plot where the fail point is near, or appears at the central position.
4. Hole result indicates a hole defect meaning there are fail test points surrounded by passing ones.

Results

One hundred samples were chosen from the 650-sample training set randomly as training inputs, and then a second set of 100 samples were used as the test set. The loss function uses the MultiLabelSoftMarginLoss function, which is commonly used in applications with a multi-label classification [6]. The learning rate is set to 0.0014. The gradient algorithm optimizer uses Adam, and the weight decay is set to 0.0004 (to reduce possible training problems) [7-9]. After 100 epochs, the test accuracy rate (pass/fail) was approximately 0.97 (blue dots in **Figure 5**), while the test accuracy rate (multi-labels) was approximately 0.89 (red dots in **Figure 5**).

In the pursuit of high accuracy and low overfitting, we found that the stability of this network structure was strongly correlated with the convolutional layer (**Figure 6a**). If any of the middle convolutional layers are removed from this model (**Figure 6b**), it leads to an accuracy drop at epoch 28 under the same training conditions. The rate decreases by approximately 3% and there are obvious accuracy fluctuations during training. It can be seen that "depth" is the key to ensuring this neural network model meets expectations. The red dots in **Figure 6** represent the accuracy of the test with the full values, and the blue dots represent the accuracy of the second-class test that only considers pass/fail results.

CNN visualization

Because deep learning is based on the back propagation algorithm to calculate and update the parameters of each

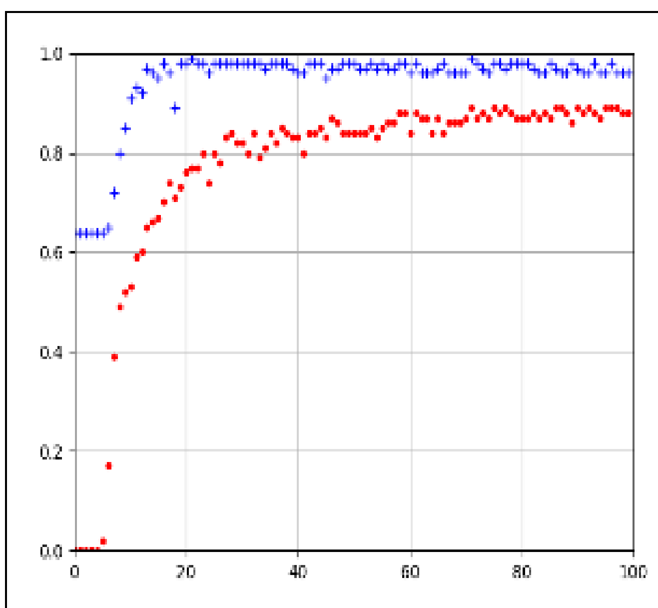


Figure 5: Training result of the test accuracy of pass/fail only (blue) and test accuracy with multiple labels.

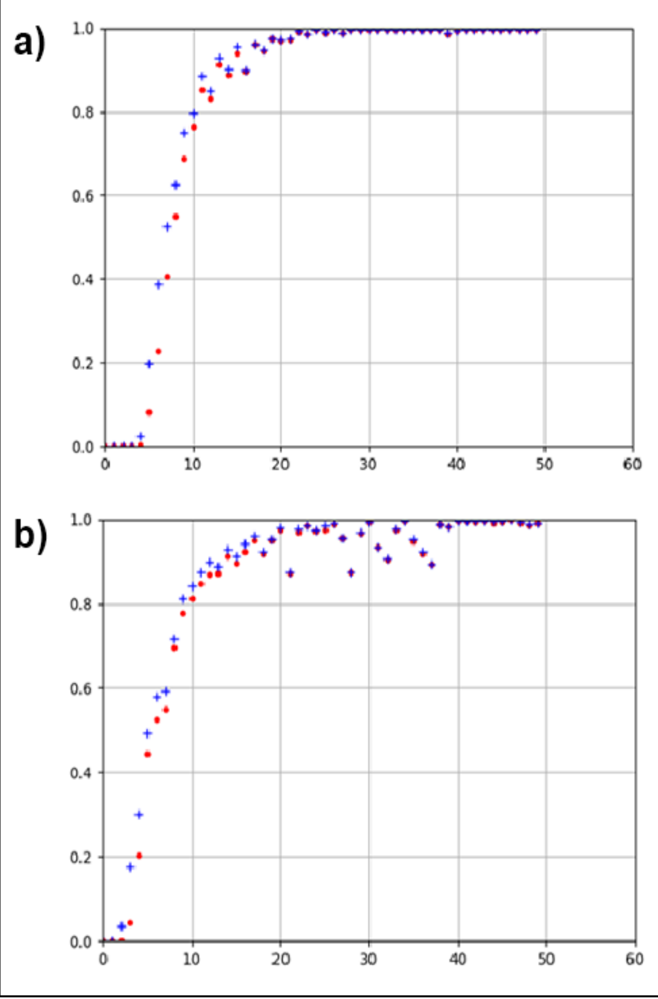


Figure 6: Training results of the a) (left) complete network model; and b) (right) the missing 2nd layer model.

CONTECH Solutions, Inc.

Serving the semiconductor industry since 1995.

Our new compact socket body is highly adaptable for mating with small packages of all types, from fine pitch WLCSP's to all types of QFN's and LGA's. Quick Turn Semi Custom Sockets for 0.4mm CSP, Single/Dual Row QFN and DFN Devices. High performance BGA/LGA sockets for all pitches and package sizes.

Contech Solutions has been providing innovative test interface tools to the worldwide semiconductor industry since 1995.

ATE contactors • Manual test sockets • Reliability sockets
FA sockets • FA boards • DUT boards
BIB probes • Socket receptacles • Adaptors

www.ContechSolutions.com
631 Montague Avenue • San Leandro, CA 94577
T: 510.357.7900 Ext. 203 • F: 510.357.7600

Connecting Semiconductors and Electronics

WORKFORCE DEVELOPMENT

Global ADVOCACY

Sustainability

1000+ STANDARDS

THOUGHT LEADERSHIP

TECH COMMUNITIES

SEMI UNIVERSITY

Cyber Security

About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

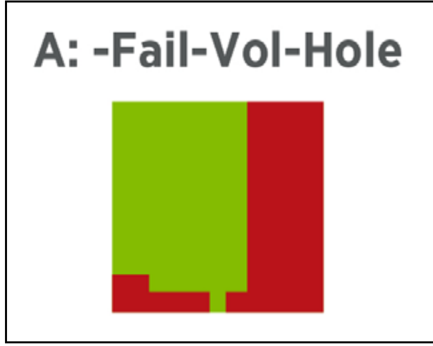


Figure 7: Sample shmoo plot.

node, observation of the output of each layer of the model can help us understand how the neural network learns, which can also help us compose the neural network structure.

From **Figures 7-9** it can be found that the feature maps of the output of the convolutional layer, which is close to the input, can still distinguish the relationship with the input shmoo. The output of the higher layer has higher-level features that humans cannot analyze manually, but it is believed that the learning of the middle layer can be a great help to artificial intelligence (AI) research. Exploring the black box problem of neural networks is bound to be a future research direction.

Figure 8: Output of the first CNN layer.

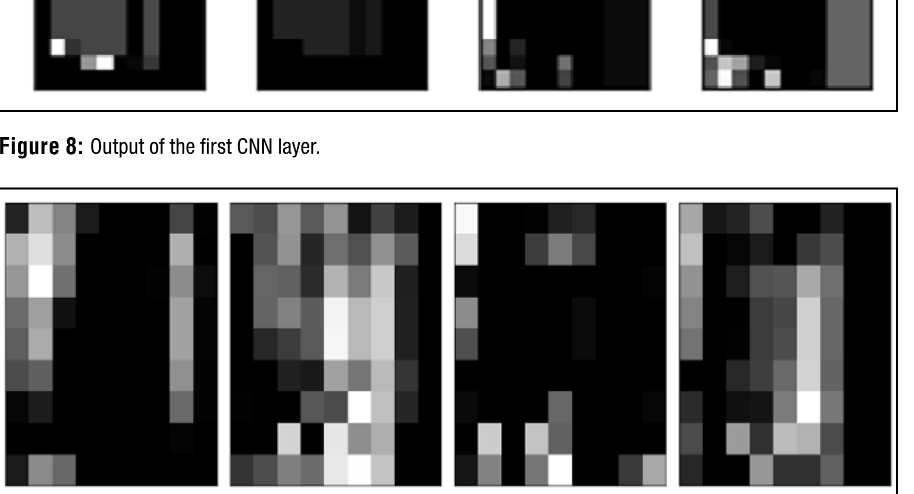


Figure 9: Output of the third CNN layer.

Future work

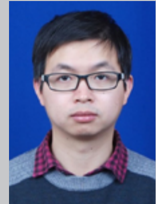
The new method has been verified on some test projects where shmoo tests currently help engineers save time on data analysis. One of the future works is to optimize the scheme so that the tool can adapt to different types of X/Y axes in shmoo plots. The second is to support shmoo center point (test base point) recognition, and the third is to simplify the neural network structure to reduce the number of trainable parameters and overfitting. Lastly, our goal is to expand the training set. Additionally, this method can be used offline or in near real time in conjunction with an ATE system to enable adaptive testing and preemptive troubleshooting based on wafer classification results while the next wafer is being tested.

Summary

This article focuses on the development and application of a deep learning method for automating the analysis of shmoo plots in ATE testing. The article demonstrates that the proposed method can classify the results of shmoo plots accurately, shortening the process from days to minutes, which significantly improves time to market while ensuring high quality levels. The findings suggest that deep learning is a valuable tool for automating the analysis of ATE test data.

References

1. O. D. Adeosun, "Shmoo analysis of integrated circuits using machine learning algorithms," Diss. 2017.
2. W. Wang, "Automated Shmoo data analysis: a machine learning approach," 15th Inter. Symp. on Quality Electronic Design, IEEE, 2014.
3. A. Krizhevsky, I. Sutskever, G. Hinton, "Imagenet classification with deep convolutional neural networks," Neural Information Processing Systems (NIPS), 2012.
4. K. He, X. Zhang, S. Ren, J. Sun, "Spatial pyramid pooling in deep convolutional networks for visual recognition," ECCV, 2014.
5. J. Brownlee, "A gentle introduction to batch normalization for deep neural networks [EB/OL]," https://machinelearningmastery.com/batch-normalization-for-training-of-deep-neural-networks/ 2019-01-16.
6. J. Brownlee, "Loss and loss functions for training deep learning neural networks [EB/OL]," https://machinelearningmastery.com/loss-and-loss-functions-for-training-deep-learning-neural-networks/ 2019-01-28.
7. S. Bhandari, "Intuition behind gradient descent for machine learning algorithms [EB/OL]," http://sijanb.com.np/posts/intuition-behind-gradient-descent-for-machine-learning-algorithms/ 2019-08-05.
8. 强波．梯度下降算法 [EB/OL]. https://paul.pub/gradient-descent/ 2019-06-19.
9. A. Singh, "Optimization algorithms for deep learning [EB/OL]," https://medium.com/@ashwin8april/optimization-algorithms-in-deep-learning-4f2c3b53f9f 2019-09-01.



Biography

Chao Zhou is a Field Application Engineer at Teradyne, Inc., Shanghai, PRC. He specializes in the development of test solutions for application processors (AP) and large digital system on chips (SoCs). He leverages his analytical expertise to enhance efficiency and quality within Teradyne's engineering operations. He holds a Master's degree in Electrical Engineering from the U. of New South Wales. Email chao.zhou@teradyne.com

PLASMA ETCH
PROGRESS THROUGH INNOVATION

PLASMA IMPROVES BONDING!

Our fully automated plasma cleaners offer:

-Improved Markability
-Enhanced Adhesion
-Better Bonds
-Easier Assembly
-Surface Modification

100% removal of organic contaminants with a low environmental impact!

STARTING AT ONLY
$ 5,900 USD

TO LEARN MORE, VISIT WWW.PLASMAETCH.COM
OR CALL 775-883-1336

ADVERTISER INDEX

Adeia 14
Amkor Technology .... 1, OBC
Brewer Science 44
Contech Solutions 45
Deca Technology 6
DL Technology 28
E-tec Interconnect 26
EV Group 2
INTEKPLUS CO., LTD. 31
Ironwood Electronics 40
ISC CO., LTD. 22
JC Cherry 24
LB Semicon 21
Leeno Industrial .... IFC, 16
Plasma Etch 48
SEMI 46
SEMI Europe 47
Smiths Interconnect 12
Sonix 25
SÜSS MicroTec 35
Syagrus Systems 11
Technic 3
Test Tooling Solutions Group 36
TFE Co. Ltd 19
TSE Co. Ltd 4,5
WinWay Technology .... IBC

July August 2023
Space Close July 3rd • Ad Materials Close July 7th
For Advertising Inquiries: ads@chipscalereview.com

Your trusted partner in IC testing

Hi-Speed Probe Head
112Gbps PAM4@150um pitch

Automation
Accuracy within 1 µm

Double Site
Top pitch > 150um
Bottom pitch > 0.8mm

Thermal Control
> 2000W@100°C

Coaxial Socket
Pitch > 0.35mm

Probing System for Co-Packaged Optics

Enabling
Innovative
Technology
We enable customers with next-generation packaging and test solutions to bring automotive, consumer, IoT and networking applications to market.
Amkor delivers innovative packaging solutions with the service and capacity global customers rely on. We offer product development, manufacturing, test services and customer support in Asia, Europe and the US.
amkor.com ▶ sales@amkor.com
© 2023 Amkor Technology, Inc. All Rights Reserved.
Amkor Technology®
Enabling the Future