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Volume 27, Number 1

January • February 2023

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Fan-out wafer-level package for memory applications

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- Optical fiber pigtails integration in co-package design
- Oxide crack risk assessment during probing over active area
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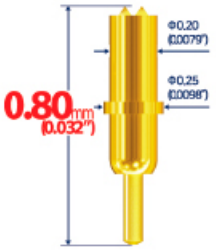

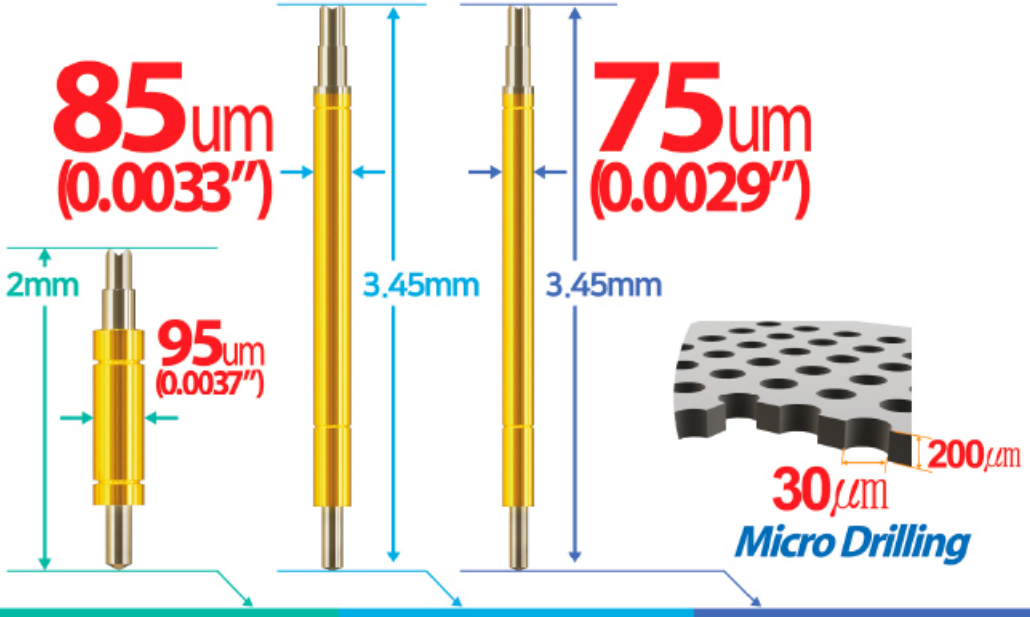

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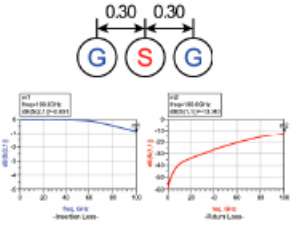
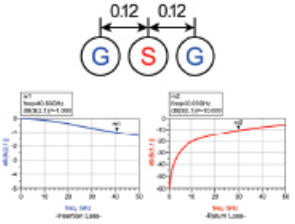
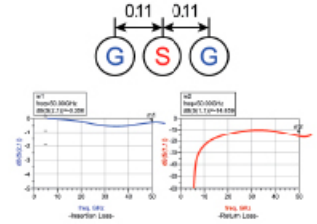
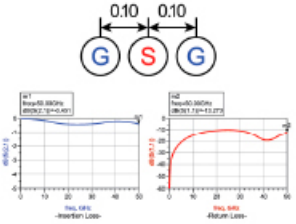
Electrical Spec. (Simulation data) • Propagation Delay : 7.68ps • Capacitance : 0.05pF • Inductance : 0.25nH • Insertion Loss : > 100GHz @ -1dB • Return Loss : > 100GHz @ -10dB (Dielectric material : MDS100)	**Electrical Spec.** (Simulation data) • Current Rating : 1.0A • Propagation Delay : 20.80ps • Capacitance : 0.21pF • Inductance : 0.38nH • Insertion Loss : 40.83GHz @ -1.000dB • Return Loss : 30.03GHz @ -10.000dB (Dielectric material : CERAMIC)	**Electrical Spec.** (Simulation data) • Current Rating : 0.9A • Propagation Delay : 38.25ps • Capacitance : 0.47pF • Inductance : 0.63nH • Insertion Loss : > 50.00GHz @ -1.000dB • Return Loss : > 50.00GHz @ -10.000dB (Dielectric material : CERAMIC)	**Electrical Spec.** (Simulation data) • Current Rating : 0.8A • Propagation Delay : 35.55ps • Capacitance : 0.44pF • Inductance : 0.66nH • Insertion Loss : > 50.00GHz @ -1.000dB • Return Loss : > 50.00GHz @ -10.000dB (Dielectric material : CERAMIC)
			

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Recently, through-silicon via (TSV) technologies have been widely used in high-bandwidth memory for high-performance computing or high-density memory modules. For mobile memory packaging, conventional wire bonding is still being used, due in part to cost considerations. As overall mobile memory system performance is improved, however, there is a need for a thinner package that has better thermal and electrical performance. Inside this latest issue of CSR, the Hynix Integrated Fan-out Memory (HIFOM) is described—it's a chip stackable fan-out wafer-level package that offers better performance than conventional wire-bonded type memory packages.

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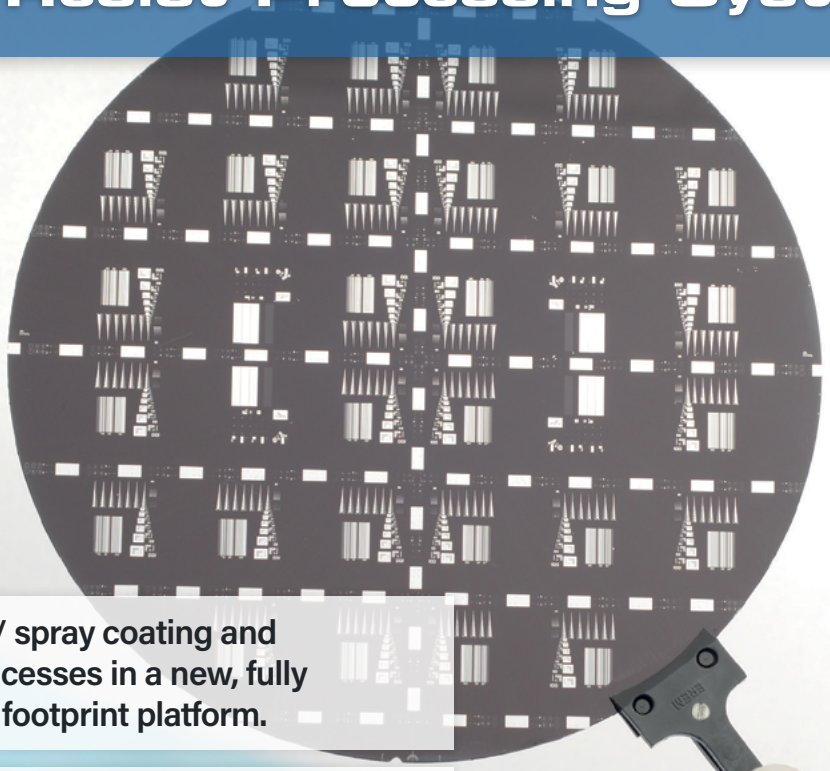

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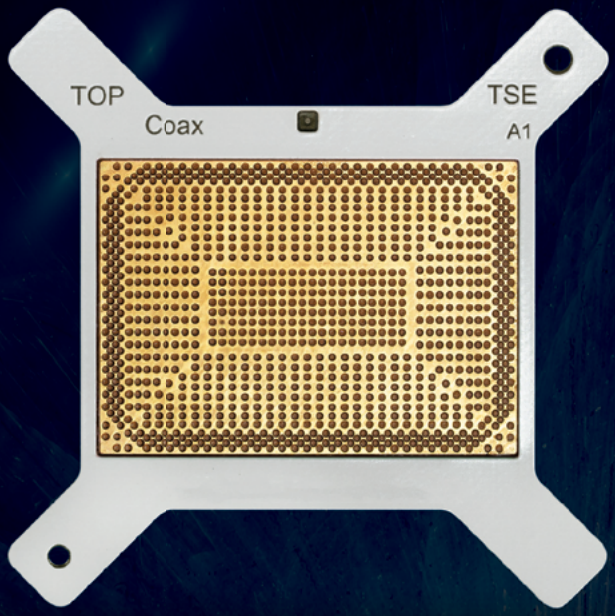

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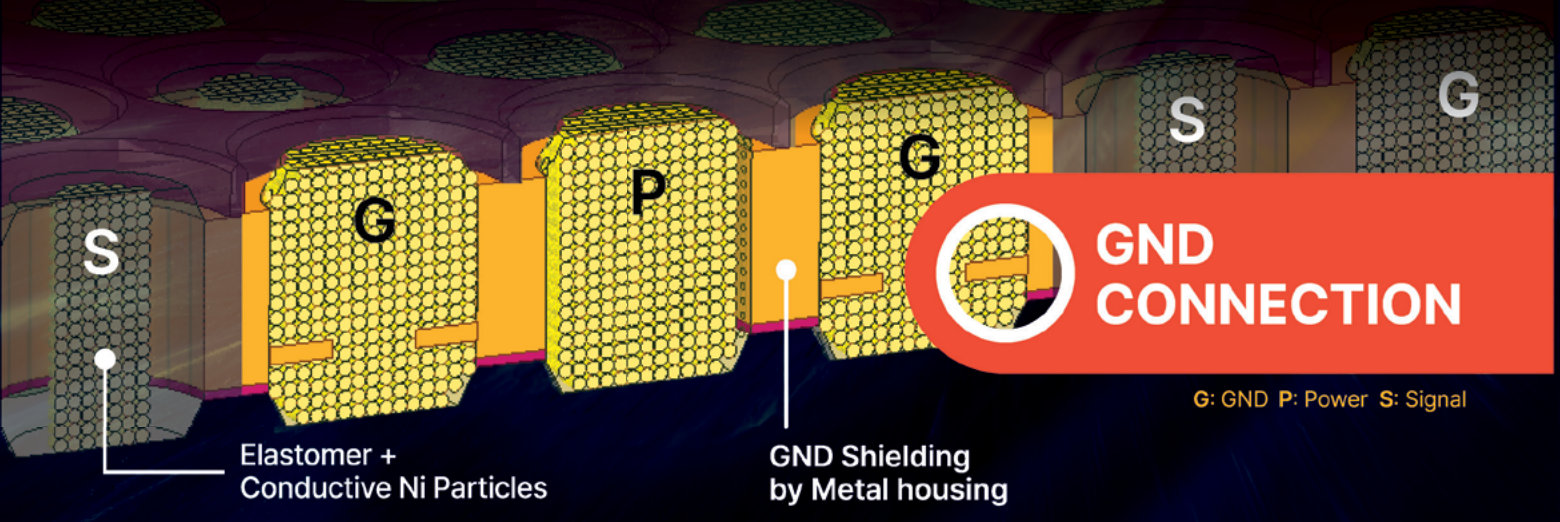

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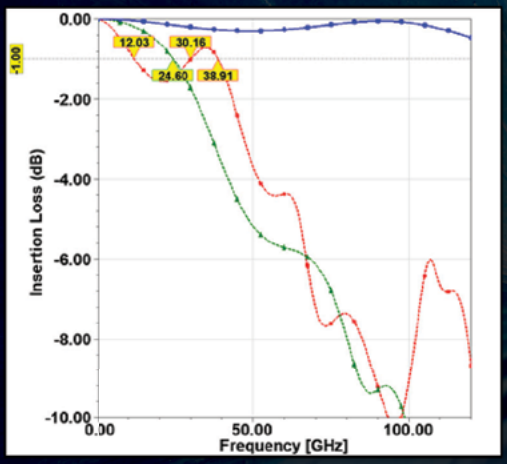
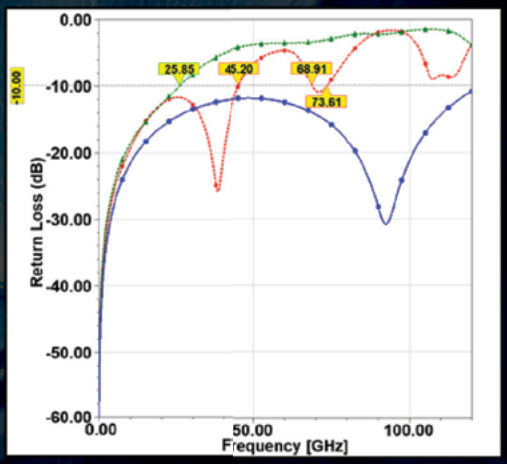


Insertion Loss



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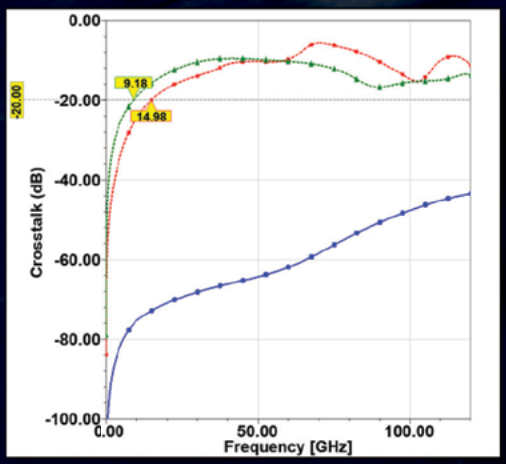

Crosstalk

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Highlights of the 24th EPTC Conference

By Ranjan Rajoo [GlobalFoundries] Andrew Tay [National University of Singapore]

The 24th IEEE Electronics Packaging Technology Conference (EPTC2022) is an international event organized by the IEEE Singapore RS/EPS/EDS Chapter and co-sponsored by the IEEE Electronics Packaging Society (EPS). Since its inauguration in 1997, EPTC has been established as a highly reputable international electronics packaging conference and is the EPS flagship conference in the Asia-Pacific Region. It aims to cover the complete spectrum of electronics packaging technology. Topics include modules, components, materials, equipment technology, assembly, reliability, interconnect design, device and systems packaging, heterogeneous integration, wafer-level packaging, flexible electronics, light-emitting diodes (LED), the internet of things (IoT), 5G, emerging technologies, 2.5D/3D integration technology, smart manufacturing, automation and artificial intelligence (AI). EPTC2022 featured keynotes, a panel, a heterogeneous integration roadmap (HIR) workshop, technical sessions, invited talks, professional development courses (PDCs), interactive sessions, packaging education workshop, and an exhibition and networking activities.

This year, the 24th EPTC2022 went in-person as opposed to being virtual the last two years (2020 and 2021) due to COVID-19. The conference was held from December 7 to December 9 at the Grand Copthorne Waterfront Hotel in Singapore. With over 430 attendees from 20 countries, it was a good opportunity to catch up with industry technologists and academicians. The conference had a total of 201 papers, with 137 oral and 36 interactive presentations; 28 papers were pre-recorded for on-demand viewing by those unable to travel due to COVID-19 restrictions in their respective countries. The conference had three keynotes, a panel session, a HIR workshop, a packaging education workshop, 6 invited presentations, two exhibitor presentations, 42 oral sessions, and two interactive presentation sessions.

The conference kicked off with 5 half-day professional development courses: 1) "Reliability Engineering Testing Methodology and Statistical Knowledge for Qualifications of Consumer and Automotive Electronic Components," by Dr. Fen Chen, Cruise LLC (a GM company); 2) "Photonic Technologies for Communication, Sensing, and Displays," by Dr. Torsten Wipiejewski, Huawei Technologies; 3) "Reliability of Heterogeneous Integration (HI) Systems - Reliability Needs of HI Stakeholders," by Prof. SB Park, The State University of New York, Binghamton; 4) "Fan-Out Packaging and Chiplet Heterogeneous Integration," by Dr. John H. Lau, Unimicron Technology; and 5) "Advanced Packaging for MEMS and Sensors," by Dr. Horst Theuss, Infineon Technologies.

Dr. Chandra Rao, General Chair of the EPTC 2022, gave the welcome address, thanking all conference delegates, sharing the conference statistics and extended appreciation to sponsors, exhibitors and conference partners for their support. In her opening speech (**Figure 1**), Dr. Kitty Pearsall, the IEEE EPS President, presented an overview of the society's mission and activities, and expressed her appreciation to the EPTC2022 organizing committee for its great work.

Figure 1: Dr. Kitty Pearsall, EPS President, giving her opening speech.

Following the opening ceremony, three keynotes were delivered by prominent leaders from industry. Dr. Ravi Mahajan, Intel Fellow, gave the first keynote on "Challenges and Opportunities in Heterogeneous Integration (**Figure 2**)." His speech addressed the tremendous opportunities that heterogeneous integration presents in different application environments. He also focused on the projected evolution of advanced packaging

Figure 2: First keynote speaker, Dr. Ravi Mahajan, Intel.

architectures. He gave specific examples showing how product implementations can take advantage of these technologies to provide an unprecedented level of performance, and described the challenges and opportunities in developing robust advanced packaging architectures.

Dr. Raj Pendse, Director of Si Packaging, Meta Reality Lab, delivered the second keynote entitled, "New Directions and Challenges in the Packaging of augmented reality/virtual reality (AR/VR) Hardware (**Figure 3**)." His presentation focused on the

Figure 3: Second keynote speaker, Dr. Raj Pendse, Meta.

new trajectory for Si packaging technology set by the emergence of AR/VR hardware and advanced wearable computing. The next major step in that evolution will be wearable computing in the form of novel, hands-off and all-day wearable AR/VR devices like AR glasses. These devices will continue the remarkable journey of miniaturization and power/performance carved out by their predecessors. Dr. Pendse also discussed the

complex array of packaging technologies that lie under the hood of such devices, spanning the three areas of augmented reality processing (ARP), display and imaging (D&I) and low-energy wireless (LW) communication. Meta has demonstrated unique approaches that combine advanced packaging technologies like flip chip, fan-out wafer-level packaging and through-silicon via (TSV)—often within the same package. He discussed the challenges created by the need to spawn new ecosystems, such as heterogeneous integration and fabrication methods that often fall in the grey zone between foundry and outsourced semiconductor and test (OSAT).

Dr. Sundar Ramamurthy, VP & GM Advanced Packaging, Applied Materials, delivered the third keynote entitled, "Materials Engineering Innovations to Address Next-Gen Electronics Packaging Challenges (**Figure 4**)." He declared that hybrid bonding needs new dielectrics and optimized copper

Figure 4: Third keynote speaker, Dr. Sundar Ramamurthy, Applied Materials.

grain morphology that enable low-temperature processing. Tuning chemical mechanical processing (CMP) for optimal bond surface profiles can improve the efficiency of the bonding process. Panel-level packaging offers the ability to reduce cost by moving to a larger format, but new challenges for handling large substrates need to be overcome. Speeding up yield learning and addressing defect sources also require increased inspection and monitoring for known-good die. Materials challenges and engineering innovations that are enabling the advances required for the next generation of electronics packaging were also shared.

Following the keynotes was a panel session on "Chiplets as an Enabler for System Scaling," which was moderated by Prof. CS Tan (**Figure 5**). The panel speakers were Dr. Ravi Mahajan, Intel; Dr. Raj Pendse, Meta Reality Labs; Dr. Bernd Dielacher, EVG Group; and Dr. Yik Yee Tan, Yole Group.

Figure 5: Panel on "Chiplets as an Enabler for System Scaling."

The panel revisited the drivers behind chiplets technology, the manufacturing ecosystem, and use cases. The Universal Chiplet Interconnect Express (UCIe®) was also discussed. The panel ended with a critical examination of the supply chain and market outlook.

The HIR workshop was held at the end of the conference with the theme: "Heterogeneous Integration Paving the Way for Global Electronics Resurgence." Heterogeneous integration through advanced packaging innovations is widely acknowledged as being increasingly important to drive performance, system availability, power efficiency, cost and time to market of microelectronics systems—from high-performance computing (HPC) and data centers, to 5G and beyond, mobile, autonomous automotive, IoT, and the medical and health markets. The HIR is a system- and application-driven roadmap inclusive of the full microelectronics technology ecosystem with the purpose of delivering the next extension of Moore's Law for decades to come. Dr. Ravi Mahajan gave an overview of HIR that was followed by presentations on: 1) the supply chain by Dr. Kitty Pearsall, EPS President; 2) thermal management by Dr. Gamal Refai-Ahmed, AMD; 3) 2D–3D Interconnects by Dr. Ravi Mahajan, Intel; and 4) updates on photonics by Prof. Amr Helmy, University of Toronto.

A Packaging Education workshop was organized by Profs. Jeff Suhling and Andrew Tay. The main objective of the workshop was to discover what some universities in Asia are doing to prepare their students to enter the electronics packaging industry. The following professors shared specialization programs on electronics packaging in their respective universities and countries: 1) Prof. K. N. Chiang, National Tsing Hua University (Taiwan); 2) Prof. Wenhui Zhu, Central South University (China); 3) Prof. Gu-Sung Kim, Kangnam University (South Korea); 4) Prof. Anandaroop Bhattacharya, IIT Kharagpur (India); and 5) Prof. Chuan Seng Tan, Nanyang Technological University (Singapore).

A highlight of the conference was the banquet (**Figure 6**), which was held on Mount Faber, from which delegates were able to enjoy a spectacular view of the southern coastline.

Figure 6: Conference banquet at the Mount Faber Restaurant.

The delegates had a great networking session after more than two years of not being able to do so in person because of COVID-19.

The EPTC2022 Executive Committee would like to thank all our conference delegates, sponsors, exhibitors, partners and all other contributors for their participation. Industry partners have continued their strong support of the EPTC in 2022, which has enabled EPTC to be an excellent platform for packaging technologists from all over the world, but especially from Asia, to share and exchange information and ideas on electronics packaging technologies. Special thanks to the Organizing Committee (**Figure 7**) for its strong commitment, dedication and support in making EPTC2022 a memorable event!

Figure 7: EPTC2022 Organizing Committee.

EPTC2023 will be the 25th Anniversary of EPTC and will be held in the Marina Bay Sands Convention Centre, Singapore, on Dec. 5-8, 2023. The normal 3-day conference will be extended by a day for an extra-special program of celebration. The fall meeting of the EPS Board of Governors (BoG) will be held in conjunction with EPTC2023 and many of the BoG members are expected to play a role in the conference. The Call for Papers will be posted soon at https://www.eptc-ieee.net/.

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Fan-out wafer-level package for memory applications

By Ho-Young Son, Ki-Jun Sung, Jong-Hoon Kim, Kangwook Lee [SK hynix Inc.]

Recently, through-silicon via (TSV) technologies have been widely used in high-bandwidth memory (HBM) for high-performance computing (HPC) or graphics applications and high-density memory modules for DDR4/DDR5. For mobile memory packaging, wire bonding technology is still being used because of the high manufacturing cost of TSVs and the performance compatibility of conventional wire bonding technologies. As the overall mobile system performance is improved, however, the conventional mobile package may have several challenges with respect to the need for a thinner package or for better thermal and electrical performance.

In this article, the Hynix Integrated Fan-out Memory (HIFOM) – a chip stackable fan-out wafer-level package – will be introduced as one of the thinnest packages that has better thermal, mechanical, and electrical performances than conventional wire-bonded type memory packages. This package has a z-height that is 15~20% thinner than conventional wire bonding-based ball grid array (BGA) packages; this was achieved by eliminating organic substrates. For thermal and mechanical characterization, the thermal resistance and warpage of a package were evaluated. Channel characteristics of memory chips were evaluated and it was found that the package had enhanced timing margin and power distribution network (PDN) impedance compared with the wire-bonded type packages.

Introduction

TSV technology is very effective as a way to increase the memory capacity by accommodating multiple chips in a package—it has also been a leading advanced technology in memory applications. However, TSV technology and its stacked chip packages require a lot of additional back-end processes and, therefore, increased manufacturing costs. Therefore, applications using TSVs are limited to leading-edge products like HBM for HPC or graphics applications and three-dimensional stacking (3DS) for high-density memory modules (see **Figure 1**) [1,2].

Contrary to the applications noted above, mobile applications are still cost sensitive and are consistently faced with requirements for thinner

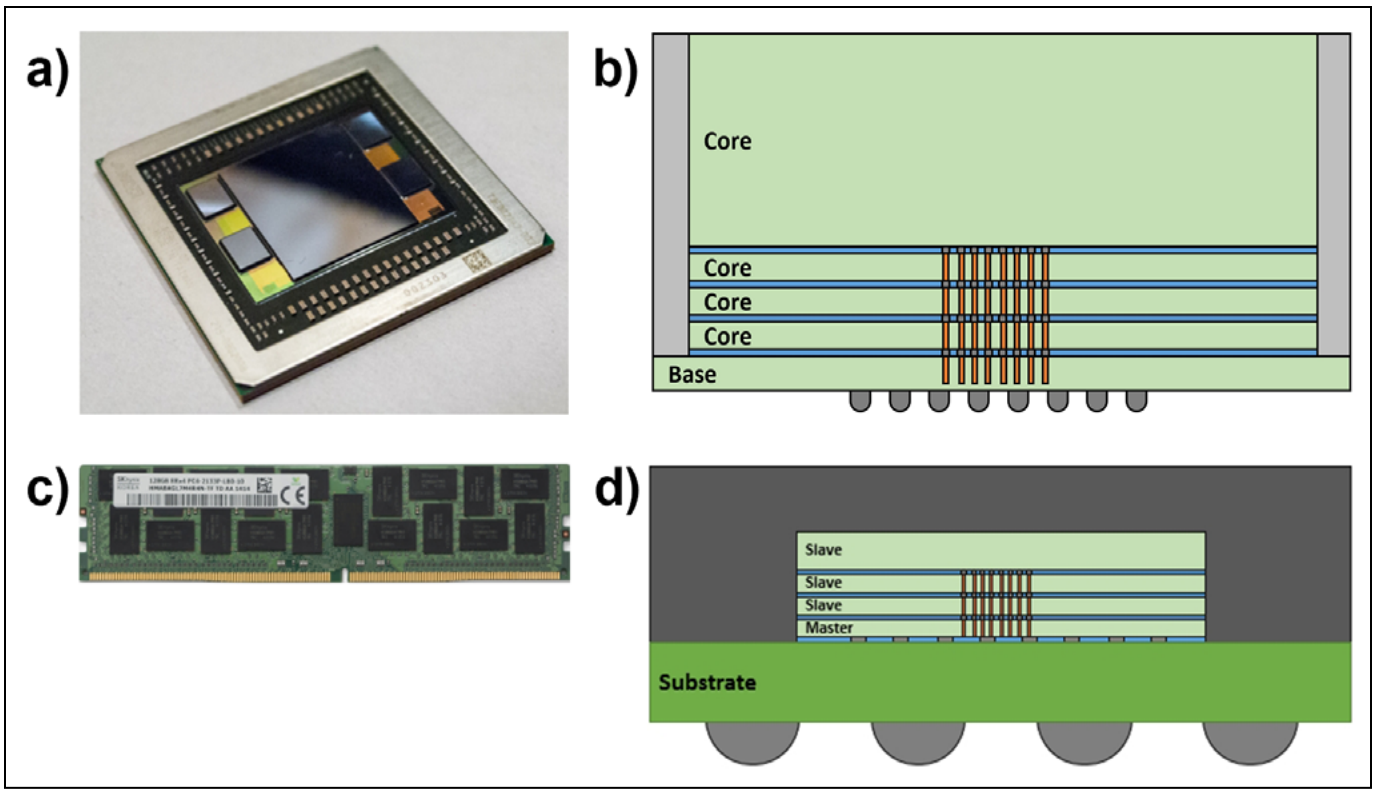


Figure 1: Memory applications using TSVs: a) 2.5D system in package (SiP) with HBM; b) schematic of a HBM known-good stacked die (KGSD); c) a 3DS memory module; and d) a schematic of a 3DS package.

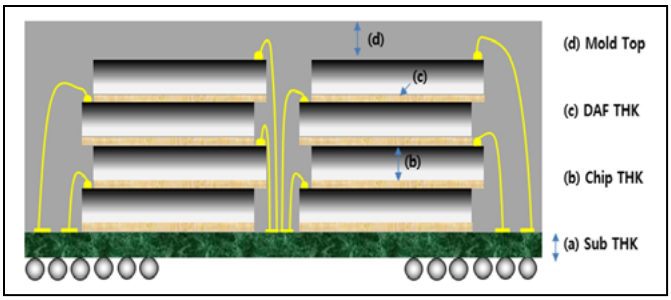


Figure 2: A simple representation of mobile memory packages with normal wire bonding interconnections.

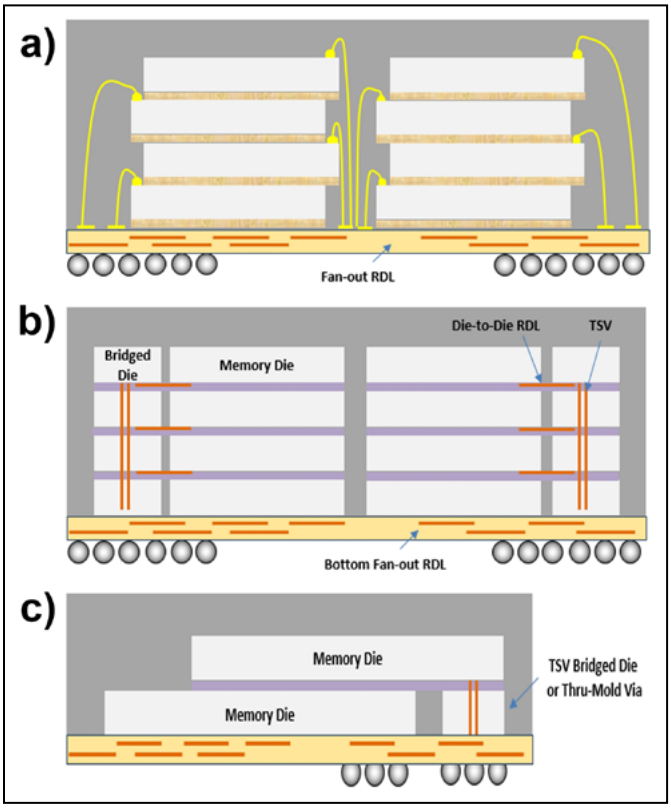


Figure 3: Several candidates of memory FOWLP.

packages and thermal and electrical performance improvements as high-performance application processors (AP) are adopted. Conventional wire bonding technologies, however, are not prone to satisfy these upcoming requirements. Figure 2 describes the typical structures of mobile memory packages with bonding wires and an organic substrate. There are several ways to reduce the package thickness by decreasing thickness of memory dies, die attached films, top mold or an organic substrate. However, everything is approaching its physical limitations, or its contribution may be very small even though it is minimized up to its critical point.

A more effective way to reduce the thickness of fan-out wafer-level packages (FOWLPs) is to eliminate organic substrates by replacing the package circuits with fan-out redistribution layer (RDL) interconnects [3,4]. Figure 3 presents several possible candidates of memory FOWLPs

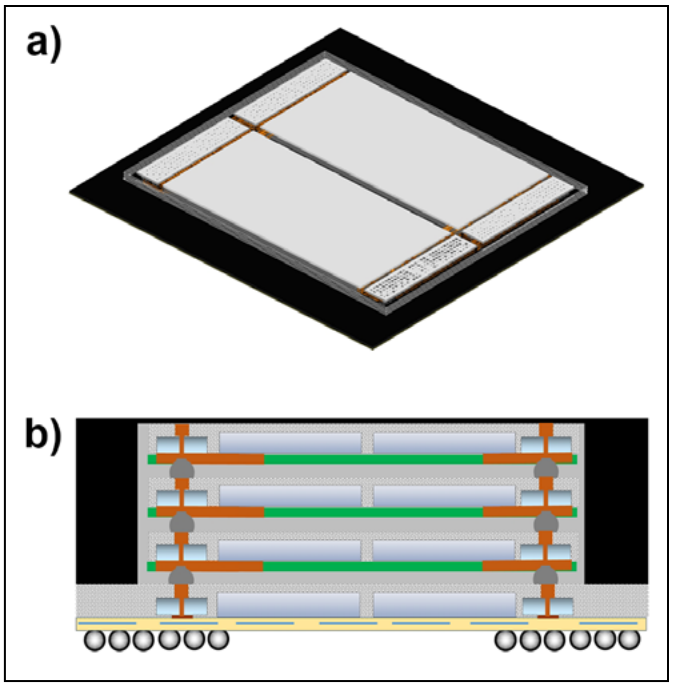


Figure 4: Schematic illustration of a HIFOM a) floor plan, and b) cross-sectional diagram.

with multiple memory dies. Figure 3a shows a fan-out package with bonding wires similar to conventional packages with no organic substrate. By the existence of loop-type bonding wires and top mold, package thickness reduction is limited. Figures 3b and 3c show two different types of FOWLPs and they are more effective at reducing package thickness because they have no bonding wires and the top mold area can be minimized. Figure 3b has a fan-out structure in which each die is individually spanned and a TSV-bridged die is connected with each die together. Its ball-out configuration is highly compatible with JEDEC standards for package on package (PoP) top packages. Figure 3c has a staircase structure using a bridged die or through-mold vias (TMVs) like tall Cu pillar bumps. Its structure is more effective when used with side-by-side packages with neighboring AP die, but it is not easy to stack up the multiple dies more than two on top of each other because its Cu pillar height should be extremely high, or

	W/B package	HIFOM	Remark
Substrate/RDL	90µm	20µm	HIFOM: RDL THK
Die THK	60µm	60µm	
DAF/BLT	10µm	40µm	
Mold Top	120µm	20µm	
Overall PKG THK	490µm	420µm (-15%)	PKG Body only, 4Hi case

Table 1: Comparison of package thickness and its constituents.

coplanarity issues may occur when separated TSV-bridged dies are used to stack three or more dies. Among three possible candidates, the structure in **Figure 3b** – called HIFOM, as noted previously – was chosen and its package characteristics were investigated in this study [5].

HIFOM structure and process flow

Figure 4 shows the detailed schematic diagram of the HIFOM package. There are a total of eight mobile memory dies with two landings and four stacks. Two dies are paired together to form one slice of a HIFOM package and then expanded by using a fan-out RDL to connect to two TSV-bridge dies. Six HIFOM slices on top have a single RDL layer and the base HIFOM on the bottom has three RDL layers along with ball grid array (BGA) balls for external interconnections. Each slice of the HIFOM is connected through TSV-bridged dies, which have no real circuitry like transistors or dynamic random access memory (DRAM) cells, and only has a back end of line (BEOL) metallization and TSV for physical interconnects. Because the HIFOM structure has no organic substrates and a wire loop on the topmost die, the package thickness can be minimized even though the bond line thickness (BLT) with micro bump joints and overmold of each HIFOM slice is a little larger than the die attached film of a conventional package. It is expected that the BLT can also be reduced by shrinking the bump size and overmold thickness later. **Table 1** presents the comparison of package thicknesses. Given that the die thickness is 60µm and the BLT of the HIFOM is 40µm, the package thickness can be significantly reduced in HIFOM.

The overall process flow of HIFOM is described in **Figure 5**. Each HIFOM slice has two mobile memory dies and four TSV-bridged dies. For the RDL fabrication, the first step is to place the memory dies and the TSV-bridged dies

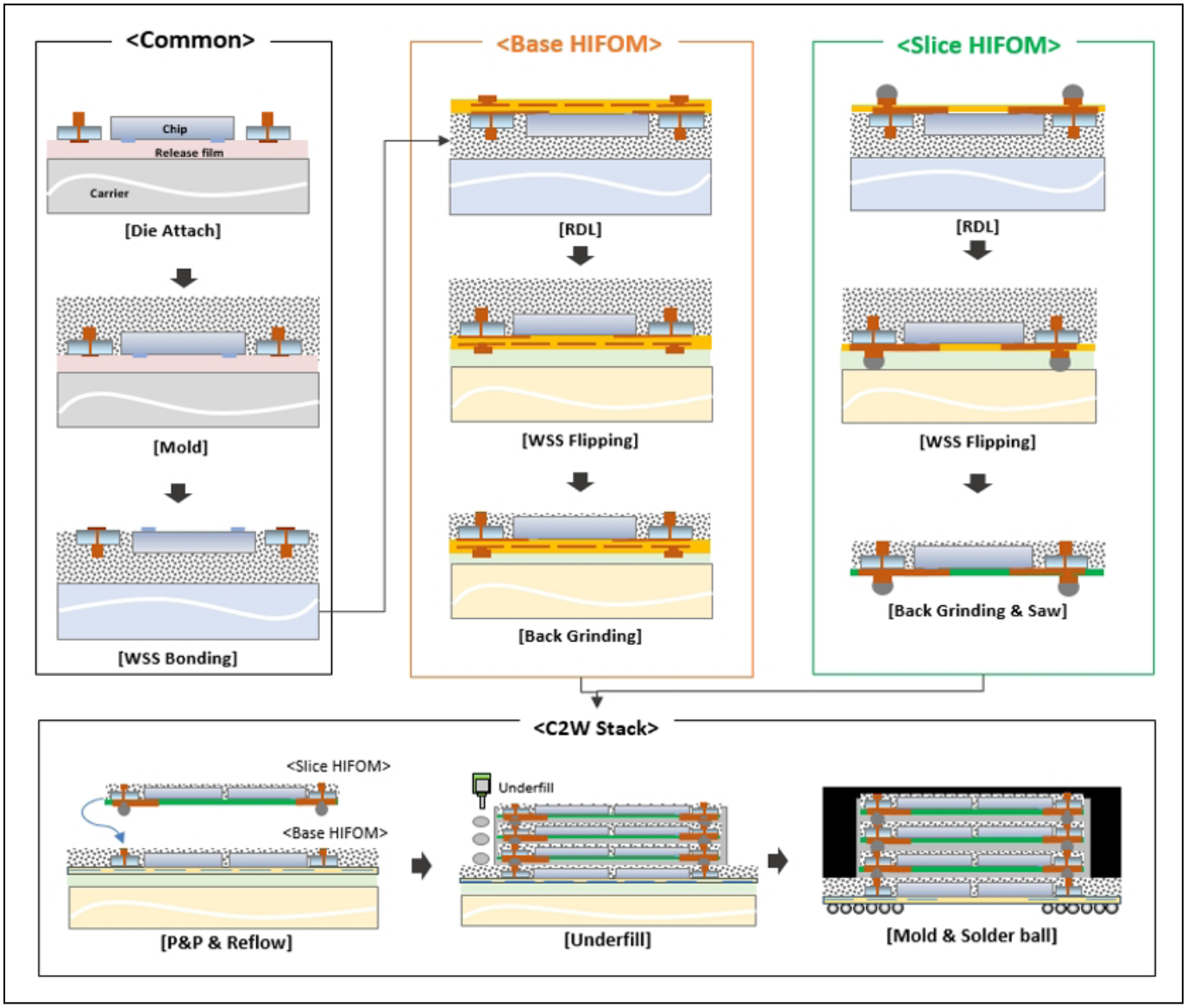


Figure 5: HIFOM process flow.

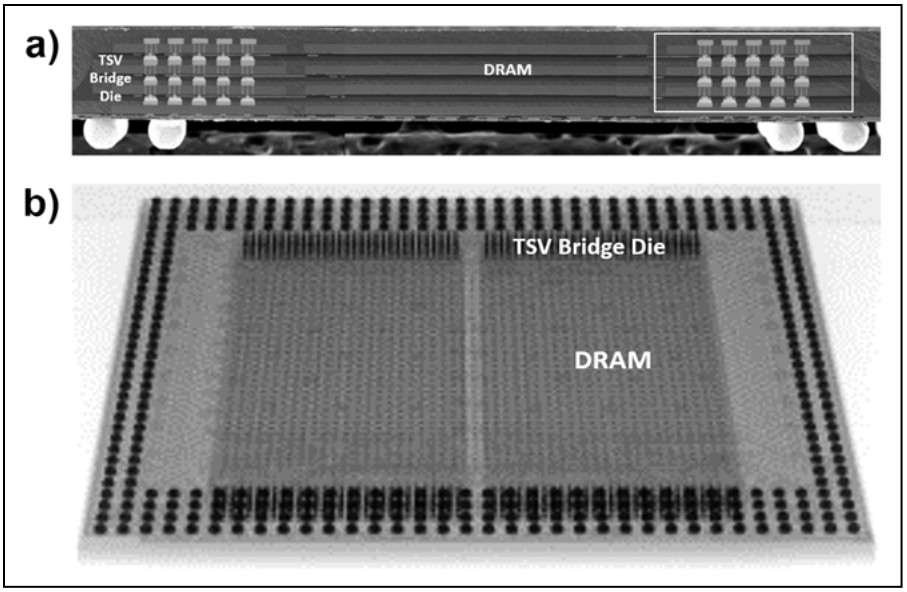


Figure 6: a) Cross sectioned and b) X-ray images of a HIFOM package.

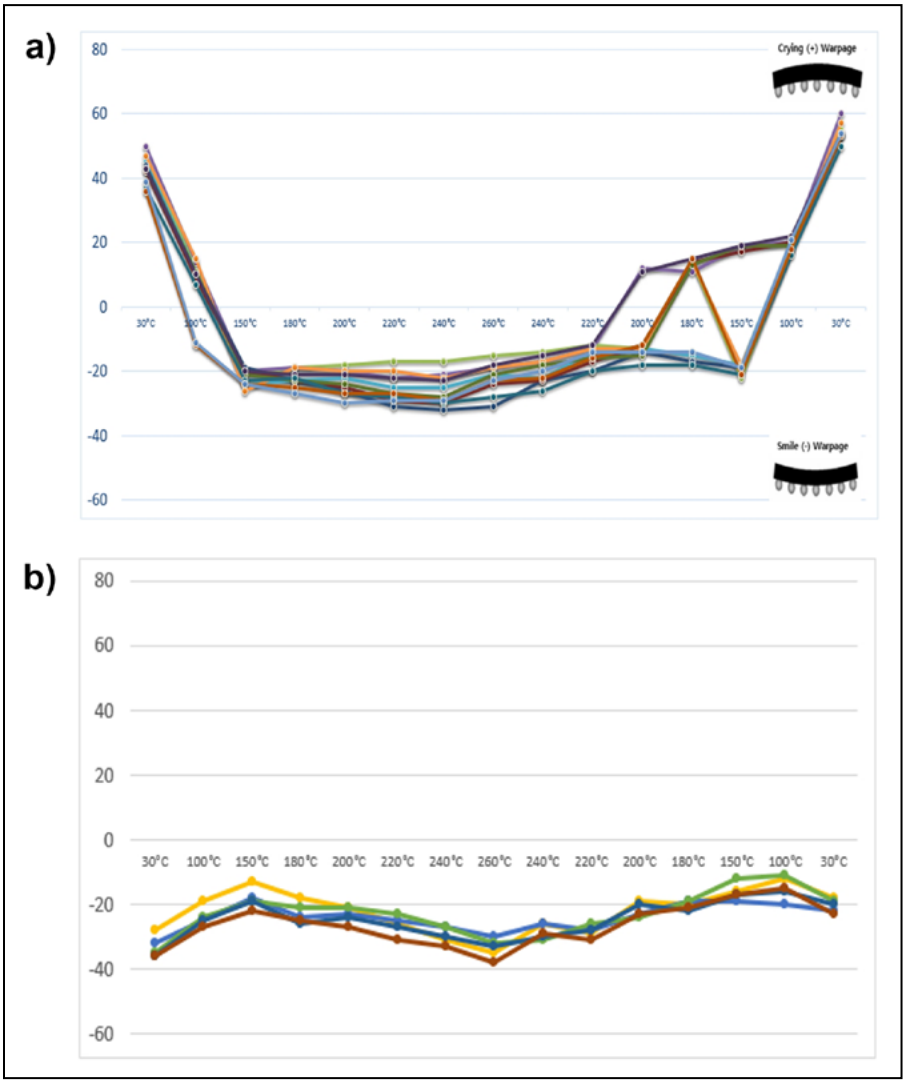


Figure 7: Warpage of a) a W/B package, and of b) a HIFOM package.

on a temporary carrier wafer using temporary adhesives and then molded and transferred to another carrier wafer using a wafer supporting system. This sequence is common for all the HIFOM slices. For the base HIFOM (i.e., on the bottom), multiple RDLs are deposited using polymer dielectrics and electroplated Cu interconnects. After RDL fabrication, the HIFOM is flipped again and the overmold is ground off using the typical backgrind process. This is a simple process that can be carried out before RDL fabrication and one carrier transferring step can be removed.

For the upper HIFOM slice, the process flow is similar to that used for the base HIFOM. The number of RDLs would be optimized depending on the pad locations of the memory die and the TSV-bridged dies. After RDL formation, solder bumps are electroplated on the RDL pads and a temporary carrier wafer is removed followed by a sawing process. Each HIFOM slice with two memory dies can be attached onto a base HIFOM and underfilled using either a capillary underfill or molded underfill process. Finally, a temporary carrier wafer at the bottom HIFOM is sliced and then BGA balls are mounted and reflowed. **Figure 6** shows the cross-sectional image and x-ray image of the HIFOM structure. It can be seen that HIFOM slices are connected with each other.

Thermal and mechanical characterization

Thermal performance of the HIFOM package in **Figure 6** was first evaluated and compared with a conventional wire-bonded (W/B) package by performing a junction temperature simulation. We assumed that the heat dissipation was in the upward and downward directions. The simulation was performed under a thermal resistance junction to ambient (θ_{JA}) and still air condition per JESD 51-2; the test board had two signals and two planes with high conductivity. Ambient temperature and power consumption were set at 25°C and 1W, respectively. As a result, thermal resistance of the top chip was much higher by the accumulation of heat flow and its junction temperature was 50.14°C for

	Conv.	HIFOM
CTE1 (50~100°C)	6.6 ppm/°C	4.1 ppm/°C
CTE2 (200~250°C)	16.3 ppm/°C	12.5 ppm/°C

Table 2: Comparison of package CTE.

the W/B package, and 48.14°C for the HIFOM package, respectively. The thermal resistance junction to ambient (θ_{JA}) of the HIFOM package was 23.1°C/W, and the thermal resistance junction to board (θ_{JB}) was 8.4°C/W. Looking at the W/B package, the θ_{JA} was 25.1°C/W, and the θ_{JB} was 9.0°C/W. Simply speaking, the HIFOM package had a 6~7% improved thermal dissipation ability compared with a normal W/B package; this result is presumed to be due to the thinner package height.

Package warpage was also measured by the shadow moiré interferometry. For the W/B package, the warpage was over 40µm with the "crying shape" at 30°C and at -20µm; the smile shape was at 260°C (see **Figure 7a**). Its warpage difference at both room and reflow temperatures was very high. However, the HIFOM package had no remarkable changes at room and reflow temperatures and its warpage difference was around 20µm (see **Figure 7b**). These results can be explained by noting that no organic substrate resulted in a lower warpage in the HIFOM packages.

The coefficient of thermal expansion (CTE) of a package was also measured and compared using a thermomechanical analyzer (TMA). A Q400 from TA Instruments was used for the TMA measurement and its temperature range was 20°C to 260°C; its ramp rate was 10°C/min. As noted in **Table 2**, the package CTE of a HIFOM package is 2.5~3.8ppm/°C less than that of a conventional W/B package. With measured package CTE and warpage, thermal cycling (T/C) stresses at the BGA ball area were also evaluated by finite element analysis. As a result, the T/C stress in the HIFOM package was 28% lower than for the conventional W/B package.

When comparing the two packages, the T/C stress corresponded to the comparison data of lower warpage and CTE value.

Electrical characterization

In this study, the electrical performance of the HIFOM package has been investigated using an electrical simulation. A high-frequency structure simulator (HFSS)

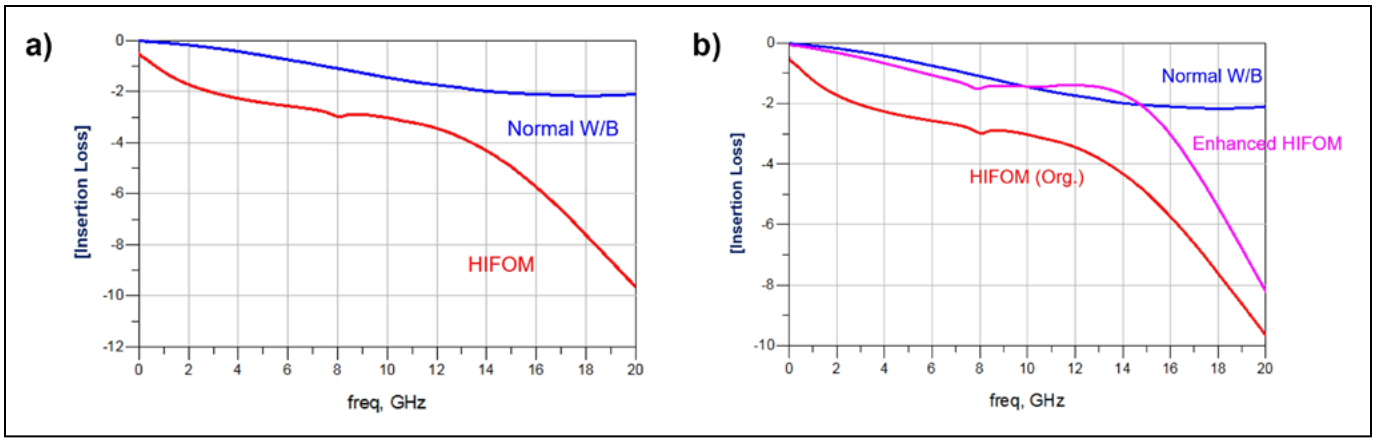


Figure 8: Insertion losses of a) W/B and HIFOM packages, and of b) an enhanced HIFOM package.

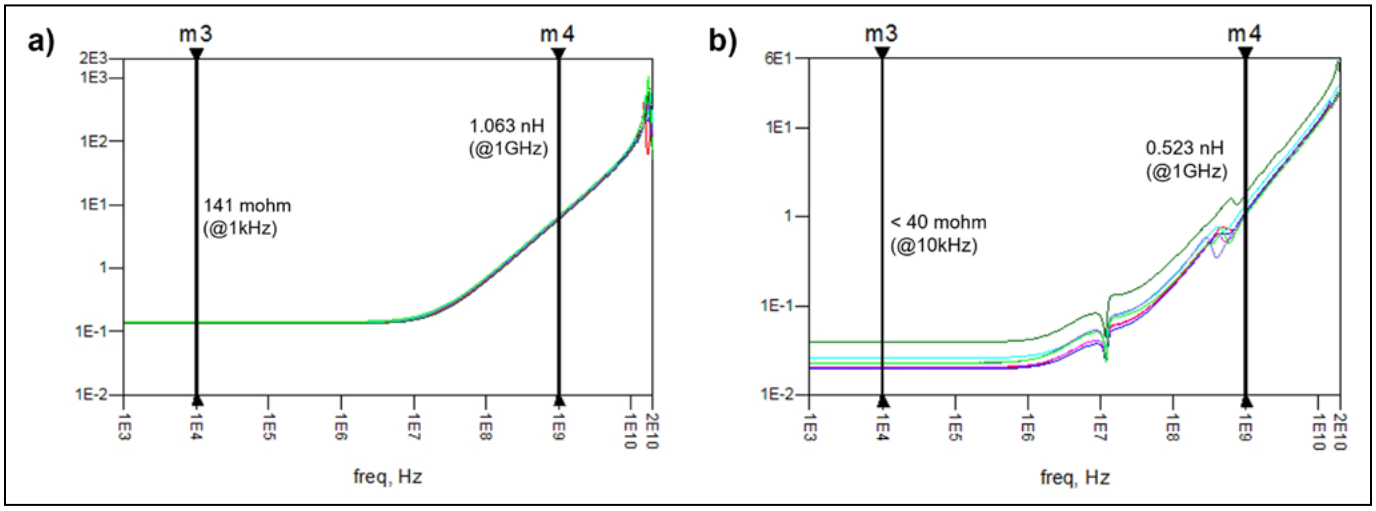


Figure 9: PDN impedances of a) a W/B package and b) a FOWLP.

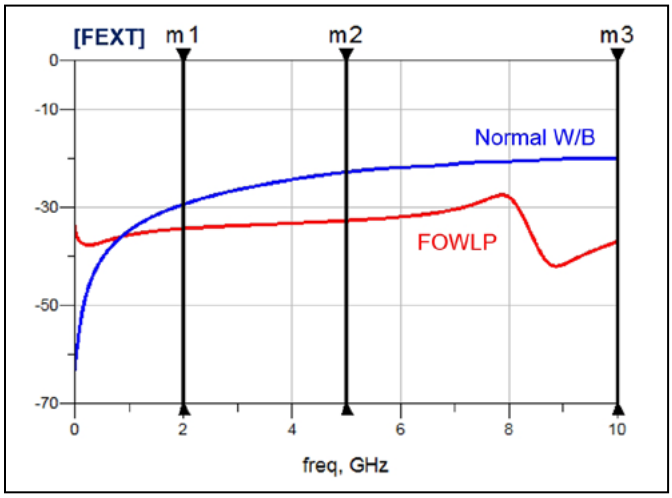
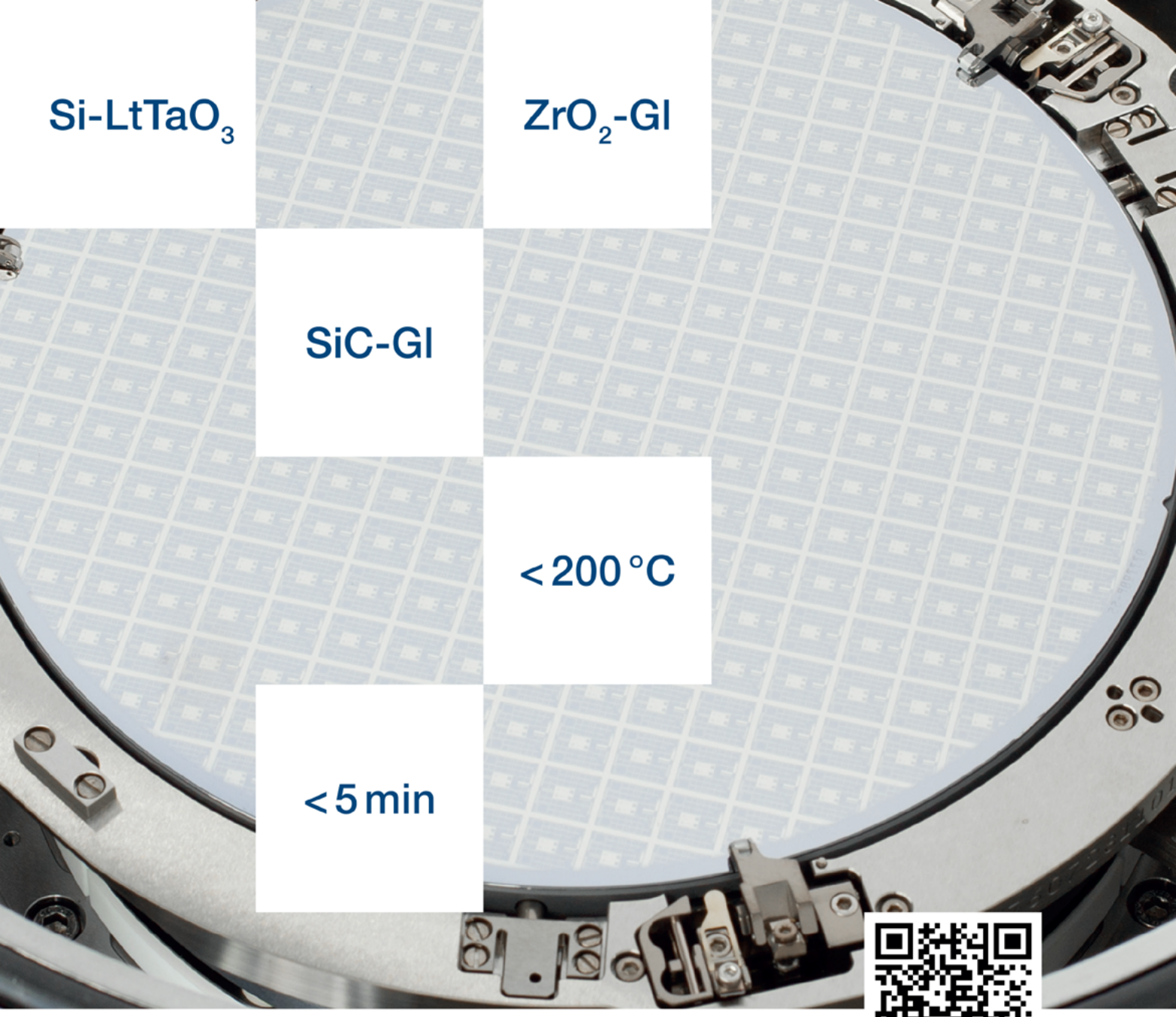


Figure 10: Crosstalk curves of a normal W/B package and of a FOWLP.

tool from ANSYS was used for the model extraction and a HSPICE simulator was used for the time domain analysis. **Figure 8a** shows the insertion loss for the normal W/B package and for the HIFOM package. Contrary to the expectation, the HIFOM package had poor insertion loss that was presumably due to high capacitive elements in the TSV-bridged dies that have a thin dielectric and large metal pad under bump joints for die stacking. Therefore, we optimized the fan-out RDL and TSV-bridged die design by adding the power ground in the metal line and reducing the pad size for better electrical performance. The purple-colored curve in **Figure 8b** shows the improved insertion loss after design optimization; the modified design had a similar insertion loss up to 16GHz.

We also evaluated channel signal integrity/power integrity (SI/PI) characteristics of a PoP package with a DRAM package at the PoP-t (top) and an AP package at the PoP-b (bottom). The driver model used in the study was based on the 1a nm 8Gb LPDDR4x spice model and typical ring-oscillator delay condition; additionally, a 150mV V_{ref} with a V_{IH}/V_{IL} of ±60mV mask was applied in order to do a comparative study of variant package conditions.

As described in **Figure 9**, a FOWLP with enhanced HIFOM showed improved PDN impedance than a normal W/B package. In the low-frequency region, the resistance was decreased by about 70%. In the high-frequency region, the inductance was also decreased by about 50%. This HIFOM package has high design flexibility in the



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	2GHz	5GHz	10GHz
Normal W/B	-29.3dB	-22.75dB	-19.9dB
FOWLP	-34.27dB	-32.67dB	-36.8dB

Table 3: Far-end cross talk (FEXT) comparison of a normal W/B package and FOWLP at various frequencies.

routing of power and ground lines. In addition, multiple power TSVs or fine interconnects of TSV-bridged dies are also able to provide the benefits of low-power impedance. Crosstalk was also evaluated as presented in **Figure 10** and it showed an extremely low value compared with the normal W/B package. As noted in **Table 3**, the crosstalk of the FOWLP is reduced by 5~17dB as the frequency. As the frequency is higher, the improvement of crosstalk is more dominant in the FOWLP.

SI timing margins of a PoP system were also investigated at various clock speeds. The data eye window in the W/B package is very narrow, while it has a much wider window in FOWLP with enhanced HIFOM, as shown in **Figure 11**. **Figure 12** shows the timing margins of the PoP system with various DRAM and AP packages. **Figure 12a** shows the timing margin for various DRAM packages with a substrate-type AP package. Compared with normal W/B DRAM packages, FOWLP-type DRAM packages showed better timing margin and enhanced HIFOM had much improved results. At 6400Mbps, PoP with enhanced HIFOM is only available at over 20%. In addition to the adoption of FOWLP to DRAM packaging, its implementation in AP packages can also provide a much wider timing margin as shown in **Figure 12b**. While the amount of improvements in the timing margin is not so much at low speeds (e.g., around 3,733Mbps or 4,266Mbps), the timing margin at high speed can be greatly enhanced and its amount is almost up to 50% at 6,400Mbps. Based on our investigation, it can be concluded that co-adoption of fan-out technologies to AP packages – and DRAM packages as well – showed the best performance in timing margin. In summary, the overall performance difference as a function of clock speed is presented in **Figure 13**. At low

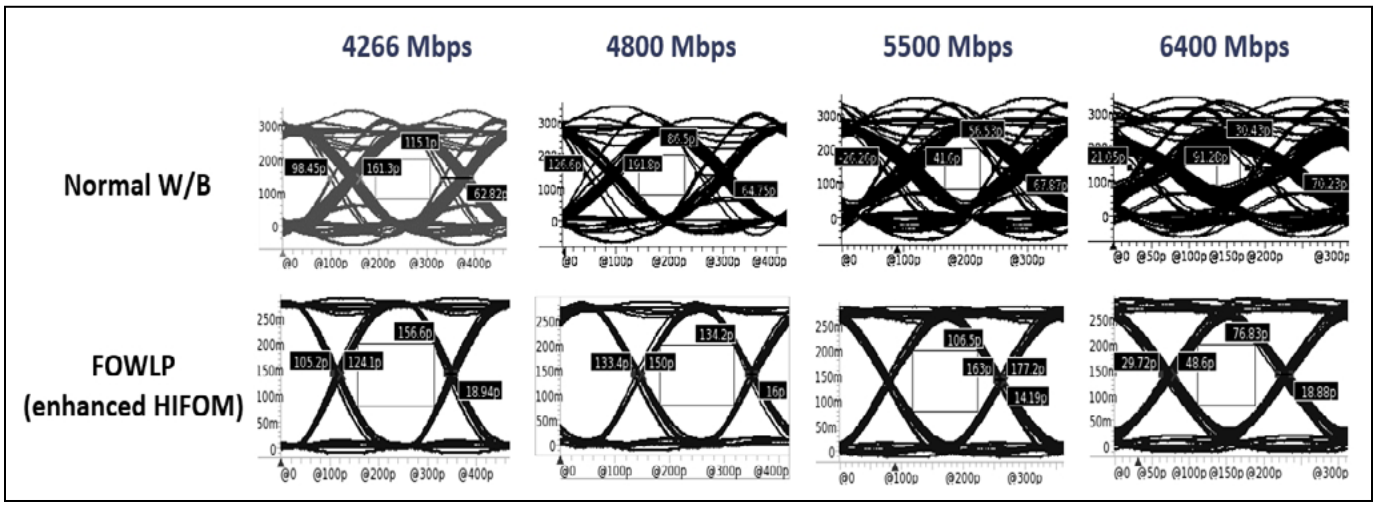

Figure 11: Data eye diagrams for two different packages at four different frequencies.

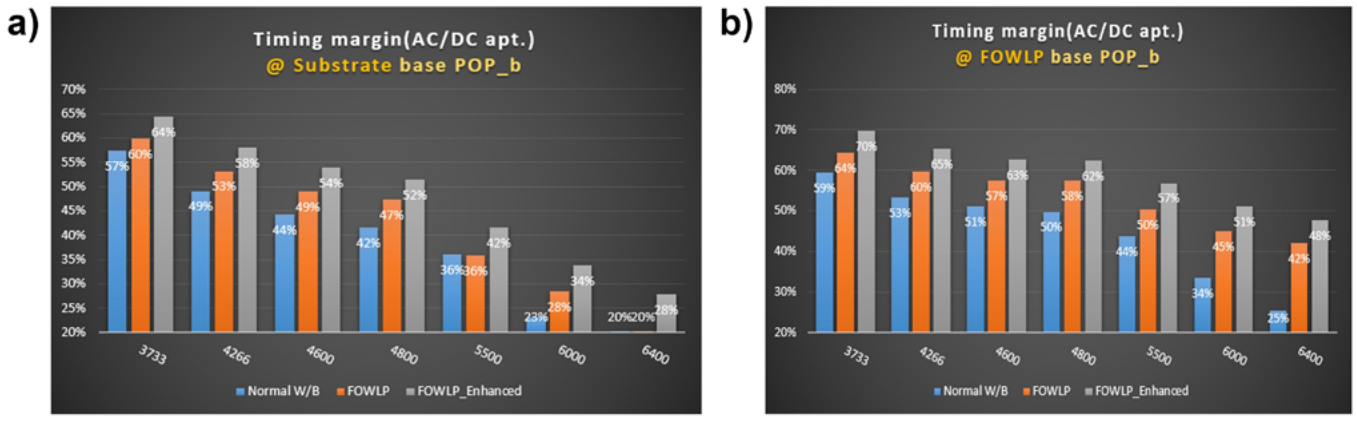

Figure 12: Timing margin of a PoP system for various DRAM package types with a) a substrate-based AP package, and b) a FOWLP-based AP package.

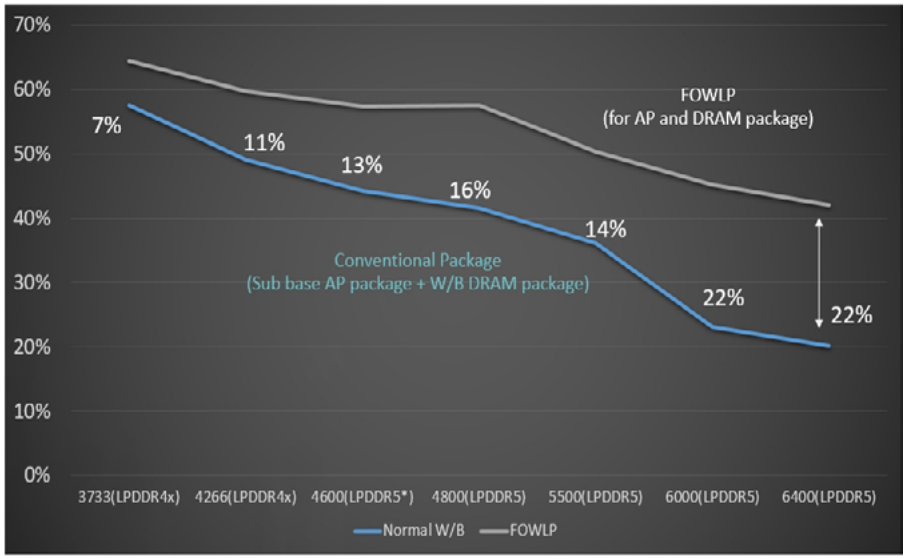

Figure 13: Delta of the timing margin as a function of clock speed.

speed, the gap of the timing margin is only 7% between the conventional package and the FOWLP. However, the gap increases up to 22% at high speeds around 6000~6400Mbps.

Summary

In this study, the utilization of FOWLP in DRAM applications and the HIFOM structure have been introduced. These structures and their effectiveness in terms of form factor, thermal, mechanical and electrical performances, have been investigated. Having a thinner package thickness in a FOWLP by eliminating organic substrates would be a distinguishable benefit—and it will be well aligned with a consistent requirement on the package z-height reduction. Adding to this advantage, low CTE and small warpage may provide a wide process window in the PoP assembly with which the thermal behavior of the two different packages should be well matched. Enhanced thermal performance that results when using a thinner package height would be a potential advantage considering the future trends of SoC power being incrementally increased. Moreover, the improved results in terms of electrical performance such as channel SI, PDN impedance, and crosstalk, can have superior aspects of FOWLP that can drive and accelerate its adoption to both DRAM and AP packages.

In spite of the huge advantages of FOWLP, there are several hurdles for its implementation to mobile applications. As expected, high manufacturing cost can be a critical problem for mobile applications because they are very sensitive to the product cost and the value chain of the ecosystem is determined by cost competitiveness. Cost reduction activity is definitely needed for FOWLP adoption in mobile products. In addition to cost reduction for a given product, broadening its adoption or application to diverse systems would be good alternatives to managing the manufacturing cost. Fortunately, more opportunities with respect to advanced packaging technologies are open to many DRAM-related systems and the use of FOWLP in DRAM packaging is one of them.

Acknowledgment

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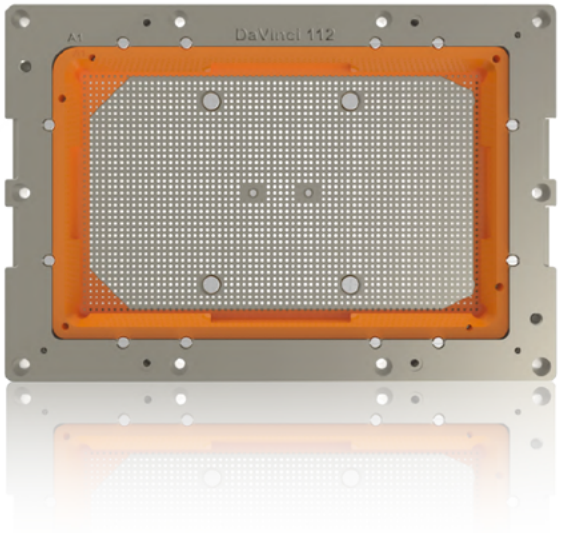

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Measuring bump height uniformity to improve yield using 3D inspection

By Tim Skunes [Nordson Test & Inspection]

Chip-scale wafer-level packaging (WLP) offers important benefits—small package size and the ability to process hundreds or thousands of dies in parallel. A variety of bump configurations are possible, depending on the application, as shown in **Figure 1** [1]. One challenge with WLP is maintaining uniformity of solder bumps or copper pillars across a 300mm wafer. Metrology and inspection are necessary to ensure device reliability. Shrinking bump heights and spacing and high aspect ratios, however, make wafer-level bump height inspection especially challenging. It is also increasingly critical because minor variations in bump height across a wafer can reduce overall yield. Defects related to bumping can affect both thermal and electrical device performance [2].

It can be tempting to cut down on the number of inspection steps or only test a sample of wafers coming through the line. Doing so can speed up production. For legacy processes where the yield is high, a partial inspection may be the best approach. When design rules change and yield drops, it becomes apparent that reducing inspection does not save time in the long run. The best way to improve yield, especially for a new process, is to identify defects early. That often requires 100% inspection across each wafer in every batch. Stringent inspection protocols help identify the root cause of defects and reduce the need to rework or scrap wafers.

Existing bump height measurement methods have two drawbacks: speed and placement in the process flow. They slow down production and often do not catch defects early enough in the process. While 100% inspection is commonplace during process development, it is often abandoned for high-volume production because of the time required for testing. Fast, accurate metrology and inspection are the key to success. This article explains the benefits of 3D fringe projection technology to inspect solder bumps and copper pillars at the wafer level, comparing it to conventional approaches for bump height measurement.

Conventional bump height measurement

Pillar bumps consist of three layers: a copper pillar, a nickel barrier layer, and a tin/silver/copper (SAC) solder bump. Bump height measurements are typically taken after the final photoresist stripping step, as shown in **Figure 2**. This occurs after all three layers of the bump have been deposited.

Conventional noncontact bump height measurement relies on line scan triangulation. An incident beam of laser or white light deflects off the object being measured. With line scan triangulation, the light source projects a line onto the object. A detector with an array of photosensors captures the reflection and calculates the distance. Scanning across a wafer produces a map of bump height data. Line scan triangulation has two primary drawbacks. One of these is speed. A 300mm wafer can contain hundreds of millions of copper micro bumps [3], and 100% inspection is not economical.

The other drawback to line scan triangulation is that it happens too late in the manufacturing process. Inconsistent copper plating is often

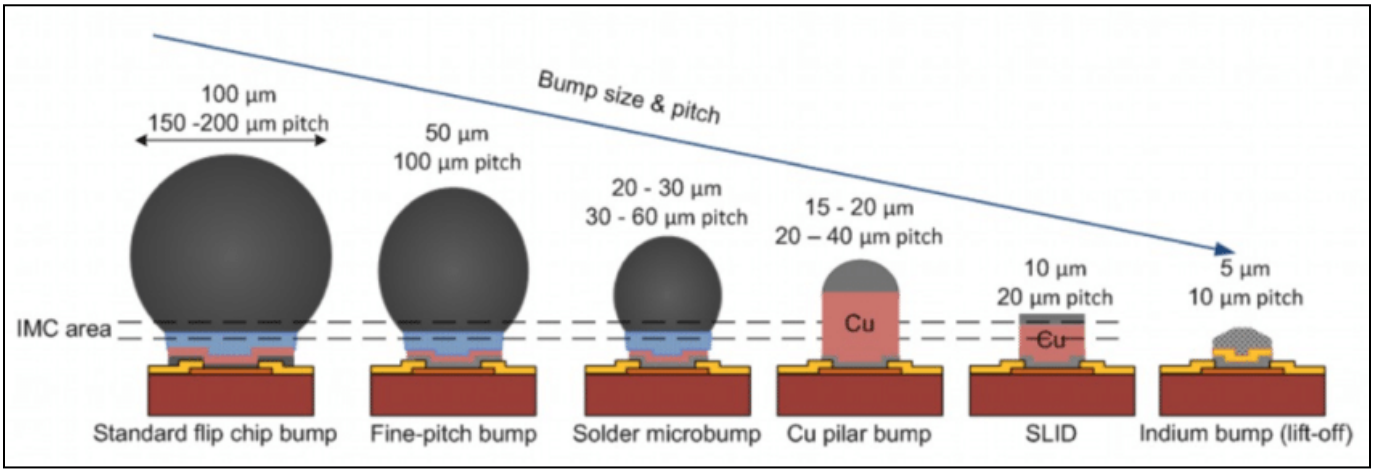

Figure 1: Evolution of bump size and pitch. Image courtesy of T. Tick and S. Vahanen [1]

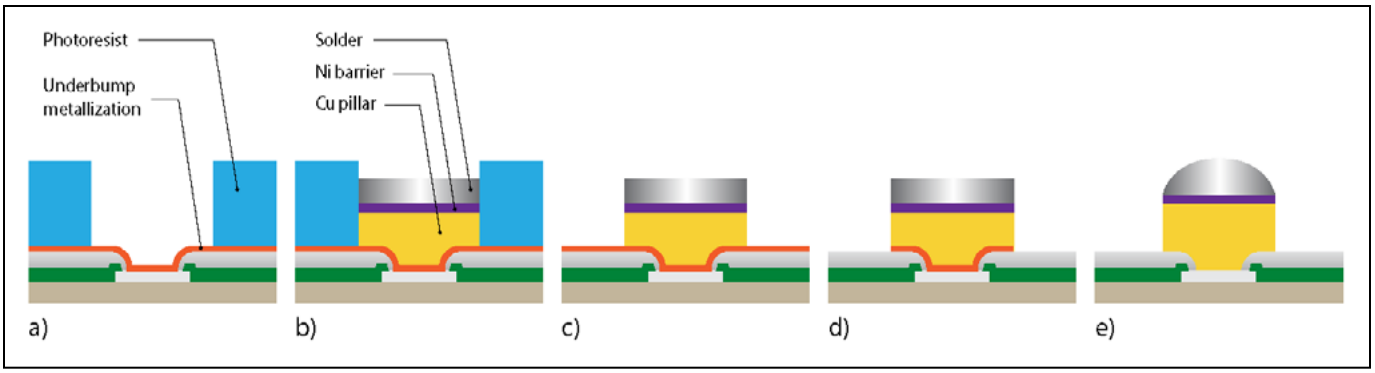

Figure 2: Copper pillar bump process flow. Conventional bump height measurement is done after photoresist stripping; a) before bumping; b) bump plating; c) photoresist strip; d) UBM etching; e) solder reflow.

the source of nonuniformity across a wafer. It is best to measure the copper pillar height as early in the process as possible and definitely before photoresist stripping. Identifying the problem at that stage is preferable so that adjustments in the plating process can be made before running more wafers through the tool. Measurement with the photoresist in place is challenging for line scan triangulation because nonuniformity in photoresist thickness affects accuracy and repeatability [4].

3D fringe projection technology

The 3D fringe projection technique, also known as fringe projection profilometry, offers a solution to these challenges [5]. The system comprises a digital projector that projects sinusoidal patterns and analyzes the projected patterns with a high-speed complementary metal-oxide semiconductor (CMOS) detector. The projector is arranged to illuminate the surface at a set angle, and the camera measures the intensity of the light reflected from the object under test. The field of view is an area rather than a line. Three-dimensional objects, including solder bumps or pillars, distort the illuminated fringe pattern. A reference image of a known height and shape, such as the very large-scale integration (VLSI) step standard in **Figure 3**, is used to verify the accuracy of the system.

The resolution of the CMOS detector and the optics determines the pixel size. There are three unknown parameters at each pixel: phase (φ_0), reflectivity (R), and modulation (m). The phase encodes bump height. By combining light intensity data from at least three fringe pattern images, it is possible to solve for the unknown parameters at each pixel and determine the bump height. The light intensity I is given by the expression in **Equation 1**, where I_0 is the peak of the projected intensity, R is surface reflectivity, and f_x is the frequency of the sinusoidal pattern.

$$I = \frac{I_0 R}{2}\left(1 + m\sin(2\pi f_x + \varphi_0)\right) \quad \textbf{(Eq. 1)}$$

Addressing multi-path reflections

One challenge with optical imaging methods is that multiple reflections from shiny surfaces like silicon wafers, copper pillars, or solder bumps can affect the accuracy of the measurement. Multi-Reflection Suppression® (MRS®) technology identifies extraneous reflections from shiny and specular surfaces. The algorithm treats these reflections as noise and rejects them. The result is an accurate, ultra-high-resolution,

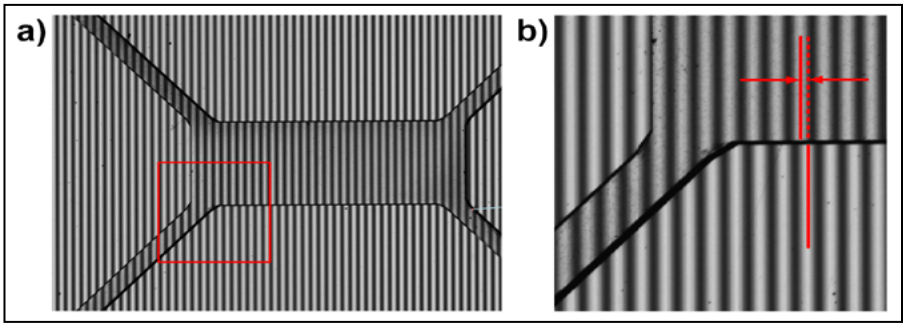

Figure 3: The projected fringe pattern is distorted (shifted) wherever the height of the imaged object changes; a) (left) The VLSI step standard in this example is a recessed rectangular feature on a flat background; b) (right) A close-up of one corner shows the phase shift, indicated by the red arrows, more clearly.

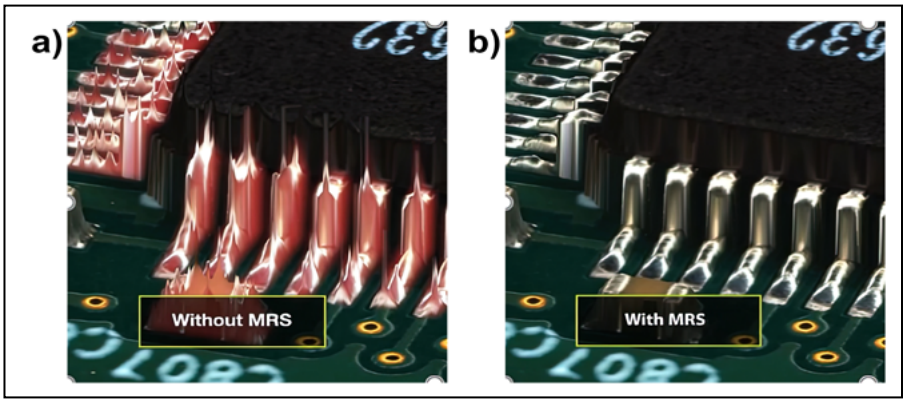

Figure 4: Imaging a) without and b) with multi-reflection supression technology®.

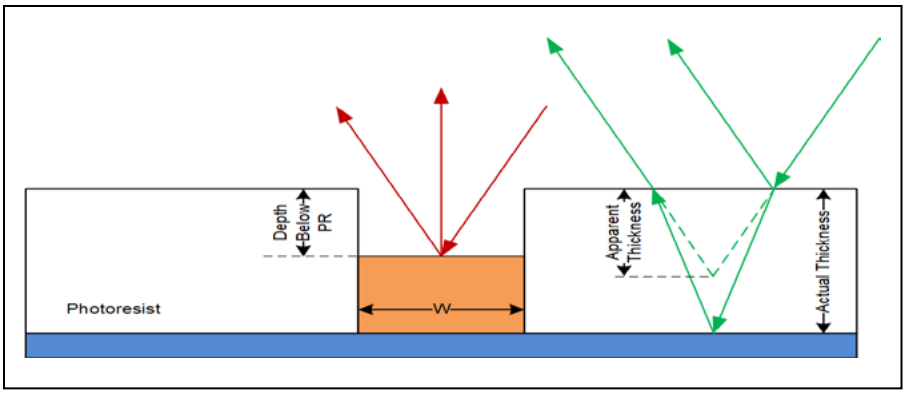

Figure 5: Measurement of bump height before photoresist stripping, using light refracted through the photoresist to determine the photoresist thickness and calculate bump height above the wafer surface.

image free from distracting artifacts. Beyond the visual appeal (see **Figure 4**), the MRS system enables more precise height measurements. It is currently capable of measuring bumps 25µm in diameter with 3µm lateral resolution and 0.05µm vertical (Z height) resolution.

Advantages of fringe projection with MRS

Fringe projection technology offers greater throughput compared to line scan triangulation, in part because it images an entire area at once rather than line by line. The field of view and frame rate are important parameters. A system with multiple cameras and projectors operating in parallel at high frame rates allows the technology to scale.

Our new fringe projection technology is rapid—collecting a 2D scan of the wafer and height measurements of 3D features in a single pass. The system inspects 100% of the bumps on a 300mm wafer in minutes. By analyzing 75 million points every second, it achieves a throughput of greater than 25 wafers per hour. The fringe projection system images copper pillars before the photoresist is stripped, either directly after copper electroplating or after applying a solder cap but before reflowing the solder. This is a critical advantage because it provides diagnostic data on the copper plating and solder bumping processes. This allows for process correction if the plating is out of tolerance.

As the wafer is scanned at high speed, photoresist thickness is measured to determine the substrate height. A portion of the incoming light reflects directly off the top surface of the photoresist. The rest of the light passes through the photoresist to the wafer surface and is refracted as it exits the photoresist. Given the photoresist index of refraction and data from the sensor, the system measures the photoresist thickness.

Because the imaging system scans an area instead of a line, it can simultaneously measure photoresist thickness and bump height. There are geometrical limitations on the photoresist and the bump to enable accurate bump height calculation. Currently, the photoresist must be at least 45µm-thick to distinguish between direct reflection from the photoresist surface and reflection from the substrate. The bump height must be less than the photoresist thickness but not too far below it. The maximum difference between the bump and photoresist thickness – the depth below photoresist, as shown in **Figure 5** – is approximately twice the width of the pillar. If the aspect ratio between the depth and the width is too high, the light will deflect off the sides of the photoresist rather than reflect directly to the CMOS detector.

Bump height uniformity measurements from 3D fringe projection are consistent with data from a reference confocal measurement system. The reference system is highly accurate but takes

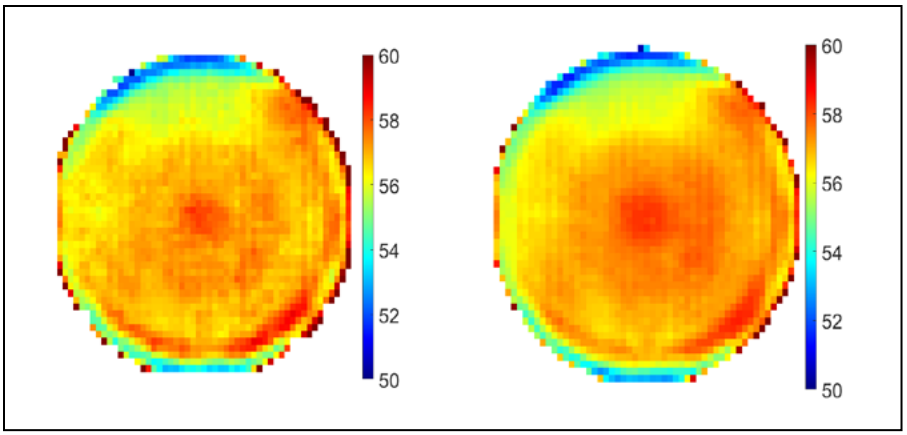

Figure 6: a) (left) Bump height uniformity measured with the NanoResolution MRS sensor, and b) (right) the reference confocal measurement system show consistent results. Units are in µm.

several hours to inspect one 300mm wafer. The sample wafer in **Figure 6** has regions at the top and bottom of the wafer where bump height is low and regions at the sides and center of the wafer where bumps are higher than average. The correlation between the two images demonstrates the accuracy of the 3D fringe projection data.

Benefits of 100% inspection

There are several reasons to conduct a 100% inspection on every wafer during the bumping process. By collecting comprehensive bump height data, operators can identify the following:

- Cluster defects, which indicate an equipment or process issue;
- Repeating defects, which suggest mask or reticle errors; and
- Variable bump height distribution, which can reveal performance differences between plating machines or plating cells.

The results of these measurements allow operators to adjust the process in real time to improve yield and reduce the need for rework. Why wouldn't a fab do 100% inspection? The answer lies in the method. Probe cards, for example, can measure an entire wafer at once but cause damage that could affect yield in subsequent process steps. Conventional triangulation is often too time-consuming to conduct on every bump on every wafer. Fringe projection technology with MRS overcomes the limitations of both conventional triangulation and probe cards. It is nondestructive, rapid, and accurate.

Key applications

Fringe projection technology is ideal for WLP applications with millions of solder bumps or copper pillars per wafer. Performing 3D and 2D metrology and inspection in a single pass is especially valuable. Conventional triangulation with either lasers or white light involves a single light source and only one receiver. That approach requires a separate scan with a 2D camera to measure lateral bump size or inspect for surface defects. The MRS sensor merges multiple 3D images and one 2D image from a coaxial camera. The result is a combined image that displays the location and size of the bumps on the wafer along with bump height data, as shown in **Figure 7**. The system acquires these images in 150 milliseconds.

The approach described above is not only valid for wafers, however. The technology has been demonstrated with surface mount technology (SMT) components, mini and micro light emitting didoes (LEDs), memory modules, and printer cartridges. It is helpful in backend semiconductor applications for inspecting integrated circuit (IC) packages. For example, consider a substrate with C4 solder bumps distributed across an area of 22 by 50mm. The 3D fringe

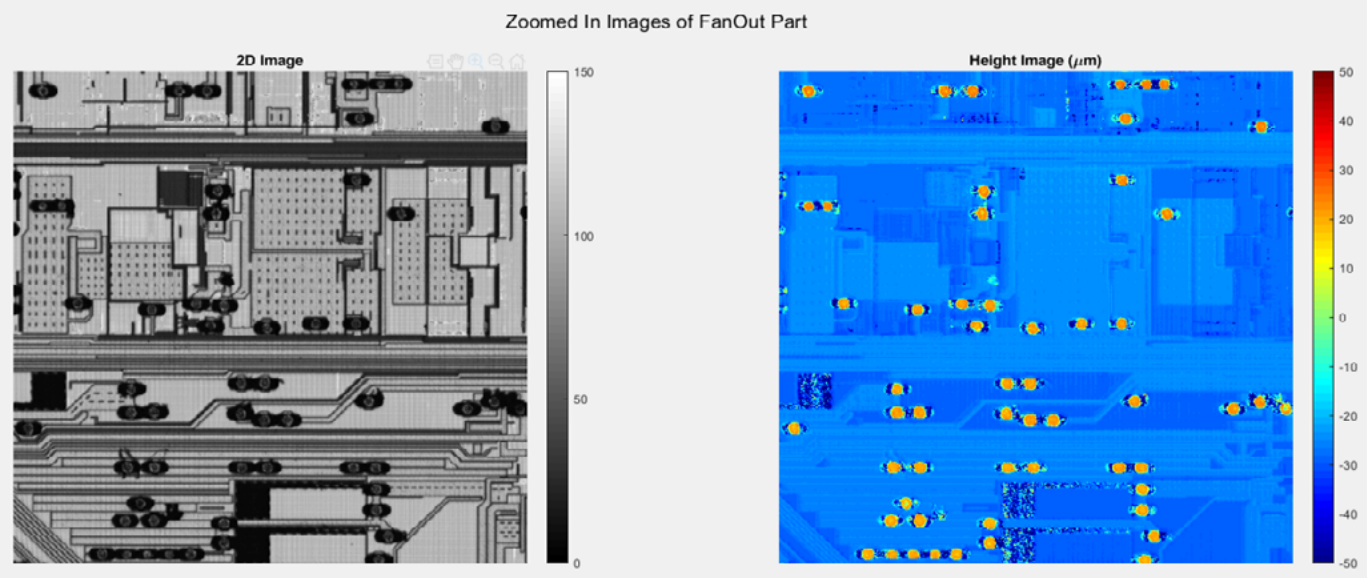

Figure 7: a) (left) A 2D image of fan-out patterns on a wafer; and b) (right) a merged image showing superimposed bump height data.

projection system can inspect 600 units per hour compared to around 200 units per hour for competing approaches. In addition to throughput advantages, fringe projection technology measures both photoresist thickness and bump height uniformity during the bumping process.

Summary

3D fringe projection is a nondestructive measurement technique that combines speed and accuracy. It can measure the height of solder bumps and copper pillars before photoresist stripping for WLP and other applications. Wafers that do not pass uniformity screening may be able to be reworked before further processing. Patterns in bump height uniformity across the wafer provide valuable clues to the source of the defects, identifying whether to adjust process parameters or address mask or reticle errors. This allows engineers to make real-time adjustments that reduce waste and maximize yield. Doing so avoids the cost of scrapping large numbers of wafers that might otherwise proceed through a faulty plating process.

The technology is scalable to meet future industry roadmaps (see **Figure 1**). The second-generation MRS system features more precise sensors that cut the resolution in half, allowing for accurate measurement of smaller features. As a result, fabs can commit to a 100% bump height inspection on every wafer, improving yields and reducing cost.

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Biography

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Ultra-thin mold cap for advanced packaging

By Nabankur Deb, Xavier Brun [Intel Corporation], Chris Masuyama, Yoshikazu Hirano, Kei Ganbayashi, Hiroki Oshida [TOWA Corporation]

To enable advanced, smaller and cheaper packages with finer-pitched structures, wafer-level packaging (WLP) has emerged in recent years as a solution [1-2]. For the development of the mold process with WLP, previous research has investigated several different aspects of molding. These include carrying out the process with different types of mold compounds (granular, liquid and sheet mold) [3-5] as well as different molding processes (transfer molding, face-up and face-down compression molding [6], and vacuum imprinting). Sheet-type mold material has been gathering some interest lately [4], but liquid and granular materials are still more ubiquitous. While liquid materials have been shown to be good for filling finer gaps and easier to flow, granular materials are easier to use and cheaper—and with the right filler size, also enable better fill of finer pitches, as well as good thickness and warpage control [2-3]. This has led to more interest in utilization of granular material in WLP development. Similarly, the vacuum-assisted face-down compression molding process developed in the last few years has shown promise for WLP because it avoids the drawbacks of some of the other processes in terms of low-pressure processing and the void-free requirement of the mold layer, while minimizing die shift [6-7]. Through our current studies, we have looked to leverage the compression molding process to devise a new ultra-thin mold cap solution for WLP. By controlling the processing conditions, we managed to obtain a low warpage, ultra-thin uniform mold cap with applications in fine-pitch WLP.

Materials and experimental setup

The following sections discuss various aspects of the materials used, the experimental setup and process skews.

Compression molding. To help achieve a thin and uniform mold cap with properly encapsulated solder balls at significantly lower pitches, we chose to leverage the use of the compression molding technique. Samples were prepared at Intel Corporation and subsequently compression molded at TOWA Corporation.

In this process, the wafer is held face down on the upper chase, while resin is dispensed on the release film to set on the lower chase. An optimized release film was utilized to ensure proper encapsulation of the bumps. Both top and bottom mold chases can control the process temperature independently, which gives good control of temperature during processing.

The top mold chase can preheat the wafer prior to the mold process, then clamp down for the uniform temperature mold process. As a result, uniform resin covers the entire wafer evenly, thereby minimizing or eliminating excessive resin flow and/or localized resin overheating for a wide range of process parameters (Figure 1a).

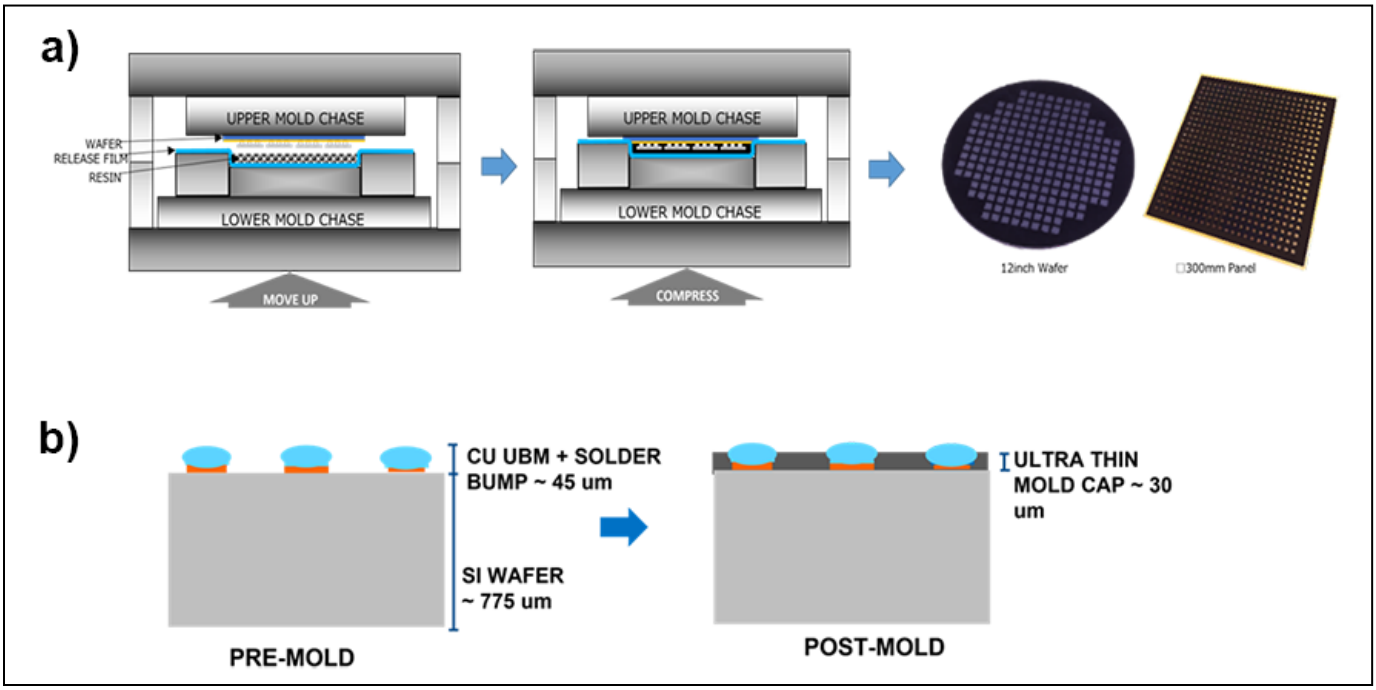

Figure 1: a) Stepwise compression molding at the wafer or panel level; b) Wafer stack with thin mold cap and exposed solder balls pre- and post-mold.

Resin Type	Granular	Liquid
Filler Cut Size (µm)	Large (10-20 µm)	Small (<=10 µm)
Gel Time (s)	Lower (Higher temp)	Higher (Lower temp)
Specific Gravity	Higher	Lower
CTE1 (ppm)	Lower	Higher
CTE2 (ppm)	Lower	Higher
Tg (°C)	Higher	Lower
Resin cut size	0.7-1 mm, 1-1.5 mm, < 2 mm	NA

Table 1: Resin chemical and physical properties.

Skew	Purpose	Parameter
Granular size	Evaluate influence of different dispensing patterns	<2.0 mm 1.0-1.5 mm 0.7-1.0 mm
Temperature	Evaluate influence of different reaction speeds	150°C 130°C
Pressure	Evaluate influence of different process pressures	11 MPa 8 MPa
Press speed	Evaluate influence of different flow speeds	0.2 mm/s 0.1 mm/s
Material amount	Evaluate the effect of different material quantities	4 mg 3 mg

Table 2: Compression molding process skews.

Sample No.	Process skews	Wafer mold coverage
1	Resin size 0.7 – 1.0 mm	ok
2	Resin size 1.0 – 1.5 mm	ok
3	Resin size <2.0 mm	ok
4	Temperature 150°C →130°C	ok
5	Resin size <2 mm, Press pressure 11 MPa → 8 MPa	incomplete fill
6	Resin size <2 mm, Press speed 0.2 mm/s → 0.1 mm/s	incomplete fill
7	Resin size 0.7 – 1.0 mm, Press pressure 11 MPa → 8MPa	incomplete fill
8	Resin size 0.7 – 1.0 mm, Press pressure 8 MPa, Press speed 0.05 mm/s	incomplete fill
9	Resin size 0.7-1.0 mm, less material	incomplete fill
10-11	Liquid resin	incomplete fill/resin bleed-out
12	Pre-mold	N/A Control

Table 3: Wafer processing skews and wafer mold coverage.

The target products were 12-inch silicon wafers (~775µm) + Cu Pillar + SnAg µBump (~45µm). Shallow edge trim was used on these wafers to clean the wafer edge and allow for better clamping of the wafers during the mold process and prevent any leakage of resin material. Consequently, the thin resin layer of 30µm is molded onto the wafers, while leaving the top of the solder ball exposed over the entire wafer (Figure 1b).

Types of materials. We wanted to study the effect of the resin type on both the warpage and mold thickness uniformity. Therefore, both granular and liquid compounds are used for this evaluation (Table 1). Liquid resin has a number of advantages including a lower melt viscosity that allows better flow properties and easily fills tighter pitches. Granular compounds, on the other hand, have a longer shelf life, lower material cost, and lower material shrinkage [8]. To see the effect of resin cut size on the flow properties and consequently on the final mold characteristics, different granular resin cut sizes were used.

Types of process skews. Based on previous experiments by TOWA and reported in earlier studies [6], the processing temperature, press pressure and the clamp press speed were seen to be the main parameters to control the final molded wafer properties. Different processing skews were selected as shown in Table 2. Each of the parameters was tweaked to test their effect on the post-mold wafer warpage and mold uniformity. Because the liquid resin mold showed incomplete coverage (discussed further in the section entitled, "Results and discussion"), these skews were all carried out on the granular mold compound.

Material characterization

The following sections discuss wafer mold coverage, warpage measurements, mold height measurements, and various scanning electron microscope (SEM) measurements.

Wafer mold coverage. Optical microscopy was used to verify full wafer coverage by mold material using a Keyence VK-3000 microscope. Images captured at the center and edge, post mold, were used to confirm proper encapsulation of the solder balls within

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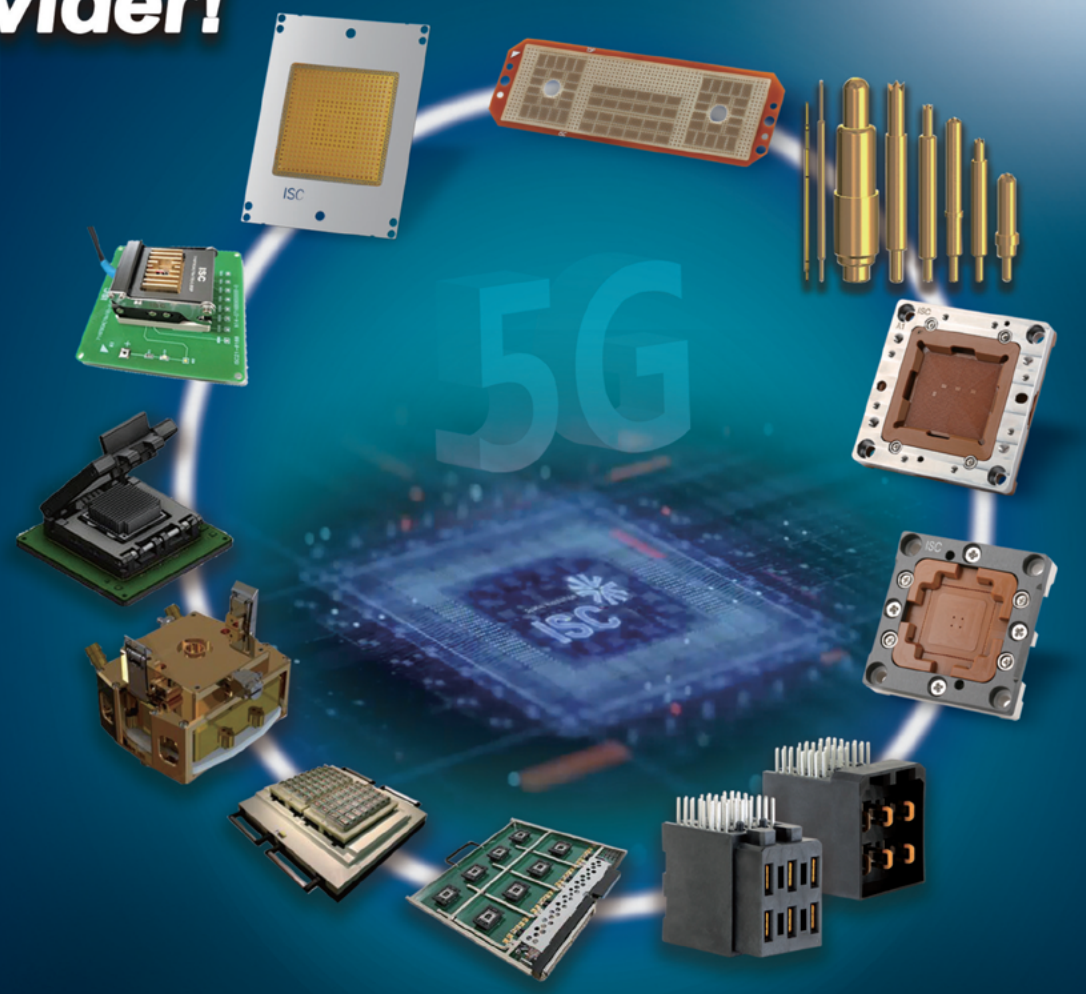

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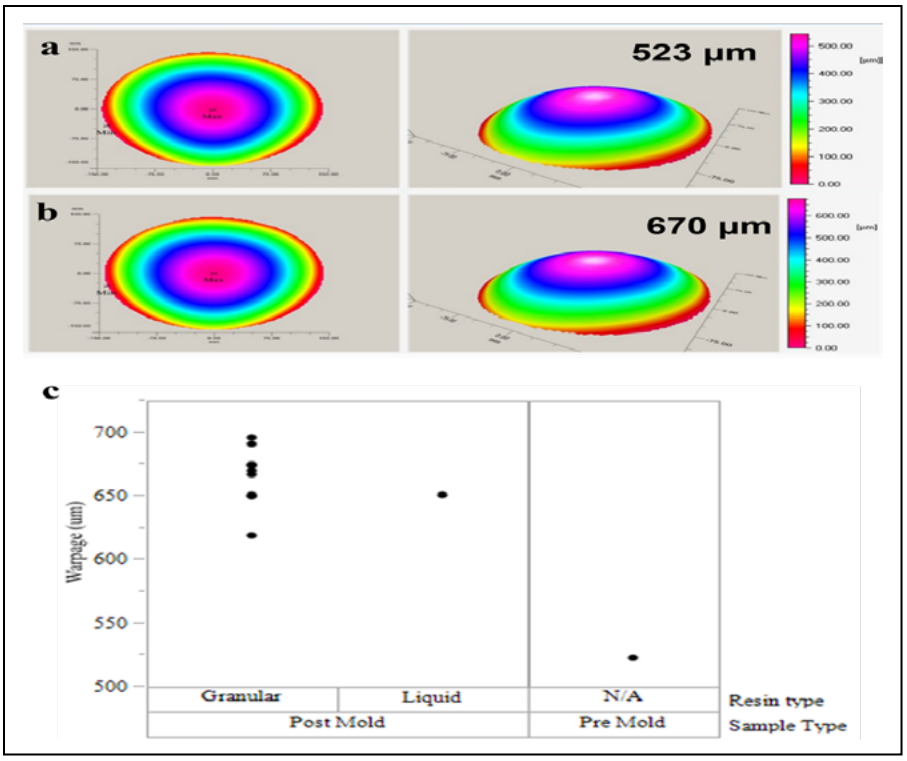

Figure 2: Representative 3-D warpage image for: a) pre- and b) post-mold wafers; and c) warpage value for pre- and post-mold wafers

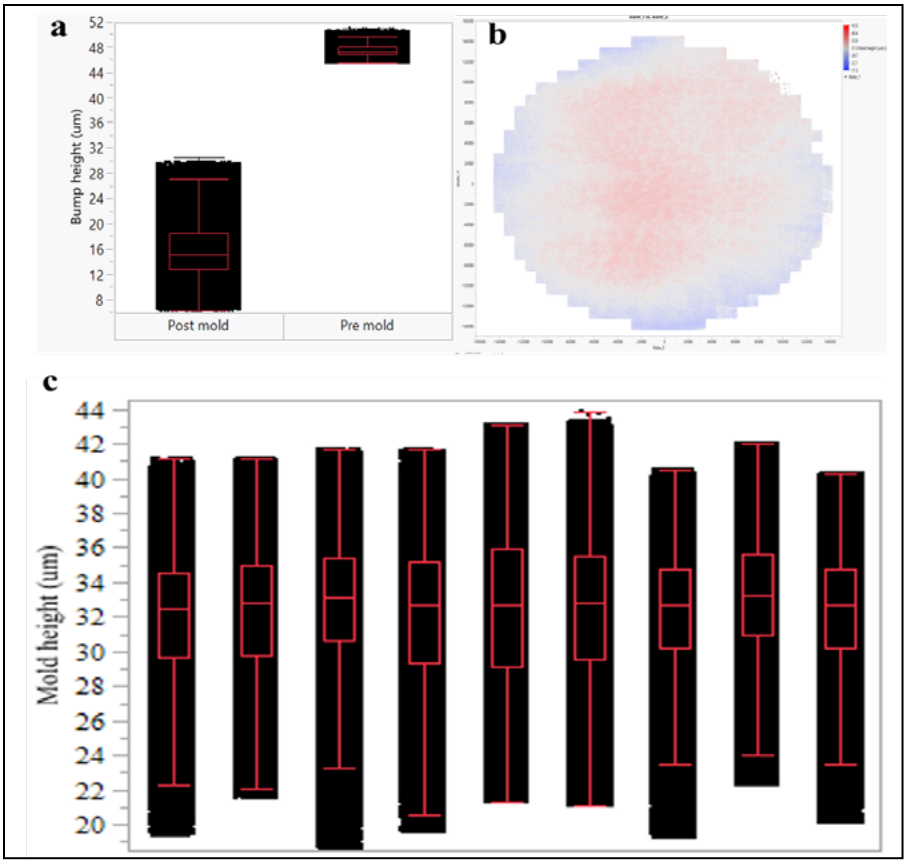

Figure 3: a) Bump height measurements pre- and post-mold; b) Mold height wafer map calculated from bump height measurements; c) Mold thickness distribution and range (TTV) for the different skews.

the mold material and therefore, the full coverage of the wafer. All the different process skews and their mold coverage were tabulated (Table 3). Results were further discussed in the section entitled, "Results and discussion."

Warpage measurements. Representative 3-D warpage images are shown in Figure 2. As can be seen in the figure, the warpage values are similar for both the pre- and post-mold wafers, with a difference on the order of ~100µm. Despite the CTE mismatch between the mold and the silicon substrate, the low thickness of the mold (on the order of ~30µm) relative to the substrate thickness leads to better control of the entire package temperature during the processing and therefore, lower warpage. In addition, both granular and liquid resin mold wafers show similar warpage values, which suggests that there isn't any specific benefit of one over the other in terms of warpage. The combination of the two allow better temperature control and lower wafer warpage than seen in other compression molding studies. None of the processing skews showed any warpage value different from each other, suggesting that the reasons listed previously play a greater part in warpage control than modification of the material or processing conditions.

Mold height measurements. Bump height measurements were carried out on a TAKAOKA multi-substrate bump inspection system. Figure 3a shows the pre- and post-mold bump height distribution of every bump on a wafer. The difference of the pre- and post-mold bump height was used to calculate the mold thickness distribution. Using the wafer coordinates of the bumps, Figure 3b shows the wafer map of the mold thickness distribution over an entire post-mold wafer. Wafers with incomplete fill at the edges had a mold height that was significantly different from the rest of the wafer—and that was clearly visible in the wafer map. Interestingly, the wafer map of the mold height suggested regions of higher mold height near the center of the wafer and slightly lower height as we moved towards the edge.

Given the above considerations, the mold thickness range could be calculated from the distribution (Figure 3c). Because of the significant

Sample count	Mean (µm)	Std Dev (µm)	TTV (µm)
9	32.5	3.7	21.3

Table 4: Mold thickness mean, standard deviation, and TTV average for different wafer processing skews.

incomplete fill at the edges with liquid mold material, their mold thickness range wasn't calculated here. The mold thickness range over the entire wafer gives us the mold total thickness variation (TTV) for the various processing conditions. The average of the data collected over 9 samples at different processing conditions is shown in Table 4. For incomplete molded samples, out of distribution measurements were excluded from the calculations. Based on the remaining sampling, for the best-case samples with granular resin mold, we see a TTV of around 19µm (+/-9.5µm). In addition, while in terms of coverage, some of the skews show incomplete fill, the TTV for the rest of the area is controlled rather tightly (~21µm or +/-10.5µm), on average, for all the different processing condition skews.

Wafer X-ray scanning electron microscopy (X-SEM) and SEM energy-dispersive X-ray (EDX). Wafer cross-sectioning was carried out at the center and edge of a wafer to confirm the adherence of the mold and provide an estimate of the mold thickness. Figures 4a and b show us cross sections of a bump + mold at the center and edge of a wafer (sample 1). The bump was a bit off-center for both cross sections, hence, the difference in width dimensions between the two bump cross sections. However, the mold area clearly showed that for a wafer with complete coverage, we can obtain a higher mold thickness at the wafer center compared to the edge—this is consistent with our estimates from bump height measurements.

SEM measurements were carried out using a Hitachi SU3900 SEM microscope. Image and EDX data were collected at the center and the edge of the wafer for the samples. Wafers with full coverage of the mold clearly showed solder balls completely encapsulated by the mold material. The solder ball itself shows a lack of mold signal, which suggests minimal contamination onto the solder ball during the process (Figure 4c) owing to the use of the optimized release film described previously (in the section entitled, "Materials and experimental setup").

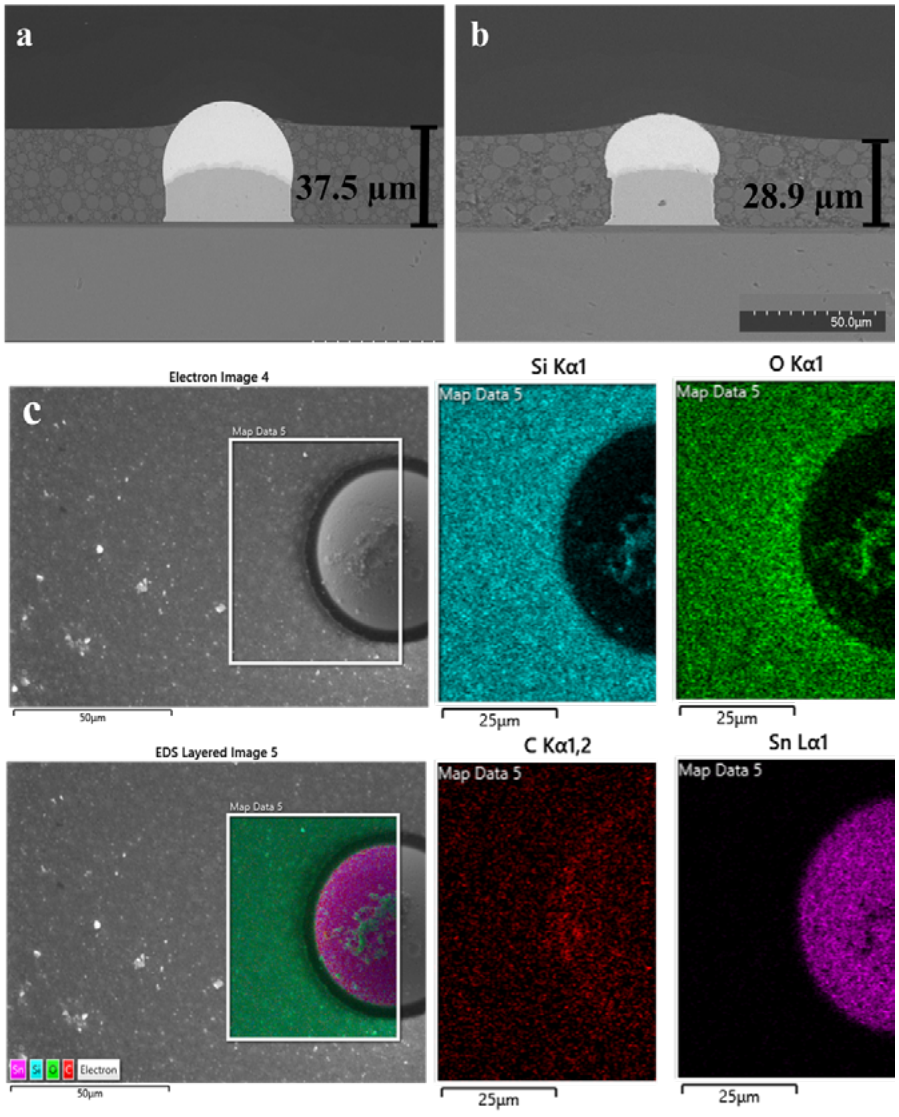

Figure 4: Mold height at the a) center and b) edge of the wafer; c) SEM microscopy and EDX profile showing solder ball encapsulated by mold material all around. The center and edge both showed comparable encapsulation and minimal contamination.

Results and discussion

The sections below address the effects of the liquid vs. the granular mold, the liquid mold itself, the effects of different mold cut sizes and temperature, as well as the effect of process skews.

Effect of liquid vs. granular mold. Under standard processing conditions, most of the granular resin mold samples managed to show complete and uniform fill of the mold compound from center to edge. The reason for this is possibly because granular compound can be dispensed evenly over the whole mold area (wafer area) during the pre-compression molding step as seen in Figure 5d. This, in turn, reduces the compound flow distance during the molding process and allows the compound to fill up to the edge of the wafer. In cases where filler size is smaller (e.g., liquid resin), we see incomplete fill or resin bleed out (Figure 5b, 5c)

In comparison to the granular mold, when using a liquid mold the liquid resin needs to be dispensed in a specific pattern pre-mold. In the final dispense pattern chosen, liquid

resin needs to be dispensed as one point at the center. Numerous other dispensing patterns like the spiral one were evaluated (Figure 6a). However, because the resin compound volume is too small, it starts to harden before reaching to the end of the wafer while creating an uneven mold thickness and an incomplete fill (Figure 6b) shows an example of a spiral pattern with incomplete fill). In contrast, we observed that a center point dispensing creates an even thickness of the resin as it travels from the center to the edge of the wafer. However, this pattern gives us the largest distance between the compound dispense and the wafer edge. The flow of the compound isn't fast enough to help ensure a complete fill till the wafer edges. Figure 6c shows a wafer with a center dispensing pattern with incomplete coverage at the edges. Adding additional liquid resin material was one option, but that, in turn, led to lower control of the mold thickness and resulted in similar edge coverage issues.

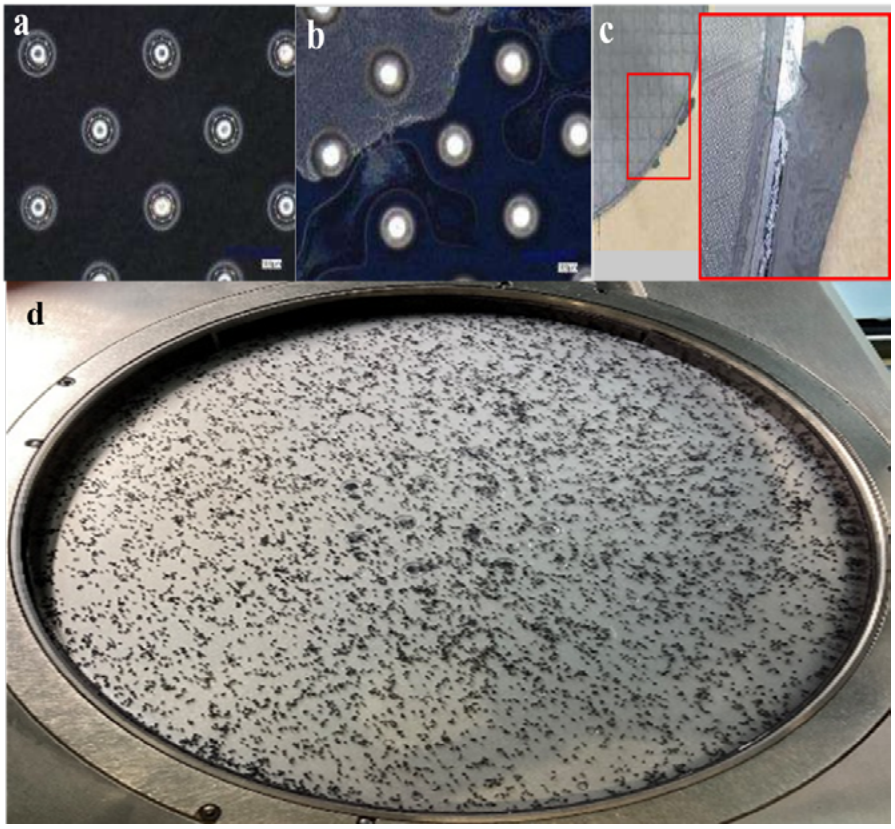

Figure 5: a) Bump mold encapsulation at center; b) the edge of an incomplete filled wafer; c) resin bleed-out at the edge of the wafer; and d) granular resin distribution on the bottom chase pre-compression molding.

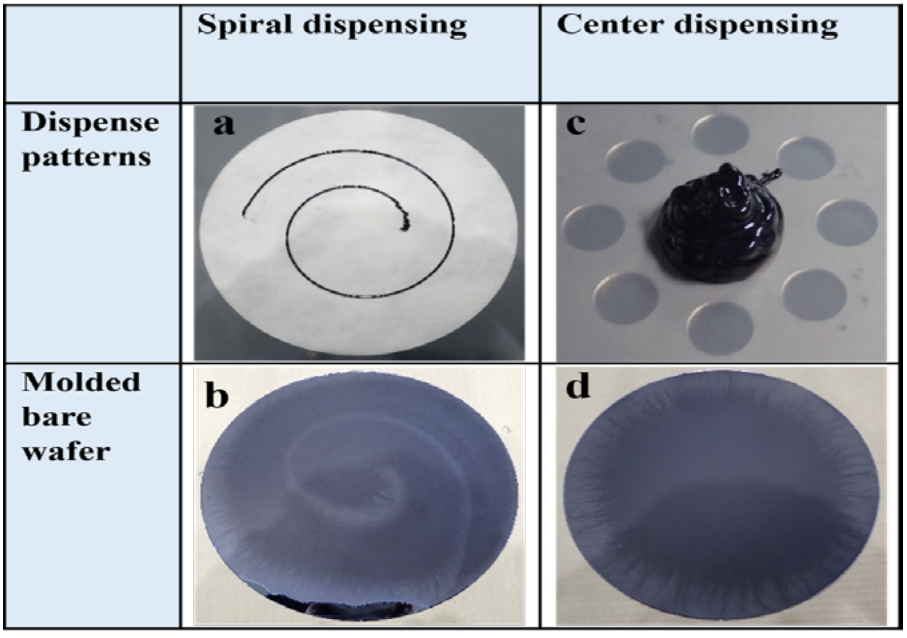

Figure 6: a-b) Spiral dispense pattern pre-mold and final post-mold coverage; and c-d) center dispense pattern pre-mold and final post-mold coverage.

Effects of different mold cut sizes and temperature. Three types of different mold cut sizes of a granular compound were evaluated and all showed a fully-molded wafer appearance (Figure 7a.). The granular cut size of 0.7-1.0mm was the easiest to dispense most evenly over the entire molding area. By using this cut size, the margin of compound filling can be expected to be wider. A granular cut size <2mm contains a wide range of particle sizes and much more size variability, ranging from smallest (~0.7mm) to the largest (~2mm). So even though it is possible to be dispensed evenly and provide full coverage, the performance stability becomes a potential concern.

Because temperature will influence compound melt and cure speed, we tried two different temperatures to confirm the influence on compound filling. However, not a lot of differences were observed in the compound filling or warpage with different molding temperatures for various resin cut sizes. We were able to lower the temperature to 130°C and still successfully achieve molded wafers with full coverage.

Effect of process skews. One of the parameters that should be considered is the impact of press speed. Different press speeds will lead to different compound flow speeds. Consequently, this can result in the lack of control of compound filling. When the press speed was set to a lower speed (Figure 7b), incomplete fill was observed. The reason can be attributed to the longer filling time, which caused the melt

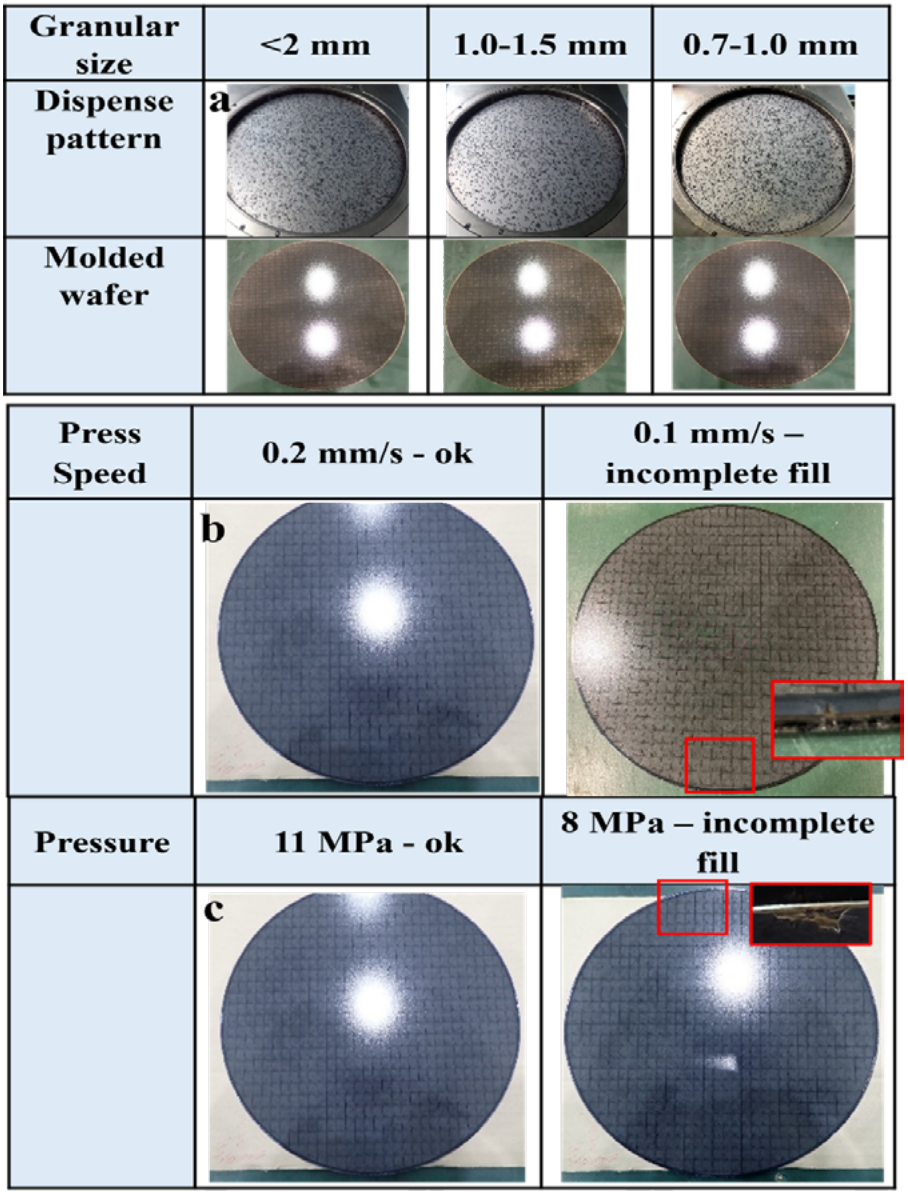

Figure 7: a) Granular mold dispense (for different resin sizes) for the pre-mold and the final molded wafer, which shows full coverage. Post-mold wafers showing incomplete coverage b) at the slower press speed (0.1mm/s) and c) at the lower process pressure of 8MPa.

compound to begin the cure, that, in turn, led to a higher viscosity while the resin was still flowing. This process margin can be improved by extending compound gel time (i.e., change the compound gel time, or use a lower temperature).

Another significant process parameter is pressure. Different pressures were also evaluated because it will influence the compound filling speed. Higher pressure at 11MPa shows a better result in filling. On the other hand, when using a lower pressure at 8MPa was tested, it was not able to fill completely at one of the edges (Figure 7c.). The compression molding setup with the temperature-controlled lower clamp that is pressed to the wafer on the upper clamp is ideal for low-pressure molding. However, in this case, we are possibly limited by the flowability of the granular resin material (e.g., incomplete fill was seen for both the smallest and largest granular cut size). It is worth noting that other granular resin materials with lower melt viscosity could possibly allow us to drive to a lower press pressure as well.

Summary

To help develop a WLP having robust, uniform and thin mold caps with lower warpage, we used a compression molding system with good temperature control and optimized release film. We successfully achieved a 30µm-thin mold cap that encapsulated the solder balls uniformly across the wafer with low warpage and mold TTV. Warpage was seen to be well controlled by virtue of the compression molding process as well as the low thickness of mold with respect to the die thickness. Processing conditions and the type of resin material did not seem to have as much of an impact on warpage. The mold encapsulation and wafer coverage were seen to be much better for granular mold materials compared to liquid resin mold because the initial distribution of the granular material uniformly over the wafer surface allows easy and minimal flow across the entire wafer. In terms of the granular cut size, smaller cut sizes show better flow properties and also a tighter size control of the resin. The ideal filler size, however, needs to be optimized to ensure a balance between good flow properties while avoiding a risk of bleed out at the wafer edge. The optimization of the release film used as a liner helped the control of resin flow while protecting the solder bumps from contamination. In terms of mold thickness TTV, most processing condition skews showed thickness variation on the order of +/- 10µm for granular resin material (of all cut sizes).

Acknowledgments

Additional co-authors on this article are: Naoki Hamada, Koichiro Wada, Lingling Zhou, and Tingyu Lyu—all from TOWA Corporation. Portions of this article were presented at ECTC 2022.

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Biographies

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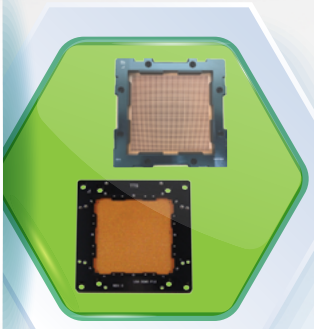

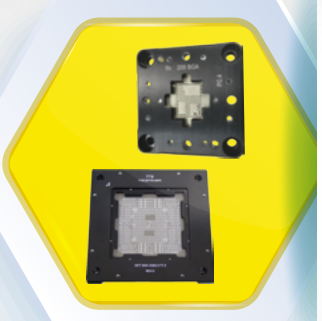

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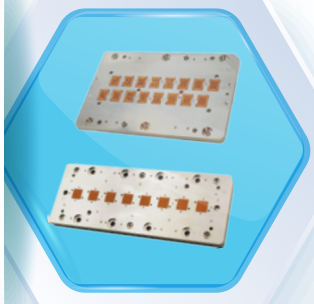

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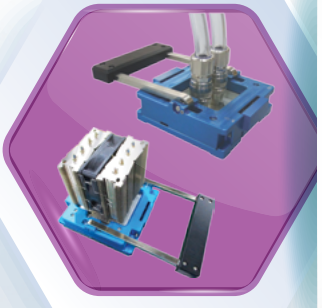
RF & mmWAVE SOLUTION

Min. Pitch
≥0.40mm

Insertion Loss
>60GHz@-1dB

Return Loss
>30GHz@-20dB



HAND SOCKET LID

Heatsink
<100W

Heatpipe
100W - 1000W

Liquid Cooling
300W - 1500W

BROCHURE

Oxide crack risk assessment during probing over active area

By Oliver Nagler, Marianne Unterreitmeier [Infineon Technologies AG]

Continuously smaller structural sizes of integrated circuits (ICs) of advanced semiconductors, higher signal integrity, faster switching speed, new materials, and design optimizations, bring essential performance benefits and yield improvements to electronic devices. On the other hand, during wafer test, it is getting more and more important to use the complete surface of the wafer for probing and bonding instead of placing contact pads outside the active circuit area on top of pure silicon (Si). The latter methodology was usually done in the past to avoid any damage to the IC during assembly, packaging, and test. This also means that the area below the bonding and probing pads is used, which is called pad-over-active-area (POAA). This IC design concept can reduce the chip size up to 20% (see Figure 1a). For a typical complementary metal-oxide semiconductor (CMOS) POAA layer stack, the contact pad is placed directly beneath the dielectric oxide layer (see Figure 1b). As a consequence of POAA, there is a great need for a fundamental understanding of the correlation between the electrical contact and the applied mechanical forces during wafer probing. Typical problems are the appearance of deep probe marks and oxide layer damages underneath the pad that are mechanically stressed during probing—these are a severe risk to reliability [1,2].

During wafer probing, elastic contactor springs – called probes – are used to mechanically and electrically connect the pads of the chip with external programmable electronic instruments called testers. The input/output (I/O) pads placed on the top side of the chip are electrically conductive without passivation on top and are therefore capable of being contacted by needles or wires. The number of pads per chip, which are typically made of aluminum (Al), copper (Cu), or other conductive metal alloys, can vary from less than ten, to up to hundreds, depending on the application. These pads are also different in size and thickness.

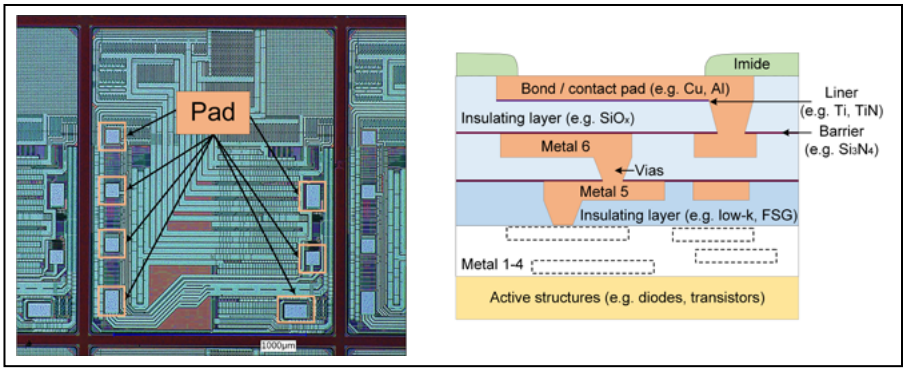


Figure 1: POAA layout for a) (left) CMOS chip design, and b) (right) a schematic cross-section view [2].

There are various categories of probe card technologies that enable the electrical connection between the tester channels and the pads of the chip. The most-relevant types of probe technologies are cantilever, vertical, and microelectromechanical system (MEMS) probes. With decreasing pad pitches (i.e., the minimum distance between two pads) and the goal to increase test parallelism to decrease testing time, vertical needles offer a good solution. A low and stable contact resistance is required to avoid a contact-related yield loss during wafer test. Therefore, a sufficient contact force is needed to penetrate the top pad layer (e.g., oxide layer of an Al-Cu pad) and establish a stable contact. However, due to the placement of the pads, the contact force cannot be too high—if it is, it can induce cracks in intermediate oxide layers of chips that are critical with regard to the reliability of ICs [3].

Figure 2 explains the challenge of POAA schematically for a single vertical probe. The elastic probe is contacting the pad, which is placed on top of the backend-of-line (BEOL) stack, which is based on CMOS technology. The

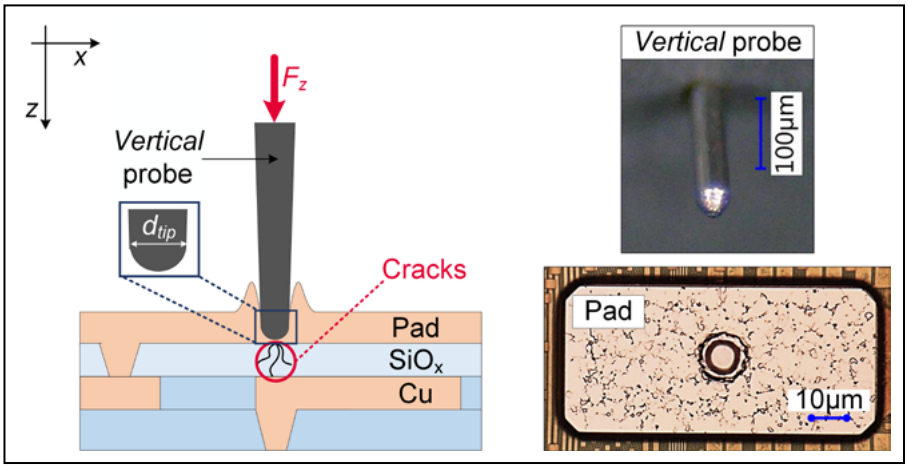


Figure 2: Vertical probe contacting a POAA, thereby inducing oxide cracks [2].

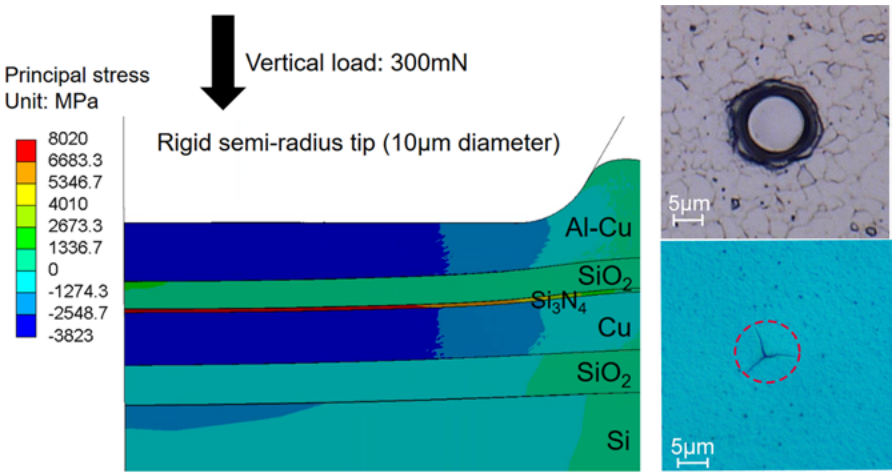


Figure 3: Stress in a layer stack during contacting causing oxide cracks.

probe tip is causing a high mechanical stress that can generate an oxide crack if the material-dependent fractural stress is reached. In the case of a pure vertical force vector of the probe, the contact-related mechanical stress in the thin layers during probing is mostly compressive within the contact area.

Figure 3a shows a half-symmetrical finite-element model (FEM) with a simulated contour plot of the first principle stress for a flat cylindrical tip contacting a multi-layer stack with an Al-Cu pad on top of a silicon oxide layer (SiO_2) and additional thin layers below. For a flat tip of 10µm diameter and at a maximum contact force of 300mN, the highest stress values are approximately ±8.02N/m² (=8.02GPa) and are located below the center of the indenter tip in the region of the Si_3N_4 layer below the upper SiO_2 layer.

With increasing contact force, the SiO_2 layer is elastically deflected downwards at the same time the Al-Cu pad metal and the Cu layer below are plastically deformed under vertical load. This creates a U-shaped deformation of the uppermost layers in the region of the tip contact area. The upper SiO_2 layer and the Si_3N_4 layer of the structure are subjected to alternating tension and compression during the indentation. The Cu layer and the area below the indenter tip are predominantly under compressive stress in the vertical direction. Immediately beneath the center of the tip is a region of high stress concentration. The optical inspections (see Figure 3b) of the probe mark and oxide cracks are highly correlated with the simulation results [4].

Pad stack crack assessment

The acoustic emission (AE) test method is one of the most efficient techniques used for the non-destructive testing (NDT) of material characterization. It can detect, localize, and monitor material defects without any destruction of the sample. For this purpose, AE sensors are glued or pressed to the surface of the body of the sample to detect elastic acoustic shock waves that are expanding spherically from the location of an acoustic event like a crack or plastic deformation. This advanced method of AE crack detection during probing has been developed by Dr.-Ing. Marianne Unterreitmeier during her PhD work [2] at Infineon Technologies, and is based on state-of-the-art AE testing. The methodology has been modified in a way to apply it for the qualification of the wafer probing process, in order to detect low-energetic acoustic signals of brittle layer cracks in nanometer dimensions.

Figure 4 shows a schematic view of the AE measurement chain. An AE event releases an elastic wave propagating within the solid body. After the induced AE wave has reached the location of the AE sensor, it penetrates the couplant and then reaches the sensor. The AE sensor converts the dynamic surface-motion, which is caused by the elastic wave, into an electrical (AC) voltage signal. The AE signal is subsequently amplified and commonly filtered by the preamplifier and transmitted to the AE system where the signal processing takes place. Finally, the generated data set is transmitted to a computer where it is stored, evaluated, and displayed [2; p. 81].

A specially developed and patented sensor-indenter system (see Figure 5a) [4] is able to precisely generate cracks in brittle isolation layers of thin-layer pad stacks of all kinds of chip designs (see Figure 5b) and measure the released acoustic waves by using a diamond tip indenter similar to the probes of a probe card in production. Over a certain period of time, the contact force is increased, held, and then unloaded (see Figure 5d). During this process, AE burst signals, so-called hits, can be visualized in the time- and/or frequency-domains (see Figure 5c).

The hits are triggered above the noise threshold voltage, recorded, and plotted synchronized with the contact force as a function of the time in order to identify signals that are classified as cracks or other acoustic events like plastic deformation or friction. For a better statistically-proven data analysis, the contact cycle is repeated from 100 up to 1,000 times and the recorded AE data are cumulated and saved chronologically in an ASCII file.

CMOS BEOL design options A and B

To demonstrate the advantage of the new method for determining the crack probability during probing, we present an application example using a CMOS chip with an evaluation of different pad stack design variants. The objective of this study, which was presented at SWTest conference 2022 by Dr.-Ing. Oliver Nagler [5], was to

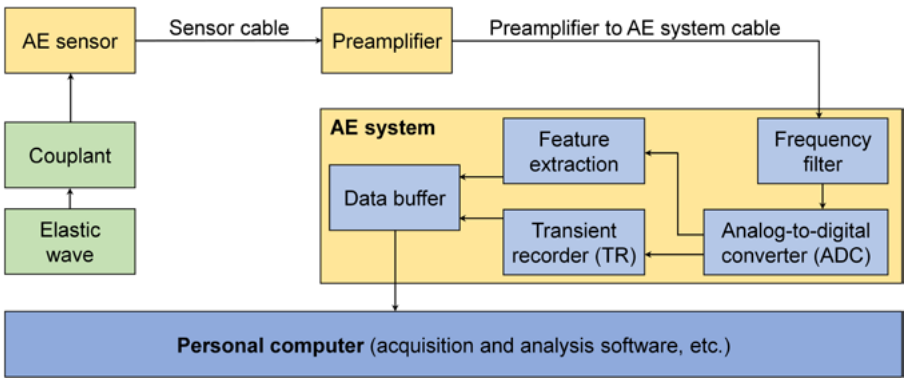


Figure 4: Schematic view of AE measurement chain [2].

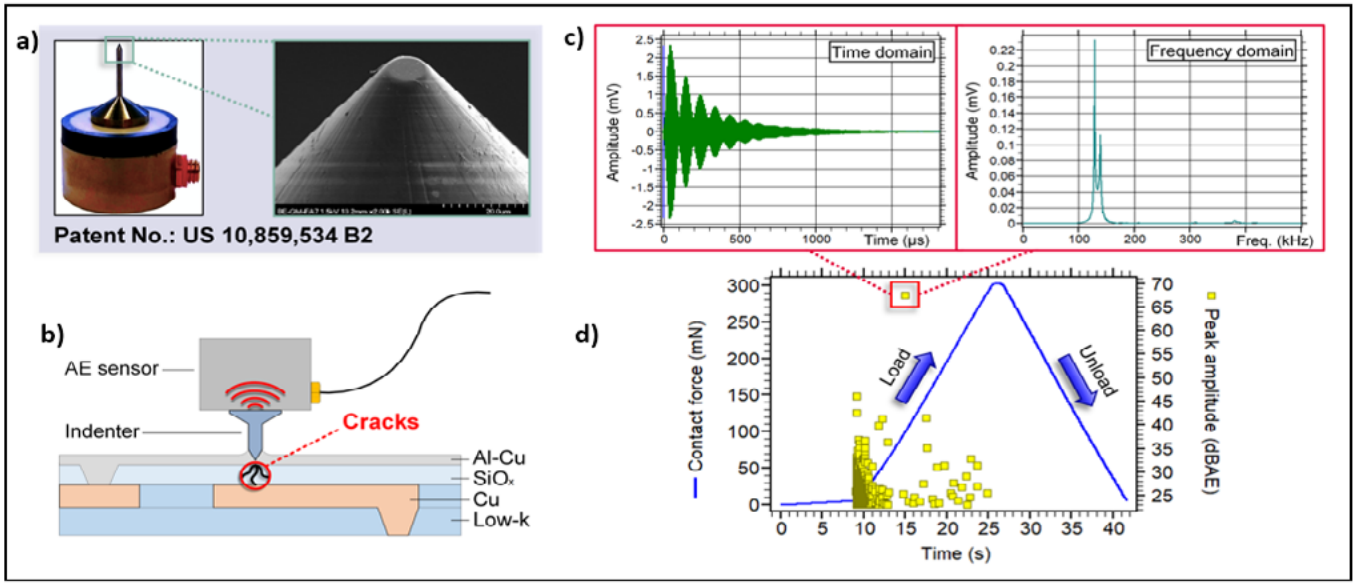


Figure 5: a) Patented sensor-indenter system; b) Crack detection by AE test method; c) Acoustic signal in time and frequency domains; and d) Typical contact cycle.

determine the crack probability during wafer probing under conditions that occur during manufacturing, and to identify the most robust pad stack design in order to avoid oxide cracks. The first chip variant (option A) has a Cu-pad on top with a "checkerboard" routing pattern in the upper oxide layer and another metal fill in the oxide layer below. In contrast, the second variant (option B) has the same pad metal design, but a double oxide layer without metal routing in the upper-most isolation layers (Figure 6).

In order to assess the risk of generating probing-related cracks, the tolerances of the probe geometries are considered during the study. Two different tip diameters, 5µm and 10µm, were used for the contact cycles. The tips are flat with a small edge radius representing the typical dimensions and geometry of a manufacturing probe card for a similar range of contact force.

In total, 150 contact cycles with a maximum contact force of 250mN for each pad stack/tip combination were performed to achieve nearly 100% crack probability. During contacting, the AE signals were cumulatively recorded and later graphically visualized in a scatter plot (Figure 7). The burst signal energy in units of eu ($1eu=10^{14}V^2s$) is used here as a characteristic feature of an AE event.

Figure 7 shows the burst signal energy in logarithmic scale as a function of contact force for all hits derived during 150 contact cycles for pad option A and a tip diameter of 5µm. Here, one can see that the burst signal energies are high at the beginning and

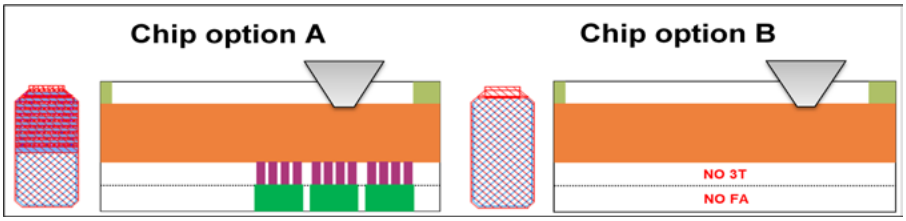


Figure 6: Pad stack options A and B.

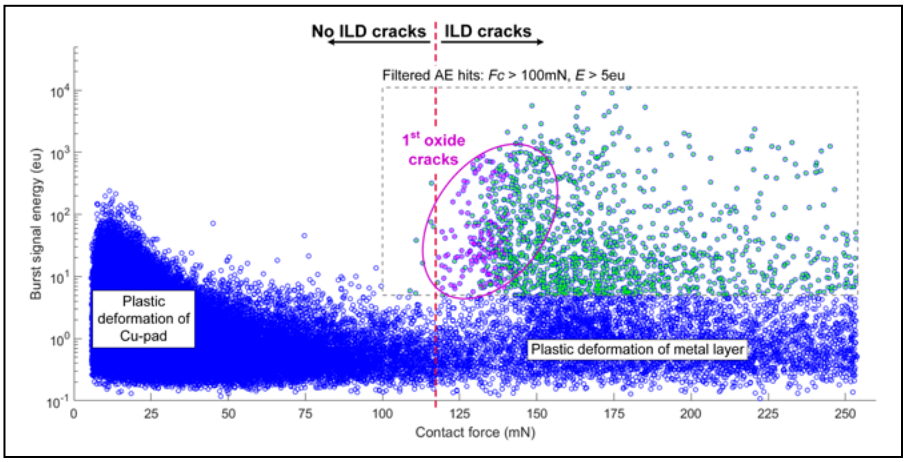


Figure 7: Scatter plot of clustered AE signals.

decreasing during penetration of the pad metal up to a critical contact force of around 100mN—meaning no AE crack events were observed. For a contact force higher than 100mN, the burst signal energy of the hits is increasing again.

In the case of a crack, the burst signal energy is assumed to be higher than 5eu, which was correlated by optical inspections. For a meaningful data clustering of those hits, when "first oxide cracks" appear, it is important to correctly set the filter limits of contact force and burst energy. Therefore, only hits with energy higher than 5eu of each contact cycle, occurring at a certain contact force, are included and utilized for further data clustering. Hits with a

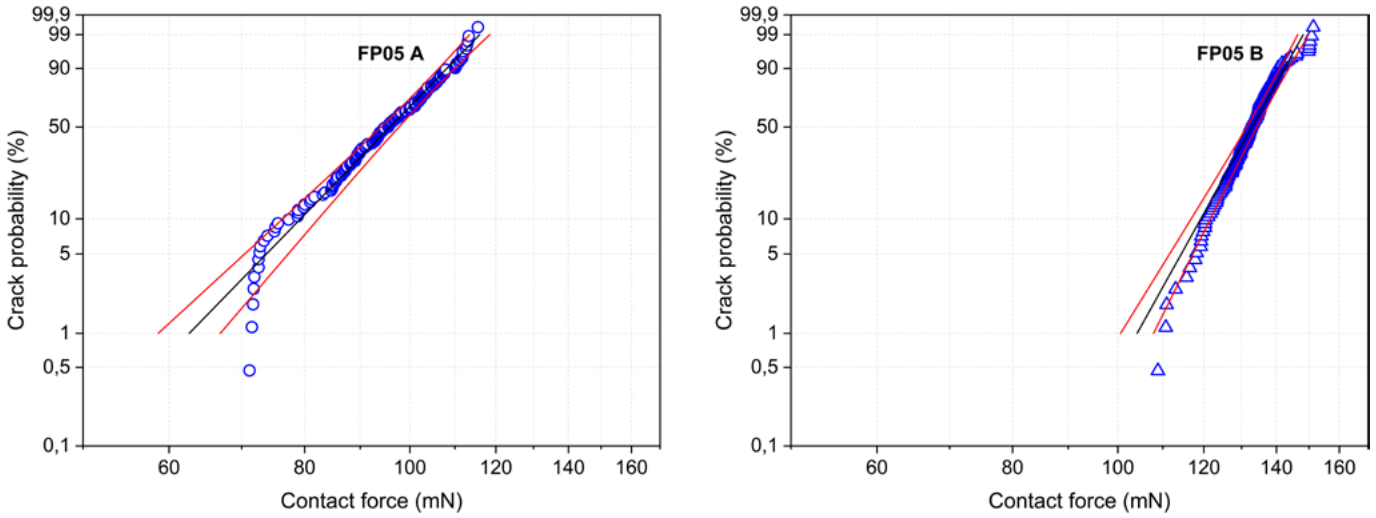


Figure 8: Crack probability plot for: a) (left) pad stack option A vs. b) (right) B and tip diameter 5µm on the Weibull scale.

burst signal energy lower than 5eu are considered as noise, friction, or plastic deformation of metal layers below the oxide layer, which are noncritical and not relevant for the crack assessment.

The critical contact forces can be statistically derived by filtering the data from the scatter plots above a certain burst signal energy and selecting only those hits that have occurred for the first time per indent ("first oxide crack"). The cumulative crack probability P_f, which follows a Weibull distribution with the Weibull modulus m and the characteristic contact force $F_{0,}$, can be graphically linearized by scaling the x-axis to ln(F) and the y-axis to ln [ln[1/(1-P_f)]. The Weibull parameters m and F_0 are extracted from a linear regression line that is fitted through the data points [2].

Figure 8 shows the graphical result for a sample size of 150 indents using a 5µm flat punch tip (FP05) each for pad option A (left graph) and B (right graph) in Weibull scale format. Both graphs show a black fitting line that has been adapted to the data points. By definition, the data analysis corresponds to the characteristic contact force F_0 with a 63% crack probability and confirms the theory that the critical forces causing cracks in brittle materials follow a Weibull distribution. Through extrapolating the regression line of the crack probability model, the crack risk at low ppm-rates can be determined, which is later important for complying with the POAA quality requirements.

Table 1 shows the results of the crack probability assessment for all combinations of pad options A and B using two different tip diameters. All experiments were done for a sample size of 150 indents.

After completing all experiments and data analysis, an assessment to identify the best pad/tip diameter combination can be visualized (see Figure 9). Comparing the four graphs, it can be seen that a two-times larger tip diameter (10µm vs. 5µm) increases the critical force up to a factor of 2.5. It is important to note that the slope of the regression lines, which corresponds to the Weibull parameter m, is steeper for pad option B. This can be interpreted as a lower crack risk for low crack probability rates. In conclusion, pad option B is approximately 35% more robust compared to option A,

Pad option	Tip diameter (µm)	Weibull modul	Critical force (mN)
A	5 (FP05)	11.5	99
B	5 (FP05)	24.7	135
A	10 (FP10)	8.6	221
B	10 (FP10)	26.1	324

Table 1: Weibull parameters for all pad/tip diameter combinations.

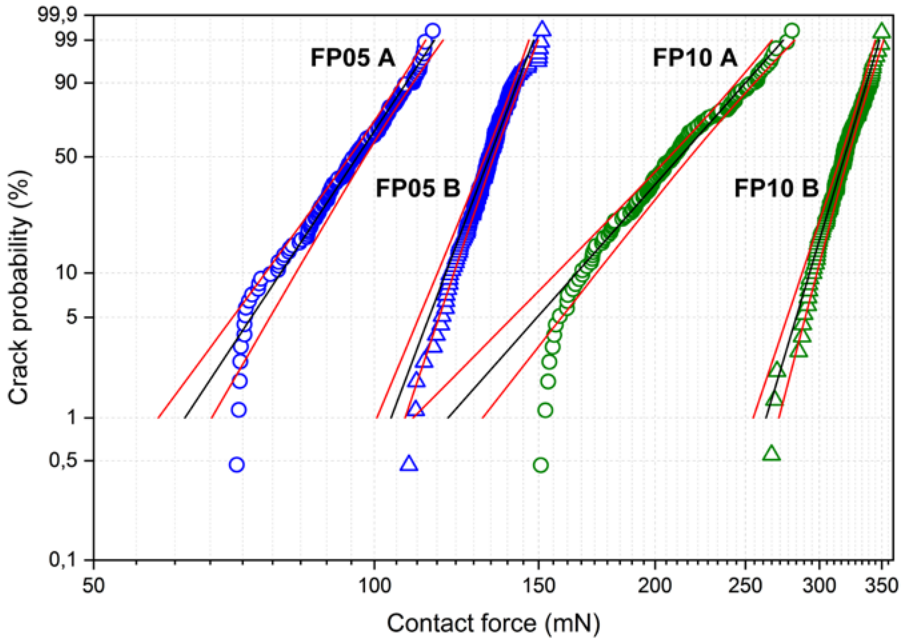


Figure 9: Crack probability plot for pad stack option A vs. B and tip diameter 5µm vs. 10µm on the Weibull scale.

which helps to define the pad stack design for a more reliable wafer test.

Summary

At Infineon Technologies, an advanced AE test method was developed and introduced that detects cracks in brittle semiconductor layers during contacting by pointed tip indenters. The process is similar to wafer probing and can be used to characterize the mechanical robustness of multi-layer stacks with a POAA design concept.

The accuracy of the AE test method was correlated by conventional failure analysis methods. We have proven that a highly accurate, reliable, and efficient detection of oxide cracks using the AE test method is possible even at the nanometer scale dimension. This POAA qualification method is used as a standardized qualification process at Infineon Technologies and is applied to characterize the robustness of semiconductor BEOL stacks for probing and other stress-related processes during the manufacturing flow.

Acknowledgment

Portions of this article were presented at SWTest 2022.

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Biographies

Dr.-Ing. Oliver Nagler is a Lead Principal for wafer test at Infineon Technologies in Munich, Germany with more than 20 years experience and is the team lead of the pre-development group. He is the Manager of the company's probing lab and supports Infineon's business units and wafer technology development regarding probing qualifications. He holds several patents and international publications in probing technology, including acoustic emission test method.

Dr.-Ing. Marianne Unterreitmeier is a technology expert for acoustic emission testing, holding several patents, in the Test Technology and Innovation department at Infineon Technology in Munich, Germany. She has a Master's degree in micro- and nanotechnology and completed her PhD with honors at the FAU Erlangen-Nuremberg in 2019. She achieved the Best Paper Award at the ESREF 2018 conference in Aalborg and the Regensburger Award for Women in Science and Art in 2021.

Optical fiber pigtails integration in co-package design

By Alexander Janta-Polczynski [IBM Canada]

The optical fibers that exit a silicon photonic device – also referred to as pigtails that are bundles or ribbons of optical fibers – need appropriate fastening within the package to protect the light-coupling interface. A strain relief element must be designed to protect the light-coupling interface from deformations that can occur from various stresses, such as from downstream assembly processes, from the thermal expansion cycles experienced during device lifetime, and from external forces applied to the pigtail. We will discuss here a parametric model developed to evaluate latching configurations that use fiber bending as a strategy to accommodate thermal and mechanical strain of the fiber ribbons. This model can help the design of optimal geometries to control within the limits the stress at both anchoring points: the photonics interconnect and the ribbon strain relief area.

The work from [1] is resumed here, where we demonstrated the benefits of using a free-fiber length of 8mm or more to incorporate the bends with low stress on our selected layouts. Also, we showed that an exit angle of a few degrees of the fiber ribbon provides advantages in controlling the fiber bending and buckling direction to reduce the fiber pistoning. (Pistoning refers to the fiber butting motion and forces on the photonic coupler.) Finally, the use of boots was also explored because they provide significant benefits with respect to controlling the radius of curvature and stress for the ribbon side pull stress tests; also, a novel boot morphology study showed up to a 33% stress reduction. These results provide guidance for optimizing the layout of optical fibers inside a package and how to manage the strain on the photonic interconnect by leveraging fiber bending designs.

High-bandwidth silicon photonic modules require a multi-fiber interface, and fiber optic ribbons that exit the co-packaged module need to be properly secured, especially to protect the photonic die's connection where light coupling occurs. Several techniques can be used to secure the optical fibers to the photonic chip with adhesive. One cost-effective solution for co-packaged components is to use automated self-alignment to assemble pigtails to V/U grooves and secure single-mode fibers to silicon photonic integrated circuits (PICs) [2]. The geometrical design and methods of how the fiber ribbon is fixed within the module must protect this photonic interconnection from the stresses that will occur during downstream assembly steps and during environmental stress conditions that optoelectronic modules must withstand. Furthermore, this solution must also provide a sufficient retention strength for the ribbon to allow the expected level of handling required by the pigtail. We resume here the model and results used to evaluate solutions that include optical fibers inside co-packaged optical modules for ribbons connecting photonics devices.

The fiber pigtail length exiting the module is usually set by the application requirement and how it will connect to the system, but in addition to such application requirements on the length, there can be benefits for high-volume manufacturing (HVM) to having certain lengths. The sets of parameters for the manufacturing approach includes how to grab and assemble the component into the package, with either short pigtails, or small fiber rolls for longer pigtails. In automated manufacturing as proposed by IBM, the ribbon array is grabbed by a robotic handling head of a high-throughput pick-and-place tool [3,4]. Two attachment points between the picking head and the fiber ribbon are desired: one close to the fiber array that will be attached to the photonic die, and the other to support the weight of the ribbons and connector termination [5]. This arrangement also enables the control of the shape of the fiber ribbon while it is being anchored inside the module. The fibers remaining inside the package need to be properly laid out to ease the manufacturability and increase the robustness of the integration. In particular, proper layout is needed to support the environmental and stress conditions that optoelectronics and photonics modules with fiber pigtails must withstand, such as: Telcordia, UPC, JEDEC, OIF, COBO, ITU, IEC, to name a few. Furthermore, this approach is suitable for use in HVM environments where automated high-throughput pick-and-place tools must handle the pigtails efficiently and allow for scalability of fiber count. Co-package modules that use multi-ribbon assemblies in close proximity maximize the optical bandwidth at the PIC interface, something that only direct-attach fiber pigtails provide [6].

When integrating optical pigtails within a package, the main challenge is to create a strain-relieving structure that protects the optical interface from the external loads applied on the ribbon while accommodating the strain from the high thermal expansion coefficient mismatch between the optical fiber anchoring points and the package structure—throughout the temperature range of the application. The intent is to use fiber bending to accommodate the deformation (thermal and mechanical) and control the stress at both anchoring points. The deformations are either thermally-induced through temperature excursions, or mechanical, such as pulling on the ribbon. Optical fiber reliability and optical performance is ensured with stringent control with respect to the radius of curvature, which is a significant challenge when the ribbons are exiting abruptly from a package edge.

Fiber force must be controlled at the V-groove interface to maintain the sub-micron alignment required by single-mode optics, and the fiber radius of curvature must be adequate for fiber reliability. Furthermore, the exiting ribbons must withstand various pull and retention tests, as well as provide proper strain relief for the protection of the photonic die interface. To overcome those challenges, we analyzed the design of the pigtail integration to reduce the impact of the stresses at the various interfaces. Ribbons pulls and twists are some of the most challenging tests to pass for optical modules.

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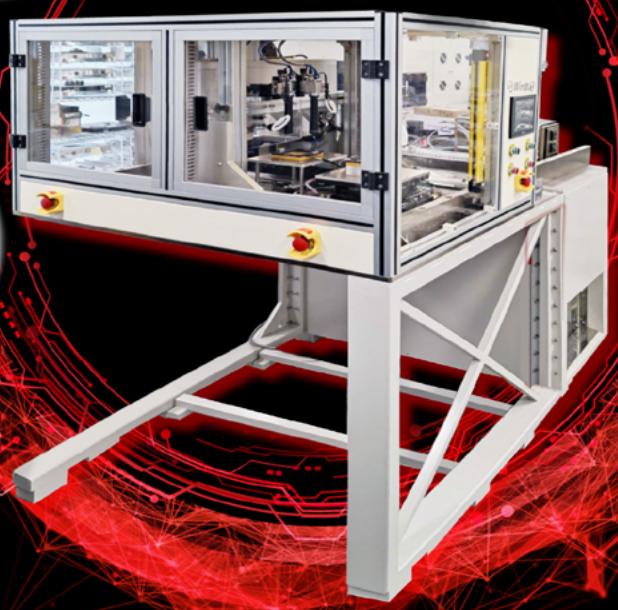

Probing System for Co-Packaged Optics

The strain relief allows some deformation to accommodate pulls and thermal loads, as well as to protect the tight sub-micron level alignment at the photonic die. In our case, the assembly can rely on the self-aligning V-grooves to provide strong anchoring points for the fibers and accommodate fiber bending caused by package deformations.

Methodology

A multi-fibers ribbon integration inside a photonic co-package is studied here in which the strain and stress distribution against various fiber layout geometries within the module are compared [1]. We will evaluate how the strain relieving structure affects the stress with different load cases (thermal and mechanical) and how the optical fiber can bend within the package to reduce stress. The resulting forces at the fiber connections to the PIC are compared to experimental fiber pull data. The module includes an array of optical communication fibers aligned with V-grooves and secured to the photonic die using an adhesive that inherently creates a fillet with the fibers at the die's edge. The fibers are then encased within a ribbon coating (either flat or bundled) that is itself anchored inside the photonic module at a specified location where bending can be induced by changing the height of the ribbon. A typical arrangement is shown in **Figure 1**.

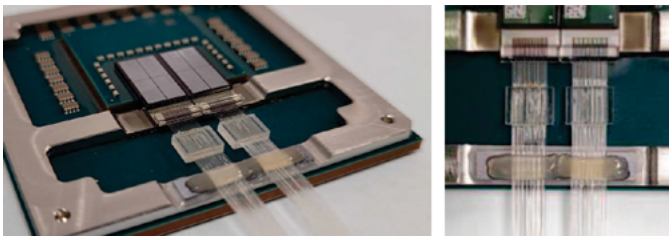

Figure 1: Photo of a co-package photonic module [6] with two pigtails, where the ribbon strain relief is created with adhesive on the package stiffener.

The advantages of using transition boots and ribbon sleeves surrounding the fibers in the pigtail retention solution will also be evaluated.

The stress at interfaces and bending radii control are some of the critical aspects of the optical fiber layout inside the package [8]. Two attachment approaches are compared and shown in **Figures 2** and **3**, where the ribbon can be secured to the top of the module lid cover plate or to the stiffener ring that surrounds the module. The ribbon attachment and latching within the module relies on the dispense of a hard ultraviolet (UV) adhesive that holds the ribbon jackets in place. As the attach solution needs to be compatible with microelectronic environmental stressing and solder reflow [9,10], we will use those load cases in the simulation. Furthermore, we use the ribbons' axial and lateral pulls to analyze how the package design around the fiber can help to relieve strain for the package integrity.

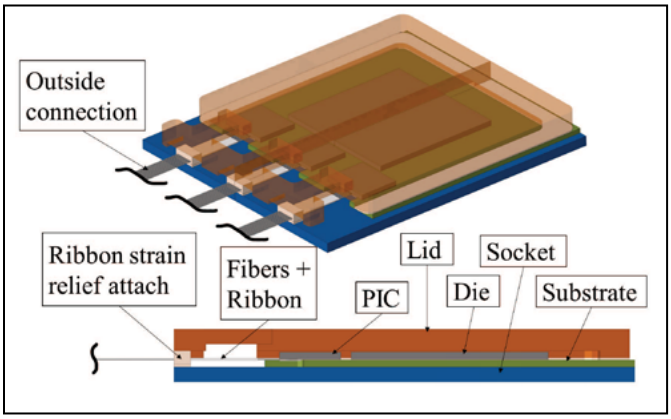

Figure 2: Photonic device with three pigtail ribbons exiting the module; also shown is the ribbon strain relief between the lid and substrate.

The pigtail strain relief on the lid configuration is shown in **Figure 2**. This architecture connects the fibers at the PIC and at a supplemental anchoring location for the fiber ribbon near the edge of the module. In the test module studied, the fibers are attached using an adhesive bridge that is in contact with both the substrate and the lid, while in a second configuration studied, the anchoring is done on a stiffener. Constraining the fibers in this configuration induces thermal stresses due to differences in thermal expansion coefficients of the materials as they are exposed to curing, solder reflow and environmental conditions. It is, therefore, necessary to evaluate how the fibers behave under these conditions, especially in terms of stress, curvature, and internal force as they are transferred to the PIC V-groove interface. With both architectures, it is possible to drastically affect the fiber ribbon exit angle by bending or machining an angle where the fibers are attached, as shown in **Figure 3**. The lid cover plate or stiffener helps to limit module warpage, and also provides flexibility to attach different parts using fastening methods, and can even be extended to accommodate further lengths.

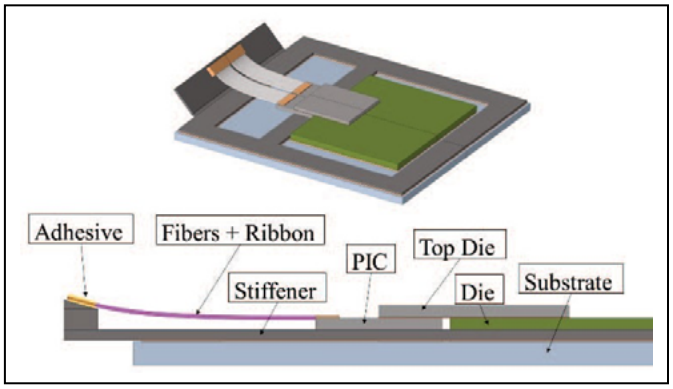

Figure 3: Photonic device with pigtail strain relief is the attachment on the module's stiffener.

We propose to track the fibers' bending and the forces applied at the photonic die coupler for various lengths and geometries. The initial bending will help transfer the thermal strain from axial strain in the fibers to a bending that accepts deformation and strains that occur with the ribbon. The bending also allows the accommodation of the strain relief deformation that occurs when pulling the ribbons. We did examine the effects of the following geometric parameters: the free fiber length, vertical offset of anchoring height, exiting angle, and boot shape and location. **Figure 4** shows how the variable geometric parameters are defined. We will compare the benefits of various cases and track radii of curvature of the ribbon and the stresses at the interface.

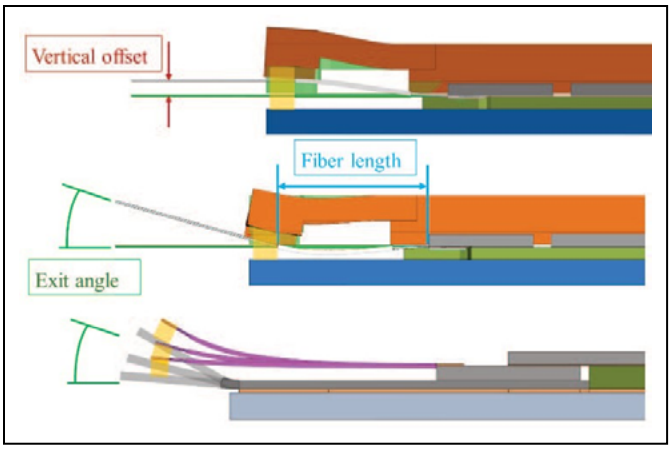

Figure 4: Illustration of the geometric parameters for lid and stiffener configurations; deformations were exaggerated for clarity. Anchoring outside of the package is also considered to evaluate extended fiber length.

A nonlinear finite element model is used to evaluate the above-mentioned strategies on a selected module geometry for various fiber layouts inside the package. The mechanical stresses and strains in the assembly are calculated with a nonlinear algorithm to take into account the complex phenomena that occur under the various loading conditions that were used. First, the contact element between different parts of the module is modeled and activated due to thermally-induced warpage. Second, the instability inherent because of the high slenderness ratio of the optical fibers is taken into account by using a large displacement methodology. Therefore, fiber buckling under compressive efforts is accurately represented in the finite element model.

The last significant nonlinear phenomenon captured by the model is the material properties' dependence on temperature. In the temperature range considered in the present study, some materials undergo glass transition, which induces a sudden variation in the thermal expansion coefficient and elastic modulus. A pseudo-rheological strategy specifically developed for modeling the glass transition, described in [8], is used. The analysis also includes the effect of the assembly process to correctly track the stresses in the module because the fiber ribbons are placed and positioned using interference-based fabrication. Once the adhesives are properly cured, the module is cooled down to room temperature. The interference fabrication, curing and subsequent cooling induce bending in the fibers, which influences stress and how the fibers will deform under thermal and mechanical loading. The model described above captures all these effects in the simulation, and a linear superposition of both the module assembly stress and the applied load cases stress conditions, such as ribbons pull/twist and thermal cycling, is performed. A uniform temperature is varied over time for the entire model from the assembly using a large-displacement condition, and a nonlinear approach is used to account for the contact between parts and the geometric instability effects such as buckling.

Figure 5 shows an example of a second-order finite element mesh used for the analysis of the module's stresses. The adhesives' behavior when undergoing the glass transition is considered in the model and the modulated stiffness with regards to the temperature excursion is described in [8].

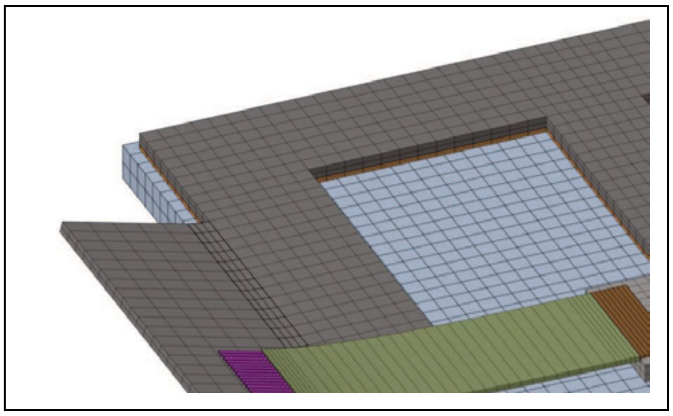

Figure 5: Illustration of a finite element mesh used for this study.

Our model adds the loads condition over the induced "as-assembled" fiber bends. From the assembled condition, the load cases start with one of the following: 1) thermo-mechanical loading over a wide range of temperatures, from deep cold environments (-40°C), to 250°C solder reflow for surface-mount technology (SMT) compatibility and ball grid array (BGA) attached co-package; or 2) the retention forces that ribbons must withstand when pulled. Our goal is to ensure that the fiber bending, and implied stresses are below the expected limits for these conditions. **Table 1** details the loading

Load case code	Name	Description
PS	Pre-stress	Initial Bending of the fiber with imposed anchoring
RT	Room Temperature	From Curing temperature to room temperature, amplification of the initial bending
SR	Solder Reflow	Profile temperature up to 250°C.
OT	Operational Temperature	95°C
ES	Environmental Stress	Low temperature of -40°C and short-term radii considered

Table 1: Simulation loading conditions.

conditions, which are also illustrated in **Figure 6**. The fiber stresses and curvature are extracted as performance criteria to understand key parameters influencing how the fibers are loaded within the module. Also, the fiber needs to conserve the radius of curvature above a certain threshold, and there are limits to the anchoring force of the fibers, as more specifically the pistoning forces along the fiber in the V-groove need to be limited below certain thresholds to guarantee robustness.

A first mathematical analysis was used to evaluate the optimal anchoring distance of the strain relief of the ribbon pigtails with regards to photonic die. The radii and force on the fibers were calculated for various lengths. The differential equations for the fiber in a simplified 2D case were solved, and **Figure 7** presents the variation of fiber forces and radii for a range of fiber lengths. The forces on the fiber at the PIC die are calculated and compared to our experimental limits. These forces come from the thermal strain induced by environmental

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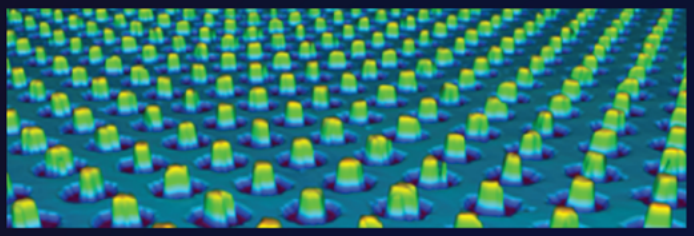

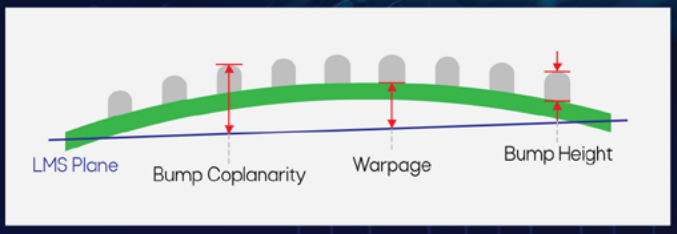

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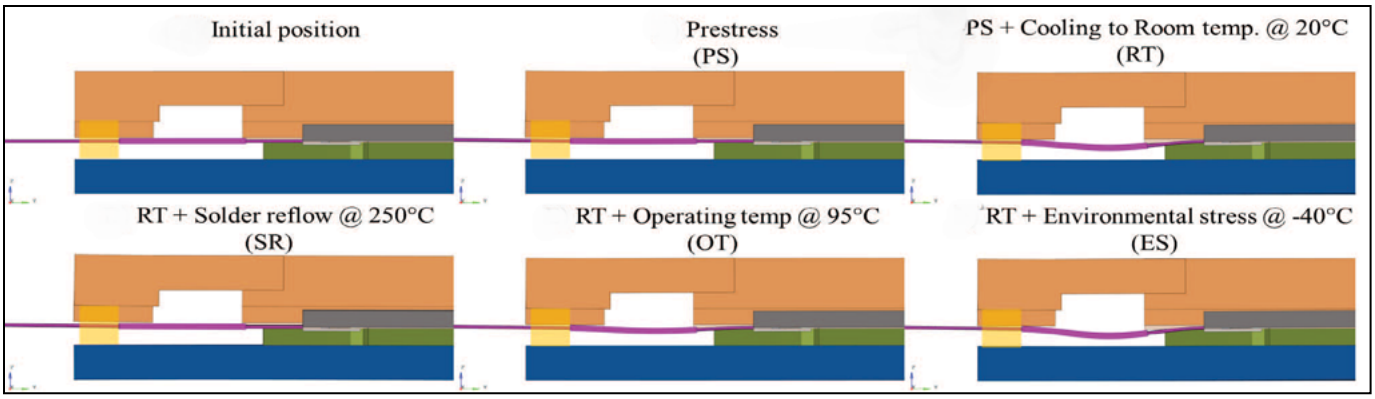


Figure 6: Illustration of the module geometry after the various assembly steps and loading conditions, where an S-bend in the fibers is present at temperatures below the adhesive cure.

cycling, or from the axial pull force on the pigtail strain relief resulting in a certain net force at the PIC. We see how the layout of the fiber and bend can absorb the force and reduce the strain to the PIC interface.

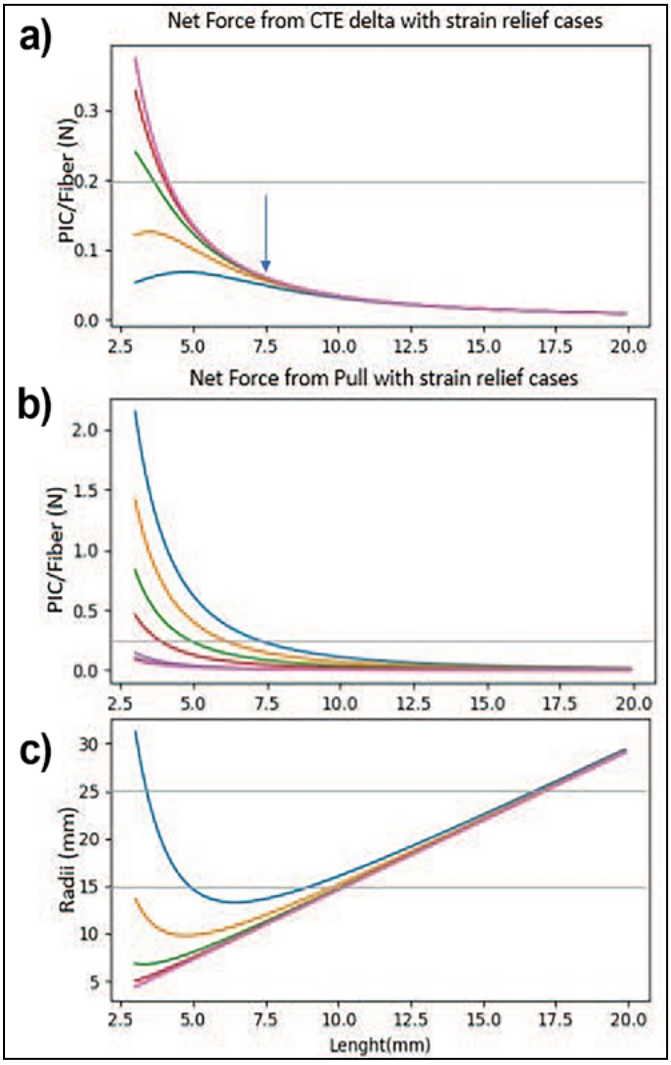


Figure 7: Impact on anchoring distance for various height values for: a) (top) CTE force, b) (middle) pull force; and c) (bottom) radii.

We also gathered experimental data for strain relief to be able to align model selection criteria. Adhesion to the ribbon jacket is key to ensuring a proper retention, and the securing can be done either on the lid, stiffener or substrate. As part of the selection process, the strain relief adhesives are subjected to the tests listed below and their performance was evaluated. The experimental data consist of the following tests to evaluate the adhesives to be used as fiber ribbon strain relief material:

1. A solder reflow profile excursion at 250°C@1min, then optical read out and ribbon pull.
2. An accelerated thermal cycling -40°C/125°C for 500 cycles, then optical read out and ribbon pull.
3. Application of damped heat at 85°C and 85% relative humidity for 500 hours, then optical read out and ribbon pull.

The samples are prepared by placing the ribbon on a metal plate, then dispensing and curing the strain relief adhesive; an example is presented in **Figure 8**. The fibers in V-grooves are held very tightly with a structural adhesive, and the strain relief must ensure some safety limit to protect the assembly.

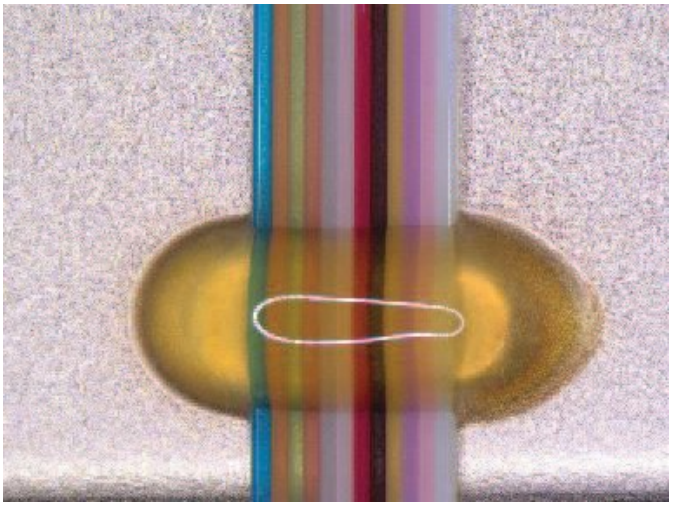


Figure 8: Example of ribbon attach with an adhesive on a metal-plated finish. The adhesion to the ribbon is critical to guarantee satisfactory results for the pigtail's retention tests.

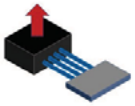
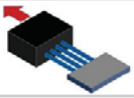
Fiber retention mode	Schema	Min Force Range (N) (Per fiber)
Shear force out V-groove		2
Axial pulling		5+

Table 2: Experimental measures or retention forces of the fibers attached to the V-groove.

Strain Relief location	Ribbons 12	Pull force range after solder reflow
On Stiffener	Type F	> 45 N (10 lb)
On Lid	Type F	62-67 N (14-15 lb)
On Stiffener	Type S	67-80 N (15-18 lb)
On Lid	Type S	49-67 N (11-15 lb)

Table 3: Experimental retention force pull data of ribbons of 12 optical fibers (typical sample size of 12) on a metallic surface.

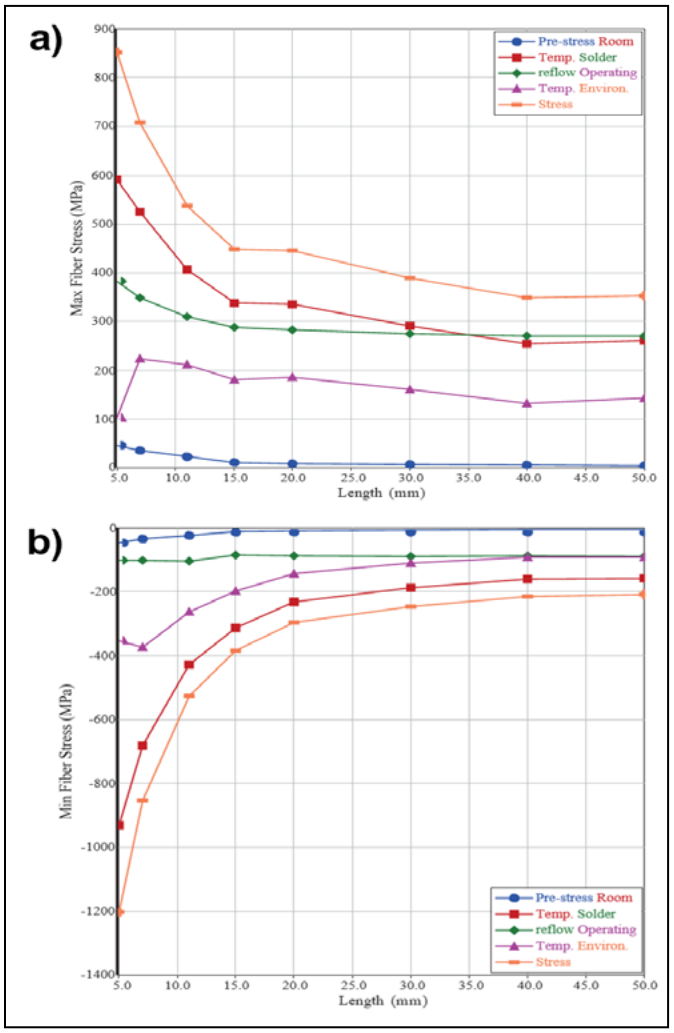


Figure 9: a) Maximum and b) minimum fiber stresses vs. the fiber free length for the pigtail configuration.

The experimental measure of the fiber attach retention force to the PIC V-groove depends on the direction of the applied force as shown in Table 2. Naturally, the axial pulling force is the strongest one, while the shear force out of the V-groove is lower. The strength measurements are also obtained for the ribbon pull at the anchoring points – either the lid or the stiffener depending on the configuration. Table 3 shows the typical axial pull force at failure for an array of 12 fibers for different configurations. Those experimental values are used as limits to guide our model optimization.

Model results

The variation of the fiber free length between the attach point on the maximal fiber axial stress in the pigtail configuration is presented in Figure 9. In general, stress decreases with increasing length, which is expected because longer fibers require less force and curvature to accommodate the thermal strain. The environmental stress test with low-temperature loading creates the maximum thermal stress condition, as the thermal shrinkage with respect to the adhesive curing temperature induces the most bending in the fibers. A similar effect is observed in the minimum fiber axial stress for the fiber length range studied. It is noted that the stress of the optical fiber for the pre-stress condition is nonzero because we applied an initial fiber bending from an initial offset and exiting angle when placed and attached in the package. The bending of the fiber is illustrated in Figure 10 and shows the evolution of fiber curvature for various fiber free lengths. If the fiber bend radius gets too small, the integrity of the fiber may be at risk. We have traced lines showing common minimum radius thresholds of 15 and 25 millimeters. Modules with shorter free fibers exhibit more curvature and stress.

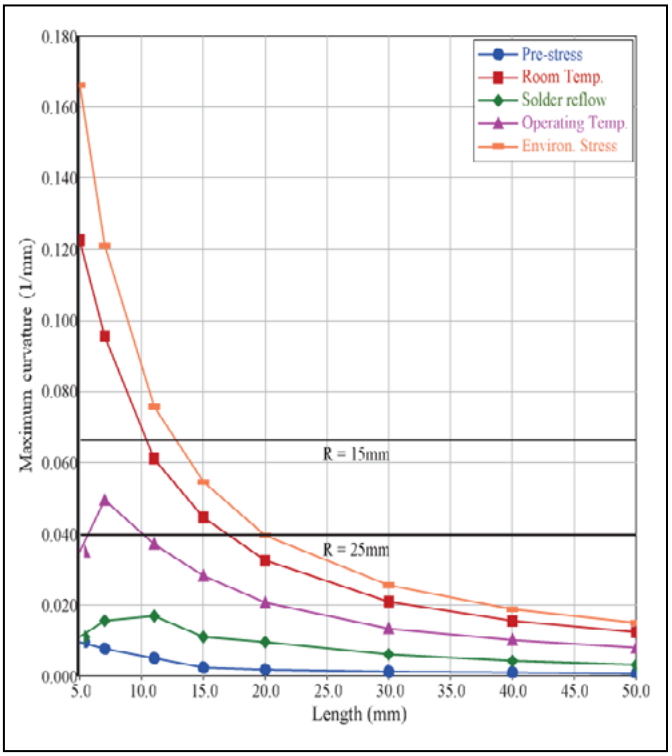


Figure 10: Maximum fiber curvature of various fiber free lengths of the pigtail latching within the module.

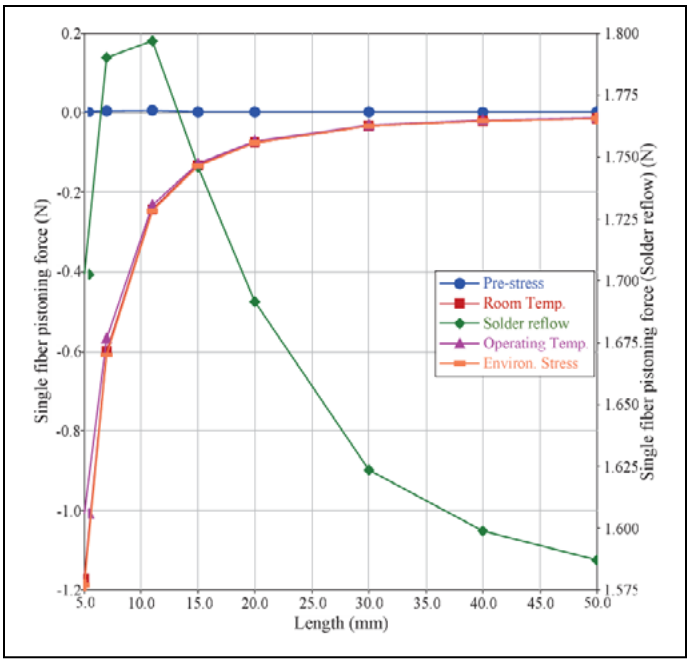


Figure 11: Fiber pistoning force for various fiber free lengths secured inside the package of the pigtail fiber ribbons. The solder reflow load case is read along the right axis. As the length is reduced, a higher pistoning force is measured on the V-groove because there is less bending to accept the various strains induced by the load cases.

With the fibers coupled to V-grooves, **Figure 11** shows the fiber pistoning force generated at the interface for loading conditions, where the forces for the solder reflow condition are plotted along the right axis, while other conditions are plotted along the left axis. The cold conditions (room, operating and environmental stress temperatures) all follow a similar trend—the force decreases with an increase in fiber length. This is coherent with the buckling phenomenon; once the fiber undergoes instability and lateral deformation, the axial force reaches a plateau and does not increase with additional increments in compressive displacement of its ends. The force required to reach this plateau increases sharply with decreasing length, which explains the drastic increase in pistoning force for shorter fibers. For the solder reflow load case, the force does not vary as much with length as compared to the other loading conditions—excluding assembly pre-stress for which the pistoning force is negligible. While it may be desirable to reduce the fiber free length in order to minimize the footprint of the package, it is clear that a short fiber presents a greater reliability risk when used in this architecture. We clearly see the benefit of using a longer fiber free length inside the package to reduce stress.

In the case of attachment on a stiffener, a similar trend is observed, where longer fibers have more space to generate the required displacements to accommodate the strain variations caused by temperature changes. Another significant trend is that the maximum and minimum stresses increase in magnitude with increasing bend angle. Although the bend intuitively introduces a certain level of strain relief, the bending stress rapidly increases with the angle, because the bending of the fiber is directly related to the exit angle and offset. Maximum curvature increases with the exit angle and generally decreases with length—this indicates that shorter lengths might be more challenging with regards to stress and temperature variations. The pistoning forces calculated in the simulations are significantly smaller when introducing an initial internal bend, showing the ability

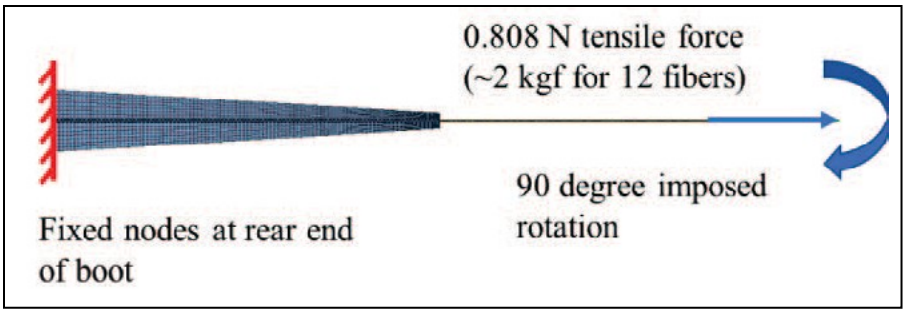


Figure 12: Description of the loading conditions used for boot optimization.

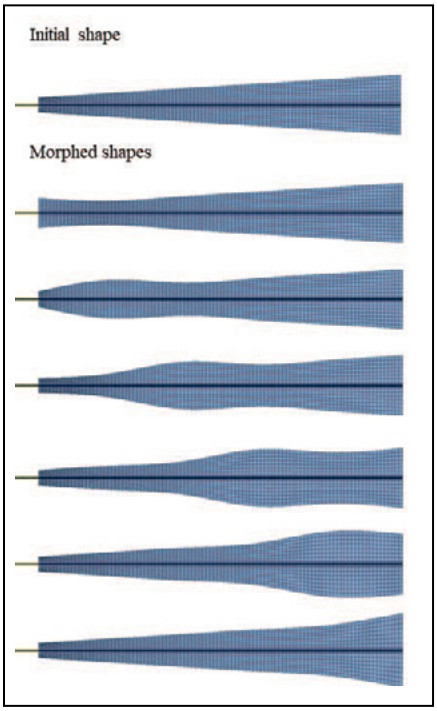


Figure 13: Shape perturbations used for boot geometric optimization.

of the bending control of the fibers to act as a strain relief mechanism. However, we must be careful that the fiber curvature and anchoring forces do not exceed the allowable thresholds. The benefit of the initial bend of the fibers are demonstrated [1], and an optimization was performed to balance the stress for the optimal strain relieving effect. The fiber bends and radii are the best indicators to track the fiber loads and ensure that they are within our specification. All these values need to be below the long-term and short-term bending radius thresholds for all loading conditions, to ensure robustness.

Boot optimization for ribbon pull

It's possible to add a boot at the point where optical fibers exit the module to prevent fibers failures when loads are applied to them. This feature is commonly used on all kinds of cables to mitigate the bending force and stresses. A gradual change of shape enables stiffness control to redistribute and reduce stress concentrations and therefore, to improve the overall cable strength when it is subjected to external loads. We studied the fiber stress response on the ribbon array for various boot materials and geometries, and presented some of the results of design optimization performed on a simplified quasi-2D model to take advantage of the boot-fiber system uniformity along its middle section to minimize fiber stress under a side pull force.

Preliminary studies showed the benefits of a boot with a tapered shape using softer material—it tends to distribute the stress. The loading condition is applied sequentially as described in **Figure 12**, with a first axial load before an imposed rotation of 90 degrees to reproduce the side pull test on the fiber. The initially applied tensile axial force prevents local bending and excessive unbalanced forces, both of which improve the stability of the simulation. A morphing model was used as a strategy to optimize the boot geometric parameter, where the finite element mesh is deformed using a combination of six smooth and continuous perturbations as shown in **Figure 13** in the computational domain. In our model, the material's elastic modulus is varied during the optimization process, but the length of the boot is kept constant at the minimal size to achieve an acceptable radius of curvature for the side pull test. The morphology of the boot is optimized toward minimization of the fiber's maximal principal stress. The boot shape morphology optimization experimental results suggested that there should be an increase in the root base of 27% in the thickness and an increase of 32% in the elastic modulus with respect to the original values. The combination of these two modifications leads to a reduction in fiber stress by 33% in our model as shown in **Figure 14**. Also, the location of the maximum stress has moved out from the root attachment to one fifth inside the boot length, indicating that the boot is able to distribute the fiber stress over a wider area, thereby decreasing the maximum stress level and improving the robustness of the fibers under this type of loading.

Several boot shapes have been tested in lateral load in **Figure 15** with the objective of improving the resistance of the fibers when subjected to lateral loads. Those boots add stiffness around the fiber ribbon at the edge discontinuity and the

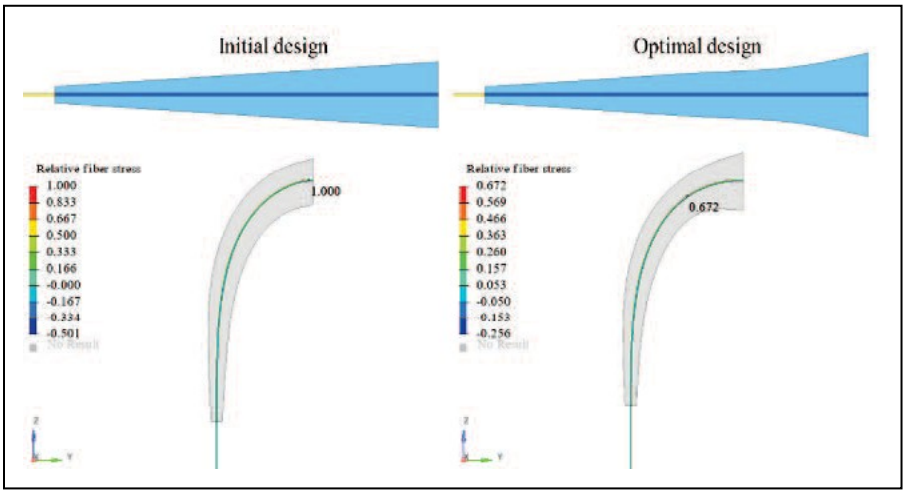


Figure 14: Morphologic optimization of the tapered boot. The initial and optimal shapes for such a boot are presented along with the resulting fiber stress in the side pull test load application. The shape did reduce by 33% the stress in the fiber used in our model.

exiting radii at this transition. A loading is applied at a distance of 22mm from the end of the module lid for all cases for this strength requirement. We also did account for the pre-bent free fibers inside of the module and the model uses a nonlinear large displacement analysis to take into account the effects of geometry changes during load application.

The configuration giving the smallest stress level is the tapered boot with a softer material, which reduced the stress by 17%. Also, the material variation had more impact on reducing the stress than the shape and therefore plays an important role when the fibers are deflected to the side. The pigtail retention between the side pull and the axial pull are totally different—**Figure 16** represents the comparison between the stresses calculated for a tapered oval boot configuration with the softer material. The stresses are normalized to the maximum of the axial pull load case, and a side pull load case that is 5.8x higher is observed, indicating that this condition is likely to be critical for the robustness of the module. This result is consistent with the experimental strength measurement of the fiber in the V-groove experiments where axial cases are significantly stronger than shear cases.

Summary

Fiber optics integration in the first-level package is required to enable high-bandwidth demands for data communication. The work in [1] studied the best anchoring location of a strain relief for fiber optics ribbon in order to protect the photonic die V-groove's interconnect. The fiber layout within the package between the strain relief and the photonic die uses fiber bending to compensate for thermal and mechanical strain of the package. An optimization of the parameters permits the maintenance and control of the fiber bends, thereby alleviating the stress within the co-package photonic device.

Our model has shown that longer lengths induce less stress and are easier to facilitate bending. Also, with fiber lengths below 8mm, the required bends needed for strain relief would be past the acceptable threshold limits for the fiber and would create excessive stress in the fiber. Also, the misalignment in the fibers caused by the exit angle

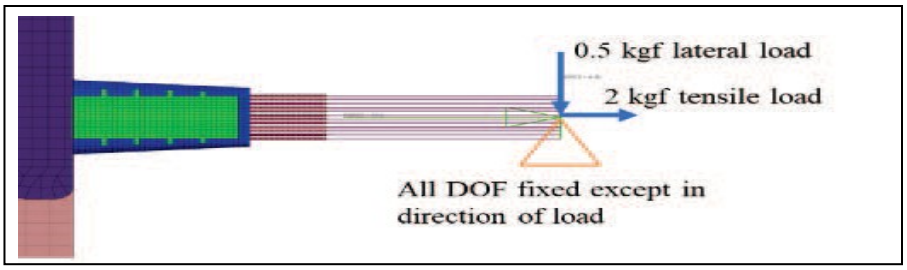


Figure 15: Example of loading conditions considered on the pigtail exiting the module. The tapered boot design that was included in this study is shown.

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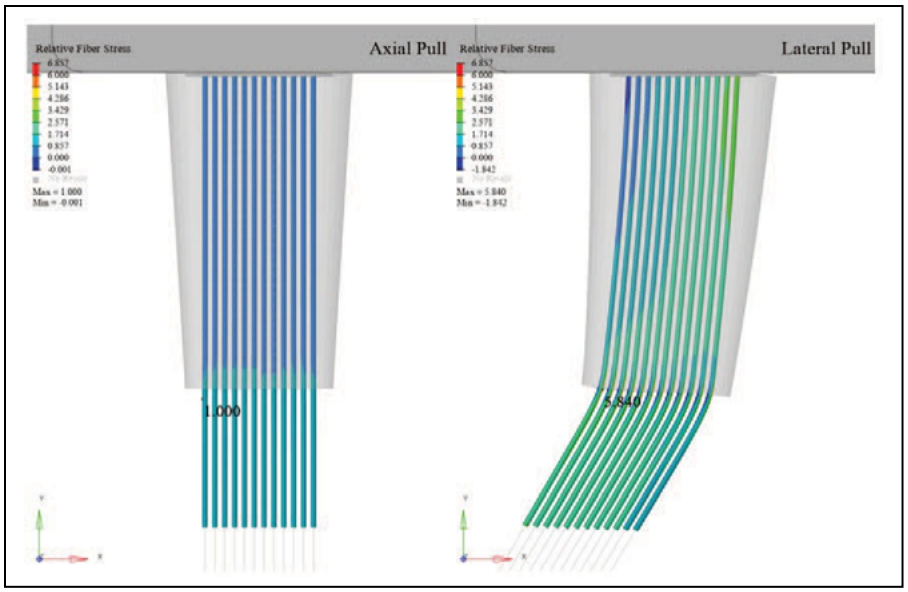

Figure 16: Stress comparison between the axial pull and lateral pull load cases on the tapered oval boot. The stresses from the lateral case are ~6X higher than those of the axial case.

geometry is slightly beneficial for small angles, and permits reduction in the pistoning force in the studied configuration. Finally, a boot that protects the exiting ribbon is of great importance to provide compliance with side pull test standards because the fiber radii of the module at that location must be controlled. Also, our data indicates that the lateral force applies approximately 6 times more stress than in the axial direction, adding to the benefit of a boot. Various boot shapes and materials were compared, and a morphologic optimization was performed—an up to 33% stress reduction is predicted by our models. This work enables us to propose module designs for pigtails that are optimized to control package stress and fiber curvature, thereby enhancing long-term integrity and simplifying the assembly process. This review highlighted the importance of the fiber configuration, such as bend and supporting structures, to reduce fiber stresses for optimal and reliable photonics interconnects in CPO.

Acknowledgment

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Biography

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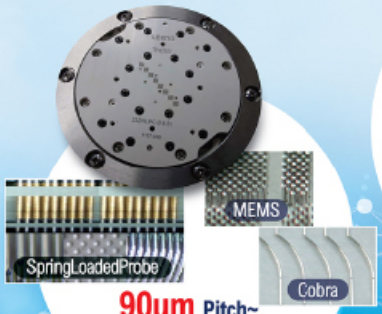

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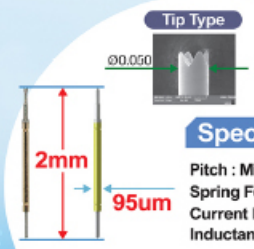

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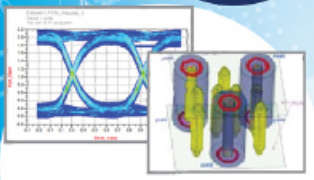
Pitch : Min.120um
Spring Force : 8.0g@ 250um
Current Rating : 1.0A
Inductance : 0.38nH

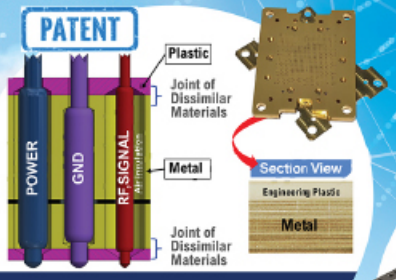
RF Probe for Fine Pitch Probe Head


0.18mm Pitch~
RF Coaxial Spring Probe & Impedance Controlled

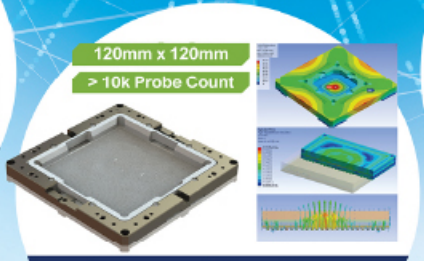

Logic Test Socket


High Speed
Frequency : >20GHz
VSWR : < 1.2
Automatic Coaxial Probe


Electrical Analysis
CCC Test, HFSS, TDR
Eye Diagram
4 Port VNA Test

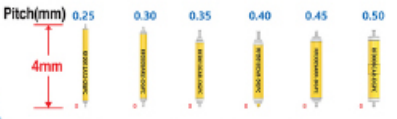


MP Socket



Large Device Socket

Specification
Frequency : 80GHz(BGA),
100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%



Coaxial Probe 100GHz

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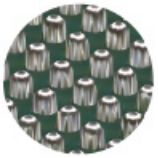
Seriously Fast.

WX3000™ Metrology and Inspection Systems for Wafer-Level and Advanced Packaging


Copper Pillar


Micro Bump


Flip Chip (c4)


BGA Ball

Powered by Multi-Reflection Suppression™ (MRS™) Technology

2-3X Faster with High Resolution and High Accuracy

WX3000 3D and 2D metrology and inspection system provides the ultimate combination of high speed, high resolution and high accuracy for wafer-level and advanced packaging applications to improve yields and processes.

Powered by Multi-Reflection Suppression (MRS) Sensor Technology

The 3-micron NanoResolution (X/Y resolution of 3 micron, Z resolution of 50 nanometer) MRS sensor enables metrology grade accuracy with superior 100% 3D and 2D measurement performance for features as small as 25-micron.

100% 3D and 2D metrology and inspection can be completed simultaneously at high speed (25 300mm wafers/hour and 55 200mm wafers/hour) as compared to a slow method that requires two separate scans for 2D and 3D, and only a sampling process.

Nordson TEST & INSPECTION

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