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The Future of Semiconductor Packaging

Volume 26, Number 6

November • December 2022

Double-sided probing system for 150µm pitch co-packaged optics

page 11

- Powering chips from the backside
- Device validation: the ultimate test frontier
- HPC applications drive reliability of HD FO packaging
- Large-panel FO perspective on cost, yield, and capability
- Cooperation is key to success of the CHIPS and Science Act

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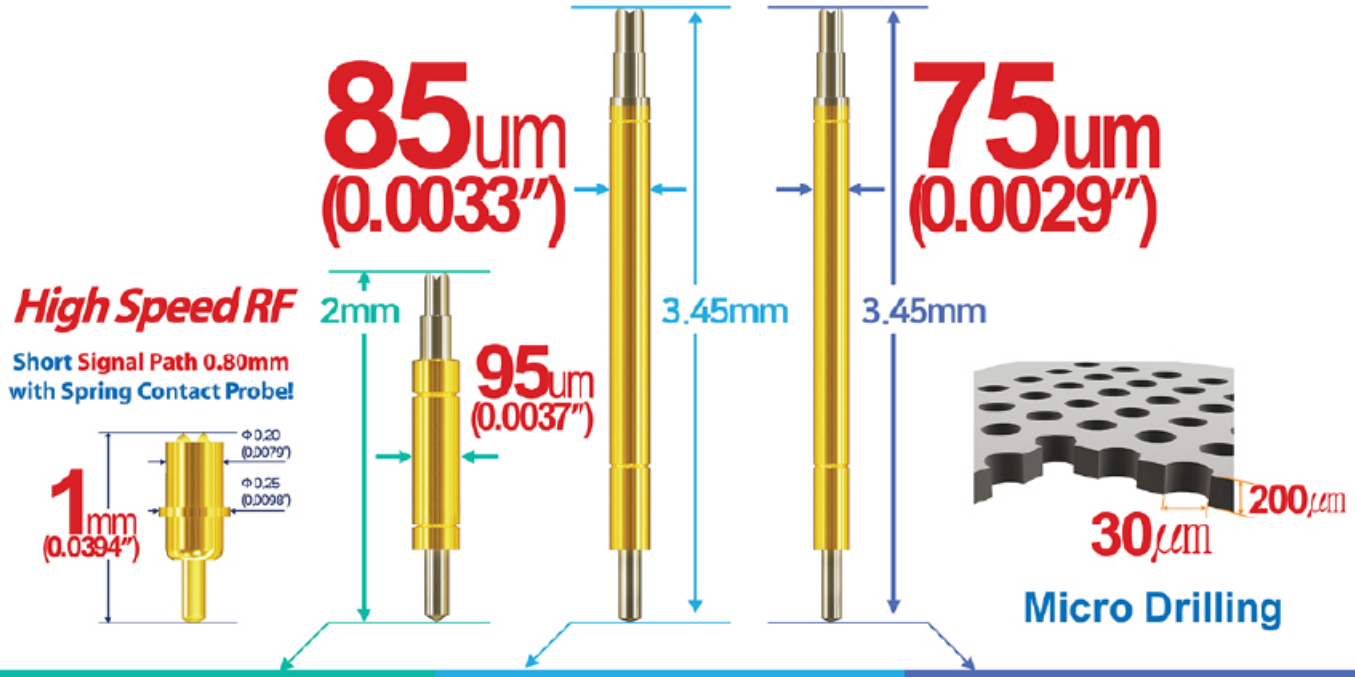


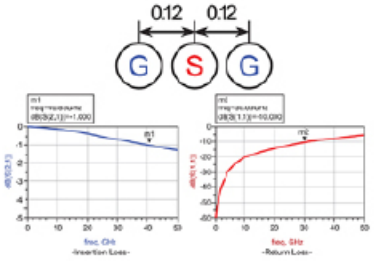
120㎛ Pitch

Mechanical Spec.

- Spring Force : 0.281oz (8.0g) @ .0098 (0.25mm)
- Recommended Travel : .0098 (0.25mm)
- Full Travel : .0118 (0.30mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No pleted
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation Data)

- Current Rating : 1.0A
- Propagation Delay : 20.80ps
- Capacitance : 0.21pF
- Inductance : 0.38nH
- Insertion Loss : 40.83GHz @ -1.000dB
- Return Loss : 30.03GHz @ -10.000dB
  (Dielectric material : CERAMIC)



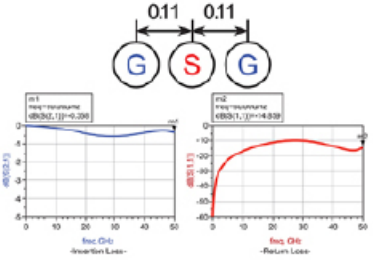
110㎛ Pitch

Mechanical Spec.

- Spring Force : 0.212oz (6.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation Data)

- Current Rating : 0.9A
- Propagation Delay : 38.25ps
- Capacitance : 0.47pF
- Inductance : 0.63nH
- Insertion Loss : > 50.00GHz @ -1.000dB
- Return Loss : > 50.00GHz @ -10.000dB
  (Dielectric material : CERAMIC)



100㎛ Pitch

Mechanical Spec.

- Spring Force : 0.247oz (7.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation Data)

- Current Rating : 0.8A
- Propagation Delay : 35.55ps
- Capacitance : 0.44pF
- Inductance : 0.66nH
- Insertion Loss : > 50.00GHz @ -1.000dB
- Return Loss : > 50.00GHz @ -10.000dB
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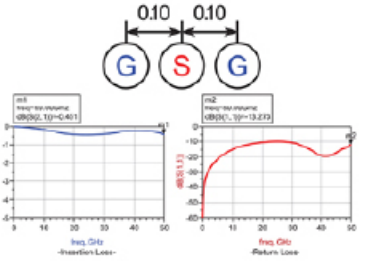

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November • December 2022
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CONTENTS

The cover article describes a double-sided probing system for 150µm-pitch co-packaged optics (CPO). Such probing systems address the growing need for assured yield, particularly as heterogeneous integration is combined with silicon photonics needed for higher performance Ethernet applications to 800G.

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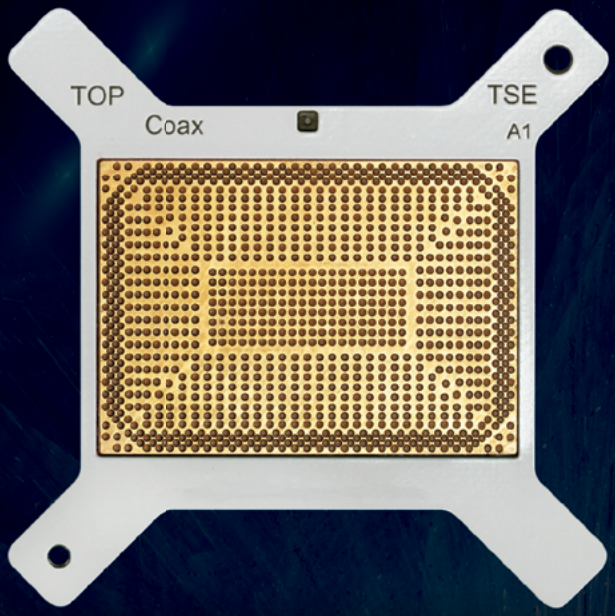

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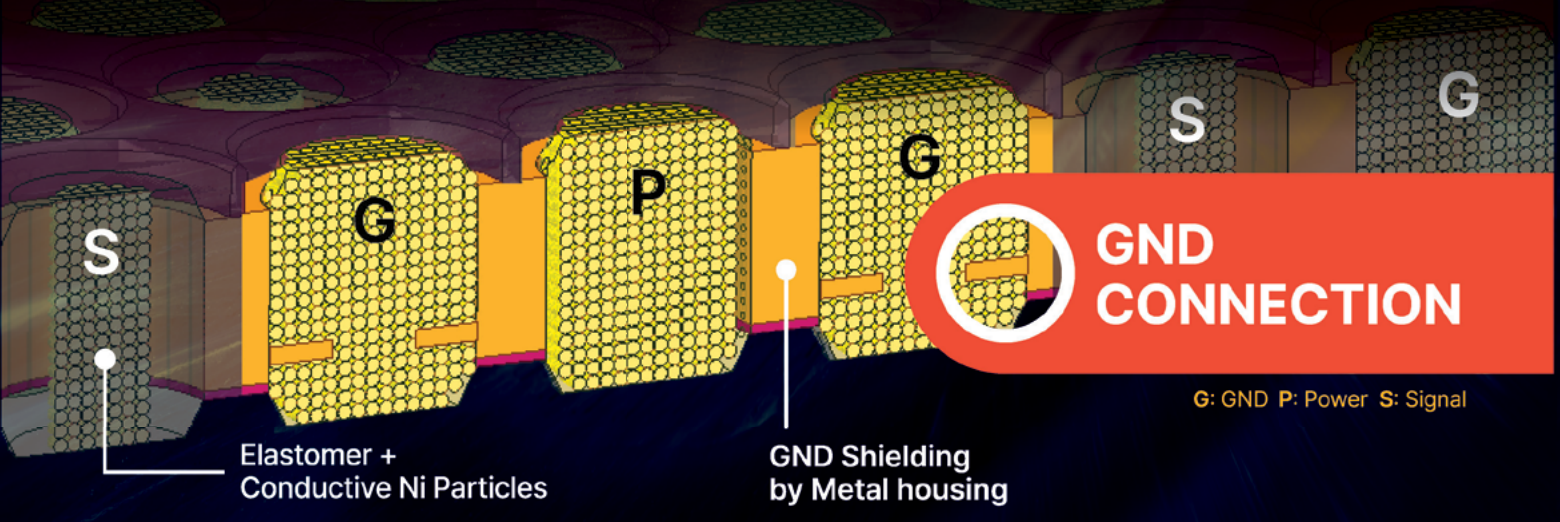

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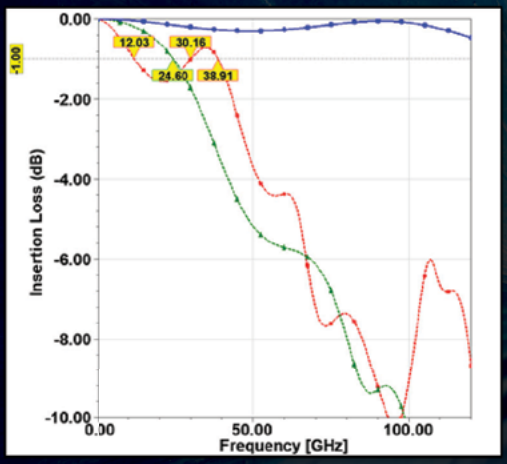
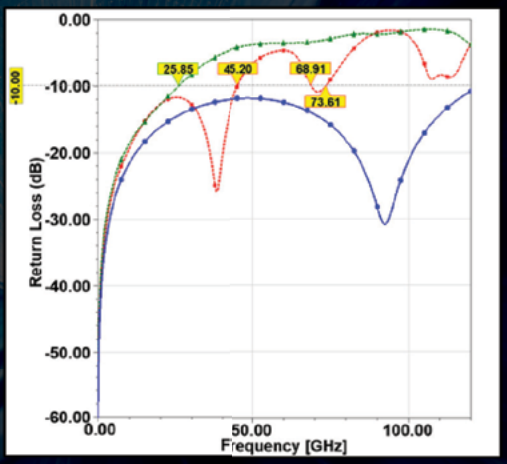
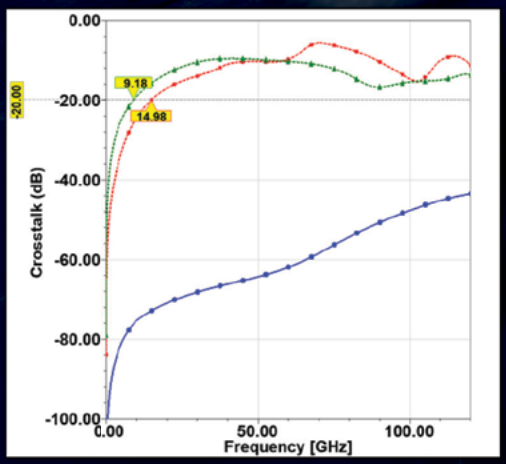
Return Loss (S11) @-10dB	45.20	25.85	>100
Crosstalk (S31) @-20dB	14.98	9.18	>100



Insertion Loss



Return Loss



Crosstalk

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Cooperation is key to success of the CHIPS and Science Act

By Asif R. Chowdhury [UTAC Group]

There has been a lot of talk and discussion regarding the recent CHIPS and Science Act. Passed by the U.S. Congress in an unusual show of bipartisan support, the bill allocates US$52.7 billion in the form of subsidies to promote a domestic semiconductor eco-system and achieve a higher level of national independence through increased domestic manufacturing of semiconductors. About US$39 billion of the funds is earmarked for semiconductor fabrication facilities, with US$2 billion specifically allocated for mature semiconductor products that are considered vital for national defense and security—this also includes chips used in the automotive sector. The balance of the funds is targeted to foster increased research and development efforts and cultivate a talent pool essential for the sector. The bill does come with some guardrails, i.e., imposing restrictions in establishing manufacturing sites in certain geographic regions.

Three sides to the debate

The discussions and debates about the CHIPS Act have evolved mostly around three primary views and arguments. The patriotic argument is that such focus is essential for the United States to have long-term sovereign independence of critical semiconductor components, economic growth and national security. After all, microchips are ubiquitous today, used in literally everything from toaster ovens to watches, to our every-day vacuum cleaners, to weapons systems.

Another side argues that such protectionist moves play against the free-market dynamics. The natural flow of the evolution of semiconductor manufacturing over the past decades has followed the market path of optimum labor and technology dominance – manufacturing primarily in lower cost geographic regions (i.e., Asian nations), while advanced design is concentrated mainly in the U.S. Free-market advocates are keen to point out that this kind of national subsidy will disrupt the free market, thereby resulting in an increase in manufacturing costs and a waste of resources, ultimately hurting consumers.

Then there is a third viewpoint that argues that this whole effort is nothing more than a geopolitically-motivated, futile effort to deter an increasing manufacturing share of Asia, particularly that of China. This side also adds that, despite the subsidy, the effort will likely not achieve its goal with decades of lack of attention and funding of the industry that led to the U.S. decline in its manufacturing capability and capacity in the first place.

Each of the three perspectives has some merits, especially when reviewed in isolation. But in today's connected global ecosystem, it would be unwise to view any key semiconductor policy decision in isolation.

A global perspective

Today, the semiconductor industry contributes to less than 0.5% of the global gross domestic product (GDP), but plays a critical role in most of the balance of the 99.5% of the GDP. The significant supply chain disruption caused by COVID-19 served as a wakeup call, not only for the U.S., but also for Europe and Japan. The impact and importance of semiconductors in our daily lives and national interests quickly became apparent, and the realization was further solidified by recent geopolitical instability. These concerns prompted these regions to seriously contemplate a path towards increasing self-reliance. Undoubtedly, the trade war between the U.S. and China has become a valid concern for many countries, even though many may not necessarily openly show more support to one side than the other. Nevertheless, wheels are now being set in motion across geographic regions that will likely have a significant impact on the semiconductor manufacturing landscape by the end of the decade.

From the standpoint of recent supply chain disruptions, the trade war and the geopolitical risks, the first argument about achieving some level of sovereign semiconductor independence perhaps holds water. America still leads the world in semiconductor technology: in 2021, the U.S. held 54% of global semiconductor market share and 7 of the top 15 semiconductor companies were American. Over the past decade, the U.S. has spent almost twice as much in research and development as the rest of the world combined. These statistical figures while spectacular, provide a false sense of security. Indeed, the U.S. leads in semiconductor design and market share, but it has fallen far behind in the manufacturing sector. While semiconductor devices and technology were invented in America, only about 10% of the world's supply comes from the U.S. today—down from 37% in 1990. In comparison, China's share has grown from 0% to 24% during the same period. Today, 75% of the global chip supply are manufactured in Asia, with 40% of that coming from Taiwan alone. Taiwan accounts for 66% of the global foundry market share with TSMC commanding an impressive 56% of the share by the end of this year. **Figure 1** shows this historical trend clearly and predicts the outcome by the end of the decade—and it is not a pretty picture for the U.S., Europe and Japan. The design capability in itself is not of much use if these products can't be manufactured with access to a steady stream of supply to meet demand. MITRE Engenuity, a non-profit organization that manages federally-funded research and development centers, defines the

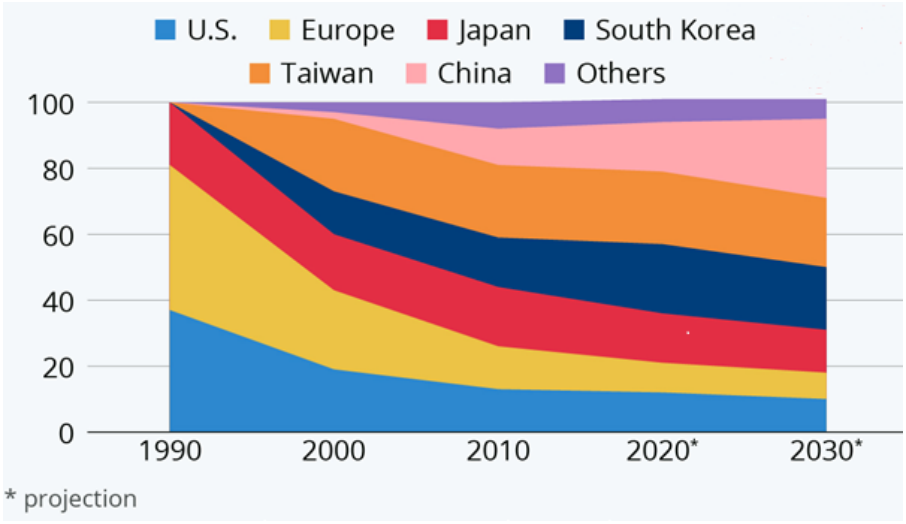

Figure 1: Global semiconductor manufacturing by location in percent. SOURCES: Boston Consulting Group, Semiconductor Industry Association, SEMI

problem statement as: "U.S. leadership in semiconductor is threatened by the lack of U.S.-based capacity for prototyping, scaling and transfer-to-manufacturing of breakthrough semiconductor technologies that are the foundation of future information and communications solutions necessary for national security and economic resiliency." The CHIPS Act is geared towards a "course correction" to grow the capability from lab-to-fab domestically.

The second argument about such industry subsidies being a protectionist move is not unfounded either. Indeed, despite all the progress in globalization made during the last decades, the recent trend seems to be more toward protectionism with an increasingly polarized view of the world—a world that has become increasingly complex by the realities of today's heightened geopolitical tensions. But the goal here is not necessarily to take over semiconductor manufacturing domination from the likes of Taiwan or the Asian nanoscale duopoly of Samsung and TSMC, but rather to achieve a healthy level of independence of the semiconductor supply chain to reduce the risk of dwindling or no supplies, at least for some of the critical products. Even if the U.S., EU and Japan tried to take over semiconductor manufacturing dominance, it will take years, perhaps even a decade or so, based on their capabilities today.

The U.S. is not alone in this quest to achieve a healthy level of independence. Both Europe and Japan have launched their own equivalent "CHIPS Act" to try to achieve their own strategic autonomy and resilience. The EU launched an ambitious project in 2013 to double its onshore share of semiconductor production. However, almost ten years on, its share has remained around 10%. This time around, seemingly more serious, the EU has launched its own "CHIPS Act" in February of this year that is geared to generate €43 billion in public and private funding. Similar to the U.S. bill, the EU Act has three distinct pillars. The first pillar is to increase research, development and pilot production lines on European soil. This partnership not only includes the 25 EU countries, but also Israel, Turkey and Norway. The second pillar is to set up more "Open EU Foundries" using advanced technology nodes. The third pillar is to ensure continuity of supply to the continent and the ability to intervene in case of a supply-related crisis.

Similar to the EU's efforts, Japan's Ministry of Economy, Trade and Industry (METI) has taken significant steps to boost domestic production of advanced chips. In the late eighties, Japan manufactured over 50% of the world's semiconductors. Today, it supplies less than 10%. **Figure 2** shows the historical trend and the 2022 forecast of semiconductor capital expenditure (CapEx) by headquarters location. The lack of focus on semiconductors on the part of the U.S., EU, and particularly Japan, is very telling in these trend lines. While the percent of the U.S. semiconductor-related CapEx has dropped from 31% to 27%, and Europe's has dropped from 8% to 3% from 1990 through today, Japan's share of semi CapEx has dropped significantly, from 51% to less than 4%, during the same period. Just like the U.S. and the EU, the Japanese government is also adopting policies to ensure "strategic autonomy and indispensability." In November of 2021, it approved a ¥774 billion package to boost domestic semiconductor production that included a ¥400 billion subsidy to TSMC for a new foundry in the southern island of Kyushu.

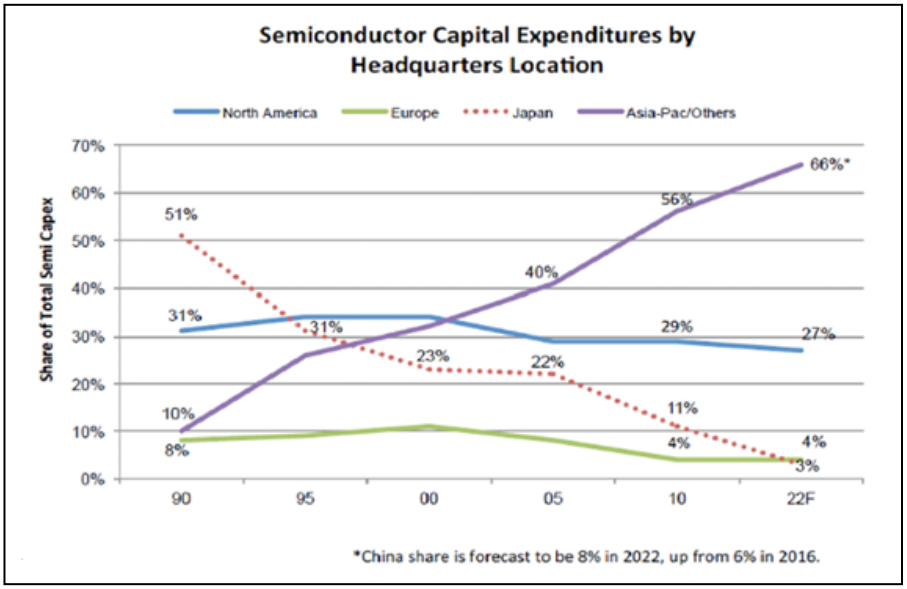

Figure 2: Semiconductor capital expenditure by headquarter locations. SOURCE: IC Insights

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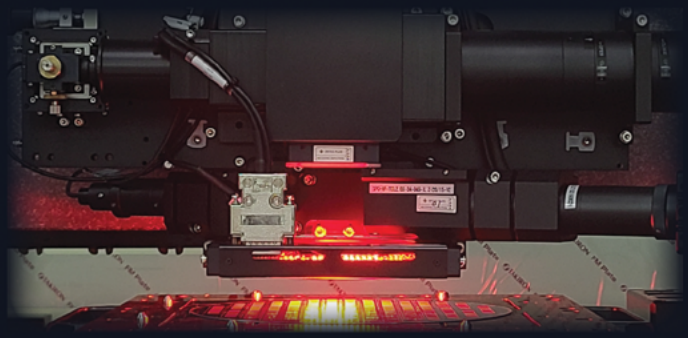

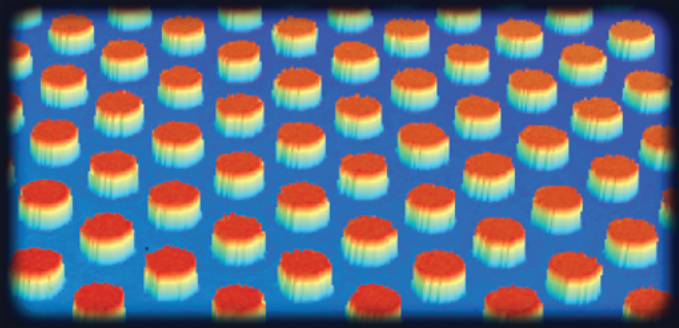

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Additionally, these seemingly protectionist moves on the part of the U.S., EU, and Japan seem to include a certain level of international cooperation. In May of 2022, President Biden and PM Kishida agreed to explore joint U.S.-Japan development of next-generation semiconductors. In October, there was a "Chip 4" meeting, led by the U.S., which included Taiwan, Japan and South Korea to discuss possible cooperation regarding semiconductor supply chain resilience. These moves toward gaining strategic autonomy in semiconductor manufacturing seem be less of isolated protectionism and effectively more of a "collective and coordinated" protectionism. If done through proper international cooperation, it can create a competitive global landscape that will, in turn, allow healthy progression of technology development and cost competitiveness.

There is nothing fundamentally wrong or immoral about an honest effort to boost the internal manufacturing capability for any nation. Government incentives such as the CHIPS Act are a common way to achieve this boost when significant capital is involved to entice companies to set up domestic manufacturing plants. While the U.S., EU and Japan have newly enacted such subsidies, China has been doing this for almost a decade starting with its 2014 National Integrated-Circuit Plan and Fund, which was endowed with US$150 billion from central and provincial governments. Their latest 14th Five-Year Plan includes significant government focus and funding for the advancement of domestic semiconductor development and production—the Shanghai municipal government alone is supposed to fund RMB 300 billion towards the initiative. China is not alone in providing such subsidies. Last year, South Korea announced tax credits up to 50% of investment in semiconductor research and development creating a US$450 billion investment from local companies.

The third argument that these moves are geopolitically motivated to a large extent is undeniable. Despite all the political rhetoric and trade sanctions, the world finds itself in the awkward position of not being able to ignore the huge China market—the largest market for semiconductors by sales commanding about a 35% share. At the same time, China is not going to sit by idly and will continue to explore ways to catch up. What China has been able to achieve on many fronts in a relatively short period of time is a testament to its national resolve, discipline and ability. It will continue to compete, at least on manufacturing at the lower end of the semiconductor manufacturing technology spectrum. Such products are, and will continue to be, widely used in many applications.

A new era of competitiveness

The new focus on manufacturing through sovereign investment in the U.S., Europe and Japan in the front end, with a similar focus of southeast Asian countries in the back end, along with China's burning ambition to catch up in the technology, could usher in a new level of market competitiveness the world hasn't witnessed in decades. And such healthy competition is always a good thing for innovation and cost-effective solutions that help propel the broader global market economy, and that ultimately, benefits the consumer.

The U.S. effort to impede China's ability to access advanced semiconductor technology is a matter of concern for many nations. Most of the players in the Asia region are playing it "safe" by trying not to displease either superpower to ensure access to both the advanced technologies and the China market. Additionally, many countries in the Asia Pacific region such as Thailand, Malaysia, Philippines, Singapore and Vietnam are likely to reap benefit as companies, worried about future sanctions, may want to start or increase production in these countries, especially in the back-end sectors of assembly and test, so as to diversify away from China. Along this line, India seems to have renewed its ambition to become a major player in the semiconductor manufacturing space, and in a true sense of support, the government is putting money behind its mouth this time around. The country is counting on benefiting from the West's increasing concern on relying too much on China and trying to become a key semiconductor manufacturing hub even though it will take at least a decade, if not longer, to do so. It is telling that, for the first time, some of Apple's iPhone 14s are assembled in India.

Finally, there is the added argument that these efforts to increase domestic manufacturing will be exercises in futility. Today, American core competency lies on the design side, whereas the state-of-the-art semiconductor manufacturing has moved to Asia, specifically Taiwan and South Korea, for advanced wafer nodes, and Southeast Asian nations for back-end assembly and test. It will take the U.S. over two years to catch up with the likes of TSMC and Samsung on the advanced wafer nodes. After letting the semiconductor manufacturing competency slowly erode away starting from the late 90s, the U.S. and Japan now lack the required talent pool to manufacture advanced semiconductors within their shores—this will take years to cultivate. Additionally, the funding required for U.S., EU and Japan to gain back the market share they once had would require substantially more capital than what the CHIPS Act has allocated. For example, the U.S. will have to spend about US$300 billion to get back the 37% market share it once had. Similarly, the EU will require a capital expenditure of US$164 billion to achieve its 20% share of semiconductor production. If these gaps in funding are to be filled from the private sector, the government will need to continually ensure such support. This may prove to be a difficult path if the political interest in achieving these goals starts to wane—one of the risks of democratic societies.

These "CHIPS Act" initiatives by governments already seem to be paying some dividends in terms of ushering in investment from the private sector. Intel, TSMC, GlobalFoundries and Samsung have all announced new wafer fab facilities in the U.S. through the next few years in Ohio, Arizona, Texas, and up-state New York. This includes a 5nm technology fab by TSMC. STMicro and GlobalFoundries just recently signed a memorandum of understanding to build a new fab in Crolles, France at a cost of €5.7 billion. Intel recently unveiled its massive €80 billion investment plan in Europe starting with two fabs in Magdeburg, Germany at a cost of €33 billion. Earlier this year, encouraged by METI's commitment to domestic semiconductor growth, TSMC planned its first ever wafer fab plant in Kumamoto in Kyushu Island, a joint venture with SONY and Denso.

It is not a zero-sum game

It is hard to argue that a certain level of global cooperation will be needed to make these acts and efforts successful and more importantly, sustainable. Market dynamics have led semiconductor manufacturing away from the U.S., Europe and Japan (while they still lead in design) to countries with lower labor costs over the last few decades. An argument can be easily made that this market led economy has produced an "efficient" global supply chain, ultimately benefitting everyone. In an ideal world, cooperation among all nations, each bringing to the table its own key ability and supply chain dynamics is best for the broader society. Even in our non-ideal reality, some level of cooperation is a must to bear fruit from these various efforts akin to the CHIPS Act. Ultimately, all these efforts to gain strategic autonomy cannot ignore the interdependent global order. Pure unilateral approaches will result in over investment, impede true innovation and misallocation of labor and precious resources. The policy makers will do well to consider the global supply chain order and allow a certain level of cooperation to ensure a positive sustainable outcome.

Despite what political leaders across the globe are trying to achieve, at the end of the day, it's not a zero-sum game. There are pockets of competencies that have been developed over decades—both on the technology front and the cost front. To try to reverse that may perhaps prove somewhat futile and lead to an inefficient use of resources. Nevertheless, the political divides we see today are a stark reality. And like everything else, the semiconductor landscape will also have to adjust to it despite the possibility of creating these pockets of inefficiencies for which, ultimately, consumers will end up paying. How these particular government interventions will play out to reshape the semiconductor manufacturing landscape, only time will tell. However, one thing is certain: given the current trajectory, the landscape will be starkly different by the end of the decade from what it is today.

Biography

Asif R. Chowdhury is SVP at UTAC Group, Singapore. He has over 30 years of experience in the semiconductor industry. Before joining UTAC, he held senior positions at Amkor Technology, Chandler, AZ, and Analog Devices, Wilmington, MA. He holds a BS in Mechanical Engineering from U. of Texas at Arlington, an MS in Mechanical Engineering from Southern Methodist U., and an MS in Finance and an MBA from Northeastern U. Asif's first book on the Japanese work culture entitled, "A Gaijin Sarariman," has just been published by Penguin Random House. Email asif_chowdhury@utacgroup.com

Double-sided probing system for 150µm pitch co-packaged optics

By Collins Sun [WinWay Technology]

The focus of the double-sided probing system described in this article is to be in alignment with trends in networking development. As expected, advanced packaging technology will continue to extend Moore's Law, particularly the rapid development of heterogeneous integration (HI). According to various organizations, such as IEEE, SEMI, and ASME, the essential spirit of HI is to integrate different process nodes and application-specific integrated circuits (ICs) into a single high-end package, such as a 3D structure system-in-package (3D SiP). When HI is combined with silicon photonics (SiPh), trace loss from pluggable optics is greatly reduced and is able to drive higher performance Ethernet applications to 800G (see **Figure 1**).

Individual active and passive optical components in a package can provide the best performance and cost benefits in a comprehensive manner. However, more sophisticated processes in package assembly also mean that it is critical to have the assured yield after assembling all the discrete chips. Co-packaged optics (CPO) is one representative application—its optical signal has a better signal-to-noise ratio than electrical signals because of the light being transmitted through an optic fiber rather than electrical signals through a copper trace. Having optical engines near the electrical switch to reduce signal trace length in the substrate by advanced package technology is a breakthrough technology. According to Yole Intelligence, the compound annual growth rate (CAGR) of the CPO market is predicted at around 55%, from US$6 million in 2020 to US$2.2 billion by 2032 [1].

SiPh have been considered a unique technology for developing high-performance networking system because of several factors. First, it can be designed and manufactured using current complementary metal-oxide semiconductor (CMOS) processes and equipment, thereby achieving lower cost and higher performance devices. Second, it can be combined with logic and digital circuits for data processing. Third, SiPh can be designed using different wafer materials, such as III-V compound semiconductors. The future of SiPh will flow into two main streams: co-packaging and chip integration. Co-packaging is the 2.5D integration of the CMOS logic or digital chip with optical

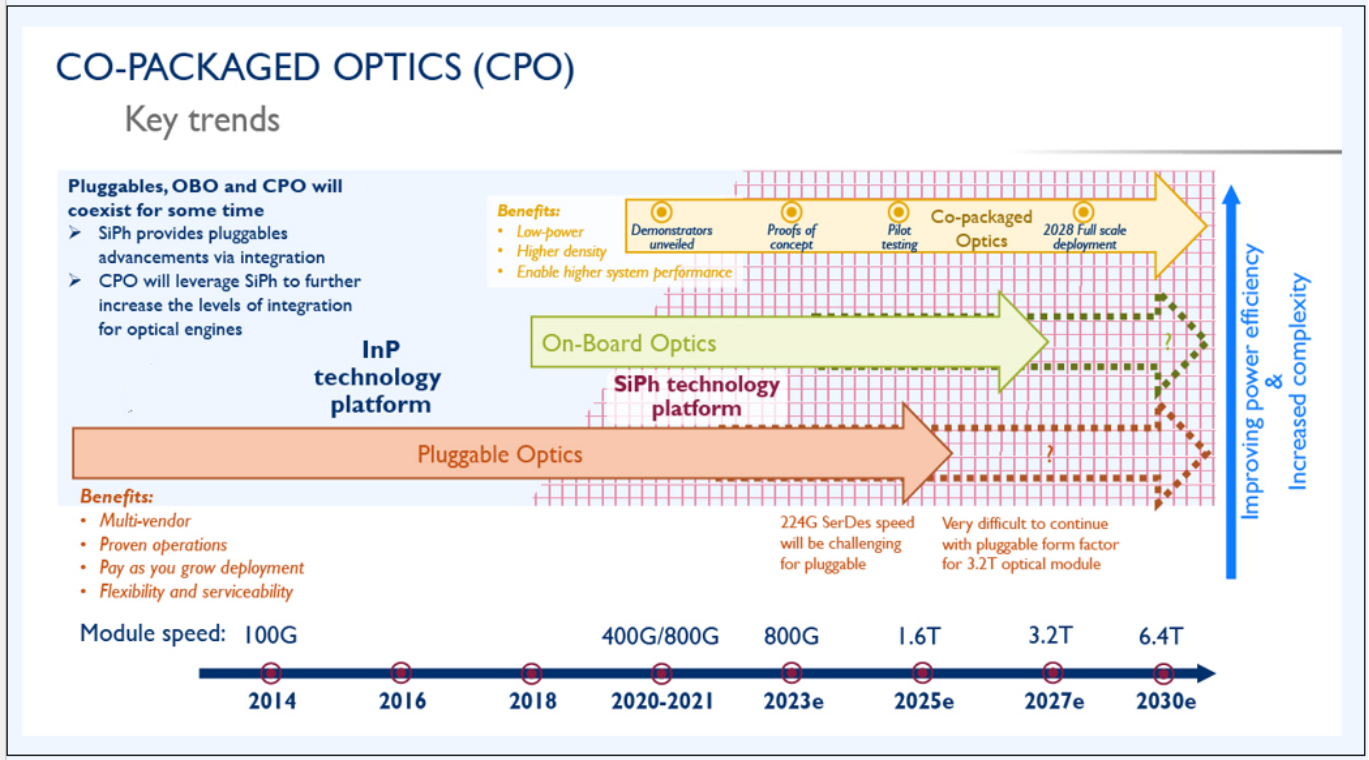

Figure 1: Development trends in pluggable optics and CPO. SOURCE: Yole Group

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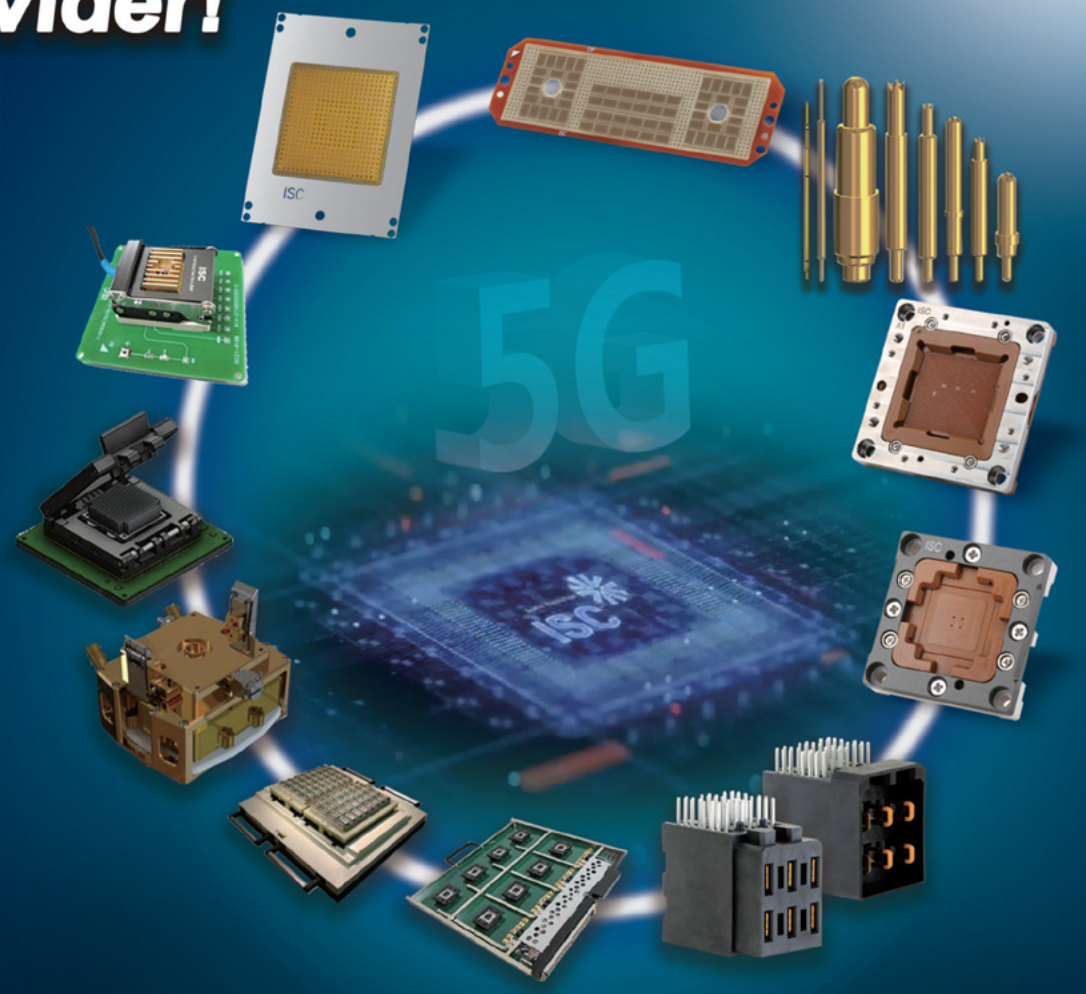

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chips connected by the copper trace of substrate. Chip integration is a single complete chip solution that includes different functional ICs using through-silicon vias (TSVs) both for ASICs and optical die. SiPh are expected to integrate all optical components, such as filter, polarization diversity, and splitter/combiner into a single die, including an active laser, modulator, and photodetector. With the help of SiPh and photonic integrated circuits (PICs), CPO applications will be more competitive overall when compared to conventional pluggable optical modules.

The packaged optical component usually requires a smaller form factor with a fine pitch. Therefore, the testing system needs precision alignment for probing C4 sides approximately 150µm from the top side, and it also must overcome thermal expansion when testing at different temperature points. These are the initial requirements for the double-sided probing system for 150µm-pitch CPO.

Double-sided probing system

The targeted specifications of CPO packaging are listed in **Figure 2**. A double-sided probing system is needed to probe four sites of 150µm-pitch micro-bumps on the top and 1.0mm land grid array (LGA) pad design on the bottom of the package. The major challenges that CPO testing must overcome are: 1) fine pitch, 2) high power, 3) high speed, and 4) a wide temperature range from room temperature (RT) to 105°C. The required test speed is up to 112Gbps, and the dissipation power of the switch application-specific integrated circuit (ASIC) chip is 600W, which needs to be tested at 105°C.

As for testing the fine-pitch CPO package, the most critical aspects include: 1) a very different pitch range for the top and bottom sides of the package, which presents serious difficulties in aligning the contact at the same time; 2) picking and placing the package in a double-sided probing design within the precision alignment requirement; 3) controlling thermal expansion at different testing temperature points to reduce the thermal gradient when probing micro-bumps; 4) achieving extremely high-speed 112Gbps test requirements

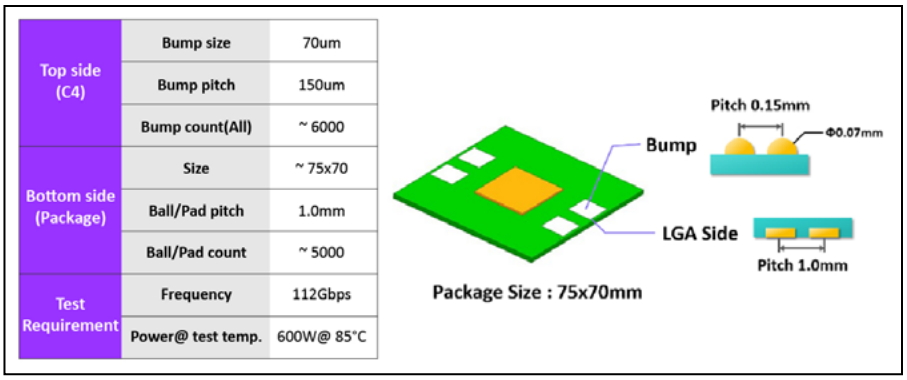

Figure 2: CPO device information.

using a 150µm-pitch wafer-level chip-scale package (WLCSP) probe head—this trend involves testing a wafer-level package at the required speed to distinguish known good dies (KGD); and 5) 600W device power must be dissipated by integrating a 150µm-pitch WLCSP probe head design, in which thermal expansion will lead to unstable contact with the fine-pitch probe.

To summarize from the above challenges: there is a need for a highly-integrated probing system that considers precision alignment and balances thermal and electrical design in a comprehensive thermal chuck design with a 150µm WLCSP probe that provides a stable contact system to handle a 100kg reflected force when testing. To meet these requirements, we propose a test module using an electric loopback interposer and bottom socket, as shown in **Figure 3**.

In the current double-sided probing system, there are four major modules that integrate the whole functionality of CPO testing requirements (**Figure 4**). The four modules are discussed below.

Actuator. The plunger is used in the actuator design to ensure a total 600kg force that can provide a stable contact force to fulfill future trends for large packages. Such packages will need to overcome the total reflected force from the WLCSP probe head and bottom socket. The mechanical strength of the probing system must be considered when applying such high force conditions. It is critical to have a strong structure to reduce micro-vibrations when connecting with the tester and performing thermal control.

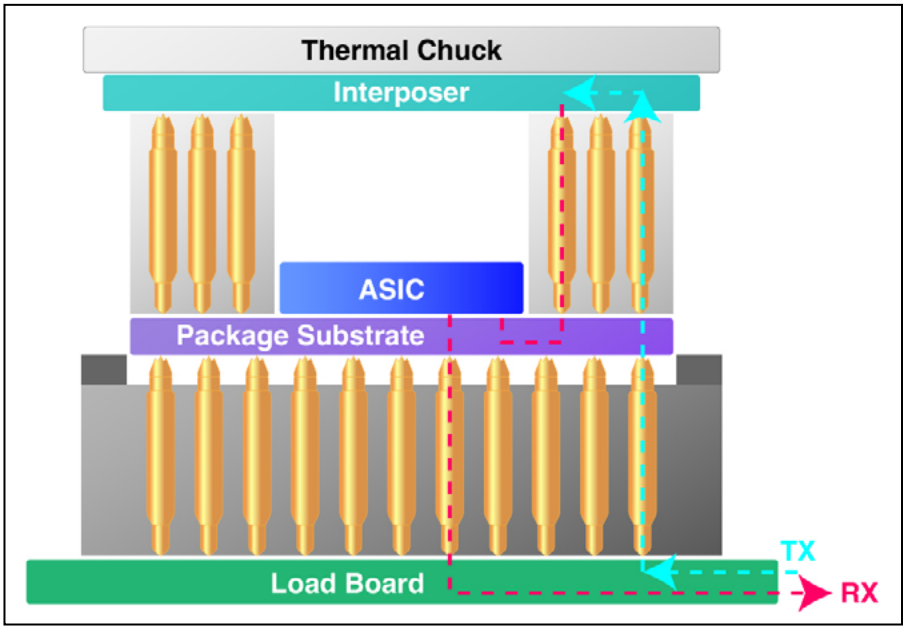

Figure 3: Proposed test module for double-sided probing design.

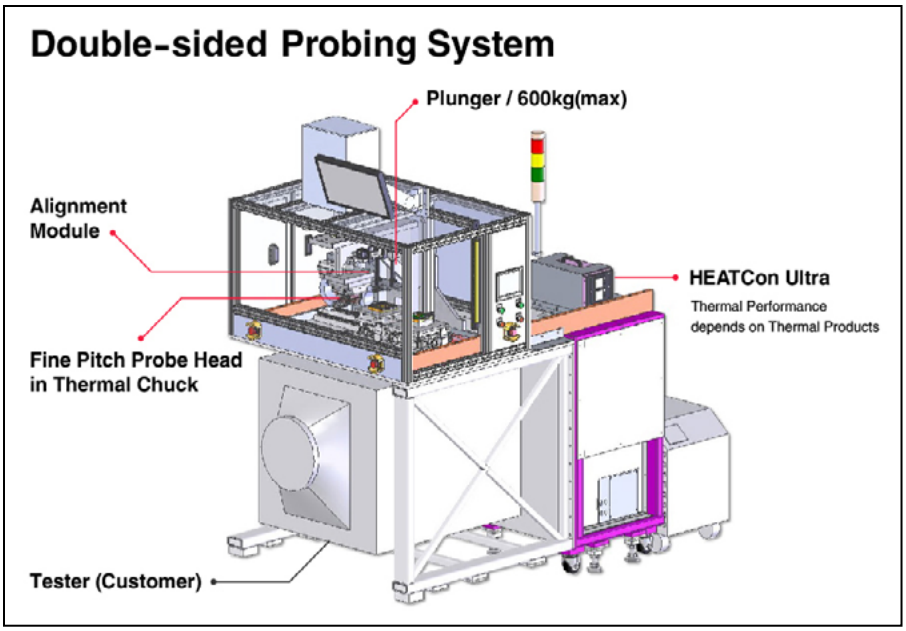

Figure 4: Double-sided probing system.

Alignment. The alignment module is a dual-charge-coupled device (CCD) module combined with a 3-axis X-Y-Θ heating shuttle design to ensure precise alignment when the temperature varies. High-resolution dual-CCD cameras are used to take a picture of the micro-bump on the top side of the package to align every package to the accurate position before picking up the device under test (DUT). Moreover, the heating shuttle plate can reduce the soaking time before reaching thermal equilibrium at the required testing temperature; it also plays an important role in auto calibration before each pick and place action on the package. Because the DUT and probe head are not on the same side, one issue is aligning the tip of the probe head with the micro-bump on the DUT.

We used a dummy device to transfer printing of the probe mark of the probe head tip and perform self-calibration by computing the relative distance to ensure the proper alignment of the probe tips to the device micro-bumps. However, thermal expansion at high temperatures will cause the alignment to be further from the original position by approximately 90µm from what it was at the initial temperature, as shown in **Figure 5**. A multiple stacked structure design that uses different materials causes nonlinear thermal expansion. It has also been proven that the trace of a temperature-dependent probe mark is repeatable. The displacement around 90µm from the initial location at 25ºC to the high temperature of 105ºC is even greater than the diameter of the size of the micro-bump at approximately 70µm, which easily causes contact instability. In consideration of the thermal expansion effect, two separate double-sided probe heads were designed so they could be adjusted to accurate positions by use of fiducial markers and precision guide pins during assembly. However, this design still requires optical re-alignment to check the precision of the final position at each testing temperature point to ensure contact stability and repeatability.

Probe head/thermal control. The high-speed and fine-pitch probe head integrated with a high-performance thermal control system is the most critical design module of the double-sided probing system. To reach the requirement for 112Gbps for the pulse amplitude modulation 4 signal (PAM4), every step in the design of the probe head must be carefully checked by simulation. Channel simulation results, including that for package substrate, fine-pitch probe head, and the loopback interposer, show the behavior of insertion, return loss, and the impedance curve (**Figure 6**).

The targeted impedance value is 93Ω, so closely achieving the values and reducing the impedance mismatch must be considered for each component. Based on the simulation results, the high-speed requirement for 112Gbps PAM4 after integration with whole channel simulation was achieved. Moreover, to prove the

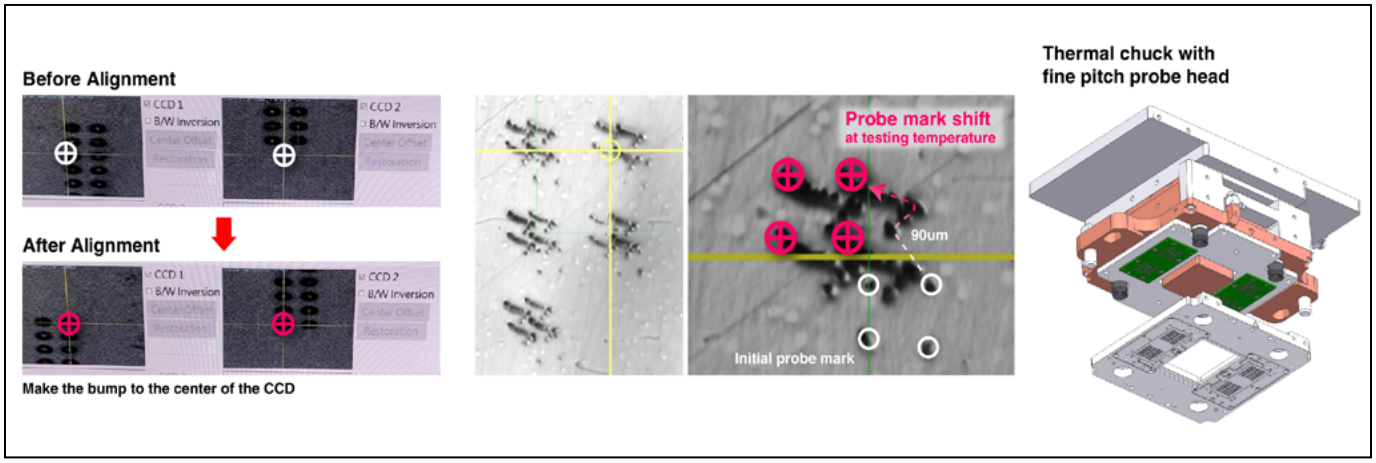

Figure 5: Optical alignment changes with thermal expansion.

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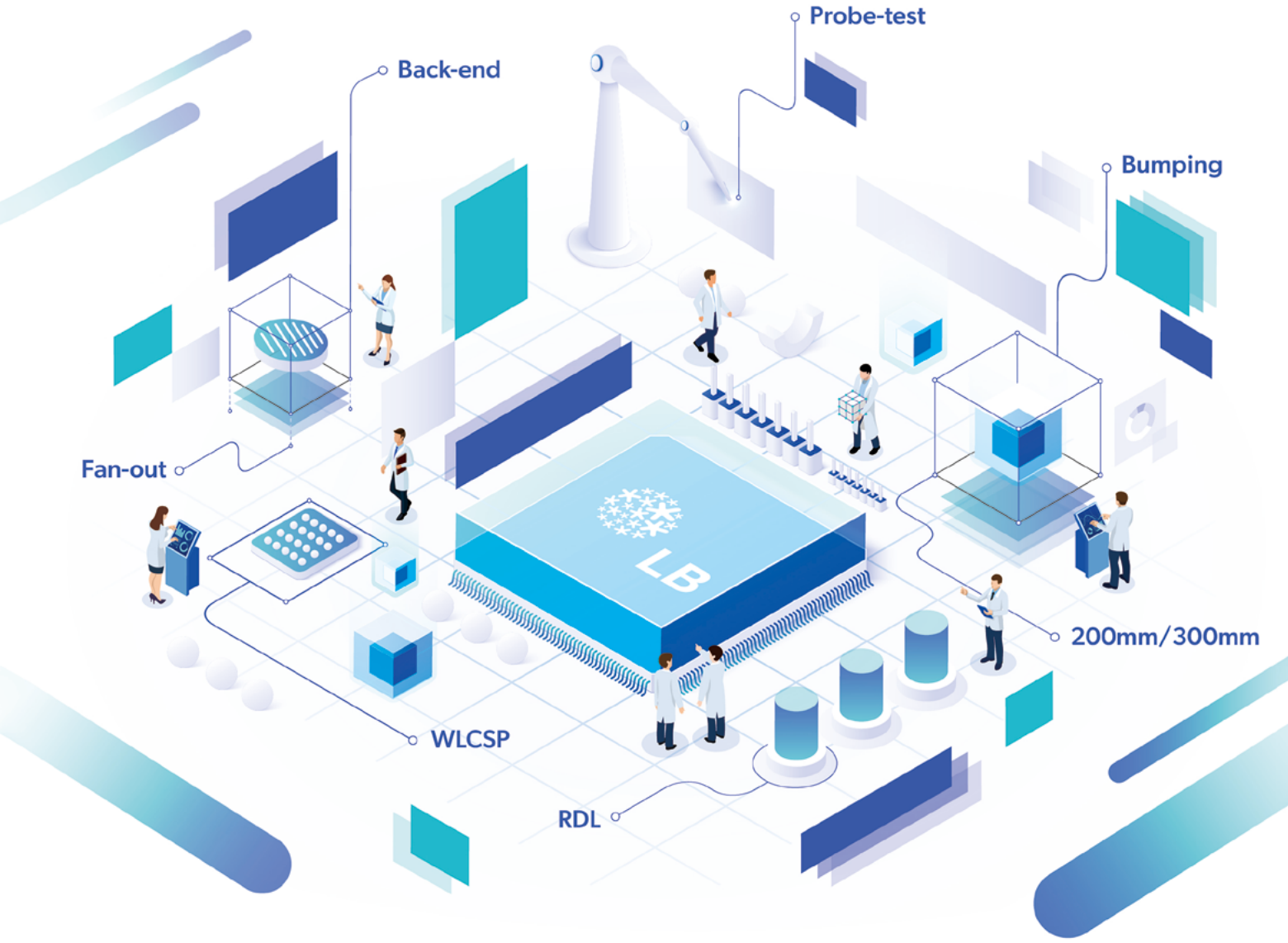

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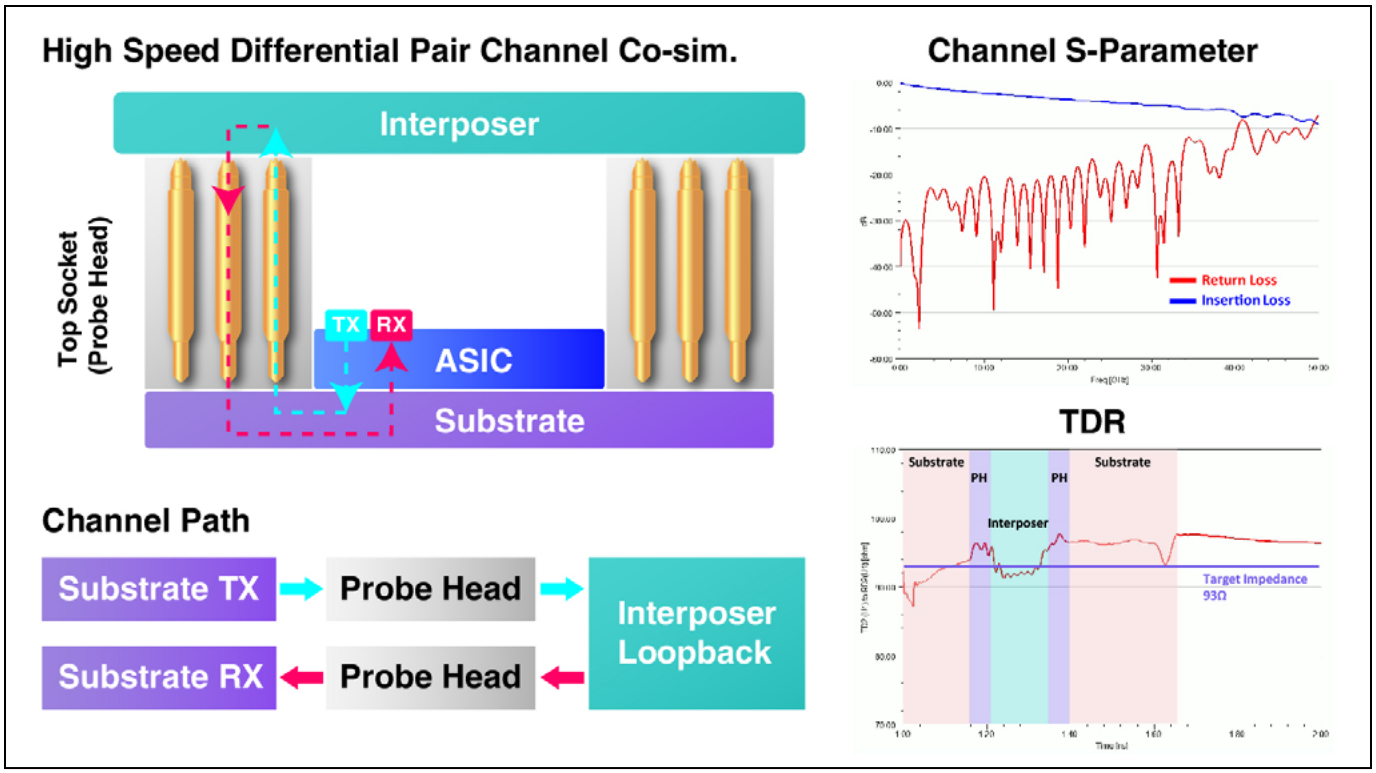

Figure 6: 112Gbps PAM4 signal loopback design in a 150µm-probe head.

simulation result at the boundary condition, we used a simplified test jig in our lab environment with a four-probe double-sided probe station and a 110GHz performance network analyzer (PNA), the results of which show good correlation of insertion loss between simulation and measurement up to 85GHz (**Figure 7**). The simulation boundary condition is also proven to be a reasonable setting for such a high bandwidth.

To align with customers' thermal test requirements, we designed the water heatsink channel and performed thermal simulation, from which we obtained the expected results. After achieving satisfactory thermal performance, a prototype thermal head was manufactured to conduct the lab test and compare the difference between the simulation and actual measurement (**Figure 8**), which is a procedure similar to electrical verification and that internally proves the capability of our product. Another checkpoint of thermal simulation is to achieve thermal distribution, which will affect the fine-pitch probing stability. Distinct material selection and structural design lead to dramatic differences in thermal expansion.

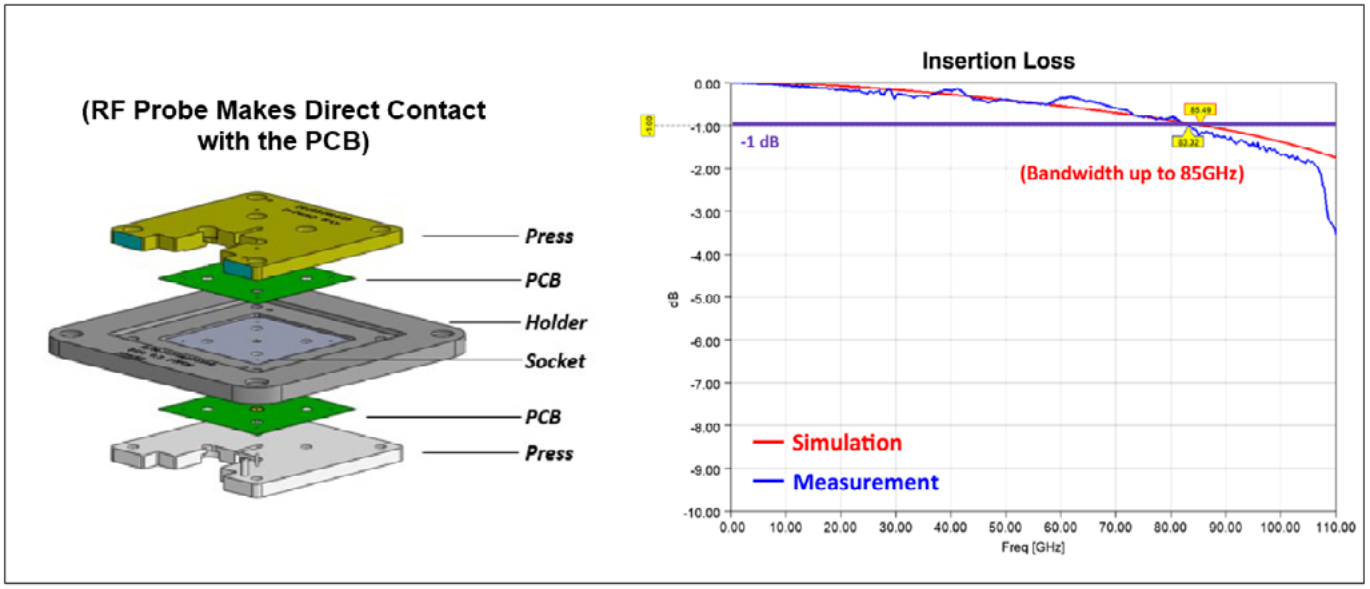

Figure 7: Electrical correlation of test fixture by 110GHz PNA .

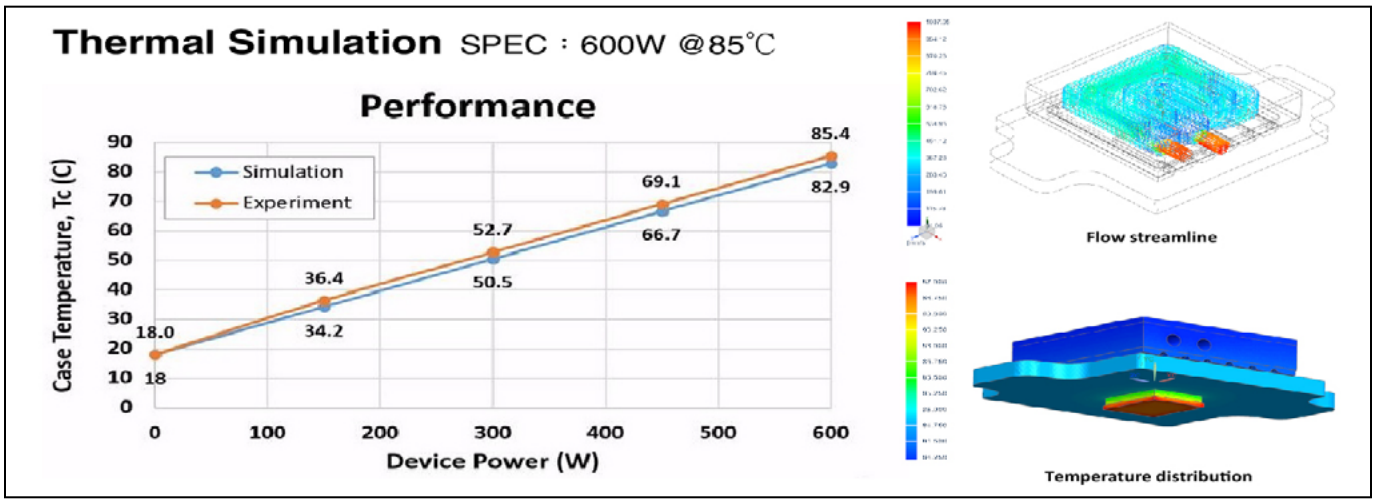

Figure 8: Thermal performance verification of HEATCon Ultra.

Summary

A double-sided probing system for 150µm-pitch CPO comprehensively integrates multiple fields, including automation for high-precision optical alignment, a 112Gbps design for a fine-pitch probe head, and a high-performance stacked thermal chuck with a double-sided probe head. Customers have used this double-sided probing system to test actual devices and the devices passed both room-temperature and high-temperature requirements. These results also support the feasibility of this test solution for the most advanced 2.5D and 3D packaged devices.

Reference

1. V. Martin, M. Pars, E. Mounier, "Co-packaged optics," https://www.yolegroup.com/product/report/co-packaged-optics-2022---focus-data-centers/#

Biography

Collins Sun is a R&D director at WinWay Technology, Taiwan. He has responsibilities in various technical fields, such as material science, high-speed product development, and thermal solutions. He received a PhD in Physics from National Sun Yat-Sen U., Taiwan. Email: collins.sun@winwayglobal.com


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High-performance computing applications drive reliability of high-density fan-out packaging

By Laurene Yip, Rosa Lin, Charles Lai, Cooper Peng [MediaTek Inc.]

The continuous drive for higher compute power and greater data bandwidth to meet the growing demands from data centers, networking, and artificial intelligence (AI), has driven the development of advanced packaging solutions for higher performance devices. Because single advanced node system on a chip (SoC) can no longer meet the increasing demands of high-performance computing (HPC) applications, there is a growing trend to use a chiplet architecture approach to split a large, monolithic die into multiple smaller functional blocks, called chiplets, and reintegrating the chiplet dies using advanced packaging. Chiplet architecture not only can bring the different functional blocks closer to each other to improve device performance, but also can improve individual die yields and help reduce the overall device cost [1-6].

Among the advanced packaging technologies, wafer-level fan-out has emerged as an attractive package solution for heterogeneous integration. Wafer-level fan-out, which uses fine-pitch redistribution layer (RDL) technology for die interconnection, can enable the development of high-performance products with large package footprint, and high interconnect density. Although silicon interposers had been widely used in the past for high-end server products, silicon interposers that utilize through-silicon via (TSV) technology have high manufacturing cost. Wafer-level fan-out with fine-pitch RDL is emerging as a lower cost alternative package solution.

Package reliability, however, is becoming a critical concern as the overall die size and package size increase to accommodate the integration of more chiplets for networking and high-performance applications. As the die size increases, the package stress also increases because of the coefficient of thermal expansion (CTE) mismatch between the die and the substrate and also increases the risk for package failures caused by bump cracks, mold compound delamination, and RDL failures in the fan-out package.

Our study assessed the reliability of large-format fan-out packages assembled with an application-specific integrated circuit (ASIC) die and 8 I/O chiplets using the chip-first approach. The package robustness was investigated using stringent component-level reliability testing, which included temperature cycling (TC), an unbiased highly-accelerated temperature stress test (uHAST), and a high-temperature storage (HTS) test.

Package description

In our study, multi-chip fan-out packages with an integrated fan-out die size of 1.6X reticle size were evaluated. The fan-out package integrated the ASIC die and 8 I/O chiplets with three layers of RDL interconnections. The fan-out die module was 41 X 33mm^2 and was assembled on low-loss organic substrates with sizes 74 X 74mm^2 and 91 X 91mm^2 as shown in **Figure 1**. Both packages used a copper stiffener ring for warpage control. The key attributes of the test vehicles are summarized in **Table 1**. The fan-out module was built using a process where the different dies were attached to a temporary carrier and molded with epoxy mold compound to form a reconstituted wafer. After molding, the multi-layer RDL lines and C4 bumps were formed to create the fan-out die

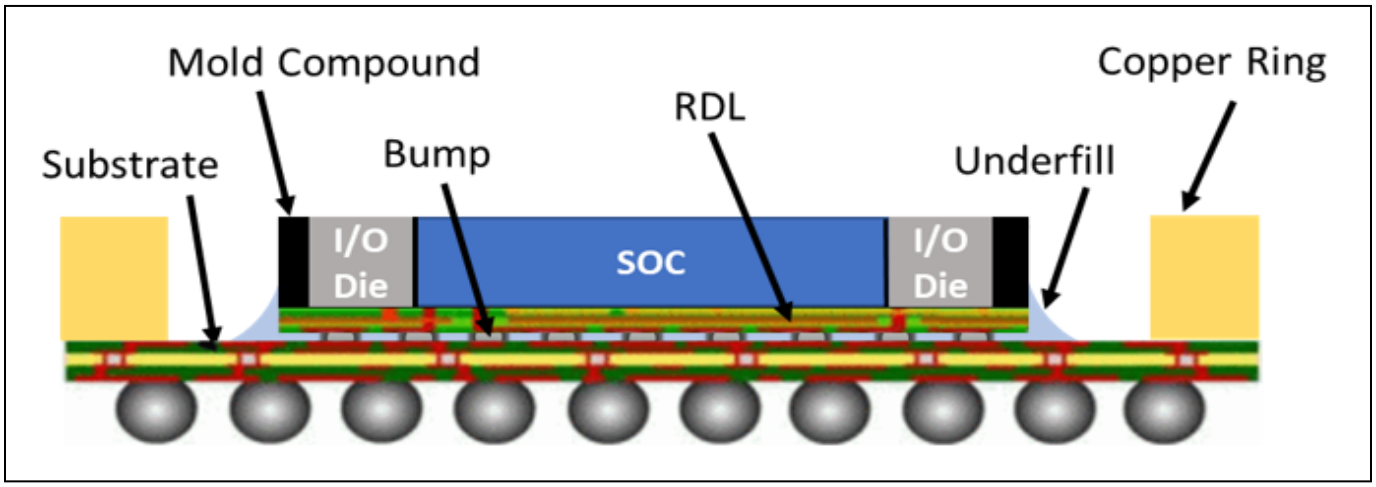

Figure 1: Cross section of a fan-out package.

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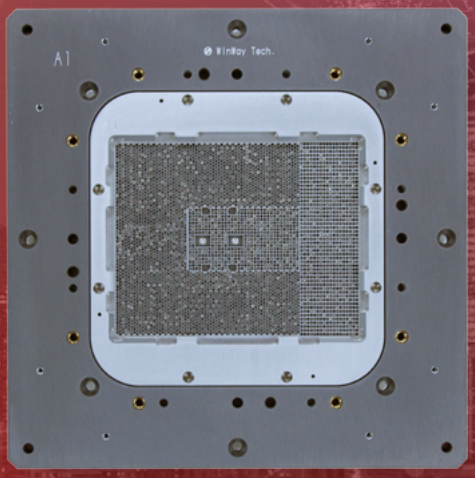
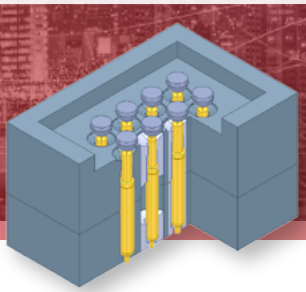
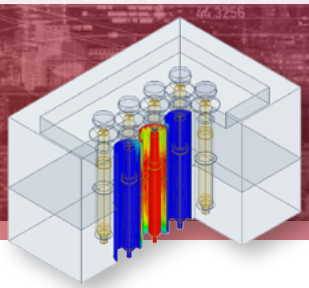


Bandwidth up to 112Gbps

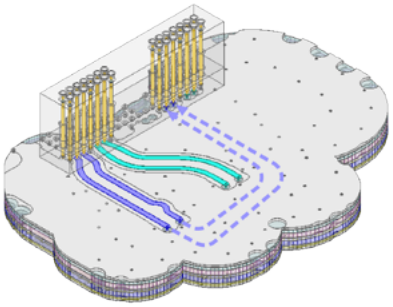


Co-grounding Design



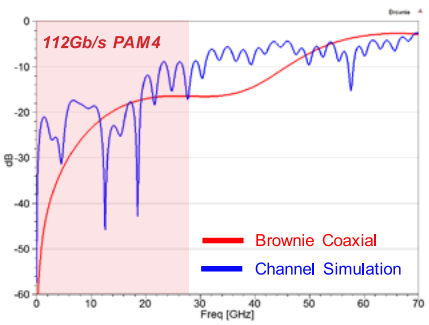
EM Wave

3D Stacking Simulation

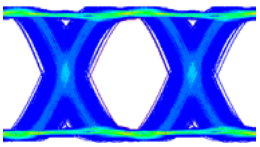
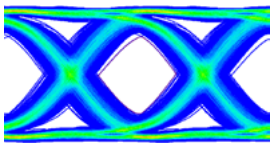
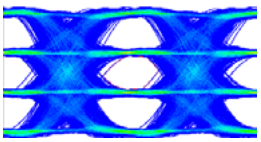
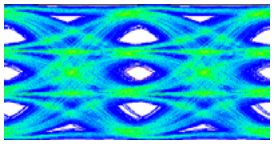


For high speed test application, it's necessary to evaluate the performance of the entire channel at engineering stage to ensure the specifications can be reasonably defined during testing.

Return Loss



Eye Diagram

	Socket Only	Channel Simulation
56Gb/s NRZ		
112Gb/s PAM4		

Solution	Bandwidth	Crosstalk	Impedance (50Ω)
Plastic Socket	<20 GHz	-10 ~ -25 dB	△>10 %
Coaxial Socket	>80 GHz	-50 ~ -70 dB	△3 ~ 5 %

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Attribute	TV1	TV2
Fan-out Module Size (mm^2)	41.3 x 33.6	41.3 x 33.6
Die Size (mm^2)	SoC: 31.5 x 23.8 I/O die: 15.5 x 4	SoC: 31.5 x 23.8 I/O die: 15.5 x 4
Substrate Size (mm^2)	74 x 74	91 x 91
Core Thickness (mm)	1.4	1.4
Ring Thickness (mm)	2.5	2.5
Ring Foot Width (mm)	13/10	17/19

Table 1: Package attributes.

structure (**Figure 2**). Because the different dies were directly connected to the RDL through the copper vias, the fan-out structure does not require the use of micro bumps or underfill between the die and the RDL layers.

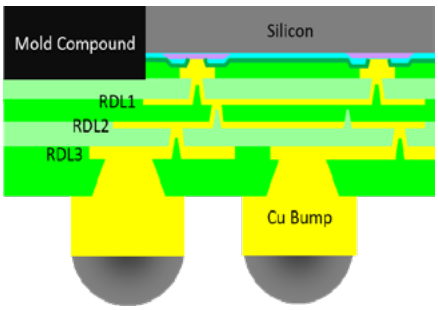


Figure 2: Cross section of an RDL structure.

The fan-out package and floor plan are shown in **Figure 3**. In the package, the SoC was connected to 8 identical I/O dies with three RDL layers with line width and spacing of 2/2µm for the first two layers and 5/5µm for the third layer. After building the fan-out module, the integrated die was attached to an organic substrate using 130µm pitch copper pillar bumps. The key attributes for the fan-out module are shown in **Table 2**.

Attribute	Dimension
Fan-out Module Size (mm^2)	41.3 x 33.6
Die Size (mm^2)	SoC: 31.5 x 23.8 I/O die: 15.5 x 4
D2D Gap (µm)	60
RDL Layer Count	3X
RDL W/S (µm)	RDL1: 2/2 RDL2: 2/2 RDL3: 5/5
C4 bump Pitch (µm)	130

Table 2: Fan-out module attributes.

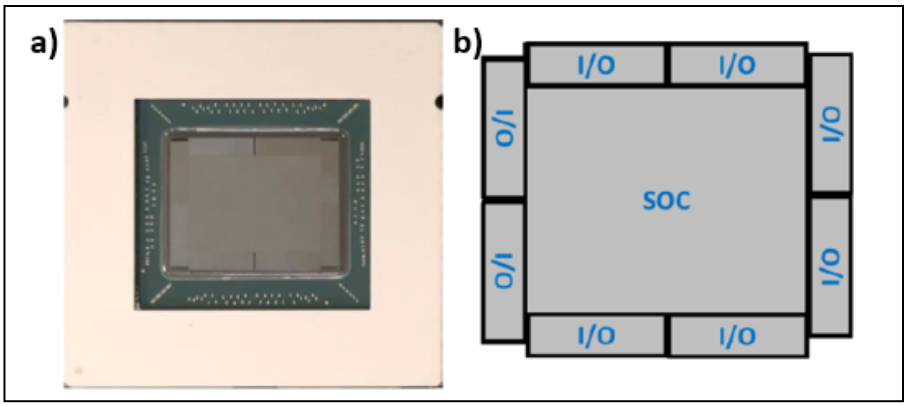


Figure 3: a) Fan-out package assembled on a 91 X 91mm^2 substrate with a stiffener ring; b) Fan-out module floor plan.

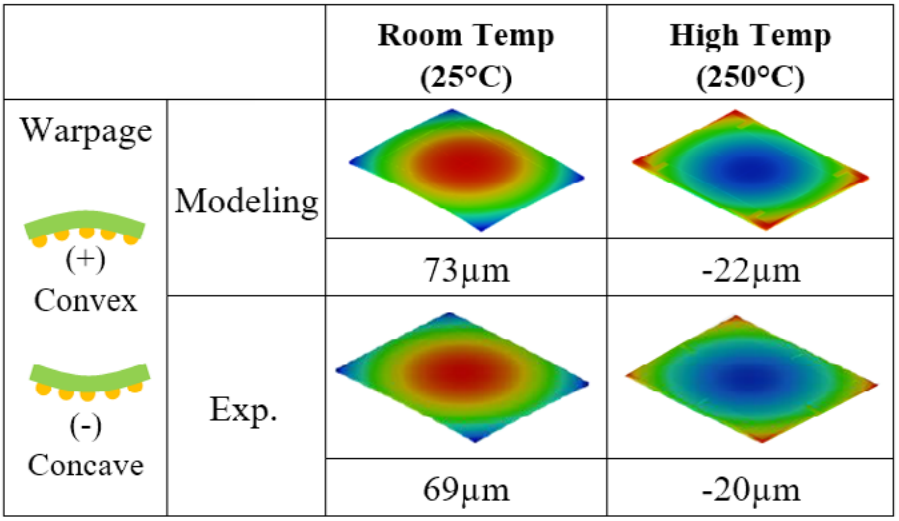


Figure 4: Fan-out module warpage contour plots.

Results and discussion

The following sections discuss the following assessments: package warpage, C4 bump reliability, and RDL reliability.

Package warpage assessment. Because warpage will affect solder joint quality, shadow moiré was performed to characterize warpage variations over temperature of the fan-out module. The samples were measured from room temperature up to 250°C to simulate the solder joint reflow temperature – and then down to room temperature. The simulated fan-out module warpage values closely matched the experimental data as shown in **Figure 4**. The fan-out module had a 69µm convex warpage shape at room temperature, but changed to a -20µm concave shape at 250°C. X-ray analysis showed the C4 bumps have good solder joint formation (**Figure 5**).

The assembled package warpage is shown in **Figure 6**. Both TV1 and TV2 had a convex warpage shape at room temperature, but turned to a concave shape at 250°C. The 91X91mm^2 package had 30% higher warpage at

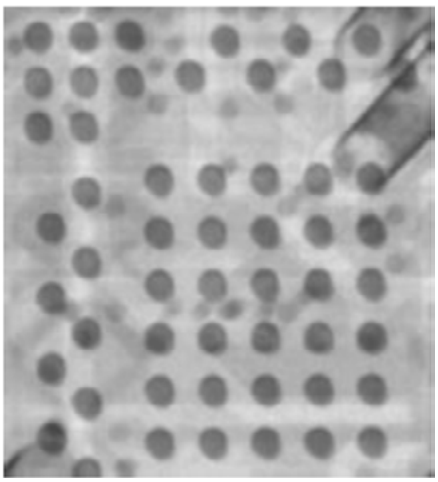


Figure 5: X-ray of C4 joints near the die corner.

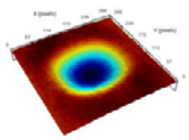
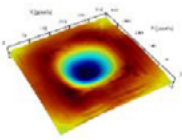
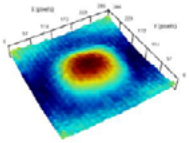
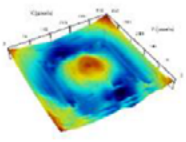
Test Vehicle		TV1	TV2
Package Size (mm^2)		74 X 74	91 X 91
Warpage @ 25°C (+)	Exp.		
		1x	1.3X
Warpage @ 250°C (-)	Exp.		
		1x	1.6X

Figure 6: Package warpage contour plots.

room temperature than the 74X74 mm^2 package. At 250°C, the 91X91mm^2 package warpage was 60% higher compared to the 74X74mm^2 package.

C4 bump reliability assessment. Temperature cycling accelerates the thermo-mechanical failures caused by CTE mismatch. C4 bump joint crack risk increases as the fan-out module size increases. Finite element analysis (FEA) showed the bumps at the die corner experience the highest stress and are at the greatest risk for cracking as shown in **Figure 7**. Both fan-out package test vehicles passed temperature cycling testing without any C4 bump failures.

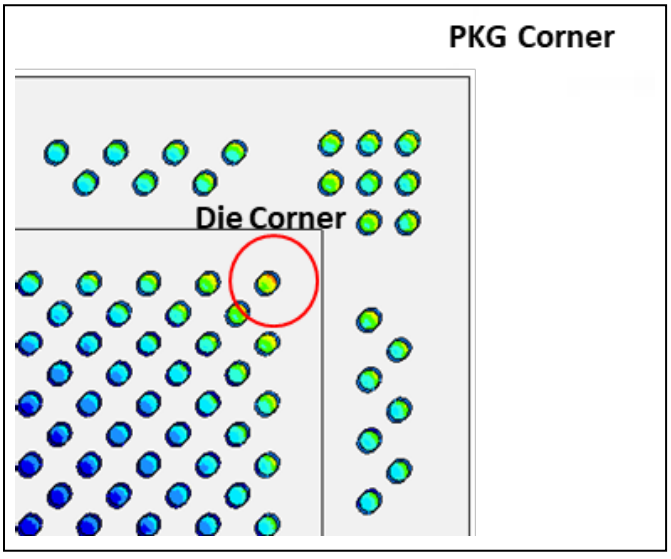


Figure 7: Copper pillar bump at the die corner.

RDL trace reliability assessment. The CTE differences between the dielectric materials and copper lines in the RDL structure cause copper/dielectric interface distortion during temperature cycling that can result in RDL trace cracking. **Figure 8** shows the die-to-die (D2D) routing areas where the high-density RDL lines interconnect the dies. Stress analysis showed the RDL traces between the gap of the dies experience

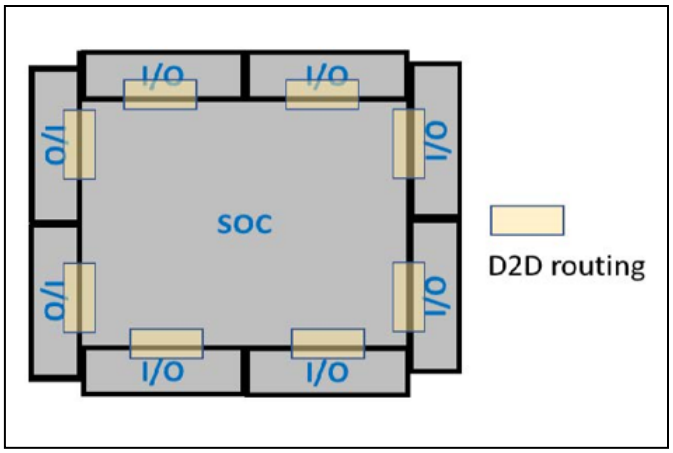


Figure 8: D2D RDL routing areas.

high stress due to the low CTE and high modulus of the silicon die constraining the thermal expansion and shrinkage of the copper lines [7]. The smaller the gap, the more the RDL line is constrained by the silicon die and the higher the stress in the copper line, which increases the RDL trace crack risk.

After TV1 and TV2 underwent multi-reflow testing at 250°C, package failures were observed to have trace cracking in the RDL lines. The trace cracks were typically observed in the RDL2 lines underneath the main SoC near the die edge. The trace cracks were mainly found on the isolated lines near the tear drop turning point as shown in **Figure 9**. A cross section of the RDL trace crack is shown in **Figure 10**. No trace cracks were found in the dense RDL metal line areas.

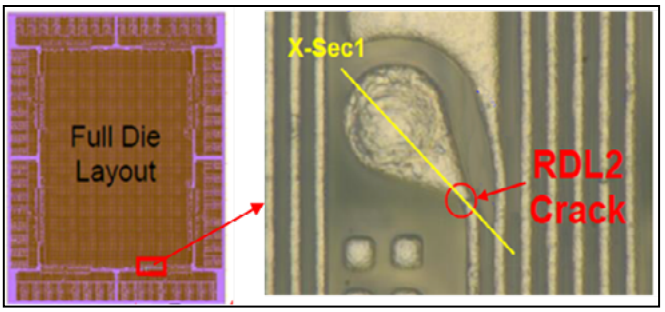


Figure 9: An RDL trace crack.

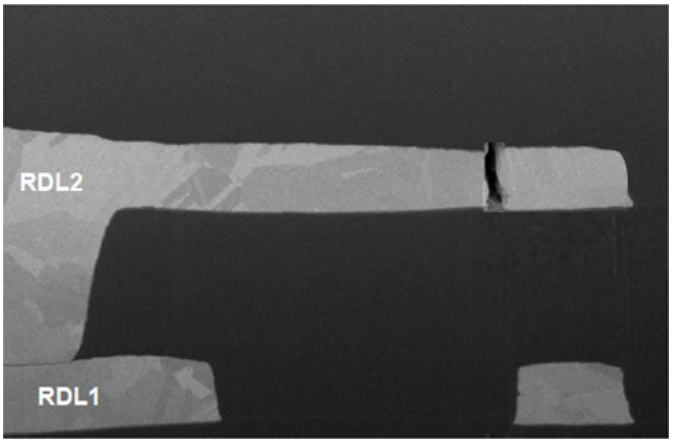


Figure 10: Cross section of the RDL trace crack.

In our study, FEA was used to investigate the risk for RDL cracking based on different trace dimensions and geometries such as trace width, trace thickness, trace length from via to turning point, and trace angle as shown in

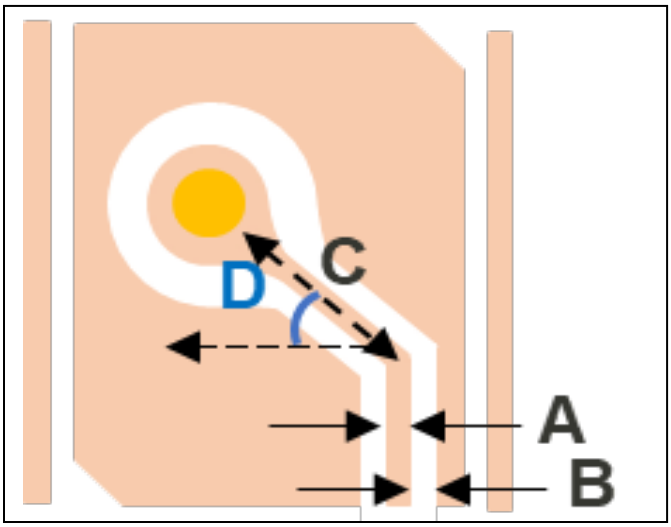


Figure 11: RDL trace geometry: A is the trace width, B is the trace space, C is the trace length from via to turning point, and D is the trace angle.

Figure 11. The simulation results of different trace widths and thicknesses are shown in Table 3. An increase in RDL trace width or thickness reduces the risk for trace cracking. Increasing the trace width by 10% and thickness by 15%

Attribute	Leg 1	Leg 2	Leg 3	Leg 4
RDL Width (µm)	2	2	1.5	2.2
RDL Thickness (µm)	2	1.5	1.5	2.3
Stress Contour @ RDL Teardrop Area				
Normalized Stress	1.00X	1.14X	1.25X	0.85X

Table 3: Line dimension effect on RDL crack risk.

resulted in a 15% reduction in the trace stress. Optimizing the trace design can also reduce the RDL crack risk. FEA showed the bends in the traces are areas with high stress concentration. The simulation results showing the effect of different RDL lengths from the via to turning point and different teardrop angles are shown in Table 4. The results showed increasing the trace distance from the via to the turning point from 12µm to 18µm had a 57% reduction in trace stress.

After optimizing the RDL design by increasing the minimum trace width to 2.2µm and the trace thickness

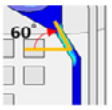
Attribute	Leg 5	Leg 6	Leg 7
RDL Width (µm)	2	2	2
RDL Thickness (µm)	2	2	2
Length from Via to turning Point (µm)	12	18	20
Tear Drop Angle	45°	45°	60°
Stress Contour @ RDL Teardrop Area			
Normalized Stress	1.00X	0.43X	0.47X

Table 4: Trace geometry effect on RDL crack risk.

to 2.3µm and optimizing the pattern to increase the line length from via to the turning point to greater than 18µm, both packages successfully passed the multi-reflow tests. Figure 12 shows an example of the RDL trace design before and after trace optimization.

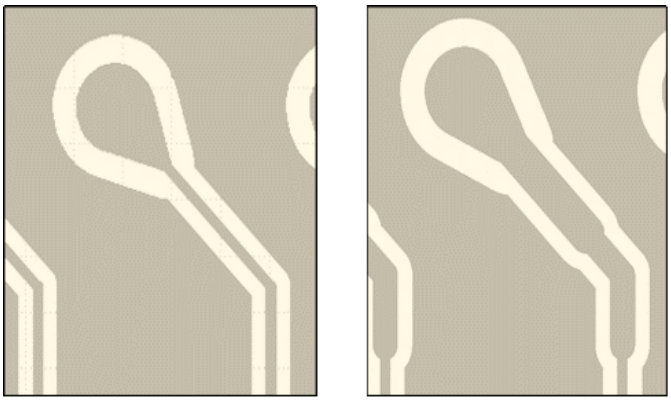


Figure 12: RDL layout a) before and b) after trace optimization.

Reliability Test	Test Conditions	TV1	TV2
Multi-reflow (250°C)	6x	Passed	Passed
Component Level Test	MSL4	Passed	Passed
	uHAST 264 hrs (110°C/85%RH)	Passed	Passed
	TCG 850 cycles (-40 to 125°C)	Passed	Passed
	HTS 1000 hrs (150°C)	Passed	Passed

Table 5: Reliability test results.

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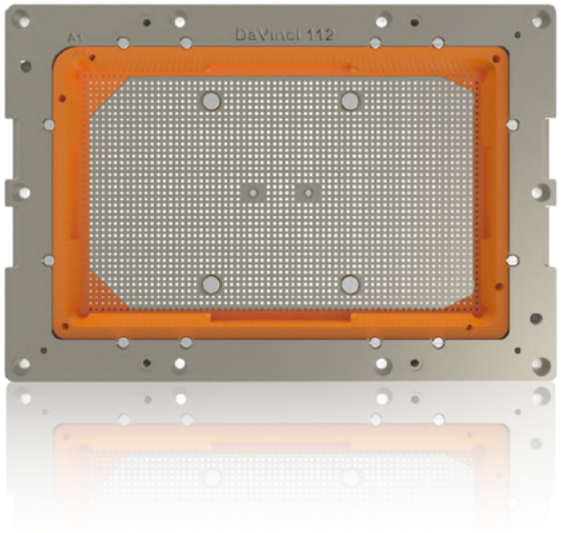

- Controlled impedance interface
- Protection against solder build-up and longer probe life thanks to homogeneous alloy spring probe technology
- Optimized ground connection to reduce crosstalk during testing
- Unrivalled mechanical strength thanks to patented insulated metal housing
- Designed for large ASIC device footprints

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Reliability performance. After optimizing the RDL design, the fan-out packages were subjected to the standard JEDEC reliability tests including moisture soaking level 4 (MSL4) as preconditioning, temperature cycling test (TCT) with -40°C to 125°C (condition G), uHAST with 110°C/85%RH, and high-temperature storage test (HTS) at 150°C. Both packages passed 6X multi-reflow and the reliability tests without any failures as shown in **Table 5**. After reliability testing, failure analysis was performed to check the integrity of the C4 joints and fine-line patterns in the RDL layers. Cross-sectional analysis of the units showed no bump cracks or trace cracks (**Figures 13** and **14**).

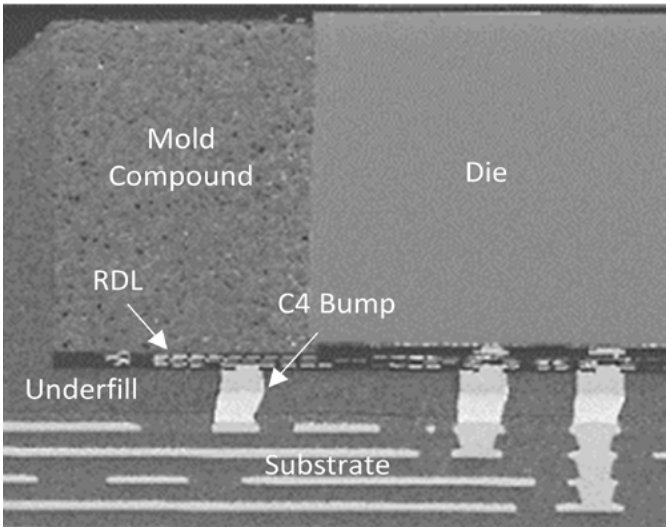

Figure 13: Cross section showing good copper pillar C4 joint integrity.

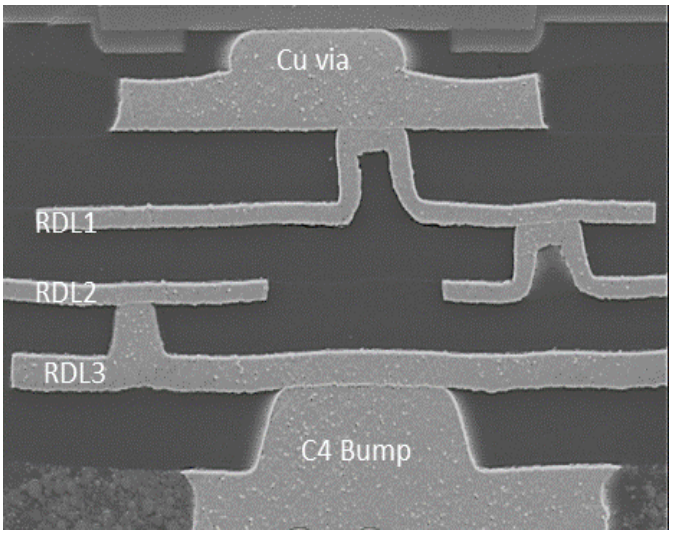

Figure 14: Cross section of the RDL structure.

Summary

The reliability of large multi-chip fan-out packages was evaluated using the multi-reflow and component-level stress tests. Our study showed that package stresses from thermal loading could cause RDL cracking in the metal traces interconnecting the dies. The RDL trace locations near the gap between the SoC and I/O die are high stress concentration areas. RDL trace design and geometric dimensions are critical to interconnect reliability. Thicker and/or wider traces reduce the risk for RDL cracking. Increasing the distance between the trace via and the turning point in the line also reduces the RDL crack risk. By optimizing the RDL design and trace dimensions, RDL stress effects can be minimized enabling large-format fan-out packages to pass the standard JEDEC reliability tests.

Acknowledgments

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References

1. Y. H. Lin, et al., "Multilayer RDL interposer for heterogeneous device and module integration," IEEE 69th Electronic Components and Technology Conference (ECTC), 2019, pp. 931-936.
2. Y. P. Chiang, et al., "InFO_oS (Integrated Fan-Out on Substrate) technology for advanced chiplet integration," IEEE 71st ECTC (2021), pp. 1-6.
3. G. J. Scott, et al., "Heterogeneous integration using organic interposer technology," IEEE 70th ECTC (2020), pp. 885-892.
4. S. Y. Hou, et al., "Wafer-level integration of an advanced logic-memory system through the second-generation CoWoS technology," IEEE Trans. Electron Devices, vol. 64, no. 10, pp. 4071–4077.
5. D. C. H. Yu, "Advanced packaging with greater simplicity," 2017 IEEE International Electron Devices Meeting (IEDM), IEEE Press, Dec. 2017, pp. 3.6.1-3.6.4.
6. C. Wang, et al., "Signal integrity of submicron InFO heterogeneous integration for high-performance computing applications," IEEE 69th ECTC (2019), Las Vegas, NV, USA, pp. 688-694.
7. T. C. Wang, et al., "RDL layout pattern reliability analysis and optimization with TCAD stress modeling," IEEE Inter. Interconnect Tech. Conf. (IITC), 2017, pp. 1-3.

Biographies

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Rosa Lin is a Technical Manager at MediaTek Inc., Hsinchu, Taiwan, with more than 10 years' advanced packaging experience. She has deep understanding of material characterizations, and processes and reliability of 2D, 2.5D and 3D packaging. By focusing on new development and applications, she also obtained over 10 patents and publications related to advanced packaging technology.

Device validation: the ultimate test frontier

By Dave Armstrong [Advantest America, Inc.]

In the early days of space exploration, spacecraft were manned by small teams of one to three astronauts. Notably, most of these astronauts were experienced test pilots who intimately understood the vehicle they were flying and the interaction between all the variables controlling the craft. Similarly, early integrated circuits (ICs) were created by small teams of engineers, who often designed, laid out, and even developed tests for their devices. Notably, the tests were most often functional, and the test interfaces were often analog. Over the years, ICs have become much more complicated, and team size and group effort have grown exponentially. Given the resource and cost constraints, it's rapidly becoming clear that the fundamental limitation to continued industry growth is no longer gate length, but team size and strength.

Contending with unconstrained growth in test data volume, as well as effort, requires a vision for taming this growth in the not too distant future. That vision must focus on intelligent application of new innovations in pre-silicon validation, first-silicon "bring-up," post-silicon validation (PSV), software-driven functional test, and production test. The challenge, paraphrasing *Star Trek*, is to boldly go where no test solution has gone before.

The first half of this paper describes how the industry has developed four different validation and test methods and how their values and focus have shifted over time. This exercise pinpoints the effort needed as a function of circuit density. The latter half discusses the limited growth of tools and methodologies in the functional testing and PSV area and the skyrocketing growth in the required effort. However, by leveraging some of the best practices of the past – such as standard interfaces, automation, and scalability – we will be able to streamline first silicon "bring-up" moving forward.

Method 1: device validation/ characterization

A small group of product experts performed early device testing and functional validation that typically involved five elements:

1. Instruments connected to primary device inputs and outputs;
2. Instruments to program the device into its various modes of operation and environmental extremes;
3. A tangle of wires to interconnect instruments, the device under test (DUT), and a test-system controller;
4. An intelligent operator (often involving the chip designer) who controlled the setup to pinpoint problems and determine optional operations; and
5. A test controller program typically coded in some proprietary test scripts.

While the picture of a functional validation setup hasn't changed much over the years, the increasing complexity of the devices and relentless time to market (TTM) pressure resulted in a need for multiple setups enabling concurrent engineering. Note that the need for functional device validation does not go away with first customer shipments. The experts will need their test setups when called upon again to help with yield investigations and field returns.

Method 2: functional test at ATE

The first automatic test equipment (ATE) tests were all functional. Some argue that the most valuable ATE-based tests, even today, are functional. These tests on the ATE use a few well understood instruments interconnected through a tightly controlled device under test (DUT) interface to confirm to the extent possible the proper operation of the device in mission mode. Functional tests on ATE are typically analog, measuring parameters such as Vmin and Fmax over temperature extremes. What ATE functional test cannot do is run tests that require attached memory, peripherals, or both. This lack of full-functional test coverage has driven the recent rise in the use of system-level test (SLT), discussed in method 4, below.

Method 3: structural test

As ICs became more digital, scan chains provided a standard way to access the innards of the DUT, and automatic test pattern generators (ATPGs) addressed the tedious pattern-generation challenges. The use of ATPGs was highly successful over the years because of multiple factors:

- It was automatic;
- It provided a testability baseline that defined a minimum acceptable quality level;
- It leveraged a consistent DUT interface that then drove consistent instrument interfaces;
- It worked well in a distributed engineering environment; and
- Enhancements such as pattern compression and homogeneous-core pattern sharing allowed test costs to scale slower than Moore's Law.

As device complexities grew, so did the test data volume needed to traverse the logic and confirm proper logic cell operation. The "International Technology Roadmap for Semiconductors" (ITRS) tracked this ever-increasing data volume, shown in blue in **Figure 1**, which also shows the number of transistors per large logic device [1] in green and announced chips [2] with purple points. The ITRS-calculated [1] flat file test data volume is a conservative indication of the effort needed to support this test generation effort (a 14x increase in the last decade).

A review of **Figure 1** indicates that the structural test generation effort is growing even faster than Moore's Law. As the levels of logic grow deeper and deeper it takes more and more vectors to gain the controllability and observability necessary to effectively test the part, as shown in **Figure 2**, which plots the ratio of the two lines in **Figure 1**.

Many industry participants, including the author, feel that **Figure 2** suggests we are fighting a losing battle with structural test. While introduction of new on-chip fabrics to more efficiently transport structural test data

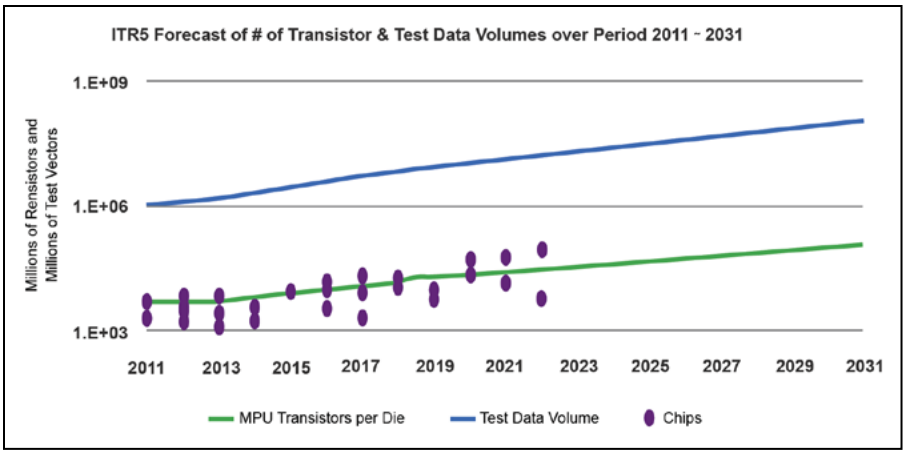

Figure 1: Test-data volumes (blue), transistors per chip (green), and announced chips (purple dots).

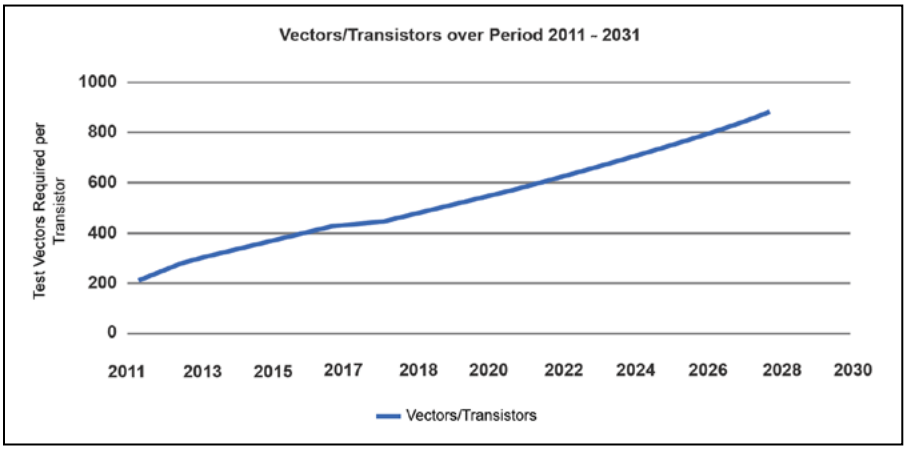

Figure 2: Estimated test vectors per transistor through 2031.

to multiple homogeneous cells will help, it is unlikely to solve this issue. Barring new ideas and approaches, test vectors and the subsequent test times will outpace the growth of the number of transistors in a single chip.

One significant limitation of structural testing, which necessitated the growth of SLT and the continued utilization of functional validation efforts, was the never-ending (or perhaps better stated, ever-growing) list of fault types that structural testing must target. Further compounding this test challenge is the trend toward More-than-Moore multi-die integrations, which bring together multiple devices and exacerbate the testing challenges.

Method 4: system-level test

For years, SLT has provided value by checking that a device can operate in its end-application mode (for example, that it can boot an operating system and run representative end user applications). Because its tests occur later in the flow, it catches more problems at the edge of the various cores and/or devices (that is, interface faults). A clean consistent setup that supports the device while maintaining the visibility needed to catch faults is key to a viable SLT hardware setup.

For devices with on-die processors, recent efforts have graduated beyond running power-up routines to running automatically-generated code sequences, which both utilize and confirm the ability of the embedded processor to sequence through tests while performing their duties. These built-in self-test (BIST)-like sequences can be effective at finding failures both on the die where one or more reprogrammable on-die processors exist, and on peripherals and chiplets in the package, such as high-bandwidth memories (HBM), as well as high-speed and photonic interfaces, which may be connected to the central IC through "no-touch" interfaces such as Universal Chiplet Interconnect Express (UCIe)®.

Four things are apparent when reviewing the path that got us to today:

1. Automatically-generated tests that leverage consistent tool sets provide the most value for the least amount of effort.
2. Clean, consistent hardware setups produce solid results.
3. SLT provides solid value—finding errors not seen elsewhere.
4. Technology does not sit still, and there is no end in sight to the device complexity that will need to be tested.

Test moving into the 21st century

Device validation/characterization, functional test at ATE, structural test, and SLT will continue finding use in the 21st century. But just as *Star Trek* had the next generation, so too, must test. The next generation of test clearly needs to be smarter and leaner. Moving forward, the role of data and artificial intelligence (AI)-driven smart tools (shown in purple in **Figure 3**) will become more pronounced. These capabilities will allow tests to be streamlined and risks reduced.

Another significant change is the prospect for using data from other sources (shown in light blue in **Figure 3**) in order to both focus the tests on areas of concern and adjust the test margins to reduce the risk of shipping a bad part, all while minimizing the cost of test. ATE's instruments and capabilities can contribute in many ways. The newest areas where ATE adds value are listed in items 2, 3, 5, and 6, below:

1. Expanded wafer testing (first view of new wafers).
2. Known-good-die (KGD) test (at-speed and at-temperature testing at the wafer or singulated-die level).
3. Enhanced first-silicon testing (device validation, driver development, and checkout).
4. Final test (at-speed and at-temperature testing after packaging).
5. System-Like-Test™ (Advantest's term for focused system testing on ATE).
6. Post-silicon validation (including parameter/register value optimization).
7. RMA testing (i.e., testing of field returns).

Several key test steps are evolving to offer consistently clean hardware setups, automatic tools, and system-focused test generation.

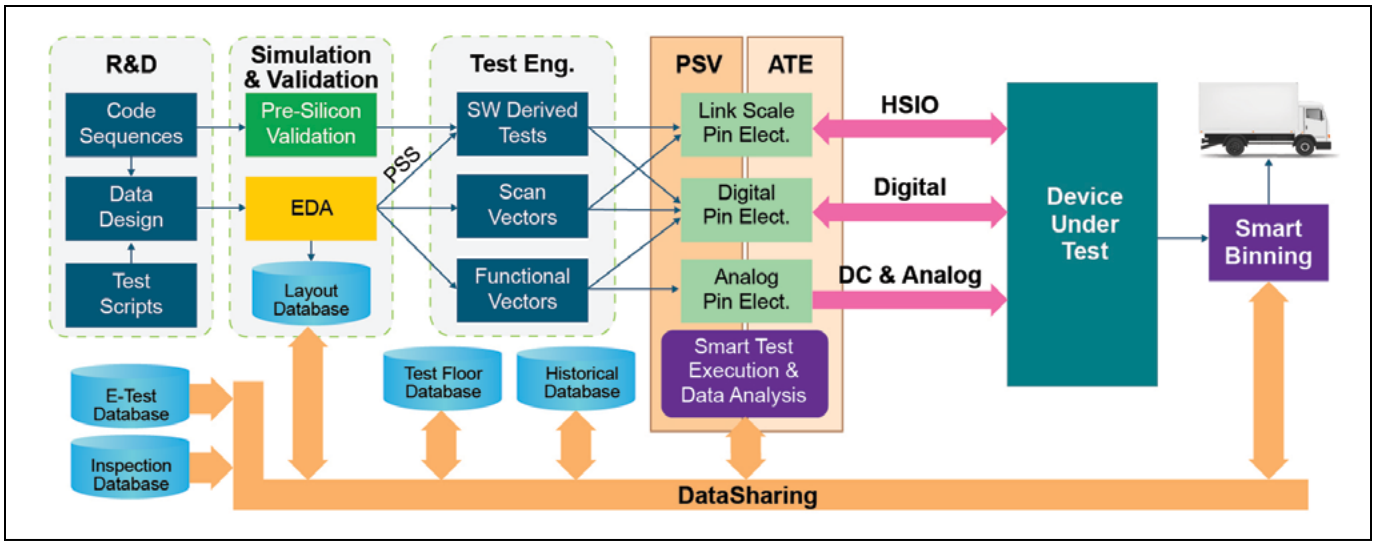

Figure 3: Multiple tools, including PSV and ATE, for device checkout.

Pre-silicon validation

Prior to the arrival of first silicon, design verification involves running test cases in a simulator or emulator at great length. The incredible growth in device complexity has greatly increased the effort and time it takes to verify a design before its tape-out. To increase engineering productivity, test development must be supported by standardized methodologies and tools. The latest standard enabling system-level modeling and test design is the "Portable Test and Stimulus Standard" (PSS). PSS is supported by major electronic design automation tools and significantly increases test quality and shortens time to market (TTM) by improved productivity in design verification.

The value and need for the industry to "shift left" has been explored in other works [3,4]. Just as some test content must shift to wafer-level testing, so too, the preferred path to improve TTM and reduce the likelihood of a re-spin is to shift wafer test content further to the left and expand the validation efforts prior to first-silicon arrival. Accordingly, simulators and emulators must grow in capacity, performance, versatility, and focus. For example, they need to provide estimates for power consumption and performance while executing key software routines and code.

Pre-silicon validation has limitations. For example, abstract, higher-level models (such as virtual prototypes) may not provide an accurate estimate of the power consumption for given code snippets. Even detailed models often are significantly wrong in estimating maximum frequency–-particularly for new process nodes. Optimizing the test content and value of each step in the process is a key challenge in the 21st century.

First-silicon bring-up

While there is real value in running scan-based structural tests, unfortunately, history has shown that these tests are not nearly enough to confirm that a device is truly functional. Leveraging today's multi-week assembly cycles, significant value can be achieved by running some mission-mode functional tests at wafer probe. By migrating functional test content to the wafer level, companies have saved multiple weeks of TTM during their device turn-on phase. One approach toward migrating test content to an earlier phase is to use Advantest's new Link Scale™ digital channel cards for the V93000 platform (**Figure 4**). These new cards enable software-based functional testing using USB or peripheral component interconnect express (PCIe) in addition to scan testing of advanced semiconductors. The new cards address testing challenges that require these interfaces to run in full protocol mode, thereby adding System-Like-Test™ capabilities to the V93000.

Not only does a high-speed interface such as PCIe enable scan over high-speed input/output (HSIO), but it also allows the design team to confirm true functionality deep within the silicon. Tests applied using this approach enable different tests methods that were previously unavailable. Several examples of this functionality are: 1) The loading of large data sets to feed network processors real-world data streams; 2) The loading of multiple sets of control coefficients into a neural network to check performance limits; and 3) The running of R&D test scripts generated in Python, or other types of test scripts, directly in the tester's pin electronics, which allows existing test sequences to be quickly run while keeping the interface consistent and easily understood.

Our new digital channel card solution has proven its value in first-silicon situations by providing a straightforward path for R&D engineers to quickly perform traditional functional test verification steps after the arrival of first silicon. Early verification moves forward the clock for confirming truly good devices, but also to identifying problems and workarounds should they be needed. Perhaps the most important value of this approach is in the resource requirements. The new solution provides a quick and easy path enabling R&D engineers to gain full access to their design, highlighting subtleties that were difficult or impossible to discern using pre-silicon validation techniques. Furthermore, engineers can explore operational corner-cases whose impact was never fully communicated or understood—all within days of first silicon arrival!

Post-silicon validation (PSV)

Because of the limitations of pre-silicon validation, the design engineer is often called upon to tune power and high-frequency performance soon after first silicon arrives. This tuning requires an effective flow to bring up a comprehensive set of PSV tests that support flexible parameterization (for example, varying register settings). Such

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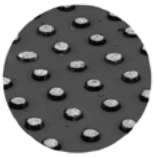
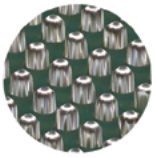

Micro Bump


Flip Chip (c4)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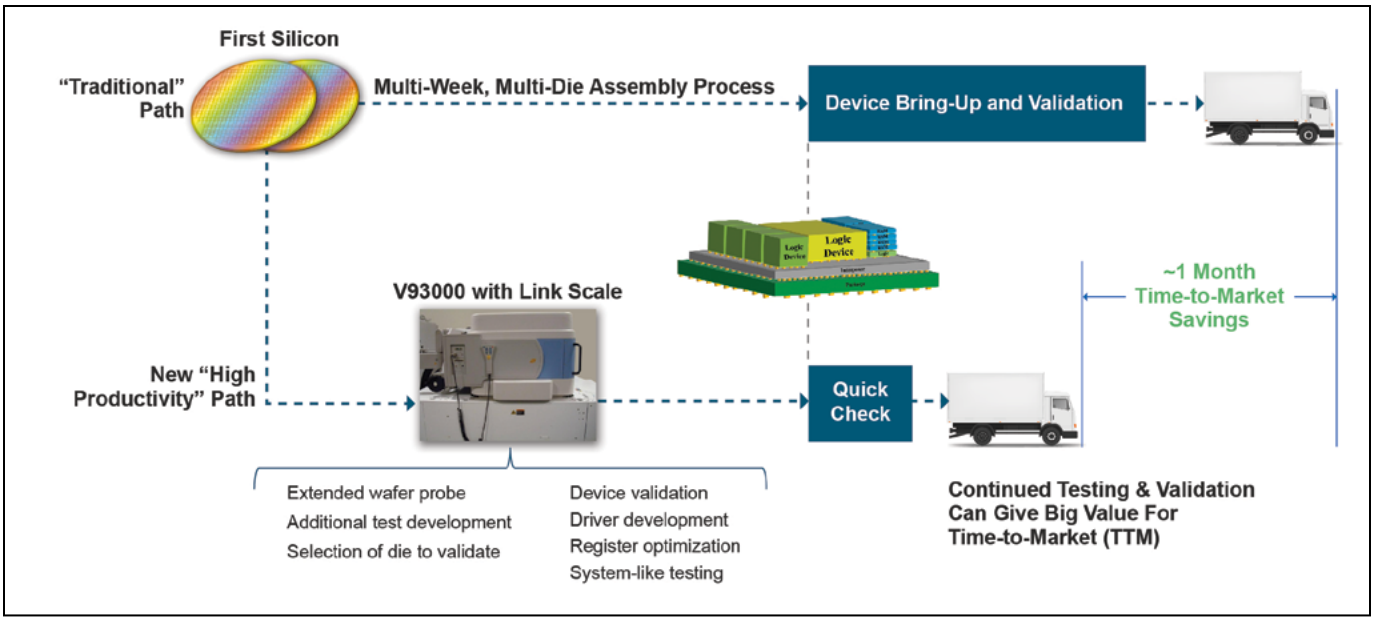

Figure 4: Continuous testing and validation adding TTM value.

tests enable volume data collection and conclusive analytics to provide feedback to the designers, improve pre-silicon models, and eventually tune each chip to its specified power and Fmax performance.

Also, without comprehensive PSV that identifies marginalities, an end product may behave erroneously under particular environmental conditions and loading, which the industry experiences in many ways—for example, as "silent data corruption" in data centers, when devices deliver wrong results under particular circumstances. PSV both confirms the functionality of each design block and optimizes its performance. Several factors are critical to performing PSV efficiently, without requiring hordes of engineers with years of experience:

- A clean and consistent workspace;
- A flexible set of instruments that can test in many different ways;
- Parallel test setups so that concurrent techniques can speed result delivery;
- Re-using test content developed pre-silicon—preferably targeted software-based tests derived from a comprehensive PSS-model of the DUT; and
- Intelligent tools that automatically find marginal test cases and pinpoint the best performance settings on their own.

The introduction of Advantest's EX Test Station provides a new tool to simplify or possibly replace yesteryear's bench setup. This test station provides for a clean and consistent workspace that also happens to be identical to the setup used in production testing on the V93000 ATE. A consistent interface achieves consistent results. The new test station supports both functional and structural test content execution, enabling the PSV engineer to move seamlessly between the two domains to confirm the root cause of incorrect behavior. The addition of structural test capabilities to the bench environment enables the test engineer to step into or over problematic sections of the test to enhance visibility and control.

Another new capability that is valuable in the PSV effort is software-driven functional test, in which software test sequences provide input to the functional test-generation effort (Figure 5). The EX Test Station, together with creative software tools, allows broad ranges of register settings to be explored automatically—over a weekend, for example—in order

Desired Code Sequence to Test

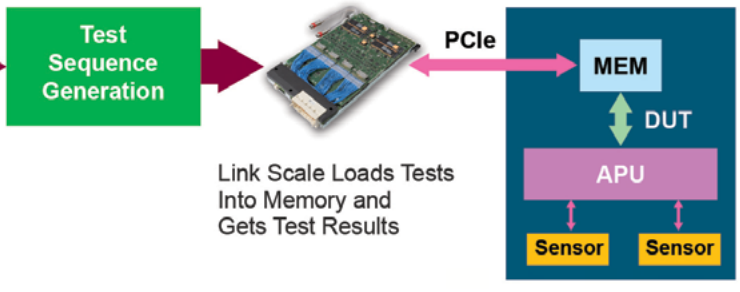

Figure 5: Software-derived tests checking that real-world code works on real-world hardware.

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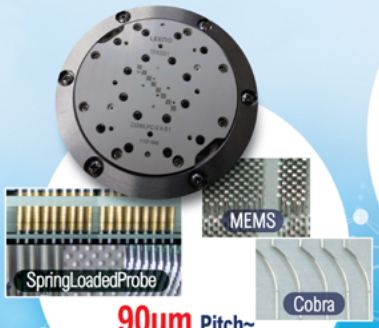
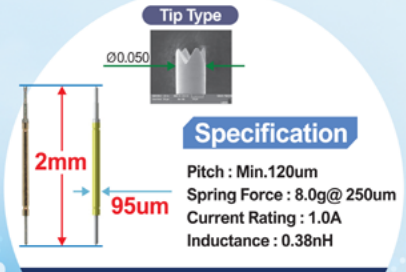


RF Probe for Fine Pitch Probe Head



Specification

Pitch : Min.120um
Spring Force : 8.0g@ 250um
Current Rating : 1.0A
Inductance : 0.38nH

RF Coaxial Spring Probe & Impedance Controlled

0.18mm Pitch~

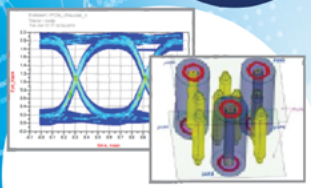
Logic Test Socket

High Speed Automatic Coaxial Probe

Frequency : >20GHz
VSWR : < 1.2

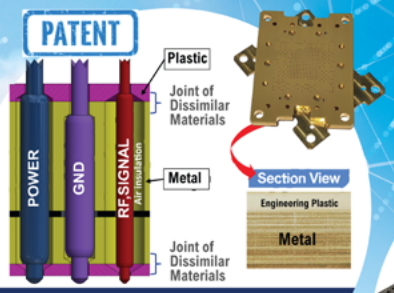
5G

Electrical Analysis



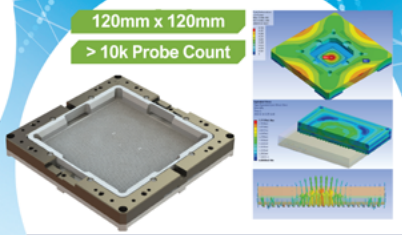
CCC Test, HFSS, TDR
Eye Diagram
4 Port VNA Test

MP Socket



Large Device Socket

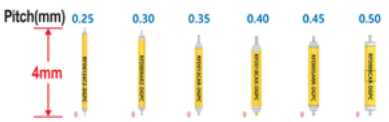
120mm x 120mm
> 10k Probe Count



Coaxial Probe 100GHz

Specification

Frequency : 80GHz(BGA),
100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%



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to pinpoint the best possible operating condition with less human effort.

The new test station can be paired with a single-site handler and thermal control solution to create a remotely accessible test platform, which has proven its worth during the recent COVID pandemic. The approach also lends itself well to "copy-exact" implementations where PSV test floors support highly-parallel device validation efforts. This approach supports concurrent testing with fewer "bench" engineers, thereby cutting TTM and reducing the validation costs.

Production test

It is becoming vividly clear that nearly all test content needs to move to the wafer test step if we are to have any chance of achieving KGD. It has also become abundantly clear that we have entered a space where we have too many tests and not enough time to run all of them. It's not unusual for manufacturers today to have to cull about 10% to 50% of their available pattern sets at wafer probe because of vector-memory and/or test time limitations. The question moving forward is how to choose which patterns to run at each test insertion point. Optimal results depend on which test content is best executed at the first wafer-probe test experience, the subsequent KGD test probe test step, the post-assembly test step, and the final SLT step. Today, this is an art left to the senior test strategists. Moving forward, this art will benefit from AI-driven tools and broad-based data sharing.

While structural and functional test content both have their place, functional test methods can more quickly confirm the proper functioning of large blocks of logic as compared to structural test methods, which check one gate at a time. The author expects an increased usage of functionally-capable test modules, such as Link Scale™, in production as a new tool to provide more test coverage in less test time.

The big opportunity for growth in this space, however, is with the addition of data-driven test selection techniques that allow both the structural and functional test selection process to proceed more intelligently. Several questions hint at how to proceed:

- Why not pull in vision inspection data and use it to decide which corner of the die to test first?
- Why not use the in-line parametric test data to anticipate power extremes and appropriately adjust limits up front?
- Why not use the results for the first few wafers to direct which tests should be executed subsequently?

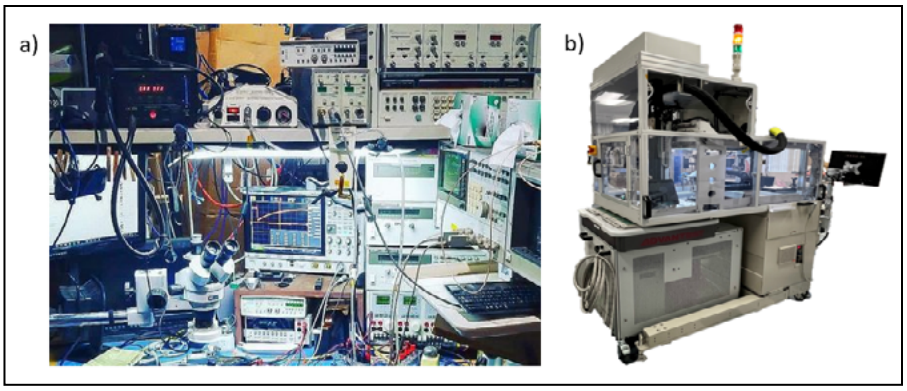


Figure 6: Replacement of a multi-instrument bench top with a streamlined integrated system.

Summary

As we move into 21st century test, things will become much more focused and dynamic. There is little doubt that data will be king. There is no doubt that test over HSIO interfaces will become critical to test time reductions. And perhaps most important, the role of big data in determining the value and limitations of each device being tested will be solidified.

The introduction of the EX Test Station (Figure 6) provides a new tool to simplify, or possibly eliminate, yesteryear's bench setup, replacing multiple instruments and tangles of wire (Figure 6a) with a streamlined integrated system (Figure 6b). The new test station provides for a clean and consistent workspace that also happens to be identical to the setup used in production testing on the V93000 ATE. A consistent interface achieves consistent results.

It's quite prophetic how the writer of *Star Trek: the Next Generation* had a robot named Data that provided such a key function on the *Enterprise D*. Clearly, the role of data in the future will continue to expand and grow. Data himself gave voice to the challenge in front of us: "It is the struggle itself which is most important. We must strive to be more than we are. It does not matter that we will never meet our ultimate goal. The effort yields its own rewards [5]."

References

1. Charts derived from an extended analysis of test-data-volume estimate in Logic Test section of Test Technology Working Group's update to the Heterogenous Integration Roadmap, https://ieee.webex.com/ieee/lsr.php?RCID=6f8af4b048a4441e9501ea473be02921
2. ibid
3. D. Armstrong, "Shift left," MEPTEC Known-Good Die Workshop, Sept. 25, 2022, https://www.youtube.com/watch?v=YObxvk5sqSQ&t=241s
4. D. Armstrong, "Heterogeneous integration prompts test content to 'shift left,'" *Chip Scale Review*, Feb. 2021, p. 7. https://chipscalereview.com/wp-content/uploads/flipbook/1/book.html
5. "69 Best Data Quotes from Star Trek TNG and the Star Trek Movies," Soda and Telepaths, April 26, 2021. https://sodaandtelepaths.com/69-data-quotes-from-star-trek-tng/

Biography

Dave Armstrong is Principal Test Strategist at Advantest America, Inc., San Jose, CA. In addition to his work with many of Advantest's customers, he has also served as the Chairman of the Test Technology Working Group for the Heterogeneous Integration Roadmap. He has degrees in Electrical, Computer, and Environmental Engineering from the U. of Michigan. Email Dave.Armstrong@Advantest.com

Large-panel fan-out perspective on cost, yield, and capability

By Clifford Sandstrom, Robin Davis, Benedict San Jose [Deca Technologies, Inc.]

With supply chain shortages for many of the traditional packaging technologies, the semiconductor industry is looking for alternative solutions. One of the key technologies under consideration by many is molded fan-out panel-level packaging (FOPLP). This technology is particularly appealing as it offers a high-density, high-throughput solution and can achieve comparable, or better, end results as compared to conventional laminate or lead frame-based packages.

Currently running at volumes in the millions of units per day on a 300mm round format, Deca's M-Series™ fan-out PLP technology and Adaptive Patterning® have been scaled up to the new industry standard 600mm x 600mm large-panel format for production. The first 600mm production implementation in nepes laweh in Cheongan, South Korea, began operations in 2021 and continues to ramp in production. The SEMI standard 600mm square format provides a 500% increase in usable area per panel vs. 300mm round, providing cost-effective capacity growth as well as a powerful platform for high-density integration of multi-die and chiplets in 2D, 2.5D, and 3D structures.

The 600mm square format was created with considerations for both short-term implementation and long-term optimized productivity. The ability to segment the 600mm panels into four 300mm square sub-panels for use with conventional 300mm round wafer probe test equipment was a driving factor for the short term (Figure 1). Extending process capability for key lithography, metal deposition, and other processes to complete the 600mm panel provided a challenging, yet achievable target for equipment suppliers.

Focusing on economies of scale, the 300mm round baseline is examined as compared to various large-panel formats. Implementation strategies of the industry's first high-volume chips-first, chips-up M-Series fan-out structure in a large-panel format will be described, including scaling to 2µm lines and spaces using mask-less laser direct imaging (LDI). Our patterning technology, a critical part of the process, provides precise real-time design and alignment. This is critical in a multi-die environment—providing the ability to implement high-density interconnects in a large-panel format.

Cost considerations

To better explain the cost advantage of using a 600mm square large panel compared to the conventional 300mm round wafer, an analysis of utilization and effective area is outlined using a concept called format efficiency. To compute for the format efficiency of a fan-out molded panel, the total usable package area is divided by the format area. For example, let's consider a 9-die chiplet fan-out device with an overall package size of 36mm x 36mm molded in a 300mm round wafer. The 300mm wafer format (70,686mm^2) can fit 40 packages per wafer (a total usable package area of 51,840mm^2) resulting in a format efficiency at 73% (see Figure 2a). In contrast, a 600mm large-panel format can fit 256 devices per panel, given the same 36mm x 36mm package area. This results in a format efficiency of 92% (see Figure 2b). The square panel format's nearly 20% higher utilization of molded area translates directly to lower cost.

Figure 3a details the most highly utilized materials in the process for M-Series 300mm round wafer, shown as a percentage of the total material cost. The polyimide and laminated films such as carrier laminate, temporary backside laminate (BSL) used for warpage control, and photo dry film (DFR) represent more than 30% of the total bill of materials (BOM) cost. Consumption of these materials is directly proportional to the panel format efficiency described earlier. These materials correspond to potential cost savings in a 600mm large-panel format by reducing material wastage.

An example of cost-saving opportunities described above includes the following: using slot or slit coating is ideal for a square panel where just 22ml of polyimide is required for a dielectric layer vs. the 8ml volume typically used in spin coating on 300mm wafers. This translates to a 44% reduction in volume

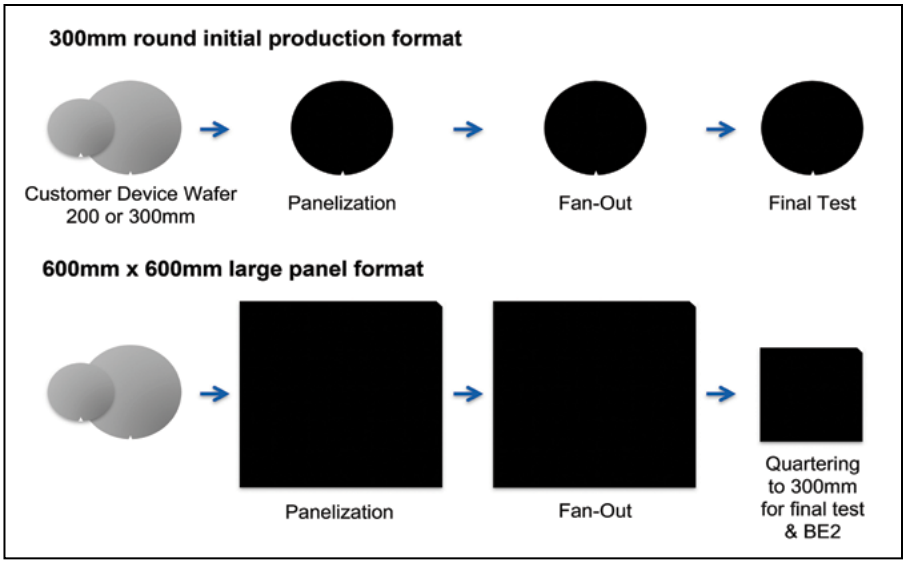


Figure 1: M-Series 300mm round and 600mm square panel.

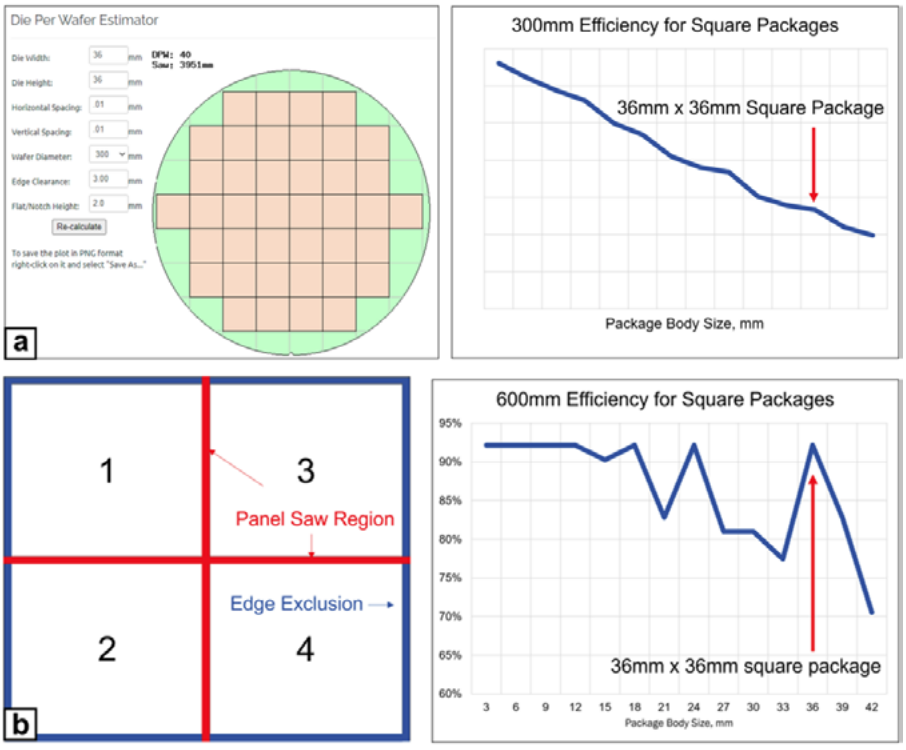


Figure 2: Format efficiency of: a) a 300mm round wafer, and b) a 600mm large panel for a 36mm x 36mm square package.

overall or for the 36mm square device example, a 57% reduction in polyimide volume can be achieved.

Another significant cost reduction opportunity is capital efficiency. While exact percentages vary with equipment selection, in a baseline study completed by our team, the 600mm large-panel format showed capability to achieve a 40% increase in capital productivity (Figure 3b). When combining format efficiency, material consumption and capital productivity increases, there exists a potential for an overall cost reduction of up to 25% with a 600mm large-panel format as compared to the 300mm wafer baseline.

Addressing critical challenges

Our patented lithographic patterning technology was developed in conjunction with M-Series fan-out to overcome the inherent inaccuracies associated with embedded die processes. When creating a composite or reconstituted wafer or panel consisting of individual devices embedded within an encapsulant, variation in the final positions of die as compared with the designed position will occur as a result of die attach placement tolerance and die shift during the encapsulation process (Figure 4a). Without the use of our patterning technology, this displacement can limit the ability to scale to finer bond pad pitches, as further discussed below. This patterning technology includes the high-speed measurement of each die location within a panel, the creation of optimized unit-specific patterns for each device according to pre-determined design constraints, and the application of each layer of the design file through a maskless lithography system. Using this patterning technology, simple devices to complex heterogeneous multi-chiplet systems can be constructed cost-effectively with assurance of high yields in manufacturing.

Multiple techniques are available to optimize the unit-specific pattern in response to die shift. The first, adaptive alignment, typically dynamically aligns the redistribution layer (RDL) and first via layer pattern to precisely match that of the die pads based on the measured lateral shift and rotation for each die. A further technique, adaptive routing, builds on top of adaptive alignment by regenerating small segments of RDL traces to maintain electrical connectivity between portions of the design that have been aligned to different die or between a fixed feature in the design and one that has rotated or shifted.

Figure 4b illustrates the process for creating the adaptively-patterned via and fan-out RDL layers [1,2]. First, a nominal fan-out RDL design is created. Then, a partially-routed RDL layer called a prestratum is formed by omitting a small portion of the RDL layer in close proximity to the Cu studs. After scanning the panel to measure the actual position and orientation of each unit, the design of each unit on the panel is completed to connect the prestratum pattern to the Cu stud pads and their corresponding dielectric vias. The adaptive region in which the RDL traces are allowed to dynamically change is typically

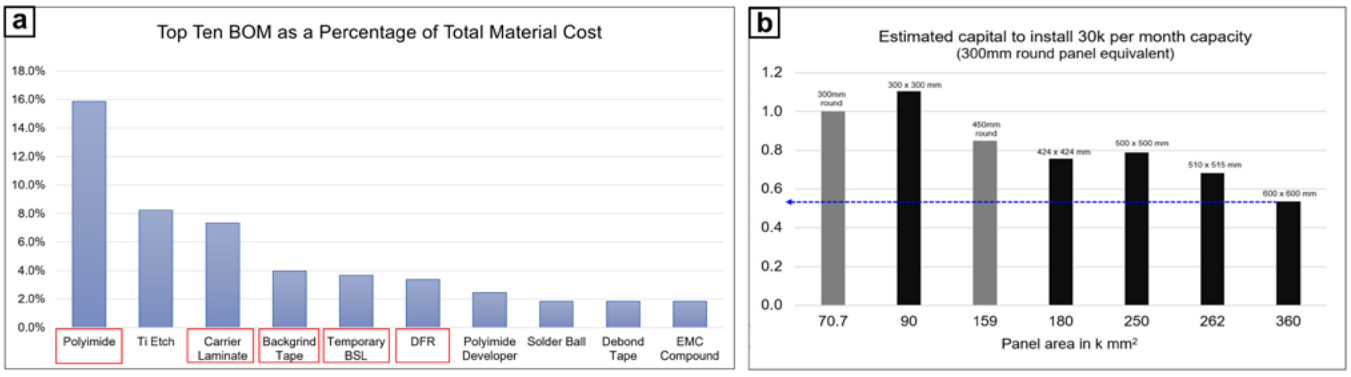


Figure 3: a) Top 10 BOM for a 300mm round wafer; materials boxed in red represent potential cost savings for a 600mm large-panel format; and b) Capital to install a 30k per month capacity based on 300mm round equivalent.

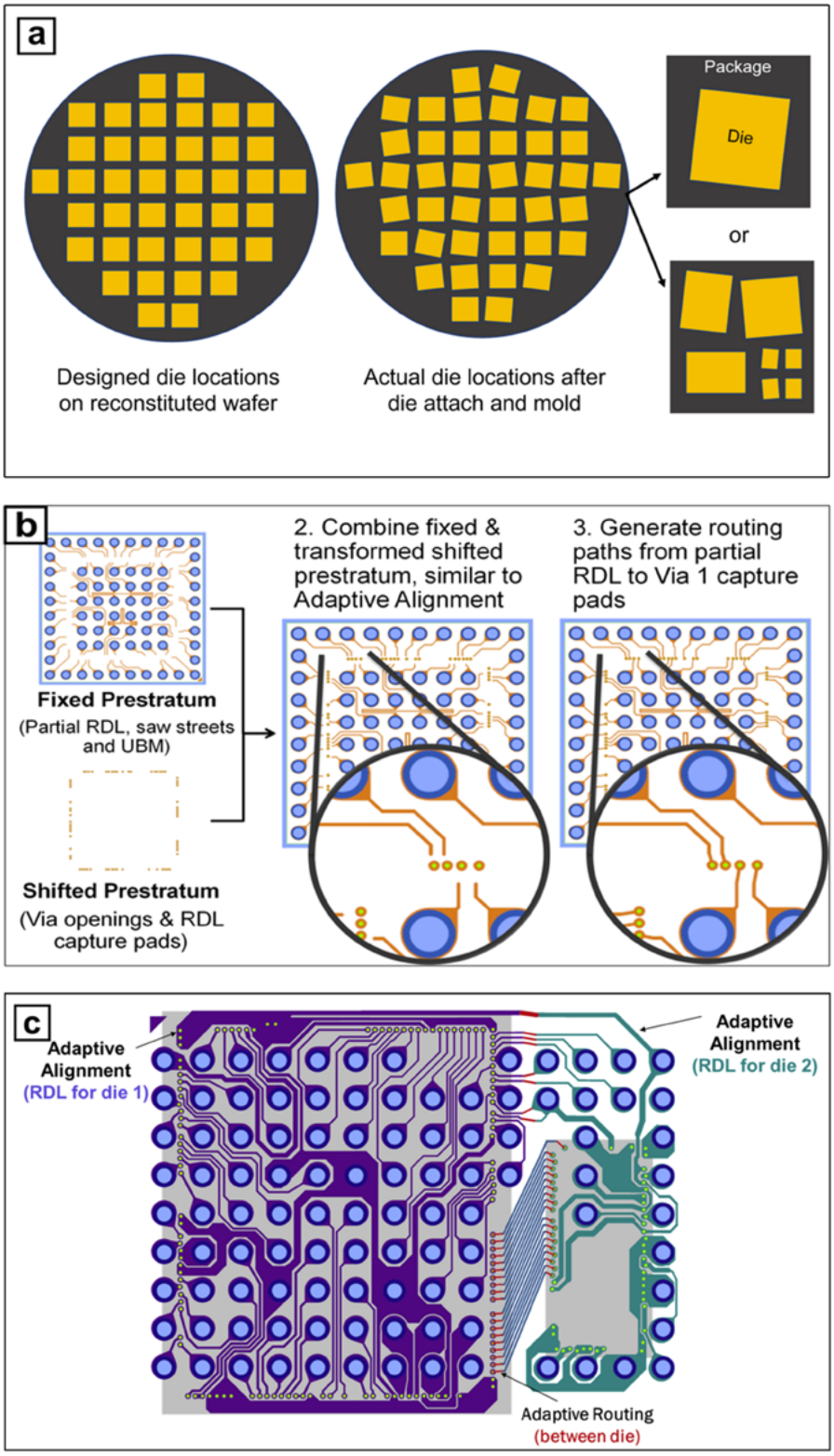


Figure 4: a) Die shift of embedded die in a FOWLP; b) Process for creating Adaptively Patterned via and fan-out RDL layers; and c) Multi-die adaptively-routed RDL shown in red using Adaptive Patterning.

on the order of 10µm to 50µm.

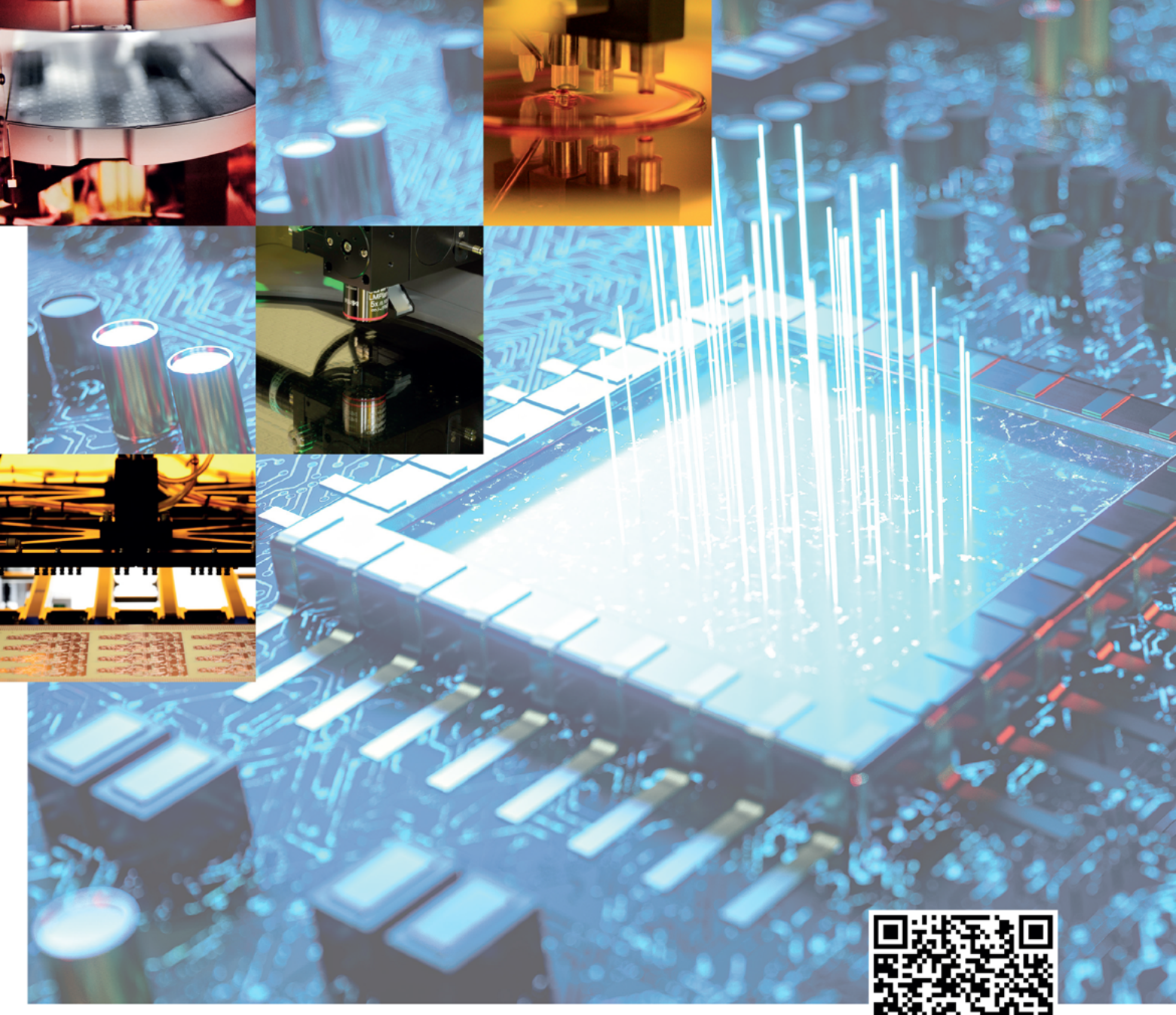
The concept outlined above is further illustrated for the connections between chips as shown in Figure 4c. The light blue circles represent the fixed under-bump metal (UBM) pattern where the future solder balls will be attached. In this multi-die example, the purple is a single RDL for a microcontroller unit (MCU) device, while the green represents a single RDL for a radio device. The routes between the die in blue represent a fixed RDL with the final connections to be completed with adaptive routing, shown in red, to precisely accommodate the actual locations of each die, as well as the adaptively-aligned RDL patterns.

For a conventional fan-out wafer-level packaging (FOWLP) process flow, the most expensive tool in terms of capital cost is the die attach process equipment. Without our patterning technology, a FOWLP process will require a very accurate and expensive die attach tool to achieve high yield in a high-density interconnect package. A very high-accuracy die attach tool with a tolerance of ±3µm at three sigma, or better, typically has a very low throughput in the range of 2,000 chips per hour. In contrast, our combined FOWLP and patterning solution can use a moderately accurate die attach tool with a tolerance of ±15µm with a throughput exceeding 25,000 chips per hour. The impact for a production capacity of 30,000 panels per month can be as much as a 10X reduction in die attach capital; $80M for conventional FOWLP die attach versus $8M for our combined solution.

Scaling to high-density integration

As previously mentioned, a key technology that enables scaling to high-density integration is the use of laser direct imaging (LDI) with our patterning technology. LDI allows the unit-specific patterns to be implemented in real-time driven by the unique Adaptive Patterning design file per wafer or panel. In addition to the maskless digital nature of LDI, additional advantages exist over other exposure methods such as conventional steppers, including a high depth of focus (DOF) that allows scaling of lines to 2µm and below with the ability to have thicker copper RDL traces. One of the other notable advantages of a 600mm panel when using maskless LDI is that there is no need for reticle stitching for large packages. Because the entire panel design is digital, the package could be up to 600mm square.

In addition to the physical RDL lines, increasing bond pad pitch and via density is critical for achieving high-density interconnects for heterogeneous and chiplet integration. Figure 5 provides an overview of the limits on bond pad density for various industry technologies



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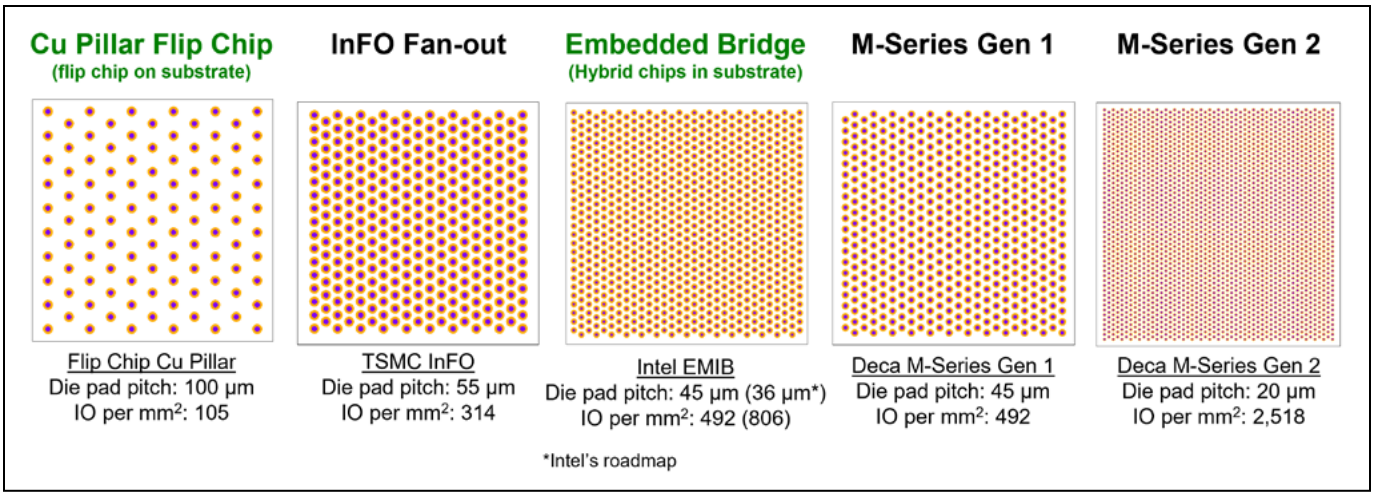

Figure 5: Comparison of interface pitch between different interconnect technologies and the M-Series.

including that of well-known Cu pillar flip-chip on laminate and Intel's embedded interconnect bridge (EMIB) technology, as well as both existing Gen 1 M-Series and Gen 2, currently in development.

As shown in Figure 5, typical Cu pillar flip-chip bonding has a die pad pitch of 100µm with an IO density of 105 IO/mm^2. TSMC's integrated fan-out (InFO) has a die pad pitch of 55µm with an IO density of 314 IO/mm^2 [3]. To further decrease interface pitch, new interconnect technologies were developed such as Intel's EMIB, which can achieve a die pad pitch of 45µm with an IO density of 492 IO/mm^2. Our first-generation M-Series with a planarized structure above the encapsulated active die coupled with our patterning technology, achieved the same 45µm interface pitch as compared to EMIB, without the need for complicated bridge chips embedded in substrates [3-5]. With the new Gen 2 technology, this die pad pitch can be further scaled to 20µm, thereby achieving a more than 5X increase in IO density of 2518 IO/mm^2. Gen 2's advanced LDI and automatic optical inspection (AOI) equipment combined with our patterning technology provides a path for the ultra-high-density die pad pitch and RDL density required for chiplets and advanced heterogeneous integration.

As previously discussed, a crucial advantage of M-Series over other chip-

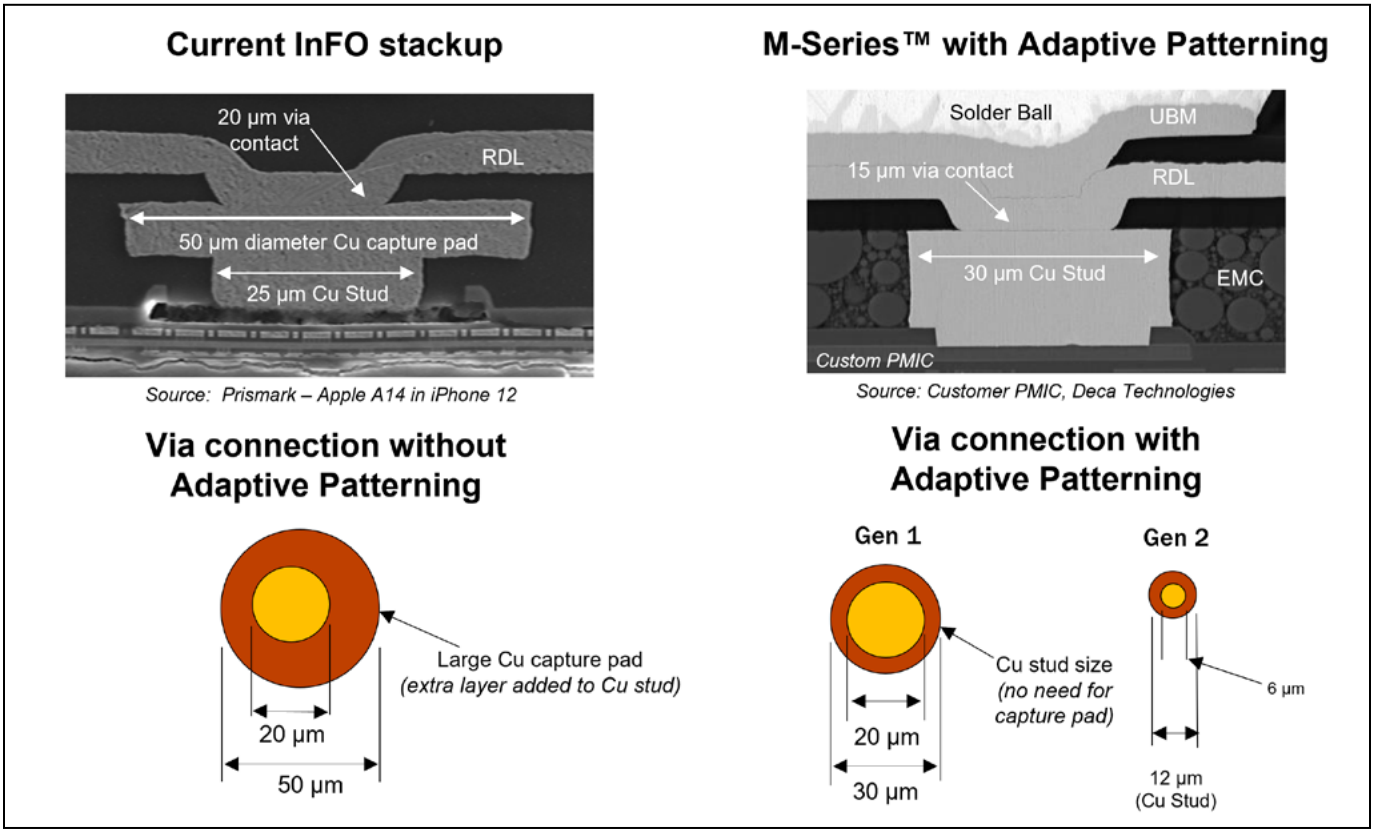

Figure 6: M-Series and Adaptive Patterning enable a significantly larger via contact area given the same bond pad pitch and scaling to fine bond pitch.

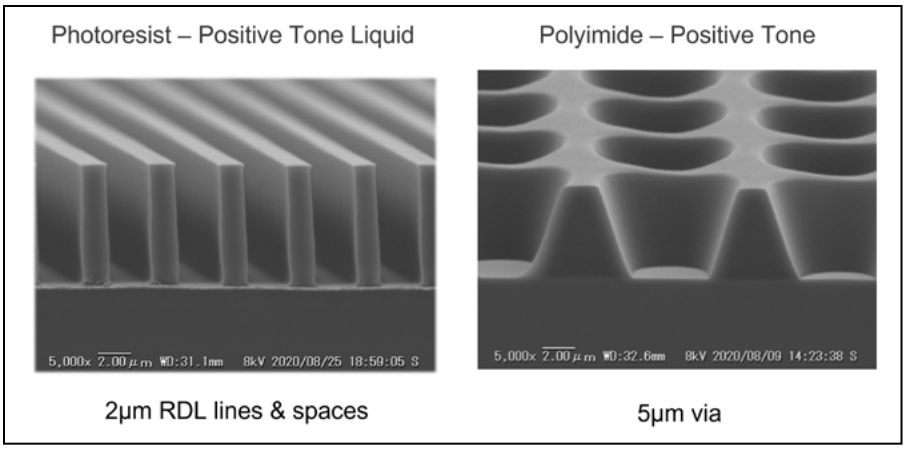

Figure 7: Gen 2 demonstrated 2µm line and spaces and 5µm vias.

first face-up FOWLP technologies such as integrated fan-out (InFO) is our patterning technology. This technique enables a significantly larger contact area for the same bond pitch. Figure 6 shows a side by side comparison of the two stackups. In the InFO structure, a large Cu capture pad is utilized to ensure contact between the RDL via contact and the Cu stud regardless of final die position [6]. The ratio between the via size and this capture pad is dictated by the die shift brought about by die placement variations and die shift during encapsulation. The pad must be large enough, as compared to the via, that should the die be displaced to its maximum, the via will still fall within the bounds of the capture pad. With the M-Series structure, there is no need for this additional capture pad layer because our lithographic patterning technology ensures the via is precisely aligned to the die pad. By compensating for die shift in this manner, M-Series enables a large via size connection on a smaller landing pad (only the Cu stud without an extra capture pad). The combination of M-Series and our patterning technology allows for an approximate 300% increase in contact area for the same bond pitch, thereby enabling improvements in electrical performance and yield. An additional benefit of removing the requirement for this additional capture pad layer is the ability to further scale the bond pad pitch to as small as 20µm with a roadmap to even higher density.

Excellent initial process results have been demonstrated in cooperation with leading material suppliers using next-generation LDI equipment achieving the Gen 2 design targets as shown in Figure 7. Lines and spaces 2µm in size, as well as 5µm via features, were successfully demonstrated paving the way forward for Gen 2's 20µm die pad pitch.

Summary

With the format efficiency gains, material reductions and capital productivity increases, an overall cost reduction of 25% can be achieved with the 600mm x 600mm large-panel format as compared to a 300mm round baseline. Utilization of chiplets from the most cost-effective IC process nodes brings further savings in creating today's leading-edge semiconductor devices.

Adaptive Patterning is a key technology for FOPLP with its ability to overcome the die shift inherent within an embedded die structure leading to the highest possible yields while delivering up to a 10x reduction in capital cost for die attach. In addition, our patterning technology provides a cost-effective approach for scaling device interconnects for ultra-high density heterogeneous integration without the use of interposers or bridge chips.

The next-generation of M-Series, or Gen 2, is launching with a 20µm bond pad pitch capability as well as scaling the RDL features down to 2µm lines. Leading material and equipment suppliers have worked closely with us to demonstrate the key design attributes required within new dielectric and photoresist formulations, as well as next-generation LDI tools.

References

1. C. Bishop, et al., "Adaptive Patterning design methodologies," IEEE 66th Electronic Components and Tech. Conf. (ECTC), Las Vegas, NV, 2016, pp. 7-12.
2. C. Scanlan, et al., "Adaptive Patterning for panelized packaging," International Wafer Level Packaging Conf. (IWLPC) Proc., Nov. 2012.
3. E. Hudson, et al., "Deca & Cadence breakthrough heterogeneous integration barriers with Adaptive Patterning," IEEE 71st ECTC, 2021.
4. B. San Jose, et al., "Adaptive Patterning and M-Series for high-density integration, *Embedded and Fan Out Wafer and Panel Level Packaging Technologies for Advanced Application Spaces: High Performance Compute and System in Package* (ed. B. Keser, S. Krohnert), pp.125–154. New Jersey: Wiley. 2021.
5. C. Sandstrom, et al., "Scaling M-Series for chiplets," IEEE 71st ECTC, 2021,
6. Prismark Partners LLC (2021), Apple A14: Customer Teardown Analysis. pp. 1-50.

Biographies

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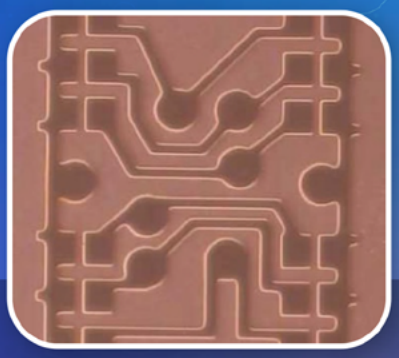

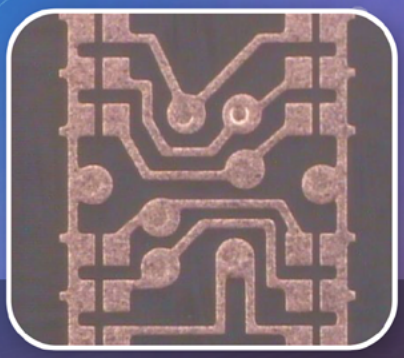

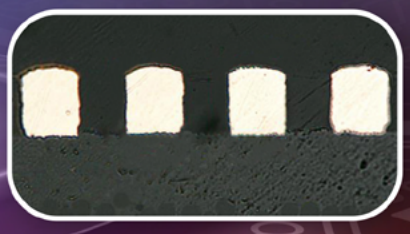

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Powering chips from the backside

By Naoto Horiguchi, Eric Beyne [imec]

A power delivery network is designed to provide power supply and reference voltage (i.e., V_{DD} and V_{SS}) to the active devices on the die most efficiently. Traditionally, it is realized as a network of low-resistive metal wires fabricated through back-end-of-line (BEOL) processing on the frontside of the wafer. The power delivery network shares this space with the signal network, i.e., the interconnects that are designed to transport the signal.

To deliver power from the package to the transistors, electrons traverse all 15-20 layers of the BEOL stack through metal wires and vias that get increasingly narrow (hence, more resistive) when approaching the transistors. On their way, they lose energy, resulting in a power delivery, or IR drop, when bringing the power down. When arriving closer to the transistor, i.e., at the standard cell level, the electrons end up in V_{DD} and V_{SS} power and ground rails organized in the M_{int} layer of the BEOL. These rails take up space at the boundary and between each standard cell. From here, they connect to the source and drain of each transistor through a middle-of-line interconnect network (**Figure 1**).

With each new technology generation, the traditional BEOL architecture described above struggles to keep pace with the transistor scaling path. Today, the "power interconnects" increasingly compete for space in the complex BEOL network and account for at least 20% of the routing resources. Also, the power and ground rails take up a considerably large area at the standard cell level, limiting further standard cell height scaling. At the system level, the power density and IR drop increase dramatically, challenging designers to maintain the 10% margin that is allowed for the power loss between the voltage regulator and the transistors.

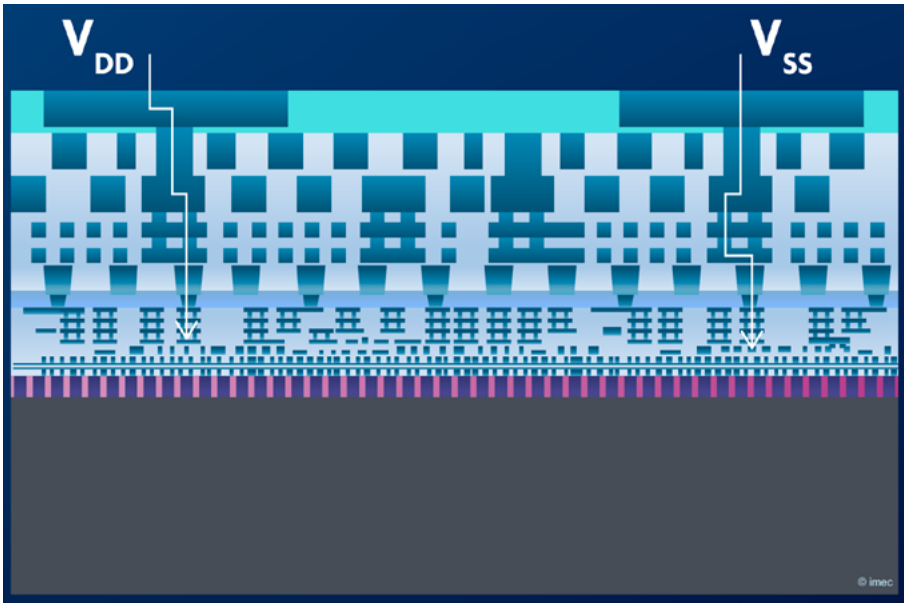

Figure 1: Schematic representation of a traditional frontside power delivery network.

Promises of a backside power delivery network

A backside power delivery network (BSPDN) promises to address the issues noted above (**Figure 2**). The idea is to decouple the power delivery network from the signal network by moving the entire power distribution network to the backside of the silicon wafer, which today serves only as a carrier. From there, it enables direct power delivery to the standard cells through wider, less resistive metal lines, without the electrons needing to travel through the complex BEOL stack. This approach promises to benefit the IR drop, improve the power delivery performance, reduce routing congestion in the BEOL, and when properly designed, allow for further standard cell height scaling [1].

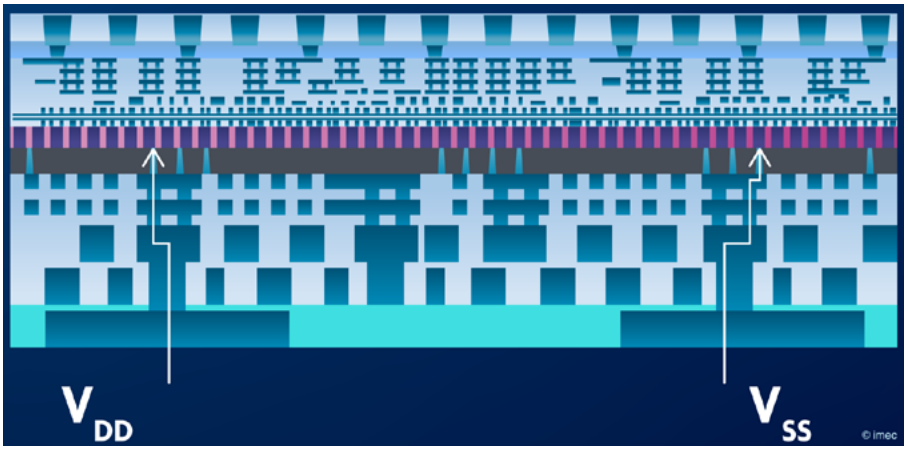

Figure 2: A BSPDN allows for decoupling the power delivery from the signal network.

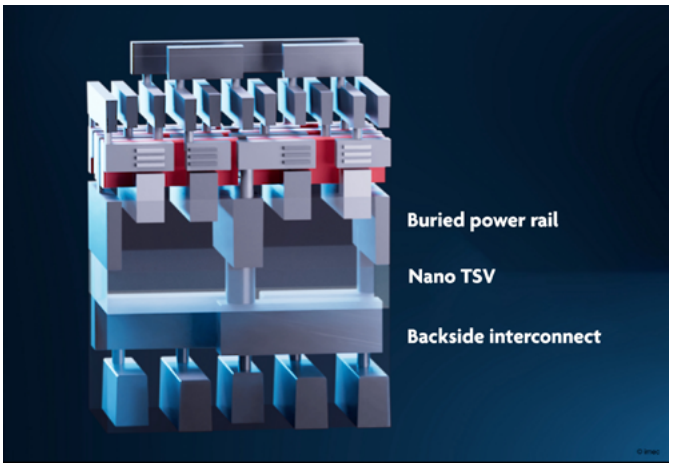

Figure 3: Schematic representation of a BSPDN implementation where nanosheets connect to the wafer's backside through BPRs and nTSVs.

Buried power rail and nTSVs: key building blocks

Before detailing the process flow to fabricate a backside power delivery network, we introduce two technology enablers: buried power rail (BPR) and nano-through-silicon-vias (nTSVs) (Figure 3). BPR is a technology scaling booster that further scales standard cell height and reduces IR drop. It is a metal line construct buried below the transistors – partially within the Si substrate, and partially within the shallow trench isolation oxide. It takes the role of the V_{DD} and V_{SS} power rails that have traditionally been implemented in the BEOL at the standard cell level. This historic move from BEOL to the front-end-of-line (FEOL) allows the reduction of the number of M_{int} tracks, enabling a further shrinking of the standard cell. In addition, when designed perpendicularly to the standard cell, the rail's size can be relaxed, which further reduces the IR drop.

The potential of the BPRs can be fully exploited when combined with nTSVs—high-aspect-ratio vias processed in the thinned wafer's backside. Together, they allow for delivering the power from the wafer's backside to the active devices in the front end in the most efficient way, i.e., with the largest gains in terms of IR drop reduction.

Quantifying the promises

At the 2019 IEDM conference, the promises of using a BSPDN with nTSVs and BPRs were quantified by imec research in collaboration with Arm [2]. Arm ran a simulation on one of its central processing units (CPUs) engineered with advanced design rules. They compared three ways to deliver the power: conventional frontside power delivery, frontside power delivery in combination with BPRs, and backside power delivery with nTSVs landing on BPRs. In terms of power delivery efficiency, the latter was the clear winner. On-chip power heat maps showed that BPRs with frontside power delivery could reduce the IR drop by ~1.7x compared to traditional frontside power delivery (Figure 4). But BPRs with backside power delivery did even better: they substantially reduced the IR drop by 7x.

The overall process flow

Below, we unravel the process flow to make one specific implementation of a BSPDN, in which nTSVs – processed in an extremely thinned wafer backside – land on top of the BPRs. The devices, e.g., scaled FinFETs processed in the wafer's frontside,

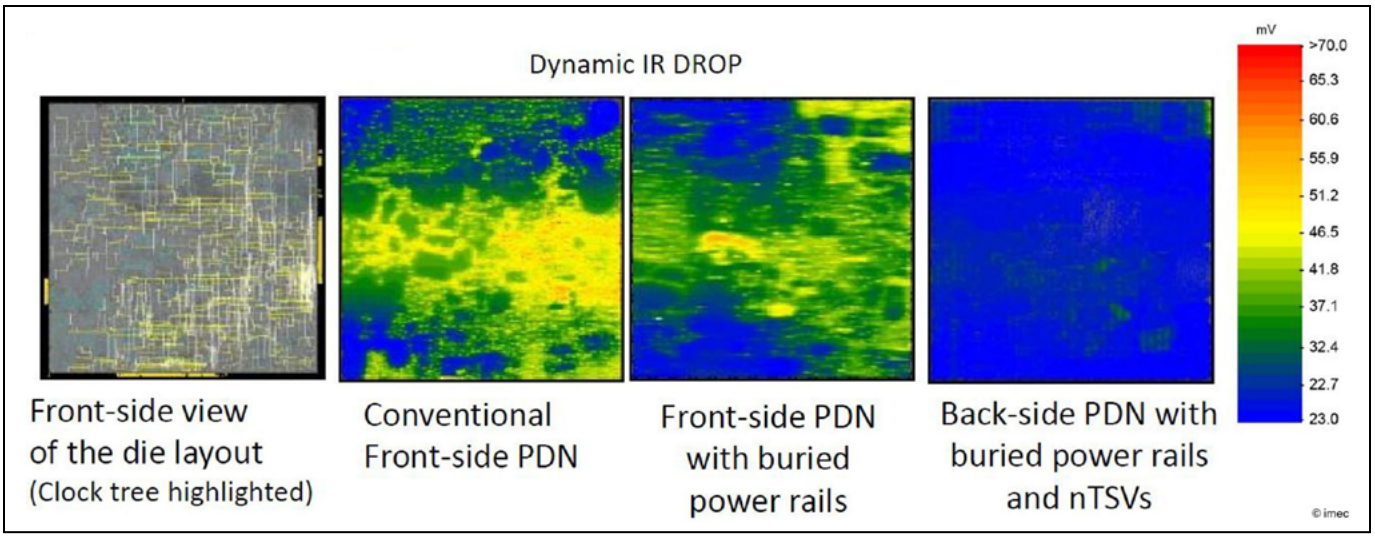

Figure 4: Comparing different power delivery approaches in terms of dynamic IR drop.

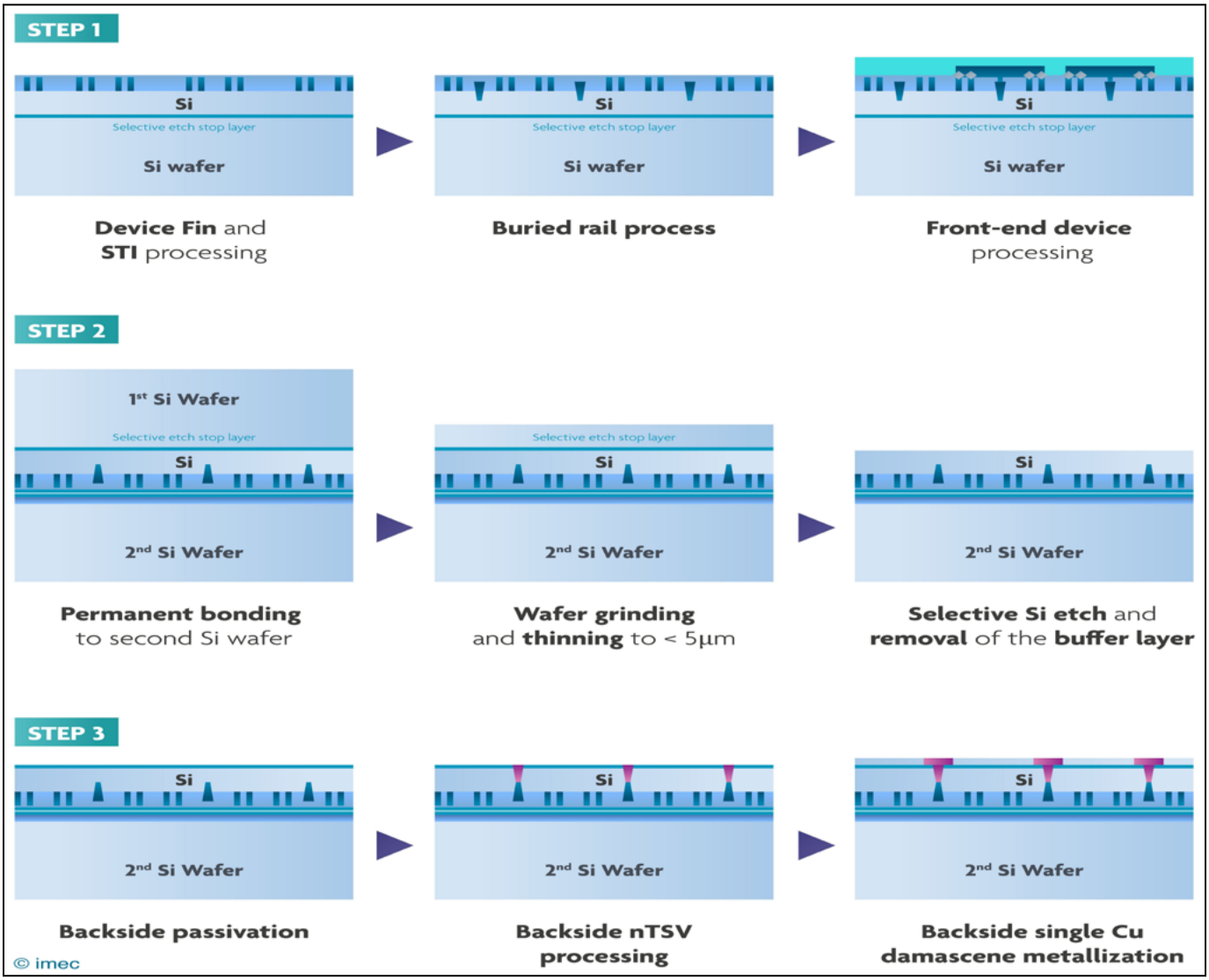

Figure 5: Process flow for a BSPDN with BPRs connecting to nTSVs. For reasons of simplification, some details from step 1 have been omitted in steps 2 and 3, including the connection between BPR and the devices.

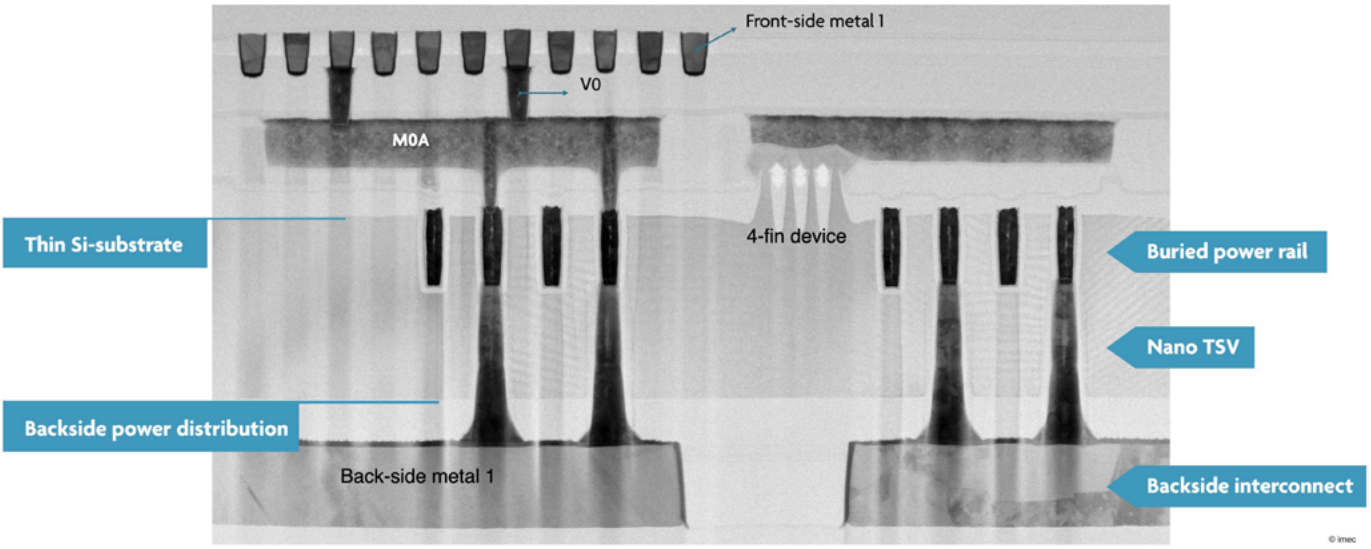

Figure 6: A transmission electron microscope (TEM) image showing scaled FinFETs connected to the wafer's backside and frontside.

connect to the backside of the wafer through the BPRs and nTSVs (Figure 5).

Step 1: frontside processing with buried rails. The process flow starts with growing a SiGe layer on top of a 300mm Si wafer. The SiGe layer later serves as an etch stop layer to end the wafer thinning (step 2). Next, a thin Si capping layer is grown on top of the SiGe layer: the starting point to fabricate the device and buried power rail. The buried power rails are defined after shallow trench isolation. The trenches, etched in the Si capping layer, are filled with oxide liner and metal, for example W or Ru. The resulting buried rails are typically ~30nm wide, at ~100nm pitch. The metal is then recessed and capped by a dielectric. Processing of the devices (in this case, scaled FinFETs) is completed after BPR implementation, and the BPRs are connected to the transistors source/drain region through the via-to-BPR (VBPR) and the M0A line. Cu metallization completes the frontside processing.

Step 2: wafer-to-wafer bonding and wafer thinning. The wafer containing the devices and BPRs is flipped over, and the "active" frontside is bonded to a blanket carrier wafer. This is accomplished using SiCN-to-SiCN dielectric fusion bonding at room temperature, followed by a post-bond anneal at 250°C. Then, the backside of the first wafer can be thinned to where the SiGe etch stop is located. Thinning is enabled by a combination of sequentially backside grinding, chemical mechanical polishing (CMP), and dry and wet etch steps. The SiGe layer is removed in the next step, and the wafer is ready for nTSV processing.

Step 3: nTSV processing and connection to BPRs. After depositing a backside passivation layer, the nTSVs are patterned from the wafer backside by a through-Si alignment lithography process. nTSVs are etched through the Si (which is several 100nm deep) and land on the tip of the BPR. Next, the nTSVs are filled with oxide liner and metal (W). In this specific implementation, they are integrated at 200nm pitch without consuming any area of the standard cell. The flow is completed by processing one or more backside metal

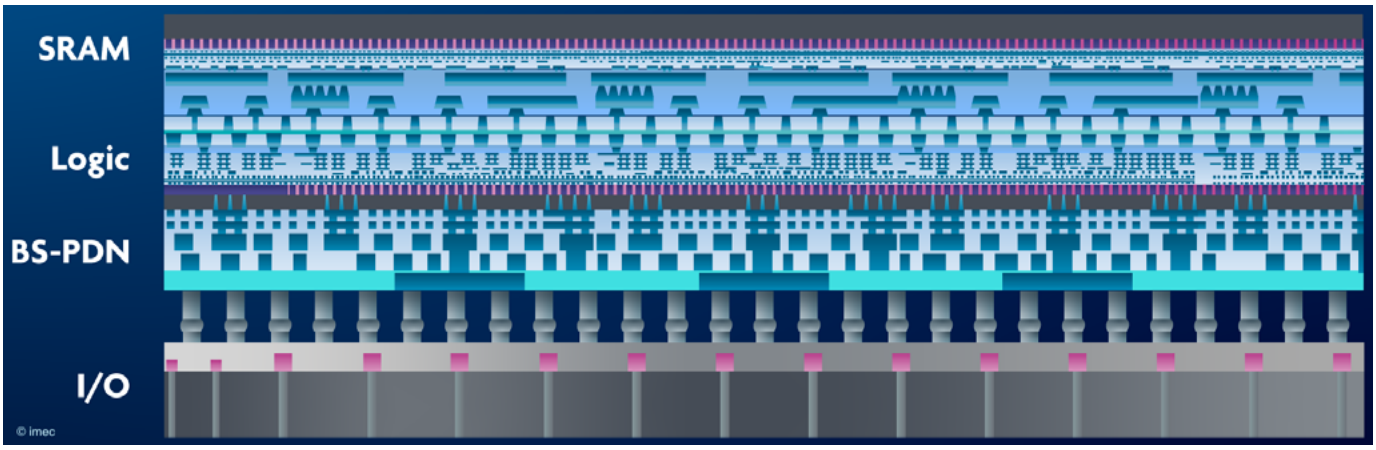

Figure 7: Schematic representation of a 3D-SoC with backside power delivery implementation.

layers, electrically connecting the backside of the wafer to the BPR in the frontside via the nTSVs.

Critical process steps

Implementing a backside power delivery network adds new steps to chip fabrication. Over the last few years, imec has demonstrated various critical technology building blocks, gradually addressing the challenges of the novel production steps [3-5].

BPR: introducing metal in the FEOL. In the proposed fabrication flow, buried power rails are implemented in the FEOL, before device processing. This implementation means the metal rail is subject to the high-temperature process steps applied during subsequent device manufacturing. For chip manufacturers, this might seem as disruptive as bringing Cu into the BEOL several decades ago. Therefore, the choice of metal used to make the BPR is crucial. Imec could successfully demonstrate the integration of buried power rails made of refractory metals – metallic elements like Ru or W that are highly resistant to heat. Keeping the metal rail en-capped during subsequent FEOL processing was an additional measure to avoid contamination of the front end.

Imec believes that using nTSVs in combination with BPRs is a very promising implementation scheme in terms of scalability and performance. Other implementations of a BSPDN exist as well, each trading off power delivery performance, standard cell area consumption and FEOL complexity.

Wafer thinning: minimizing thickness variation. Extreme wafer thinning to a few 100nm of Si is required to expose the nTSVs and minimize their resistivity (and hence, IR drop). This severely restricts the allowed thickness variation, which may be induced during the different wafer thinning steps. Imec collaborates with several partners to improve the chemistries used for etching. The final wet etch, for example, enables a highly selective soft-landing process stopping on the SiGe layer. In the final step of the thinning process, the SiGe etch stop layer is removed in a dedicated chemistry where very high selectivity to Si is required. This way, the Si capping layer can be exposed with a total thickness variation below 40nm.

Another concern is the thermal impact on the device self-heating because of the extreme thinning of the (otherwise heat-dissipating) Si substrate. Preliminary

modeling work indicates that the self-heating effect can, to a large extent, be countered by the metal lines in the wafer's backside, which provide additional lateral thermal spreading. More detailed thermal simulations are currently ongoing to gain more insights [6].

Wafer bonding: precise nTSV/BPR alignment. The wafer bonding step inherently distorts the first "active" wafer. This distortion challenges the lithography step needed to pattern the nTSVs on the wafer's backside. More specifically, it challenges the precision with which the nTSVs need to be aligned to the bottom BPR layer. Because we are dealing with features that are of standard cell dimensions, the overlay requirement should be better than 10nm. Conventional lithography alignment cannot, however, sufficiently compensate for the wafer distortion. Fortunately, advances in wafer-to-wafer bonding allow for a significant reduction in alignment errors and distortion values. In addition, by using advanced lithography correction techniques, the overlay error of the nTSV lithography with respect to the BPR structures can be reduced to less than 10nm.

No degradation of device performance

One important question remains: are the newly added process steps, such as BPR integration, wafer thinning, and nTSV processing, impacting the electrical performance of the devices fabricated in the front-end? To answer this question, imec recently built a test vehicle using the fabrication flow and the improved process steps described above. In this test vehicle, scaled FinFETs connect with tight overlay control to the wafer's backside through 320nm-deep nTSVs landing on BPRs (Figure 6). The BPRs also connect to the frontside metallization through the M0A layer and V0 via. This frontside connection, among others, allowed researchers to assess the electrical performance of the devices before and after backside processing. With this test vehicle, imec showed that FinFET performance was not degraded by BPR implementation and backside processing, provided that an anneal step is performed at the end to get optimal device properties [4].

Application to logic ICs and 3D-SoCs

Some chip manufacturers have publicly announced introducing BSPDNs in logic ICs of the 2nm and beyond technology node. This is when nanosheet transistors are making inroads. However, the novel routing technology can be used for a broad range of transistor architectures. Imec's roadmap foresees its introduction in advanced technology nodes, with nanosheet transistors in 6T standard cells. The combination with BPR will then help push standard cell heights below 6T. The application domain, however, extends beyond just 2D single-chip ICs: it also holds promises for the performance improvement of 3D systems-on-chip (3D SoCs).

Imagine 3D-SoC implementation where some or all memory macros are placed in a top die while logic is placed on a bottom die. On the technology side, this can be realized by bonding the active frontside of the "logic wafer" to the active frontside of the "memory

wafer." In this configuration, the original backsides of both wafers now reside on the outside of the 3D-SoC system (Figure 7). We can now think of exploiting the "free" backside of the "logic wafer" to deliver the power to the power-hungry core logic circuits. This can be accomplished in the same way as proposed for 2D SoCs. The main difference with this configuration is that the original dummy blanket wafer – earlier introduced to enable the wafer thinning – is now replaced by a second, active wafer (in this case, a memory wafer).

Although the design noted above is yet to be implemented experimentally, first assessments from the IR drop perspective are very encouraging. The proposed solution was validated on a memory-on-logic partitioned design using an advanced node research process design kit (PDK). Implementing a BSPDN with nTSVs and BPRs showed promising results: 81% and 77% average and peak IR drop reduction for the bottom die compared to conventional frontside power delivery. This makes backside power delivery ideal for 3D-IC power delivery in advanced complementary metal-oxide semiconductor (CMOS) nodes [7].

For both 2D and 3D designs, the concept of exploiting the wafer's free backside can potentially be expanded to other functions by adding specific devices in the backside, such as I/Os or electrostatic discharge (ESD) protection devices. Imec, for example, combined backside processing with implementing a 2.5D (i.e., pillar-like) metal-insulator-metal capacitor (MIMCAP), which serves as a decoupling capacitor. The 2.5D MIMPCAP boosts capacitance density with a factor of 4 to 5, allowing a further improvement of the IR drop. The results were derived from an IR drop modeling framework calibrated with experimental data [8].

Summary

Future chips may well break the tradition of delivering power through the frontside. A BSPDN with backside metals, buried power rails, and nTSVs has shown clear advantages in reducing the IR drop, releasing the BEOL routing strain, and improving standard cell height scaling. The critical process steps, including BPR integration, wafer bonding, wafer thinning, and nTSV processing, are gradually being improved, thereby preparing the new routing technology to introduce in advanced logic technology nodes and future 3D SoCs.

References

1. B. Cline, et al., "Power from below: buried interconnects will help save Moore's Law," *IEEE Spectrum*, vol. 58, no. 9, pp. 46-51, Sept. 2021, doi: 10.1109/MSPEC.2021.9531012
2. S. K. Moore, "Arm shows backside power delivery as path to further Moore's Law," *IEEE Spectrum*, 2019; https://spectrum.ieee.org/arm-shows-backside-power-delivery-as-path-to-further-moores-law
3. A. Veloso, et al., "Enabling logic with backside connectivity via

n-TSVs and its potential as a scaling booster," Symp. on VLSI Tech., 2021, pp. 1-2.
4. A. Veloso, et al., "Scaled FinFETs connected by using both wafer sides for routing via buried power rails," IEEE Symp. on VLSI Tech. and Circuits, 2022, pp. 284-285, doi:10.1109/VLSITechnology andCir46769.2022.9830177
5. A. Jourdain, et al., "Buried power rails and nano-scale TSV: technology boosters for backside power delivery network and 3D heterogeneous integration," IEEE 72nd Electronic Comp. and Tech. Conf. (ECTC), 2022, pp. 1531-1538, doi: 10.1109/ECTC51906.2022.00244
6. [6] H. Oprins, et al., "Package level thermal analysis of backside power delivery network (BS-PDN) configurations," 21st IEEE Intersociety Conf. on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm 2022).
7. [7] G. Sisto, et al., "IR-drop analysis of hybrid bonded 3D-ICs with backside power delivery and μ- & n-TSVs," IEEE Inter. Interconnect Tech. Conf. (IITC), 2021, pp. 1-3, doi: 10.1109/IITC51362.2021.9537541
8. [8] R. Chen, et al., "Backside PDN and 2.5D MIMCAP to double boost 2D and 3D ICs IR-drop beyond 2nm node," IEEE Symp. on VLSI Tech. and Circuits (VLSI Tech. and Circuits), 2022, pp. 429-430, doi: 10.1109/VLSITechnology andCir46769.2022.9830328

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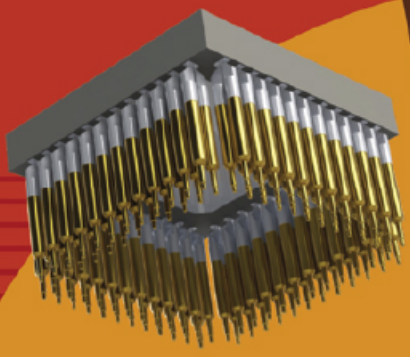

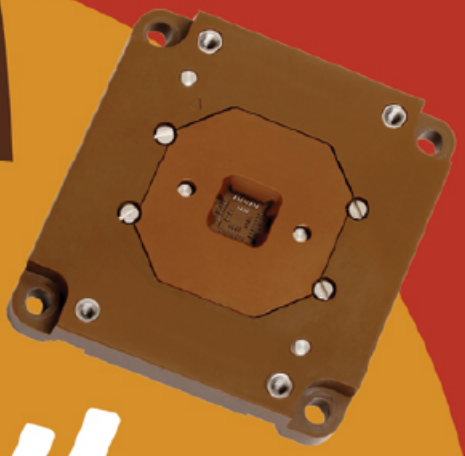

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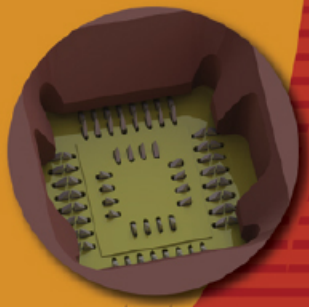

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