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Volume 26, Number 5

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3D ICs

Direct bonding: a key enabler for 3D technologies

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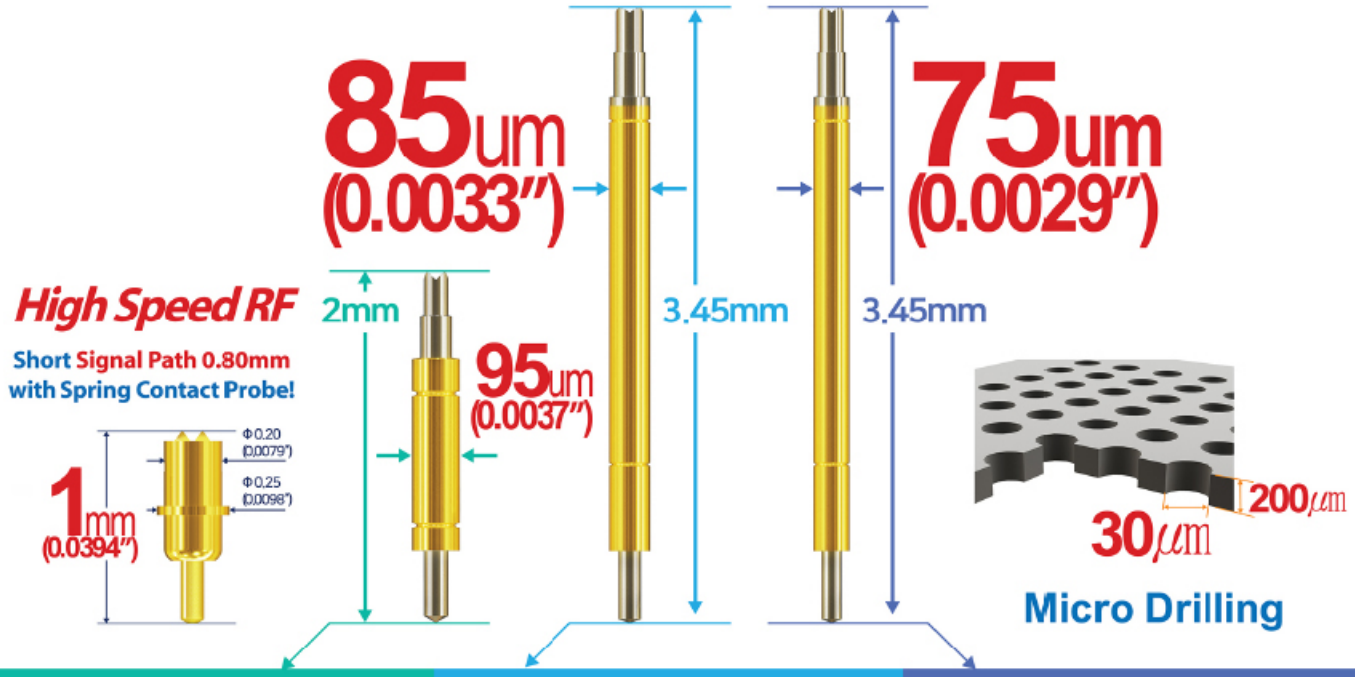

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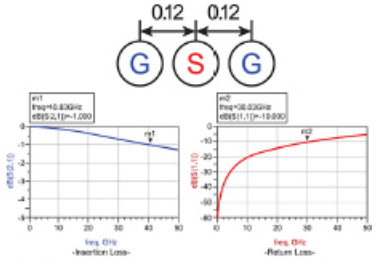

110㎛ Pitch

Mechanical Spec.

- Spring Force : 0.212oz (6.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
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Electrical Spec. (Simulation Data)

- Current Rating : 0.9A
- Propagation Delay : 38.25ps
- Capacitance : 0.47pF
- Inductance : 0.63nH
- Insertion Loss : > 50.00GHz @ -1.000dB
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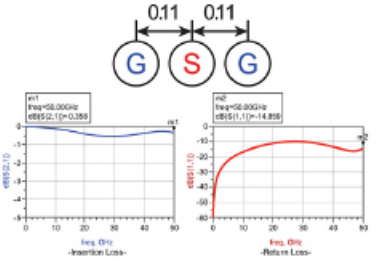
  (Dielectric material : CERAMIC)



100㎛ Pitch

Mechanical Spec.

- Spring Force : 0.247oz (7.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
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Electrical Spec. (Simulation Data)

- Current Rating : 0.8A
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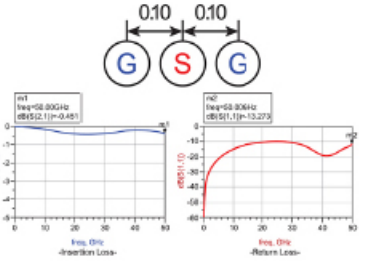

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Challenges of direct hybrid bonding D2W remain in performance, yield and cost, which are driven by alignment capability, bonding quality and throughput, respectively.

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STAFF
Kim Newman
Publisher
knewman@chipscalereview.com

Lawrence Michaels
Managing Director/Editor
lmichaels@chipscalereview.com

Debra Vogler
Senior Technical Editor
dvogler@chipscalereview.com

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Chip Scale Review
P.O. Box 2165
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Tel: +1-408-846-8580
E-Mail: subs@chipscalereview.com
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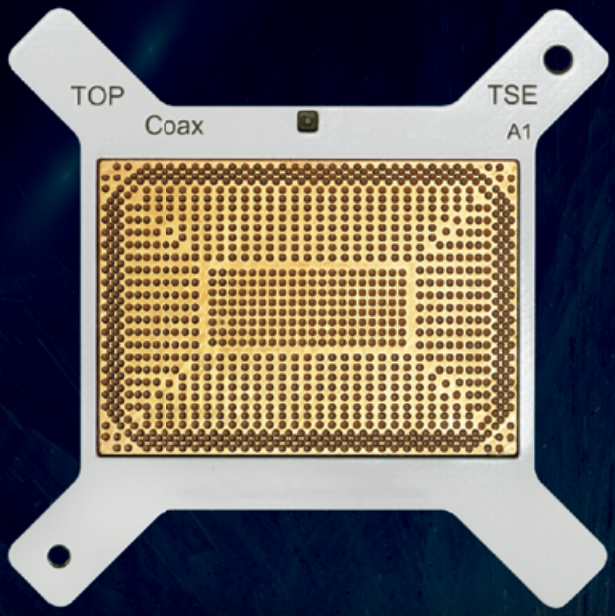

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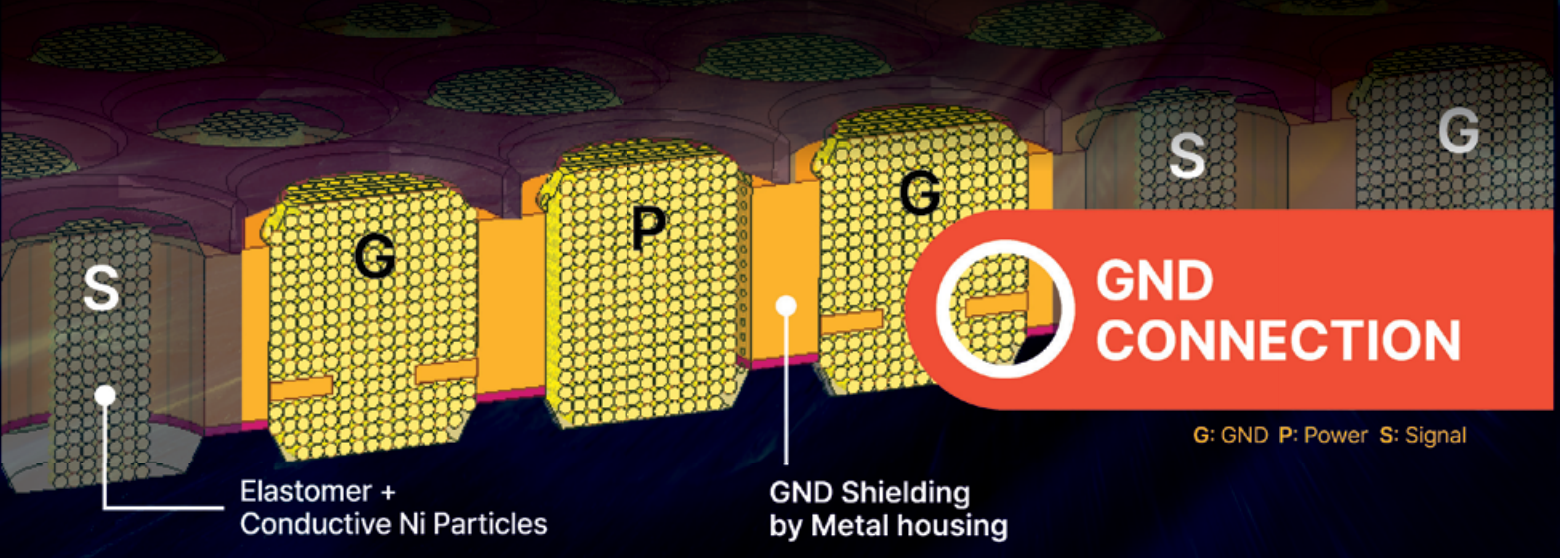

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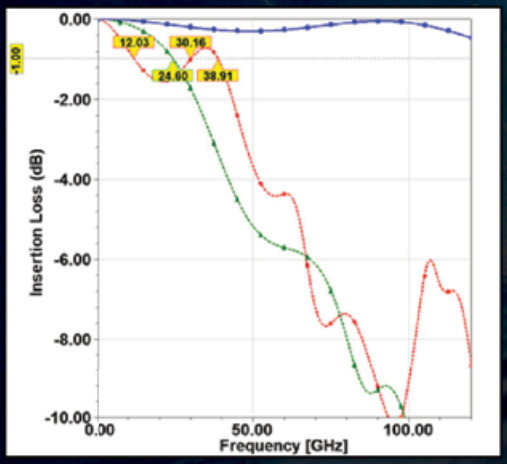
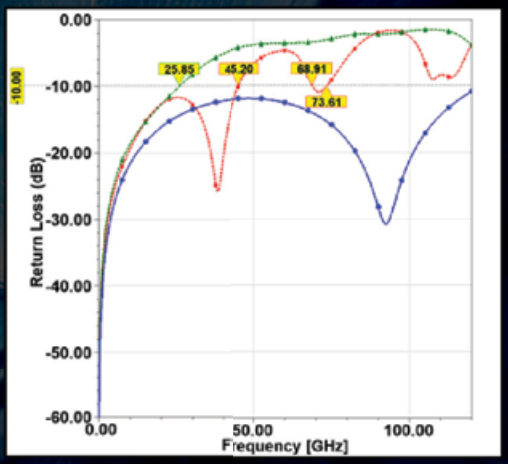
Crosstalk (S31) @-20dB	14.98	9.18	>100



Insertion Loss



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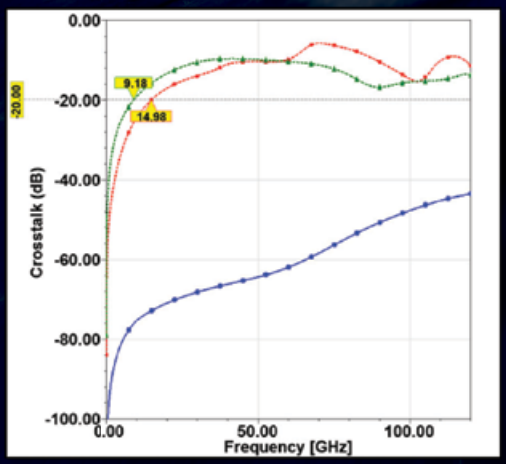

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TSE USA

Jong M. Lee jmlee@tse21.com
Kevin Kim kevin.kim@tse21.com

TSE HQ

Justin Yun justice@tse21.com
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Direct bonding: a key enabler for 3D technologies

By Emilie Bourjot, Frank Fournel [CEA-Leti]

Direct bonding techniques are constantly in evolution to address "More Moore" and "More than Moore" challenges. CEA-Leti has developed expertise in direct bonding since the '90s with the emergence of silicon-on-insulator (SOI) technology. Since then, CEA-Leti teams have continued to actively innovate in direct bonding to widen the application field. This technique is based on the cohesion of two surfaces put intimately in contact at room temperature. Then, van der Waals forces (hydrogen bonds) and capillarity bridges create the needed adhesion energy. A post-bonding annealing changes weak bonds into covalent bonds to make one piece of material at the end. Direct bonding now addresses not only substrate fabrication, but also the 3D interconnections domain with the emergence of hybrid bonding.

This article presents the different direct bonding techniques and their application in the microelectronics industry and R&D as developed by CEA-Leti. In the first part of the article, direct bonding physics are succinctly presented. Then, a summary of state-of-the-art bonding technologies is depicted, including hybrid bonding wafer-to-wafer (WTW), hybrid bonding die-to-wafer (DTW) and III-V heterogeneous bonding. Advantages, challenges, applications and stakes of each technique are compared with respect to the suitable application domain. A third part is focused on the latest hybrid bonding D2W results presented by CEA-Leti at ECTC 2022 and ESTC 2022. Integration challenges are discussed as well as the role of dedicated equipment development. The last section presents the potential markets and associated products, with an example of a chiplet with through-silicon vias (TSVs) and multi-layer stacking.

Introduction

The digitalization of the world is accelerating, which brings new useful services that increase the need for electronic components through a wide range of applications. System-in-package (SiP) and 3D integration schemes enable the possibility to mix different technologies and/or substrate materials together, addressing not only high-performance computing (HPC) applications requiring high-density interconnections, but also cost-sensitive applications (e.g., edge artificial intelligence and Internet of Things [IoT]). Breakthrough innovations are necessary to meet all specifications in terms of substrate materials and/or high-density interconnections. Direct bonding represents a group of technologies that enable the bonding of two substrates vertically. This attribute matches perfectly with 3D requirements because it can be applied to high-density interconnections through hybrid bonding and can mix different materials with tiling. After a brief introduction on our expertise in direct bonding processes, a discussion of state-of-the-art processes for hybrid bonding and heterogeneous III-V D2W bonding is presented. Finally, we highlight the latest hybrid bonding D2W improvements and the critical role of TSVs in 3D integration.

More than 30 years of expertise in bonding

CEA-Leti has developed deep expertise in direct bonding since the '90s with the emergence of SOI technology. From first lab work on oxide/silicon bonding, the technique was developed and maturated at CEA-Leti after the Unibond® SOI wafer was obtained. After more than 30 years, we have developed an international reputation in bonding development, including direct, polymer, thermocompression, eutectic and anodic bonding. Our role is to maturate bonding processes from proof-of-concept to industrialization. More than 50 scientists and engineers are developing new solutions on direct bonding processes and process integration to products and we have more than 135 patents in this field. As such, wide knowledge on bonding mechanisms was built especially in direct bonding, on which fundamental mechanism models for adhesion [1] and adherence [2] have been proposed.

Direct bonding processes

Among bonding techniques, direct bonding is of particular interest for 3D applications. Direct bonding is a spontaneous bonding of two surfaces without liquid adhesive material. Among the different direct bonding technologies, molecular bonding – which implies hydrophilic surfaces – is the most common one. When two hydrophilic surfaces are intimately in contact at room temperature, van der Waals forces, hydrogen bonds and capillarity bridges create the needed adhesion energy to start and propagate this spontaneous bonding.

Just after the bonding, even if some covalent bondings are already present at room temperature, a post-bonding annealing is necessary to increase their density. The adherence energy, which is also called "the bonding energy," increases during the annealing using different physical-chemical mechanisms depending on the joining materials.

Definitively, the direct bonding phenomenon is different from thermo-compression and adhesive bonding, which require, respectively, both temperature and pressure, or an additional material such as polymer to ensure contact between the two surfaces. Direct bonding is a spontaneous bonding and its thermal evolution does not require an external load. It is a self-made bonding. Nevertheless, the price for this phenomenon is the stringent surface requirements of topography, planarity, roughness, and particulate contamination responsible for bonding defects. Surface cleanliness and topography are critical to have a successful direct bond.

Obviously, the direct bonding phenomenon is not limited to hydrophilic surfaces. Hydrophobic surfaces can also be bonded where only weak van der Waals forces are involved for adhesion. The stakes are to manage all surface characteristics to be compatible with the bond type involved. Therefore, in-depth knowledge of bonding physics is required to integrate the most suitable bonding technique to the targeted application.

State-of-the-art direct bonding technologies

Direct bonding offers several possibilities depending on the surface to be bonded: 1) either a homogeneous material surface is bonded on another material, for example III-V on silicon, or 2) a heterogeneous (hybrid) surface composed of a mix of Cu and SiO_2, for instance, known as direct hybrid bonding. Stakes, advantages, challenges and applications depend on the technique that is used; these are summarized in Table 1 and explained in the following paragraphs.

W2W and D2W direct hybrid bonding. Packaging and 3D integration have grown in importance as two of the key technology enablers to compensate for the slowing of two-dimensional scaling associated with Moore's Law. Big players have moved to new architectures, such as chiplets, thanks to the integration of "More than Moore" technologies, such as 2.5D and 3D integration, memory cubes, accelerators and heterogeneous architectures. This integration brings key elements of success with a much larger number of I/O connections, and the trade-off between performance and energy efficiency to advanced 3D system-on-chip (SoC) devices. Hybrid bonding is a good candidate for high-interconnect density because it enables connecting dies using tiny copper-to-copper connections, as opposed to bumps.

To achieve hybrid bonding, a Cu damascene level is adapted to reach the applicable bonding specification after a crucial planarization step is done on both tiers to be assembled. Planarization by chemical mechanical planarization (CMP) is definitely a key process step to ensure high yield. Ultra-low nanotopography must be guaranteed from the millimeter scale (flat die) down to the material scale (flat surface with low roughness) and going through to the micron scale (flat pattern). Enabling this ultra-low nanotopography in the space of the design rules with different Cu densities and Cu pad sizes was a unique challenge that was solved thanks to the achievement of CMP process control of consumables (slurry/pad/diamond disk/recipe parameters). A precise alignment during the direct bonding process is required to achieve the electrical path by joining the Cu patterns together. High-density interconnections can be achieved, with pitches ranging from 10µm down to 1µm.

Direct hybrid bonding offers two configurations of assembly: W2W and D2W (Figure 1). W2W hybrid bonding is already mature for imaging applications—starting with Sony in 2016. It is characterized by the alignment at wafer scale (Figure 2). With the latest generation of W2W bonders, suppliers claim alignment capability below 50nm 3σ. The main advantage is high throughput, but the drawback is low flexibility for design because bottom and top dies need to have the same dimension. For more design flexibility, hybrid bonding D2W is more suitable. This process re-uses the know-how developed for W2W, but it adds dicing and cleanliness challenges. The known good die (KGD) concept can be applied to increase the overall product yield by selecting only good dies before assembling. DTW technology is of great interest for many applications such as edge devices with more and more real-time computing of a large amount of data with a limited power budget. Other "More than Moore" applications are good candidates like photonics with imagers and display for design flexibility, or optic transceivers and radio frequency (RF).

Heterogeneous III-V D2W bonding. While hybrid bonding is addressing Si technologies, other applications need the superior III-V materials' properties (electron and hole mobilities, direct band gap). However, III-V materials are not available in large substrate diameters, thereby closing access to advanced fabs. In addition, raw materials are scarce, making bulk substrates costly. Therefore, new solutions are needed to combine the advantages of III-V materials on a silicon wafer, which refers to heterogeneous III-V D2W bonding here. Two approaches can be considered: on the one hand, the technology (laser cavity, for instance) is performed before the assembly. It has the advantages of having good quality III-V materials and only a small amount of material is bonded at the right place [3].

A second path can be considered in which only a material thin-film template is transferred onto the silicon platform, using direct bonding of III-V coupons on a silicon wafer. The epitaxial device growth, or at least a part of it, could then be done later on the silicon wafer, allowing very narrow inter-device shrinkage [4]—this is called "tiling." This die "tiling" could be done on a sparse area but, in a very interesting manner, using the SmartCut™ technology, a large area could be covered within an industrial

	Stakes	Advantages	Challenges	Application
Hybrid bonding W2W	Interconnection density	Large know-how In production	Topography control of a Cu/dielectric surface	Imagers, memory on memory
Hybrid bonding D2W	Interconnection density Yield Heterogeneous 3D	Design flexibility Yield with KGD	Topography control of a Cu/dielectric surface Alignment Dicing and surface cleanliness	HPC, edge AI, logic
Heterogeneous III-V D2W bonding	Sparse integration of III-V material on silicon devices	Dislocation free III-V materials usually highly processed	Dicing and surface cleanliness	Displays, Imagers, RF, telecom LIFI
	III-Vs tiled on larger diameter silicon substrate	Opens doors to modern fabs Stiffer substrate Saves scarce material	CTE management Dicing and surface cleanliness Design rules Co-integration with Si technology	Displays, Imagers, RF, telecom

Table 1: Stakes, advantages, challenges and applications depend on each technique.

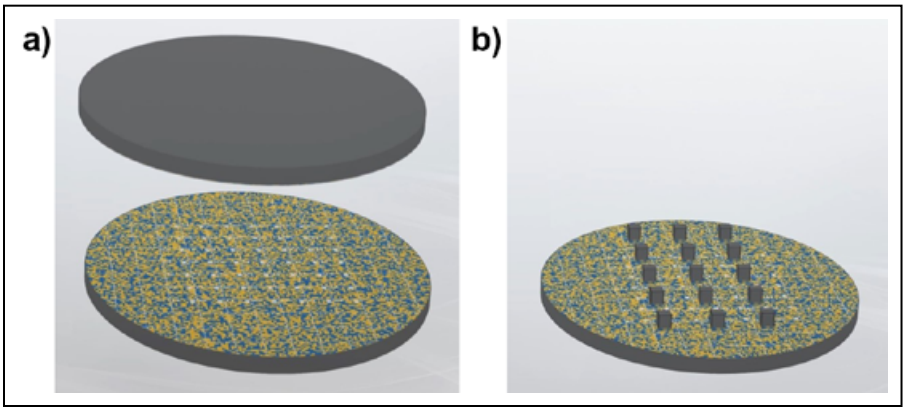

Figure 1: a) (left) W2W and b) (right) D2W bonding. SOURCE: CEA-Leti

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path (Figure 3). Using the SmartCut™ technology involves first tiling III-V dies over a 200 or 300mm silicon substrate. This creates a so-called pseudo-donor wafer paved with dies several hundred microns thick. Second, this pseudo-donor is used to transfer collectively thin layers (100-1,000nm) of III-V dies on another silicon substrate using the SmartCut™ technology. The pseudo-donor substrate can be reused many times. This work is underway jointly with Soitec [5].

For applications using large III-V areas, the SmartCut™ tiling is a breakthrough technology—it breaks the wafer-diameter ceiling and saves scarce material because only a thin layer is used rather than a bulk substrate. This type of tiling will be the key technology to bring these III-V materials into high-volume manufacturing for display applications, for instance. Substrates tiled with thin layers of III-V materials are then provided to foundries for further device processing. In that case, III-V material is present at the front end of the device fabrication process. This brings challenges to co-process III-V materials and silicon, but also opportunities because in that case, III-V and Si devices are next to each other, which facilitates the interconnects.

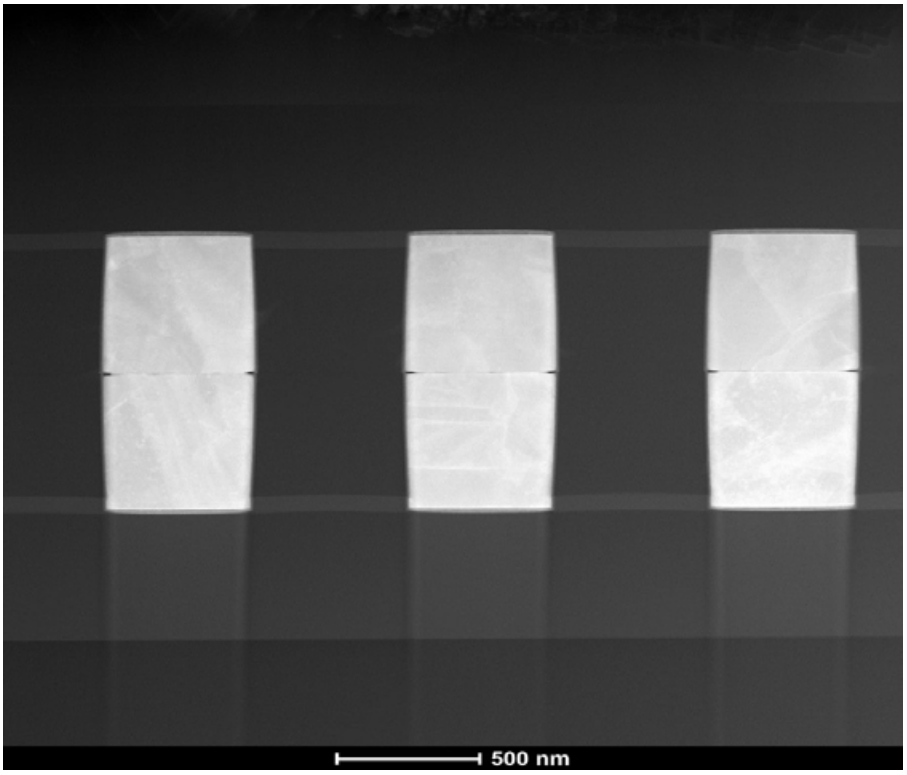

Figure 2: Direct hybrid bonding cross section in W2W. SOURCE: CEA-Leti

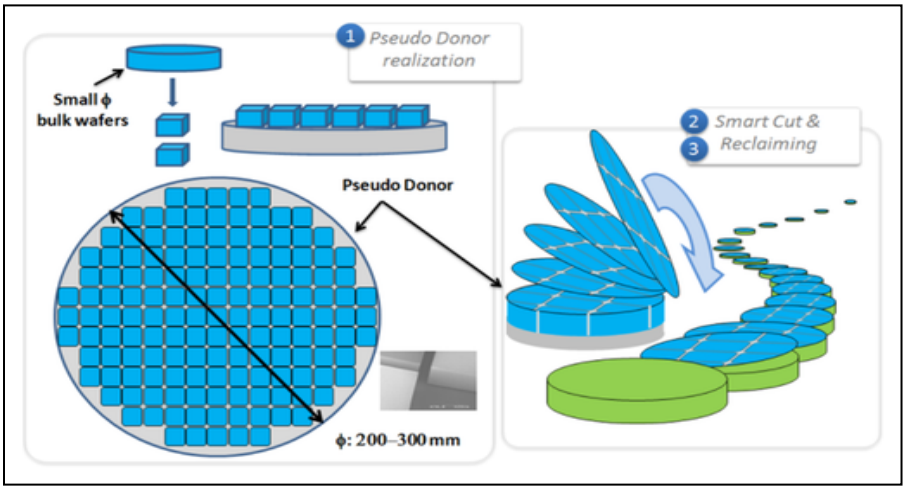

Figure 3: Schematic of the SmartCut™ tiling approach [5].

Recent hybrid bonding D2W improvements

The latest trends featured at ECTC 2022 showed a strong interest in hybrid bonding D2W. (Figures 4-5) [6–9]. Challenges of direct hybrid bonding D2W remain in performance, yield and cost, which are driven by alignment capability, bonding quality and throughput, respectively. Die bonder equipment is, therefore, a key piece for industrialization; it must meet class 1 cleanroom and accurate surface-bonding specifications. A fruitful collaboration between CEA-Leti and SET Corp. enabled emergence of a die bonder specifically designed for hybrid bonding D2W with alignment capability of 1µm 3σ post bonding. It integrates a local clean environment, adaptation of robotics to avoid particulate contamination and precise alignment thanks to its optical alignment capability. Regarding yield, the cleaning post dicing was the other challenge. Regular sawing offers a simple way of dicing dies, but it has a high level of contamination. We have developed an efficient strategy for die cleaning. The combination of those skills enables demonstration of a high-yield level and an alignment capability below <1µm 3σ (Figure 6), after bonding with high electrical yield [8-9]. However, ensuring a high throughput with a high bonding precision remains a big challenge from an economic perspective.

Before explaining the different solutions under investigation, it is important to clarify some definitions of alignment. Machine intrinsic accuracy, die placement accuracy and die alignment post bonding are three components of global alignment. Machine intrinsic accuracy and die placement depend on optics, tool parameters and environment. The die integration characteristics and the alignment measurement method also play a role. Indeed, the best representation of a misalignment is a measurement at two extreme corners of the die. Therefore, the die alignment post bonding depends on all of those parameters.

An accurate alignment takes a long time. Therefore, several approaches exist to increase throughput based on a pick and place (P&P) tool with increased speed or collective bonding. Here, collective bonding refers to pre-aligned dies with a temporary bonding and high alignment

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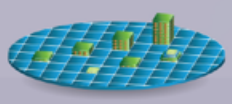

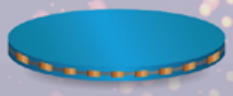

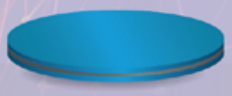

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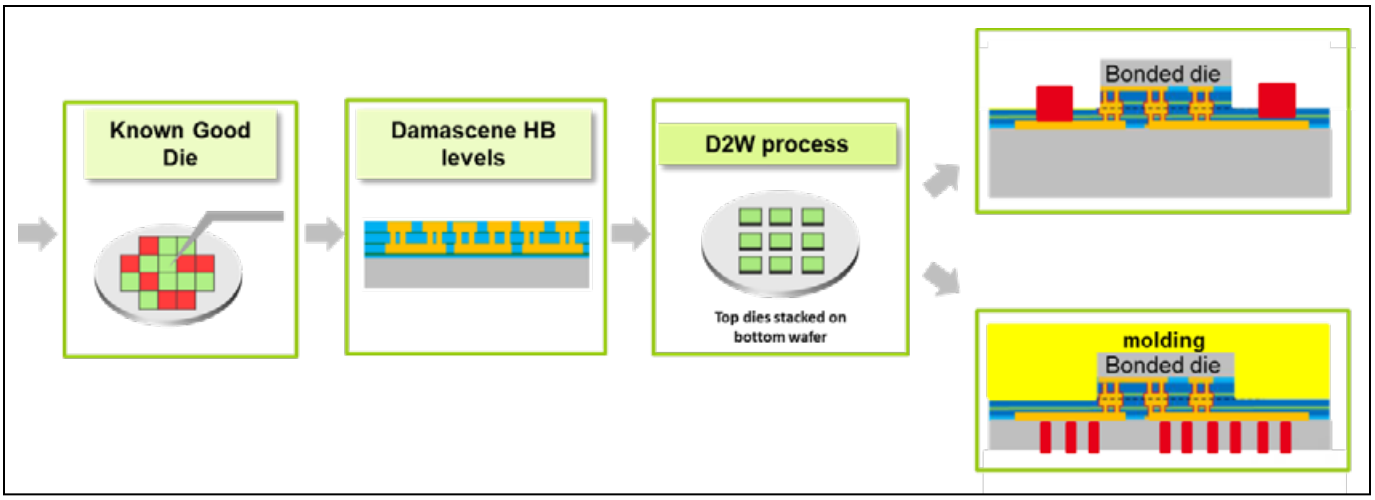

Figure 4: D2W process flow. SOURCE: CEA-Leti

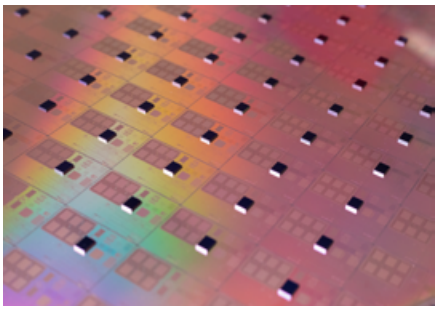

Figure 5: Die-to-wafer. SOURCE: CEA-Leti; COURTESY: P. Jayet

accuracy. The final bonding is then performed collectively by W2W. The alignment is then composed of combined D2W and W2W misalignment errors. The throughput is then limited by the P&P tool used for die placement of the temporary bonding. This solution seems to be limited to solve the D2W throughput issue.

One alternative strategy developed by CEA-Leti in collaboration with Intel is self-assembly (Figure 7). A gross pre-alignment >200µm is performed, while the fine alignment is realized by a water droplet and capillarity forces. This process can be implemented either in collective, or in P&P ways. In the collective way, dies are placed in a holder with a high-speed die sorter at low precision >200µm. All dies are then picked-up simultaneously by droplets and self-aligned. In the P&P, pre–alignment can be coarse enough to reach high throughput. The droplet completes the fine alignment to reach below 400nm 3σ. The throughput could be improved up to 2,000 dies/hour. Dedicated self-assembly equipment needs to be developed in collaboration with equipment suppliers to ensure reproducibility for high-volume manufacturing.

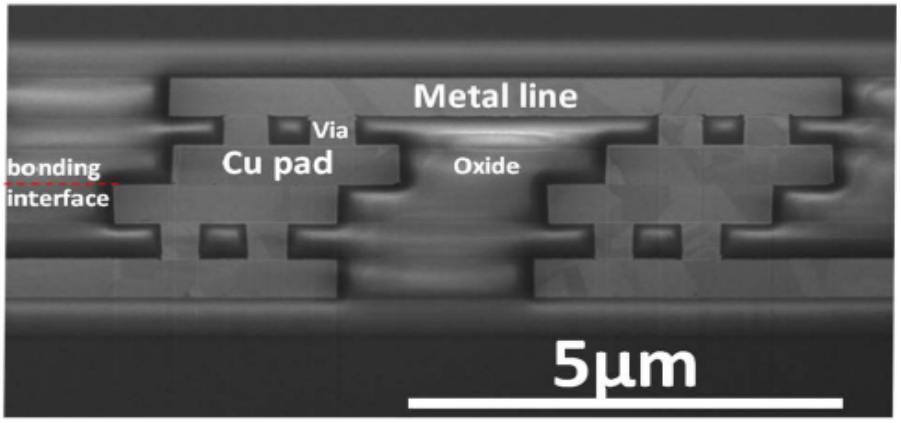

Figure 6: Direct hybrid bonding cross section in D2W. SOURCE: CEA-Leti

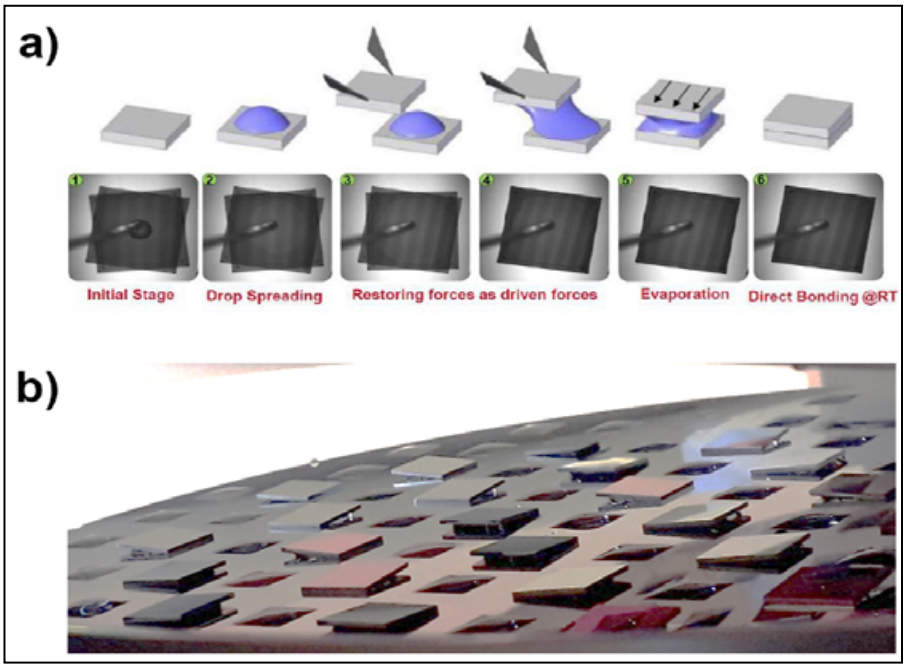

Figure 7: a) Self-assembly process flow; b) self-assembly principle—water droplet used for fine alignment thanks to capillary forces. SOURCE: CEA-Leti

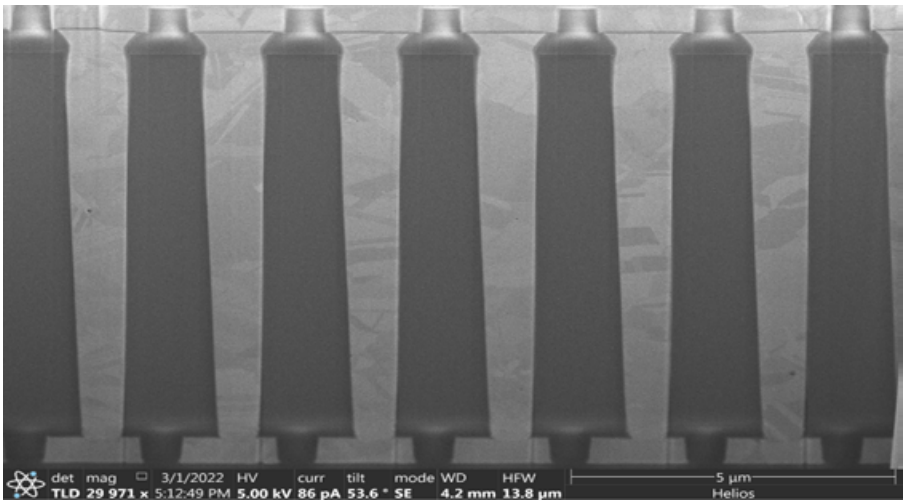

Figure 8: TSV structures. SOURCE: CEA-Leti

Benefits of TSVs for products

Concerning D2W hybrid bonding, it is important to mention the role of TSVs (Figure 8). By nature, systems featuring hybrid bonded types of interconnections will require an access to embedded metal pads and, ideally, in an array format to keep the density for further layer or ball grid array (BGA) connections, for example. An elegant way to access these contacts is the use of TSVs. Depending on the targeted products, several types of vias could be envisioned. For three-layer types of imaging devices [10], high-density TSVs in the range of Ø1µm and 10µm depth will be employed for the inner strata, while for active-interposer types of modules [11], TSV middle processes of Ø5µm to Ø10µm and 50µm to 100µm depth will be preferred. The effective coupling of appropriate TSV and hybrid bonding technologies appears as a strong leverage for the development of products with unprecedented dense interconnection architectures.

Summary

Direct bonding technologies are key enablers for 3D microelectronics. They enable the mixing of exotic material and/or different technologies in one place for performance, design flexibility or heterogeneity. A wide range of direct bonding processes meet several applications' needs, from substrate development to back-end 3D interconnections, and the ability to manage bonding mechanisms and integration. For 3D schemes, direct hybrid bonding in W2W and D2W versions are extremely attractive for increasing high-density interconnection. D2W pushes the assets of hybrid bonding by adding design flexibility and high yield. Challenges to manage the trade-off between throughput and alignment performance. Several process options are in development, such as improved P&P speed and self-assembly, where equipment suppliers play a critical role.

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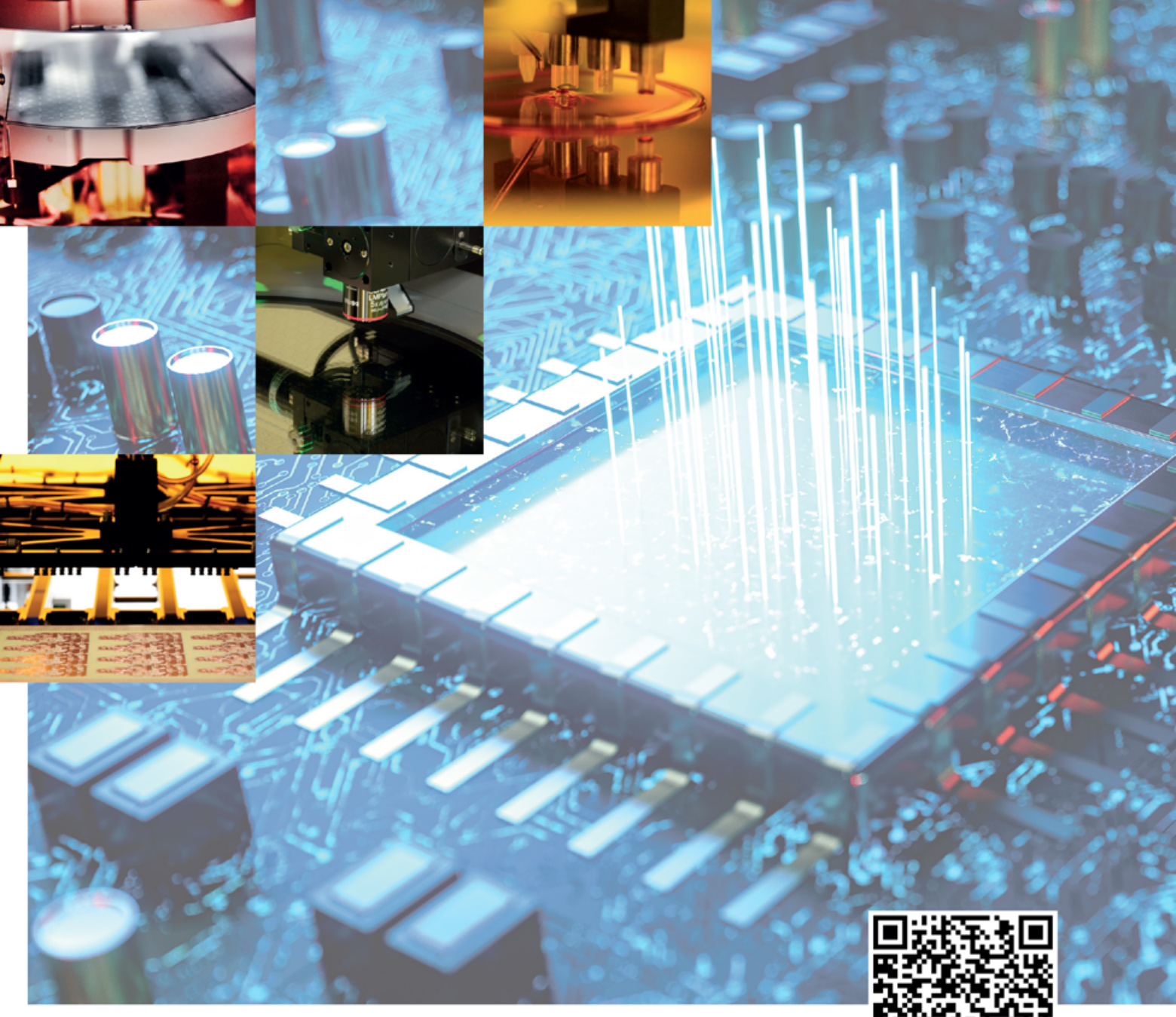
Biographies

Emilie Bourjot is a Project Manager at CEA-Leti, Grenoble, France. Her current activities involve developing advanced hybrid bonding schemes for 3D integration. Prior to joining CEA-Leti, she worked with GlobalFoundries (Germany, USA) and within the IBM Alliance (USA) on the development of advanced FDSOI technologies and sub-3nm nodes. She earned a MSc in Materials Physics from INSA Lyon (France) and a PhD from Aix-Marseille U., France. Email emilie.bourjot@cea.fr

Frank Fournel is head of wafer bonding engineering at CEA-Leti, Grenoble, France, and a board member of the international ECS Wafer Bonding Symposium Conference, the International WaferBond Conference, and the Low Temperature Bonding 3D Conference. He has a Master's in Materials Science from Ecole Supérieure de Physique et de Chimie Industrielle de la ville de Paris (ESPCI) in Materials Science, and a PhD from Grenoble U.



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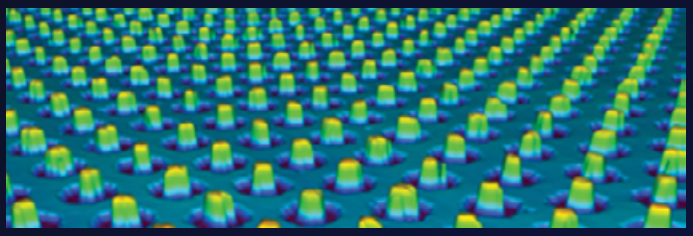

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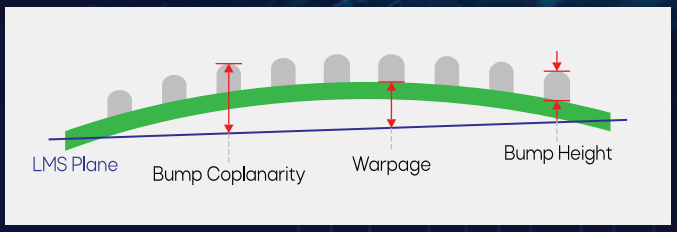

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High-precision die attach: a major pillar of advanced packaging

By Percy Lam [ASMPT Limited]

Over the last decade, semiconductor technology node advancement and the gradual increasing sophistication of advanced packaging have happened in tandem. Commencing with the introduction of embedded wafer-level ball grid array (eWLB) technology by Infineon more than 10 years ago, followed by the introduction of 2.5D packaging known as Chip on Wafer on Substrate (CoWoS®) by TSMC, a growing number of innovations in the arena of advanced packaging have been contributed by major manufacturers. According to Yole Group's advanced packaging market report in 2020 [1], advanced packaging revenue is swiftly catching up to the traditional packaging market. In 2014, advanced packaging (AP) accounted for 38% of the total packaging market. However, its (AP) market share will increase to around 50% in 2025, or around $42 billion. In an 11-year period from 2014 to 2025, AP revenue is forecast to almost catch up with that of traditional packaging.

The AP development roadmap closely follows the path of the advanced node front-end roadmap provided by the three major leaders in the world, namely TSMC, Intel and Samsung (**Figure 1**).

The continued node development from 10nm down to 2nm and even smaller is in question, however, as the commercial returns are not commensurate with the extremely high capital investment required. In order to reduce the financial commitment for future node development, an effective approach is switching from "only front-end node scaling" to "a combination of front-end scaling with back-end scaling." Heterogeneous integration (HI) is the way forward (**Figure 2**). HI is an approach using AP technologies that enable the integration of multiple chiplets with different functionalities and each fabricated using the best fit node in terms of technology and economics, to reassemble a system-on-a-chip (SoC)-like function.

A nontrivial issue usually encountered by foundries or assembly houses using AP to realize the concept of HI is the large variety of die attach requirements needed to meet the ever-evolving AP technologies. High-precision die attach requirements have become a critical factor in accomplishing a successful AP rollout (see **Figure 3**).

Important requirements for die attach tools

In order to actualize the intended advanced package structure, specifying adequate and realistic requirements for die attach tools during the tool selection process is a vital aspect of a quality-first execution strategy. The following sections discuss the applicable requirements for die attach tools.

Die placement accuracy. Capability of higher die placement accuracy depends on machine design of the die attach tool itself (**Figure 4**). Machine cost usually increases with die placement accuracy and is inversely related to productivity. **Figure 4** shows an example of a high die placement accuracy measurement result based on the bond mode of a face-up die where the local alignment is executed by a high-precision die attach tool.

Various bond modes. To support the three bond modes of fan-out packaging, i.e., die first/face up, die first/face down or die last/face down, easy switching among the different modes is a basic requirement. A heated bond collet tool and a heated bond chuck for die attach film (DAF) bonding are required for die face-up bonding at elevated temperatures. Flux dipping for mass reflow flip-chip bonding is an option for redistribution layer (RDL)-first/die-

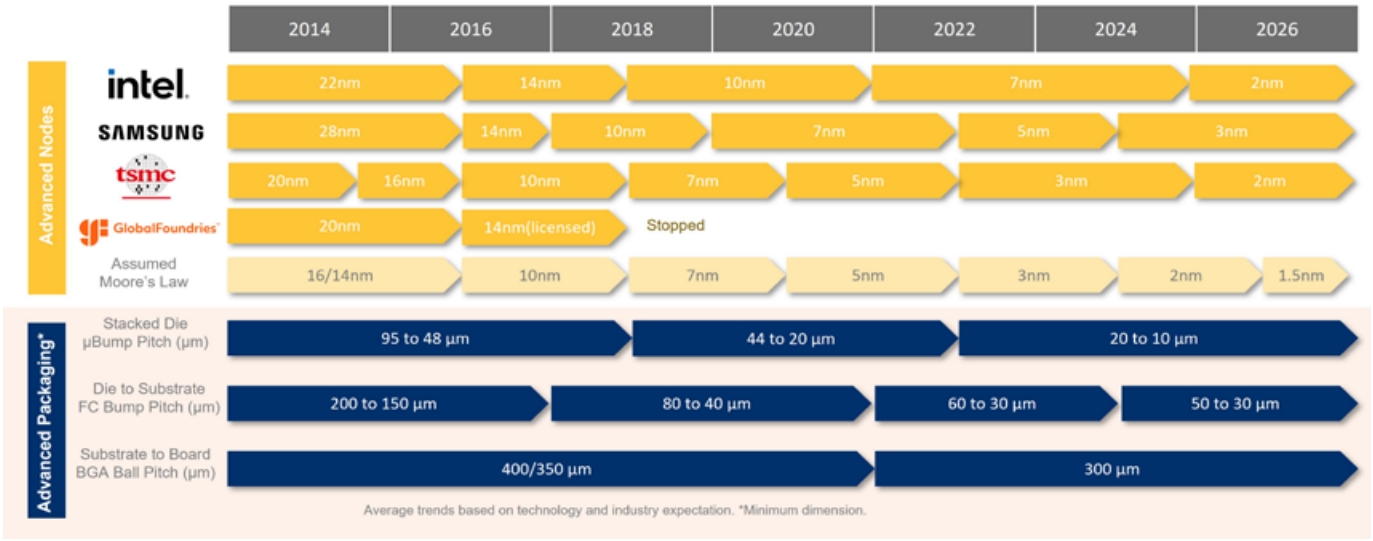

Figure 1: Technology roadmap – front-end manufacturing vs. advanced packaging. SOURCE: Yole Group, 2020 [1]

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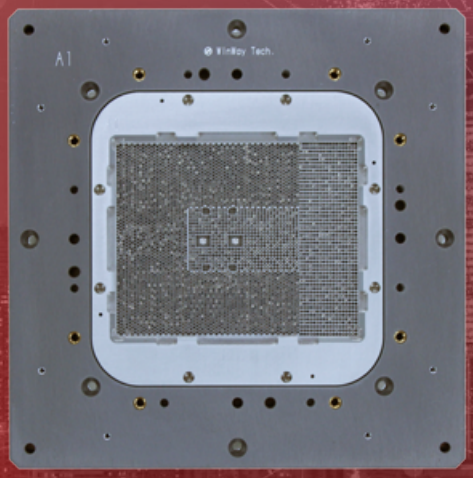

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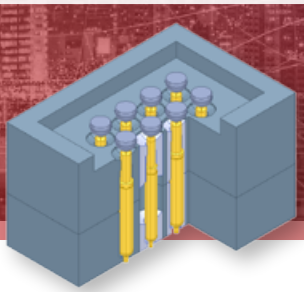
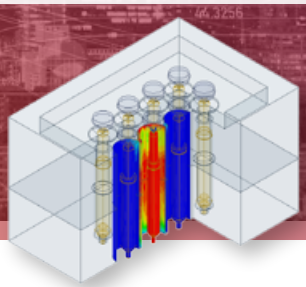
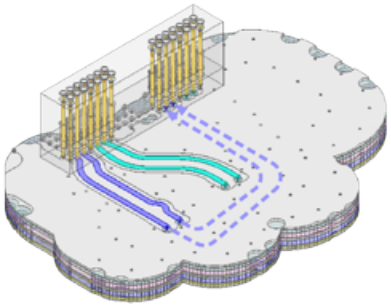


Co-grounding Design



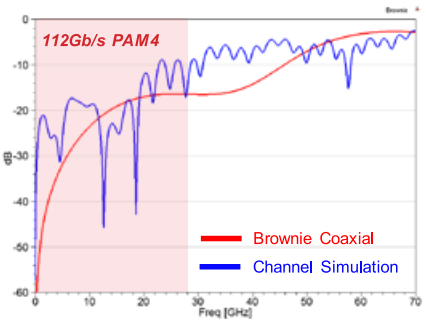
EM Wave

3D Stacking Simulation

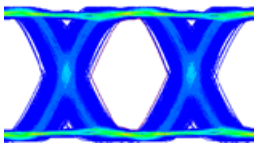
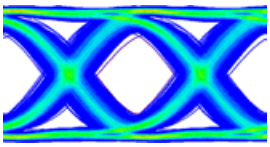
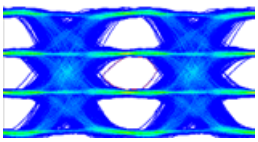
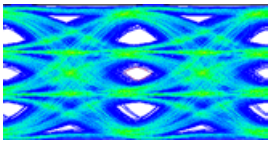


For high speed test application, it's necessary to evaluate the performance of the entire channel at engineering stage to ensure the specifications can be reasonably defined during testing.

Return Loss



Eye Diagram

	Socket Only	Channel Simulation
56Gb/s NRZ		
112Gb/s PAM4		

Solution	Bandwidth	Crosstalk	Impedance (50Ω)
Plastic Socket	<20 GHz	-10 ~ -25 dB	△>10 %
Coaxial Socket	>80 GHz	-50 ~ -70 dB	△3 ~ 5 %

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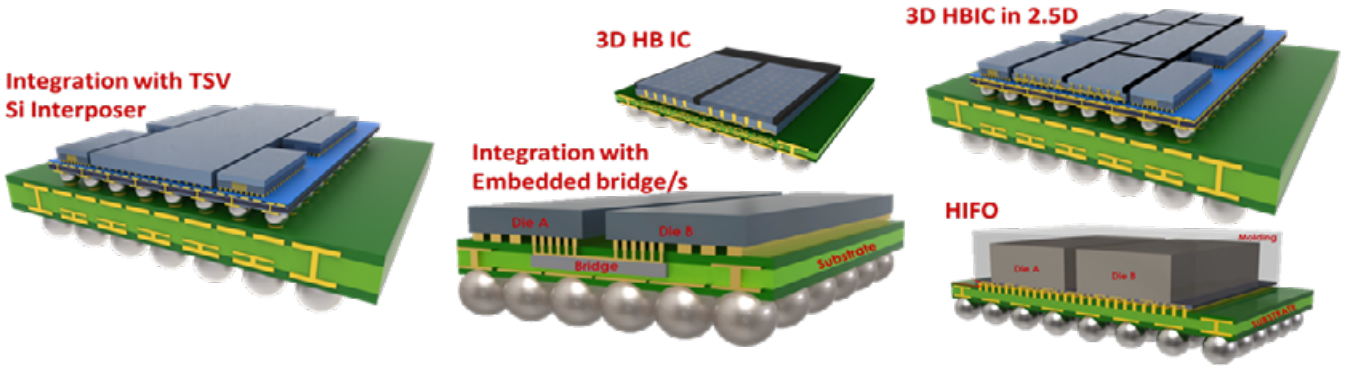


Figure 2: Various approaches of accomplishing heterogeneous integration (HI). SOURCE: ASMPT internal report, 2019

last/face-down mode, which is important for high-density fan-out applications. In the case of thermocompression bonding (TCB), flip-chip bonding with local reflow is a must requirement, though typically, it cannot co-exist with fan-out bond modes.

Die size. Because of the varying die sizes required for different processes, the range of die sizes can vary from 0.5mm x 0.5mm to a size as large as 26mm x 33mm. The size of molded compound die can be up to 70mm x 70mm. It is a challenge for a die attach tool to allow such a large die size variation from pick-up until the attach process on the substrate is complete.

Multi-die requirement. As HI continues to prevail, multi-die packages containing dies of different sizes will become common (Figure 5). The die attach tool should be able to support a single recipe to handle different die sizes. Hardware support required includes tooling designed for different die sizes and the tooling such as the ejector, die pick collet, and die bond collet should be automatically changed. Additionally, wafers of different dies should be automatically loaded from the wafer cassette, without the need for human intervention to support tooling part conversion and recipe program loading.

Thin-die requirement. Because the package profile is another essential factor when considering AP, sometimes die thickness would go down below 50µm. For some specific applications, such as memory die for stacking, as well as bridge die for embedding, the thickness could be as thin as, or less than, 30µm. Normal pin for die ejection might become insufficient to ensure crack-free die pick-up; specially designed needle-less multi-blade ejector technology has been proven to be a high-volume manufacturing (HVM) solution for thin-die handling (Figure 6).

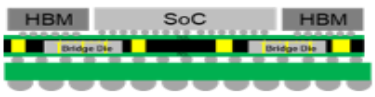
Packaging	Bonding Mode / Requirement	Placement Accuracy Required
 Fan-out SiP	• Chip-to-Wafer (C2W) or Chip-to-Panel (C2P), • Die First & Face-down mode • Global & Local alignment mode • Room Temperature and Elevated Temperature Bonding	C2W: +/-5µm C2P: +/-5~10µm
 High-Density Fan-out	• Chip-to-Wafer (C2W) Face-up DAF Bonding	+/-3µm
	• Chip-to-Wafer (C2W) Flip Chip (Mass Reflow or TCB)	MRFC: +/-3~5µm TCB: +/-2µm and <1µm
	• Bridge Die Bonding by Flip Chip (Mass Reflow or TCB)	MRFC: +/-3~5µm TCB: +/-2µm and <1µm
	• Bridge Die Bonding by Face-up DAF Bond	+/-1 to 5µm
	• Chip-to-Substrate (C2S), Compound Die Flip Chip (Mass Reflow or TCB)	MRFC: +/- 5µm TCB: +/-2µm
 2.5D Packaging	• Chip-to-Wafer (C2W) Flip Chip (Mass Reflow or TCB)	MRFC: +/-3~5µm TCB: +/-2µm and <1µm
	• Bridge Die Bonding by Flip Chip (Mass Reflow or TCB)	MRFC: +/-3~5µm TCB: +/-2µm and <1µm
	• Bridge Die Bonding by Face-up DAF Bond	+/-1 to 5µm
	• Chip-to-Substrate (C2S), Compound Die Flip Chip (Mass Reflow or TCB)	MRFC: +/- 5µm TCB: +/-2µm

Figure 3: Examples of major advanced packaging and placement accuracy requirements.

Bond force. Depending on the bonding material property, bonding processes and die sizes, the required bond force may vary across a large range. For fan-out applications, a bond force ranging from 0.5N to 30N is usually sufficient to cope with most of the requirements. In the case of TCB, the required bond force can be as high as 300N.

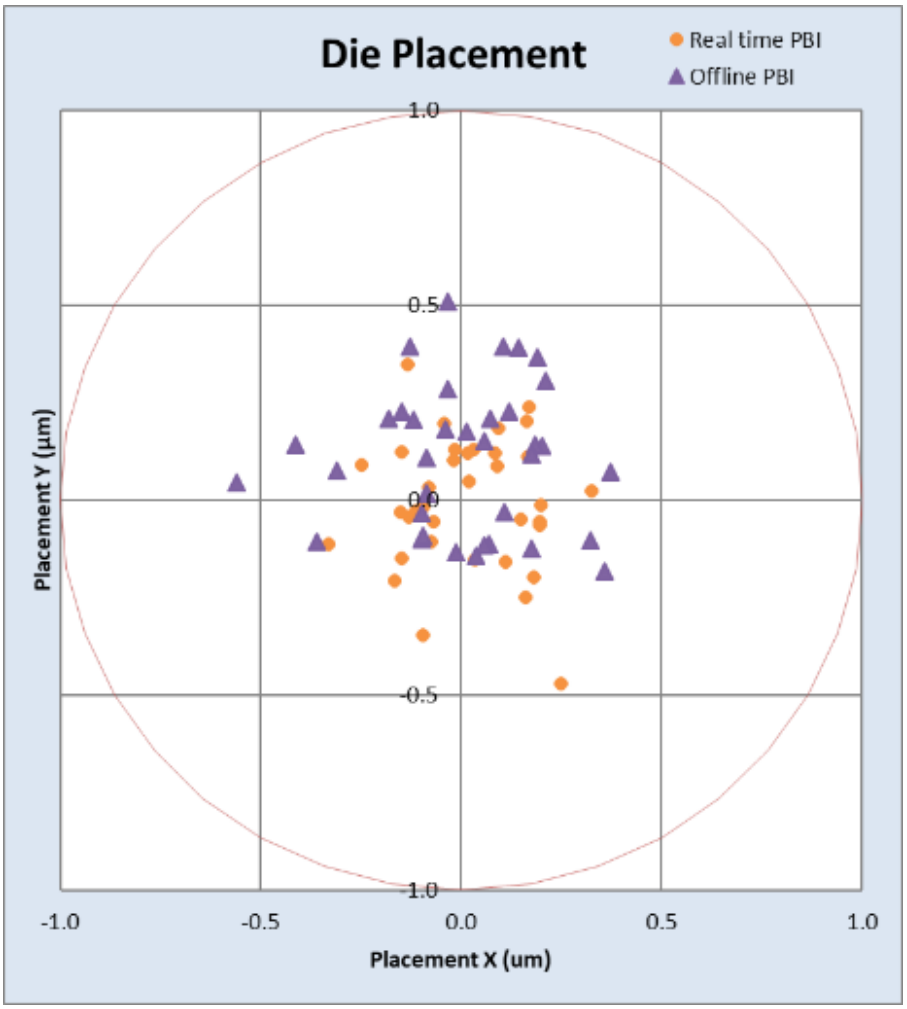


Figure 4: Die placement accuracy of 1µm. SOURCE: ASMPT internal report, 2019

Substrate dimensions. Substrates can be 12-inch wafers or glass carriers, 300mm x 300mm metal carriers, 50mm x 50mm singulated substrates, or 600mm x 600mm metal carriers. Die attach tools are typically classified as wafer-level (12-inch wafer or 300mm quad panel) or panel-level (up to a 600mm x 600mm panel); consequently, the maximum substrate dimensions must be considered while selecting a die attach tool.

Cleanliness. Class 100 is the most common cleanliness requirement for a die attach tool for AP. Certainly, demand for a higher degree of cleanliness up to Class 1 is now being required for emerging applications, and the process cost of ownership will be reflected in the technology requirement.

Inline automation. Automatic material load/unload by means of overhoist transport (OHT) or automatic guided vehicle (AGV) is recommended, especially when preparing for HVM. Semiconductor Equipment Communication Standard (SECS) and the Generic Model for Communications and Control of Manufacturing Equipment (GEM) are the basic standards that apply to communications between the die attach tool and equipment automation (EAP) host.

Traceability. Traceability is one of the most important manufacturing control requirements in HVM especially when the product is for automotive applications. Basic information such as: wafer, substrate, bonding parameters, and inspection results of all production activities, is allowed for access, storage and uploading to the manufacturing host computer database.

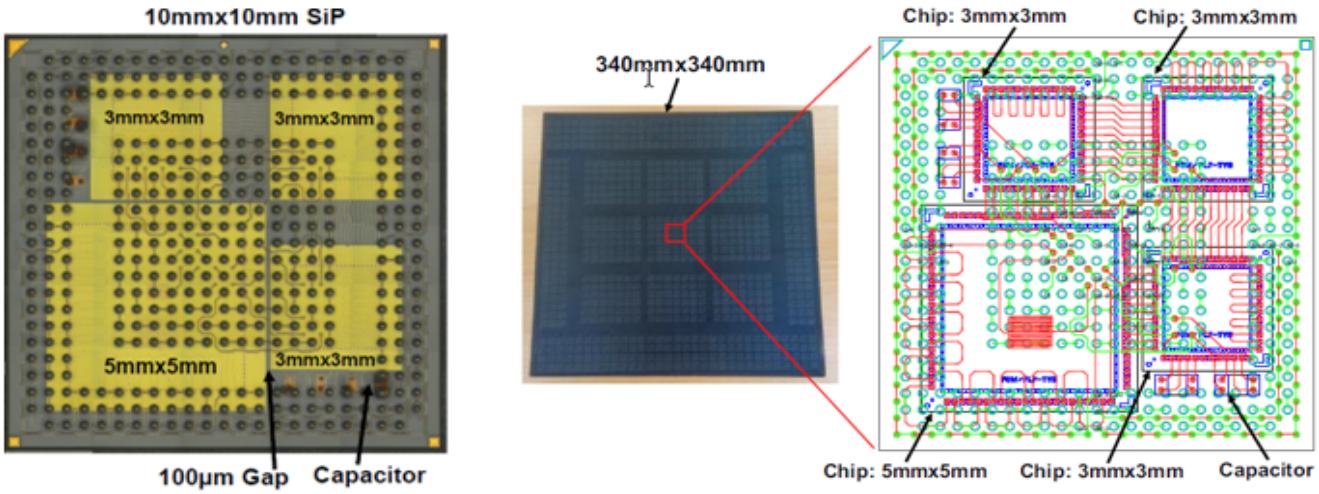


Figure 5: Multi-die fan-out package. SOURCE: [2]

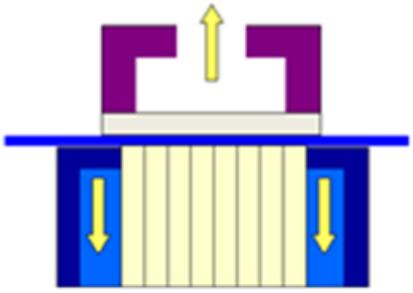


Figure 6: Needle-less ejector system for handling thin-die pick up. SOURCE: ASMPT

chemical shrinkage of the EMC, the CTE of the carrier, gravity, the debonding process, etc.

- The die shift caused by the CTE mismatch between the EMC and silicon, which is also influenced by chemical shrinkage of the EMC, the type of EMC, and the thermal release tape in use.
- The amount of die shift compensation that can be accomplished by using intelligent offset introduced during the die attach process (see Figure 7).

Die systematic shift. During encapsulation of a die-attached substrate, die shift may happen and can be found after debonding of the molded substrate (Figure 8). Oftentimes, the trend of die shift can be observed to be systematic. The major contributing factor is material-related shrinkage of the carrier, adhesive and EMC. Fortunately, the issue can be predicted and compensation provided during die pick-and-place (Figure 9).

Wafer substrate warpage handling capability. Substrate handling is often complicated by substrate warpage.

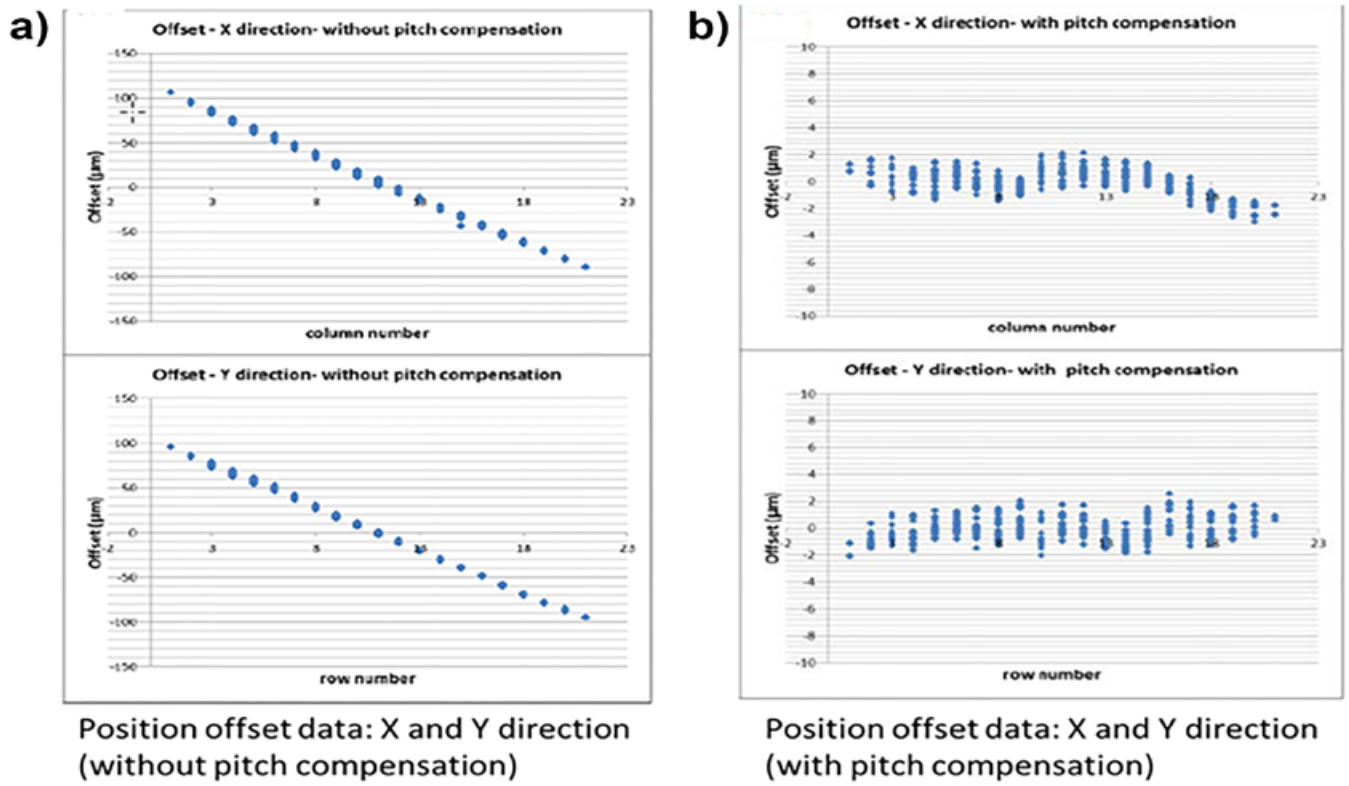


Figure 7: Die systematic shift position offset data in the X and Y directions: a) without pitch compensation; and b) with pitch compensation. SOURCE: [3]

Challenges with the die attach process

The following sections discuss the challenges associated with the die attach process.

Die shift in fan-out packaging (wafer- and panel-level fan-out). There are still many different aspects of process, material and equipment development needed for further improvement of fan-out packaging quality and yield improvement. The major challenges are as follows:

- Warpage caused by a mismatch between the coefficient of thermal expansion (CTE) for the epoxy mold compound (EMC) and silicon.
- Impact on the process caused by

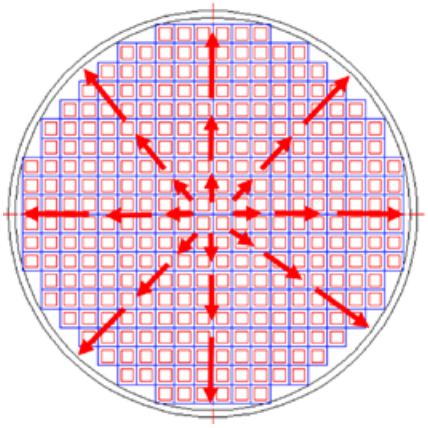


Figure 8: Directions of die shift from the wafer's center. SOURCE: ASMPT

Oftentimes substrate warpage can be as large as up to five millimeters. This serious issue is basically related to the complicated structure for the AP application where it is no longer a bare silicon or glass carrier. For example, the substrate can be fabricated with multilayer RDLs with asymmetric metal density. Or, the substrate can have unevenly distributed embedded components. Such structural differences will lead to warpage either at room temperature or at elevated temperatures. Machine design, therefore, requires appropriate attention to such mechanical and process considerations (Figure 10).

Flux-cleaning issue. When the die size increases and the bump pitch

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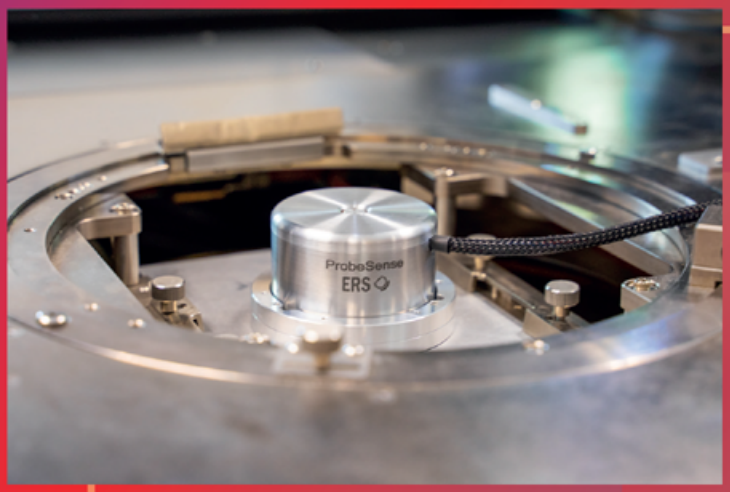
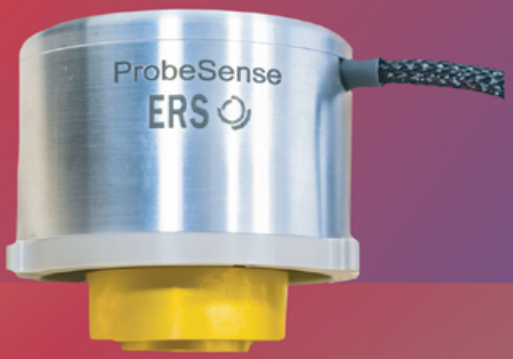


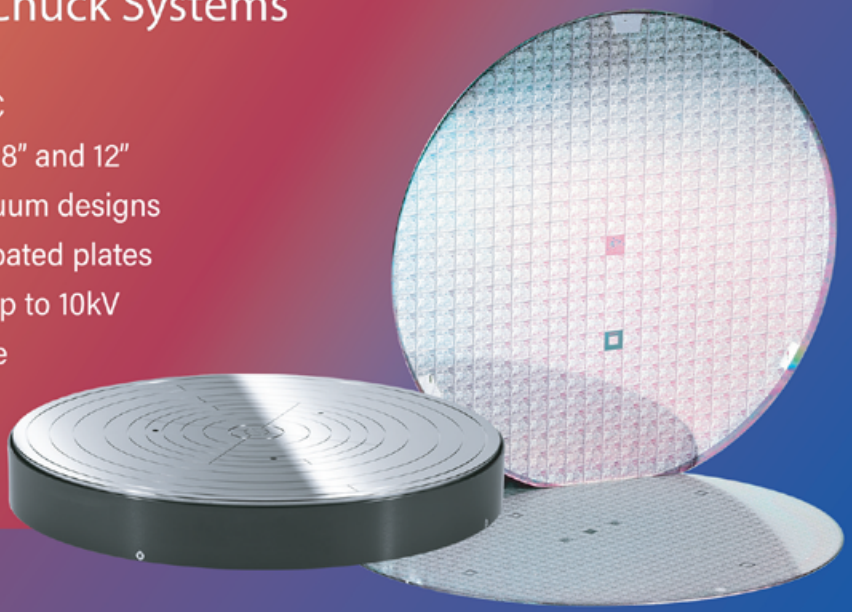


- Can be fully automated
- Robust and easy to recalibrate offline
- Highly repeatable calibration processes according to ITS90 and ISO 17025
- Temperature range: -65°C to 300°C, ice-free at cold temperatures
- Temperature accuracy below 30mK

ERS

Thermal Chuck Systems

- -65°C to 550°C
- Available in 6", 8" and 12"
- Individual vacuum designs
- Nickel/Gold coated plates
- High voltage up to 10kV
- Ultra-low noise
- Anti-magnetic



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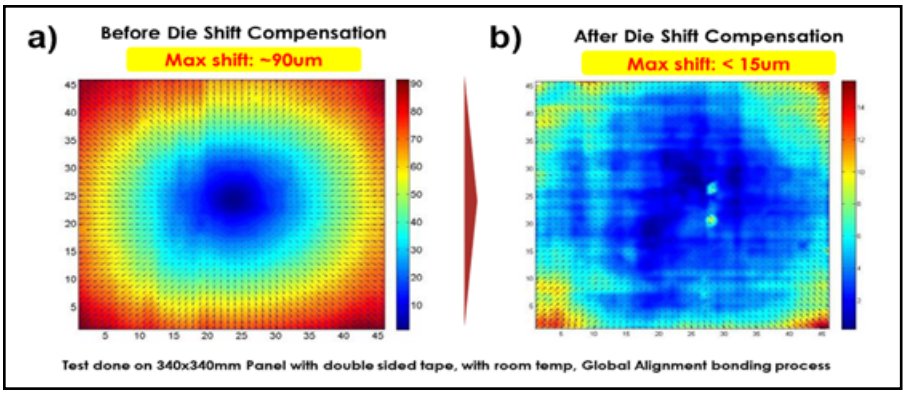

Figure 9: Die shift compensation by Nucleus FOWLP die bonder: a) before die shift compensation; and b) after die shift compensation. SOURCE: ASMPT

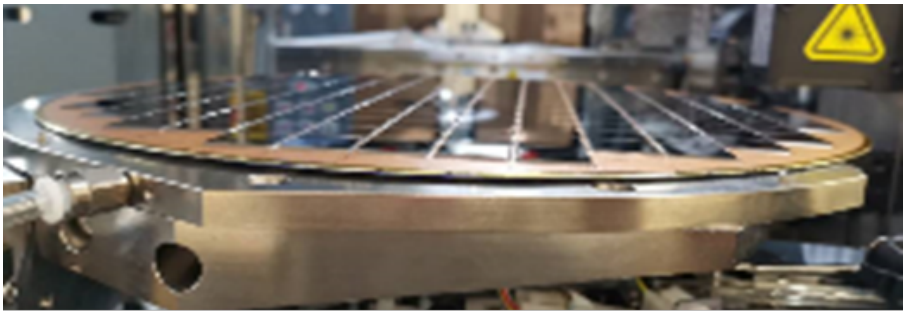

Figure 10: Wafer substrate warpage on a vacuum chuck. SOURCE: ASMPT

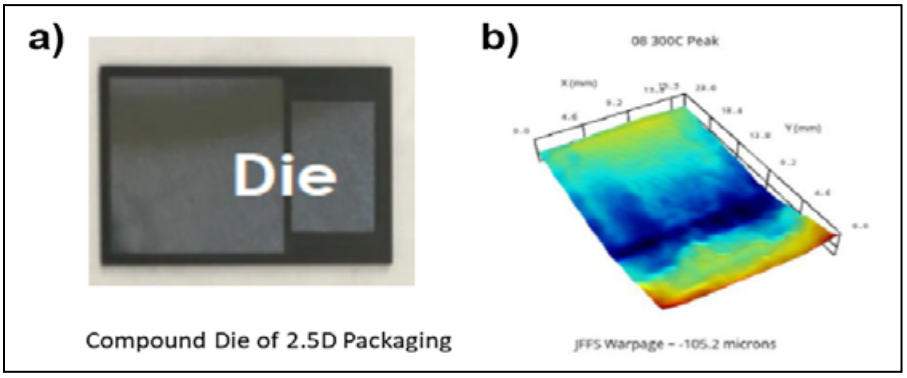

Figure 11: a) Compound die in a 2.5D package; and b) warpage scan image. SOURCE: ASMPT

decreases as a result of advanced node development, there are technical issues in removing all flux from beneath a die after die attachment via TCB. If flux residue remains beneath a die and is transferred to subsequent processes, the final yield will be reduced. The method of "flux-less TCB" is currently under development and it can be a solution for the above issues.

Large compound die handling issue. When the development trend of 2.5D packaging is toward including more chiplets in the same package, the compound die size increases to three, or even four times, the size of a reticle. Flip-chip bonding of extra large compound die on a substrate will become increasingly difficult as the size of compound die increases. A compound die consists of different-sized and thickness silicon dies and an EMC. The CTE values of silicon and EMC materials have a considerably wide range, therefore, die warpage will be compounded due to the differing degrees of expansion of the silicon and EMC materials.

Design of a die attach tool to handle an extra large compound is essential in ensuring good bondability and yield as follows (**Figure 11**): 1) Ensures temperature uniformity for a large heater for handling the extra large compound die; 2) Ensures warpage control by mechanical means; 3) A customized tooling design follows the characteristics of a particular compound die; and 4) Enables analysis of potential die crack/stress issues when handling a compound die from pick-up to attachment on the substrate

Summary

To enable heterogeneous integrations during the development of advanced packaging, a technique requiring high-precision die attach is necessary. The rising requirements of advanced packaging – in tandem with the development of advanced nodes – have raised the bar for high-precision die attach capabilities. In the new era of advanced packaging, selecting a dependable and long-term partner in equipment development to accomplish the arduous demands of advanced packaging development should be a top project goal.

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Biography

Percy Lam is Sales Manager at ASMPT Limited, Hong Kong, with responsibilities of product management and business development in the Advanced Packaging Technology Equipment sector. Areas covered are die attach solutions for FOWLP/PLP, with a focus on promoting package assembly equipment solutions for heterogeneous integration applications. He graduated from the Chinese U. of Hong Kong, majoring in Electronic Engineering. Email: percy.lam@asmpt.com

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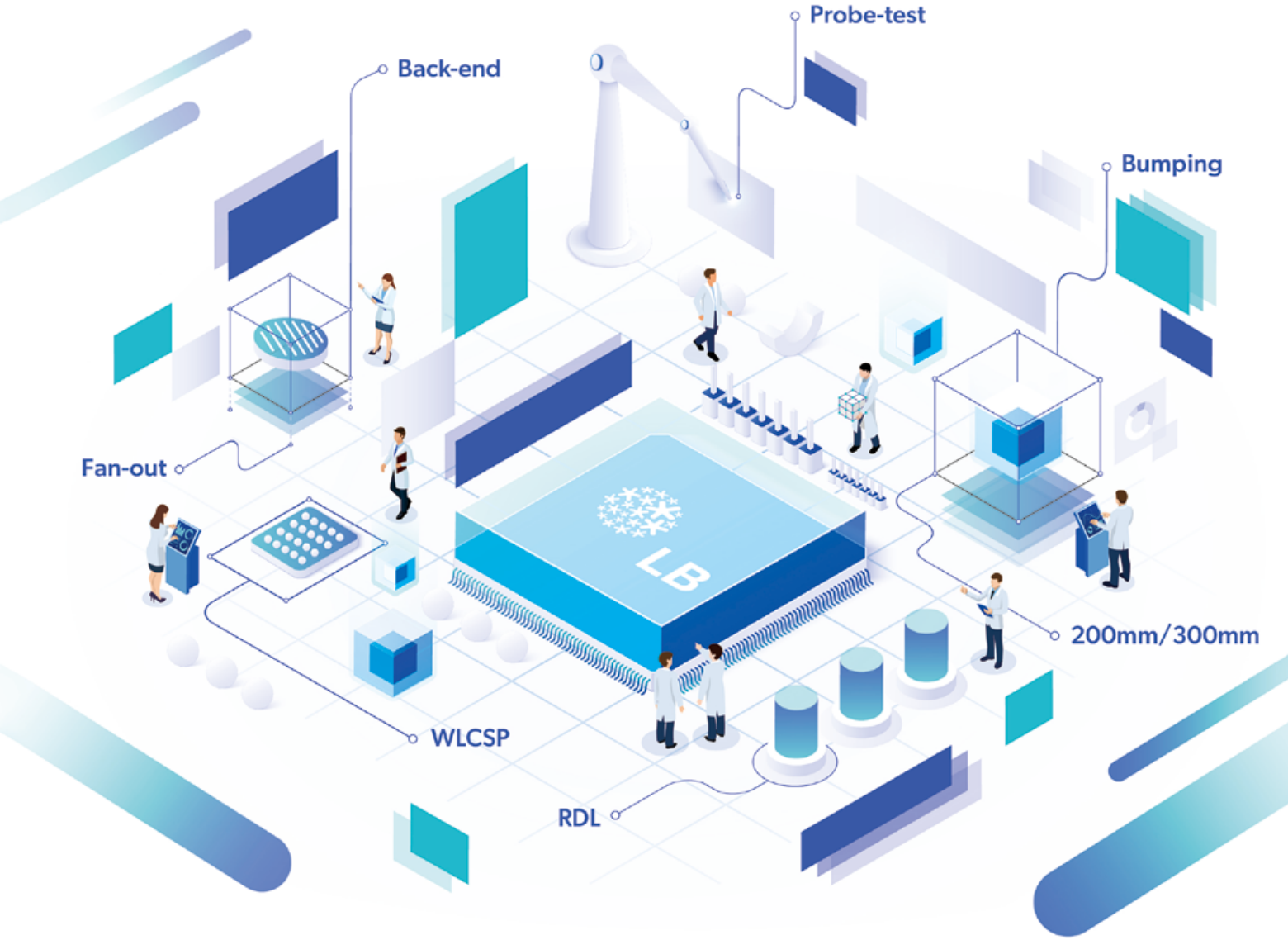

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Double-sided SiP for 5G and wearable applications

By David Wang, Mike Tsai, J. Y. Chen, YP Wang [Siliconware Precision Industries Co., Ltd]

The trend in medical wearable devices – such as those used for collecting medical data (e.g., heart rate detection, electrocardiographs (ECGs), and various sensors) – requires small form factor devices, smaller module sizes, multi-IC and component integration, low power consumption, and better heat dissipation. The module size of the single-sided system in package (SiP) device no longer meets these next-generation requirements. The double-sided SiP structure, however, is expected to provide solutions for more diverse applications of wearable products in the future. The double-sided SiP structure utilizes double-sided surface mount technology (SMT) and dual-sided molding to shrink the overall module size. Furthermore, it can be reduced in size so that it is about 40~60% lighter and thinner than single-sided SiP devices to improve power supply efficiency and reduce noise emission.

In this article, we report on tests conducted on double-sided SiP structures to assess module-level warpage and thermal dissipation performance. The simulation and experiments included a design of experiments (DOE) on the molding process using different molding compounds. Regarding thermal performance, a solution was found that can improve performance 24~38%. The double-sided SiP module can provide an advanced solution to address the module size, cost, performance, and time-to-market requirements for internet of things (IoT) devices and the wearables market.

The study described in this article will also demonstrate that the package die strength of the double-sided SiP structure can be improved by selecting the proper strip grinding process. The extra low-k (ELK) material stress performance using a 3-point test methodology was also studied so as to select the suitable double-sided SiP structure for the end product of the board-level manufacturing process. From an electrical integration point of view, a shorter signal transmission path is required to get good electrical performance (i.e., signal integrity [SI] and power integrity [PI]) rather than a side by side flip-chip based structure. The performance verification was confirmed by simulation and measurement. The reliability testing verification includes temperature cycle testing (TCT), high-temperature storage life testing (HTSL) and unbiased highly accelerated stress testing (u-HAST) performed on the double-sided SiP structure.

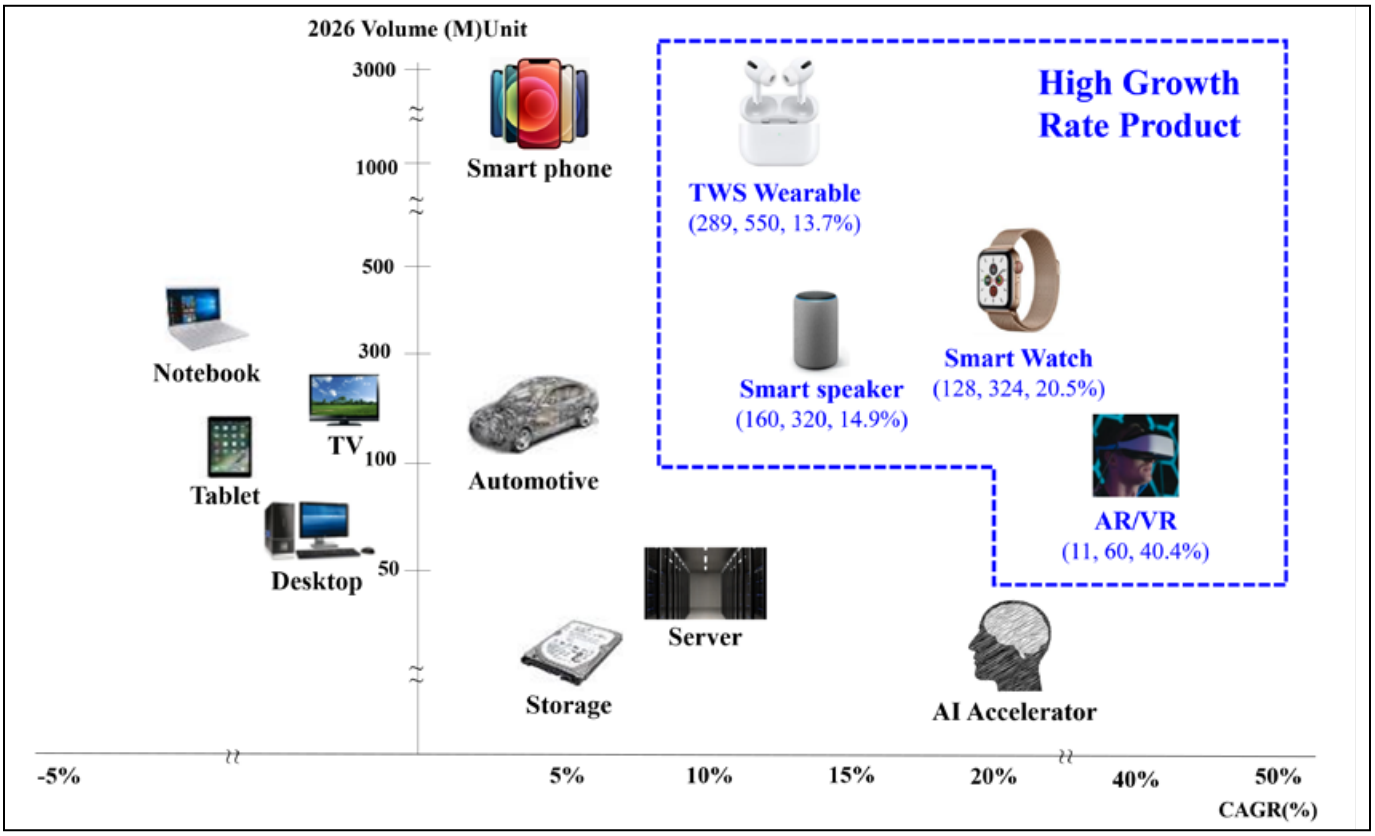


Figure 1: Market volume and SiP application. SOURCE: 2021 Vol., 2026 Vol., '21~'26 CAGR, PRISMARK

Introduction

The mobile phone and tablet computer markets have matured. The next fast-growing markets will be IoT and wearable devices. These products require a small size, a thin profile, good electrical properties and multi-functional requirements. From the perspective of packaging development, and keeping in mind the need for high-volume manufacturing of electronic products, the processing speed, and the required electrical characteristics, system on a chip (SoC) has been established as the key development direction for future electronic product design. However, with the increasing cost of SoC production in recent years, its development faces a bottleneck, therefore, the development of SiP is getting more attention by the industry.

In general, either die split (with the same function) or die partition (with a different function) will be the most effective methodology to reduce wafer cost, provide a small form factor, and realize the required product time-to-market. Chiplet integration is the way to make chips work as though they were one chip while actually being composed of several smaller ones. Chiplets are widely used to keep improving system performance despite the fact that traditional Moore's Law scaling is nearing its end.

Moore's Law is quickly approaching its limitations—its getting more difficult to reduce feature sizes. Heterogeneous integration by way of SiP, 2.5D/3D and fan-out solutions are driving the "More Than Moore" concept. The definition of heterogeneous integration includes single-chip, multi-chip, integrated photonics, microelectromechanical systems (MEMS), sensors, and radio-frequency devices. These packaging solutions are available today to make next-generation products a reality. SiP technology realizes the characteristics of light, thin, short, multifunctional, and low power consumption of the entire range of electronic products. The rise of lightweight products such as mobile devices and wearable devices make SiP an increasingly important packaging solution.

The current market share of smart watches indicates that the future of this market segment is still promising and also contributes to the trend toward SiP packaging. An advanced SiP package can reduce module size and enhance the system power. For example, a key item is connectivity with respect to receiving data from the network. The different application groups and their growth rates are shown in Figure 1. SPIL has learned from market trends that future packaging technologies will depend on increasing functionality and miniaturization. Using different assembly technologies to integrate and miniaturize components into a single package is similar to integrating active and passive partitions from other packaging platforms. The SiP platform can provide a good solution to meet performance, size, and low cost while also meeting the miniaturization requirements of each product and extend it to other applications such as IoT sensors, mobile phones, consumer products, and the automotive industry.

Double-sided SiP structure (structure 3-2)

The following sections discuss thermal dissipation performance and warpage performance of structure 3-2/double-sided molding + thermal insulation material (TIM) (see Figure 2).

Thermal dissipation performance verification. 2D and 3D integration approaches are compared side by side with respect to assembly methodology to reduce the size and space during the product layout arrangement stage (see Figure 2). A standard SiP package structure (Structure 1) is shown in Figure 2. Its advantage is that it uses the mature SMT process, but the tradeoff is the design layout limitation due to the side by side placement. Other key concerns are the small form factor as well as the thin thickness requirement that is limited on a single-sided SiP. A double-sided SiP with one side molding (Structure 2) can provide a smaller package (PKG) size, but thermal performance is the major challenge. Double-sided SiP modules (Structures 3-1, 3-2) have very small component to component spacing (40~60% smaller) and a one time molding technology. Compared to structure 2, both structures 3-1 and 3-2 with thermal pad and TIM, respectively, provide solutions that offer high heat dissipation.

The double-sided SiP thermal test vehicle was designed with 2 × 2mm thermal measurement test die on the bottom side. The junction temperature of the thermal test die is measured through epoxy molding compound (EMC) material and a thermal e-pad to verify the thermal dissipation performance result, which is directly correlated to the simulation data collection. The thermal PCB was designed in 4L PCB (4"x4.5") and measured under still air conditions with the power at 1W. Junction-to-air resistance (θJA) defines the heat flow between the chip's surface and air. Junction-to-board resistance (θJB) defines the heat flow between the chip's surface and the board's surface. The unit is mounted on a measurement printed circuit board (PCB) and connected with measured output I/O.

The simulation result shows a worse θJA with a 1.3x ratio and the θJB with 1.2y ratio by using a normal EMC (K=1W/mK) compared to a single-sided SiP. A

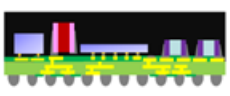
Item	Structure 1	Structure 2	Structure 3-1	Structure 3-2	Structure 3-3
Feature	Single Side	Double Side	Double Side Molding + Thermal Pad	Double Side Molding + TIM	Double Side Molding + EMI
Package Structure					
PKG Size	100%	Reduce 40~60%			
Thermal Solution	NA	NA	Add Thermal Pad	Add Thermal Interface Material	NA

Figure 2: Comparison of different SiP design structures.

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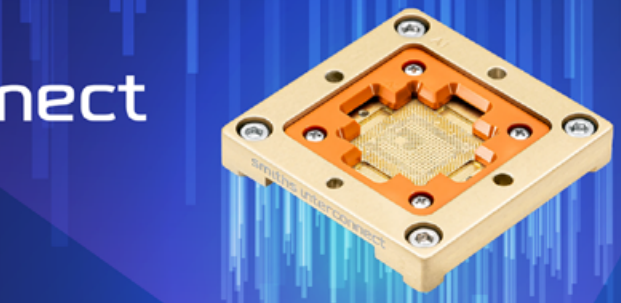
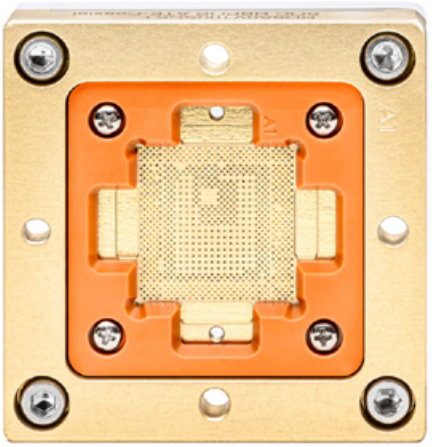


Cutting-edge Connectivity

DaVinci Micro Test Socket

The coaxial structure of the DaVinci Micro test socket provides ideal pin to pin isolation reducing the effect of cross talk during testing. This allows for at speed functional testing of your IC.

- Controlled impedance interface
- Spring probe technology with homogenous alloy, protects against solder build up and increased probe life
- Optimized for power integrity of DUT
- Patented insulated metal socket housing provides un-matched mechanical strength
- For use with manual test, bench test and HVM Production testing using the same socket



DaVinci Micro inherits the DaVinci coaxial technology for IC applications to 350µm pitch. DaVinci Micro's fully shielded signal path negates the effects of cross-talk during testing, allowing an immediate yield enhancement over non-DaVinci products.

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double-sided SiP – by using high thermal EMC material (K=2.5W/mK) – achieves a 20% θJA (1.1x) thermal enhancement, and a 30% θJB (0.9y) thermal enhancement when compared to using a normal EMC material (K=1.0W/mK). When a thermal interface material (TIM) is used (Ag epoxy with 25W/mK), the simulation data shows the 0.99x θJA ratio with a 24% thermal enhancement and a 0.75y θJB with a 38% thermal enhancement.

Warpage performance verification. Another key challenge of the proposed double-sided SiP platform is warpage performance. The DOE design factors are defined as standard normal EMC, thermal EMC type factor and TIM material. The package warpage performance is measured using the Shadow Moiré methodology (JEDEC standard). The normal EMC with TIM has a better warpage result (room temperature: -10µm; high temperature: 13µm) than using a high thermal EMC material without a TIM (room temperature: -16µm; high temperature: 8µm). The difference in these two results is due to the low coefficient of thermal expansion (CTE) mismatch during molding of the structure. Based on the signed warpage chart result, three legs are within the JEDEC warpage requirement (max. 80µm). And both instances of the normal EMC with a TIM can pass the warpage requirement for the double-sided SiP structure.

Double-sided SiP structure (structure 3-3)

The sections below discuss electrical performance verification and structural strength analysis of structure 3-3/double-sided molding + EMI (see Figure 2).

Electrical performance verification. Structure 3-3 shown in Figure 2 and the process flow shown in Figure 3 are responses to the demand for miniaturization of products. Figure 3 provides examples of SiP structure designs from single-sided SiP to double-sided SiP that enable the reduction in package size from 5.00 x 5.40mm (27mm^2) to 3.60 x 3.65mm (13mm^2). The high degree of integration along with achieving the required performance are achieved by using a double-sided stacking process as shown in Figure 4. The total area is then reduced by 50%, and better electrical performance (>40%) is achieved by using a vertical signal transmission path and adding a ground (GND) plane on L2. The RLC extraction can, therefore, be reduced by using a double-sided SiP

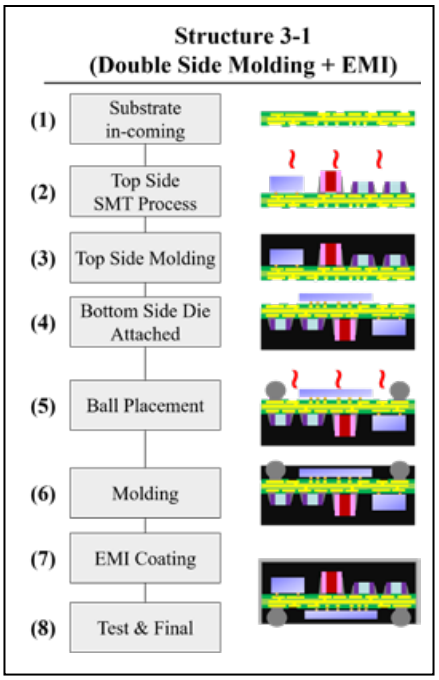

Figure 3: Process flow of a double-sided SiP structure (double-sided molding + EMI).

Structure	Net Name	Ls (nH)	Cs (pF)	R (m Ohm)
Single Side SiP	A	1.177	0.801	242.22
	B	1.185	0.806	223.40
Double Side SiP	A	0.705 (40%↓)	0.327 (59%↓)	104.32 (57%↓)
	B	0.503 (58%↓)	0.268 (67%↓)	63.39 (72%↓)

Table 1: RLC extraction simulation comparison result.

structure. Table 1 shows the simulation result for RLC extraction (i.e., R: lower resistance is better for signal loss, L: lower inductance is better for signal propagation delay control, C: lower capacitance is better for noise and voltage control).

Structural strength analysis. In this experiment, the warpage performance of different die thicknesses and of different packaged die strengths are studied—this is important because the thickness requirement is getting critical for double-sided SiP platforms. In order to evaluate the optimal die thickness and die strength, a series of grinding wheel parameters were selected—for example, the grit sizes of the teeth, concentrations, and shapes of the various teeth (see Figure 5a). As shown in Figure 5b, the scanning electron microscope (SEM) image shows how a different grinding wheel selection will result in a surface mark difference. Grinding wheel A is rougher than grinding wheel B. The finer grinding wheel will have a smooth surface, but a longer manufacturing time is required to meet the target die thickness because of the small grit size.

Another crucial parameter to be considered when optimizing ELK stress in a double-sided SiP structure is die thickness. A stress analysis was conducted to evaluate ELK stress as a function of die thickness at 200µm, 150µm, 100µm,

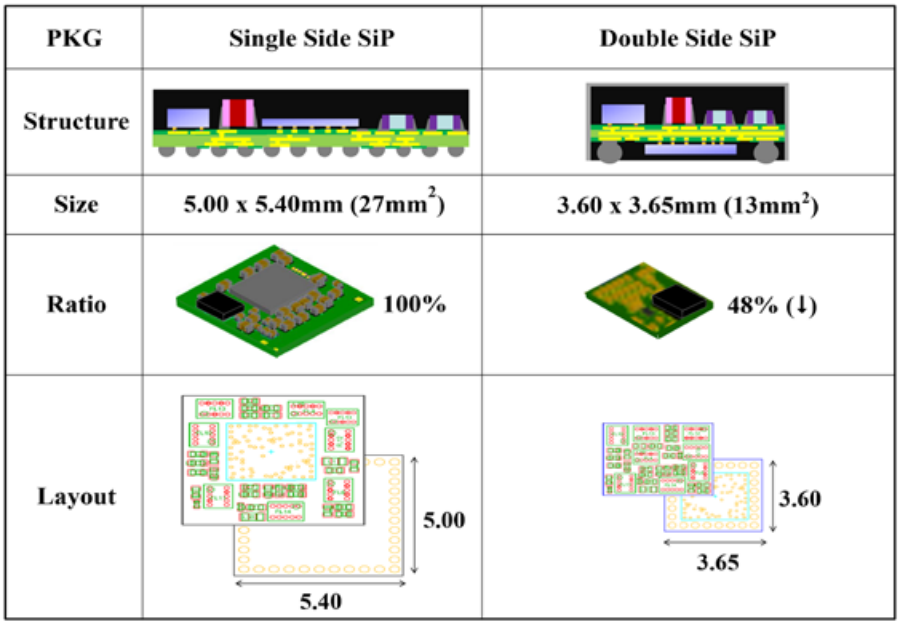

Figure 4: Comparison of single-sided SiP and double-sided SiP structures.

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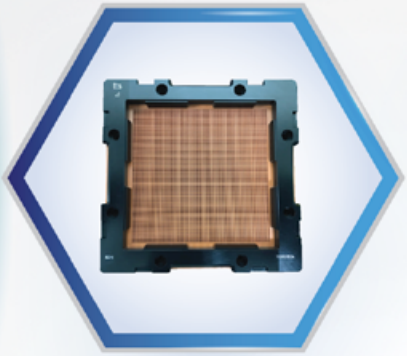
High Pin Count

Pitch
≥0.80mm

Pin Count
≥10,000

Coplanarity
<0.35mm

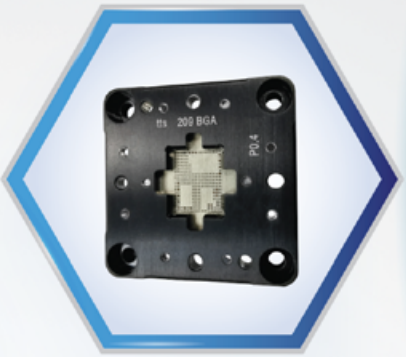


Coaxial

Pitch
≥0.40mm

Insertion Loss
>40GHz@-1dB

Crosstalk
>35GHz@-52dB

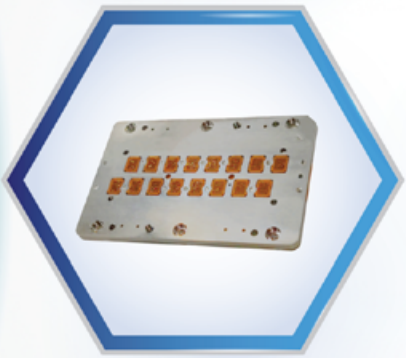


WLCSP Probe Head

Pitch
≥0.15mm

Pin Count
≤6000

Longevity
>1000K

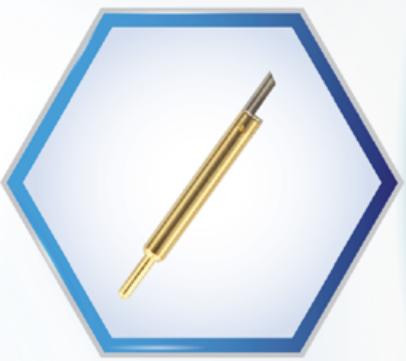


Probe Pin

Pitch
≥0.12mm

Power
≤6.5A

Frequency
>140GHz

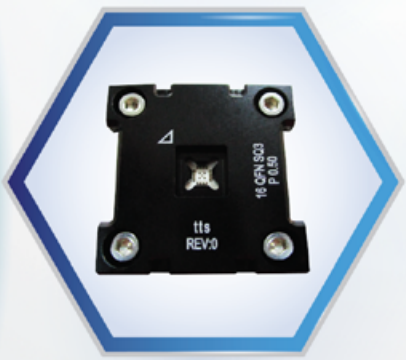


RF

Pitch
≥0.35mm

Insertion Loss
>60GHz@-1dB

Return Loss
>30GHz@-20dB

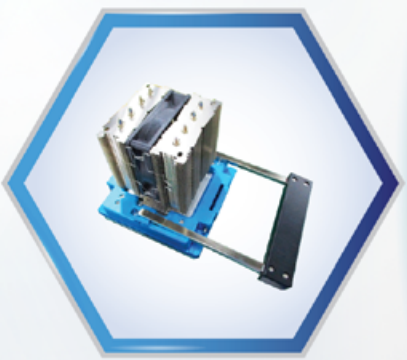


Hand Socket Lid

Heatsink
<100W

Heatpipe
100W - 1000W

Liquid Cooling
300W - 1500W



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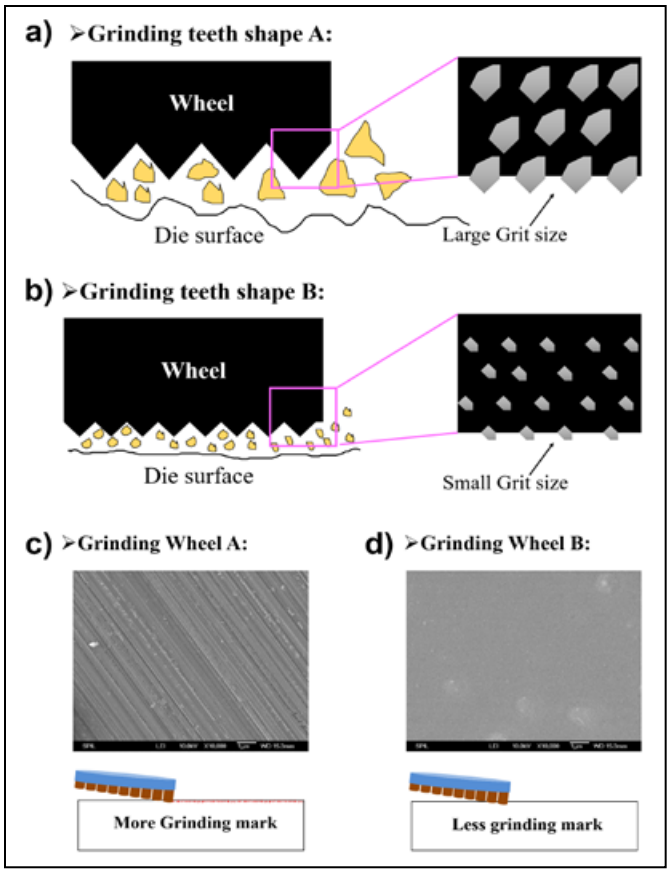

Figure 5: a) Grinding teeth shape A; b) Grinding teeth shape B; c) Grinding wheel A; and d) Grinding wheel B.

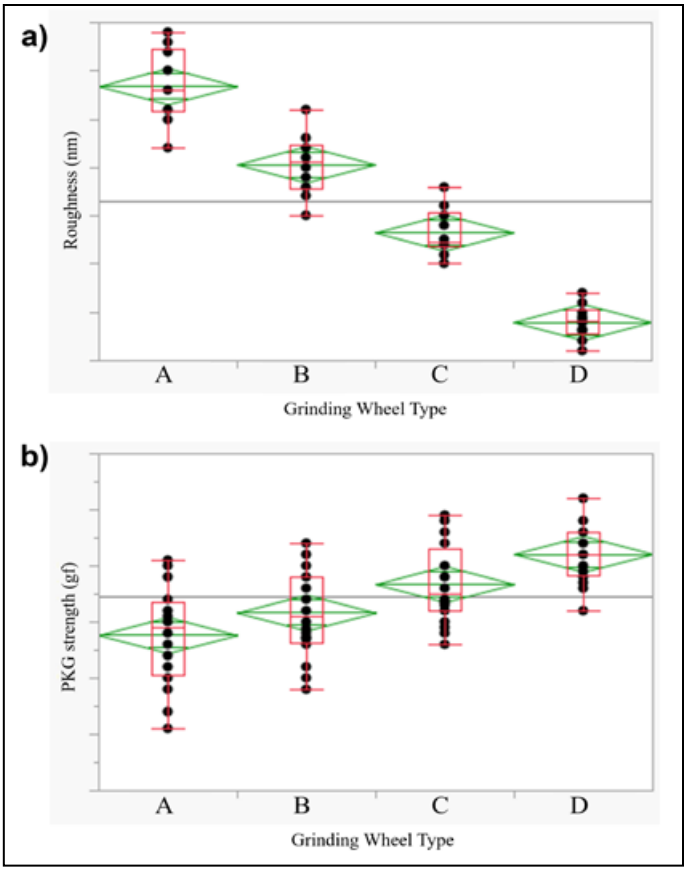

Figure 6: a) Roughness vs. grinding wheel type; and b) Package strength vs. grinding wheel type.

and 50µm. After the grinding process, the bottom thinner die resulted in the lower ELK material stress ratio, although there is a process risk during die bonding because of die warpage. The summary of die thickness impact on ELK stress in a double-sided SiP structure is shown in Table 2a.

A 3-point bending strength test was also conducted to confirm package strength, which is modulated by the external bending stress. The bending test also allows the determination of flexibility, bending strength, breaking strength and the fracture resistance of the material. During the bending test, deformation occurs at the midpoint of the test samples, and the bending force causes a concave surface or bending fracture. A force is applied to the test sample at its midpoint to form a concave surface with a pre-defined radius of curvature. The package (PKG) die strength is defined as the maximum stress that an object can withstand before being bent and broken.

To compare the effect of grinding wheel type, we selected four types of wheels for a grinding process DOE study. The grit size of the grinding wheel ranged from 7~8µm to 1~2µm, and the grit concentration ranged from 75 to 100, and the grit shape (i.e., block type of grit shape with vitrified bond structure); these parameters are summarized in Table 2b.

We also measured the die roughness on a double-sided SiP structure with different

a)

Items	Leg1	Leg2	Leg3	Leg4
Die thickness (um) after grinding	200	150	100	50
ELK stress ratio	1.15x (High)	1.00x	0.83x	0.69x (Low)
Die warpage risk @ Die bonding process	↓↓ (Low)	↓	-	↑ (High)

b)

Grinding Wheel Type	A	B	C	D
Grit size	7~8um	4~6um	2~3um	1~2um
Grit Concentration	75	75	100	100
Grit shape	Block type with vitrified bond			

Table 2: Structure strength analysis results: a) Summary of die thickness impact on ELK stress in a double-sided SiP structure; and b) Comparison of the impact of various grit sizes with respect to grinding wheel types.

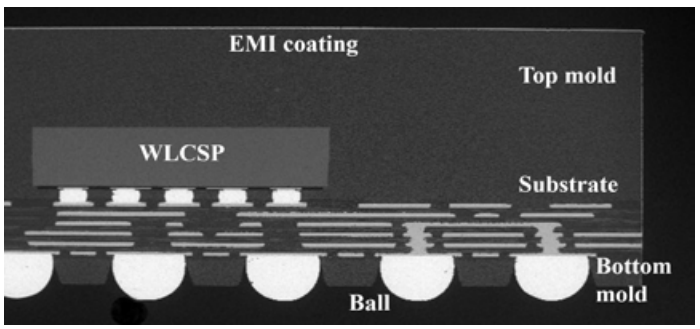

Figure 7: Double-sided SiP of a BGA ball cross-section scanning electron microscope (SEM) result.

#	Reliability Test Items	Read Point	Sample size	O/S Test and SAT Result
1	Time Zero	*T0*	0 / 231 pcs	All Pass
2	MSL3	*Pre-con*	0 / 154 pcs	All Pass
3	TCT (-55 ℃ ~+125 ℃)	*1000 Cycles*	0 / 77 pcs	All Pass
4	u-HAST (130℃/85%RH)	*96 Hours*	0 / 77 pcs	All Pass
5	HTS (150℃)	*1000 Hours*	0 / 77 pcs	All Pass

Table 3: Summary of reliability tests conducted.

grinding wheel types (A, B, C and D). The roughness level was such that A > B > C >D (i.e, wheel A is rougher than the others). We used the 3-point test to check the package (PKG) die strength. The greater PKG strength was achieved using a fine grit size with wheel D because of the higher die strength that can be accomplished with the smooth silicon die surface and mold surface. The test results of the roughness and 3-point bending using the different grinding wheel types are shown in Figures 6a and 6b.

Reliability results

The grinding wheel selection can enhance the package strength and reduce the risk of die and package cracking caused by structural warpage. The finer grinding wheel type (wheel type D) resulted in a greater package die strength due to the smooth silicon die and mold surface—but in contrast, it increased process time. The double-sided cross-section image of a SiP structure is shown in Figure 7. The SMT result shows a double-sided SiP with top side molding, bottom molding, and the main die.

In this study, the following JEDEC reliability test conditions were used: pre-condition with MSL3, temperature cycling test (TCT) at -55–125ºC for 1,000 cycles, un-biased highly accelerated stress testing (u-HAST) at 130ºC for 96 hours, and high-temperature storage life (HTSL) testing at 150ºC for 1,000 hours. The open/short (O/S) test and scanning acoustic tomography (SAT) inspection were done, and all reliability test results had passed as shown in Table 3.

Summary

Compared to a single-sided SiP structure, a double-sided SiP structure can provide good thermal performance by using a thermal pad design and TIM (i.e., Ag epoxy with 25W/mK with 0.99x θJA ratio with 24% thermal enhancement, and 0.75y θJB with a 38% thermal enhancement). The normal EMC with TIM achieved a better warpage result because of the low CTE mismatch during the molding process done on the structure.

The double-sided SiP package provides the small form factor and good electrical performance required for 5G and wearable electronics applications. For the advanced double-sided SiP structure, we studied the effects of different die thicknesses and grinding wheel roughness values on the package strength. Also, a 3-point bending test methodology was selected to evaluate the suitability of the double-sided SiP structure for use in the end product at the board-level manufacturing process. The finer grinding wheel type (wheel type D) provided a better package die strength due to the smooth silicon die and mold surface, but it resulted in a lower grinding throughput. To achieve a higher throughput, grinding wheel type A would be the best choice. Finally, the double-sided SiP structure passed reliability requirements including pre-condition MSL 3, TCT (1,000 cycles), u-HAST (96 hours) and HTSL (1,000 hours). The double-sided SiP can provide an innovative solution to address the small form factor, cost reduction, electrical performance, and time-to-market requirements for 5G and wearable products in the near future.

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Biographies

David Wang is a Department Manager, Corporate R&D at Siliconware Precision Industries Co., Ltd., Taichung, Taiwan, R.O.C. He has over 25 years of industry experience especially focusing on fan-out packaging technology development and advanced assembly analysis. He has published over 10 conference papers and patents. Email: davidwang1@spil.com.tw

Mike Tsai is a Technical Deputy Manager, Advanced SiP Product Integration at Siliconware Precision Industries Co., Ltd., Taichung, Taiwan, R.O.C. He received his MS degree from National Chung Hsing U. (NCHU). He has over 10 years of job experience and published 11 papers in the semiconductor industry, with a special focus on FC, PoP and SiP of advanced assembly technology.

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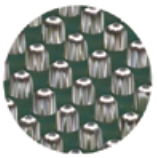
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Meeting cost and technology requirements using MLF/QFN

By Marc Mangrum [Amkor Technology, Inc.]

*Micro*LeadFrame (MLF)/quad flat no-lead (QFN) packaging technology is the fastest growing IC packaging solution today. From a market segment perspective, MLF packaging solutions represent more than a 111B-unit market for 2022 across five markets: automotive, consumer, industrial, networking, and communications (Figure 1). The package solution requirements across these markets vary but, the fundamental values the MLF packaging brings to each one is consistently the same: 1) a flexible form factor, 2) adaptable interconnect technology, 3) electrical and thermal performance, and 4) a cost-effective solution.

Flexible form factor

The flexible form factor of MLF packaging enables the technology to service all markets, meeting unique dimensional, environmental and application requirements. In these markets, the MLF packaging solution is being utilized to solve space and functionality challenges. As an example, the capability to form cavities has resulted in the MLF becoming a widely used and versatile solution in the microelectromechanical systems (MEMS) and sensor markets. The automotive industry continues to rely on this technology for solutions in all areas of the automotive electronics deployment. Applications range from infotainment systems to magnetic sensors for steering controls, to even complex moisture sensing systems for automatic windshield wiper systems and battery control management systems. Body sizes ranging from <1.0mm x 1.0mm to >12mm x 12mm are available (Figure 2).

The broad range of JEDEC package thicknesses enables the MLF packaging technology to meet the demanding size requirements of the portable hand-held, Internet of Things (IoT), gaming networking/computer, industrial and the broader consumer markets. Typical body thickness ranges from 2mm to 0.30mm. Ultra-thin capability is also possible down to less than 200µm using both wire-bond and flip-chip interconnect solutions. The thinnest IC packaging solution is the die itself followed by wafer-level chip-scale packaging (WLCSP) and then the MLF over molded packaging technology. As shown in Figure 3, MLF represents the thinnest over molded leadframe technology.

MLF package applications are in almost every electronic system utilized in the world today: radio-frequency ID (RFID), smart home devices, light-emitting diode (LED) bulbs, security tags, electric tools, heating/ventilation/air-conditioning (HVAC) systems, medical devices, satellite systems, audio/visual home electronics, and home and commercial appliances. In any identified electronic product, there is a 99.9% chance a device utilizing QFN packaging technology is in it. The wide use of this packaging technology is not just about body thickness either. Body size, lead

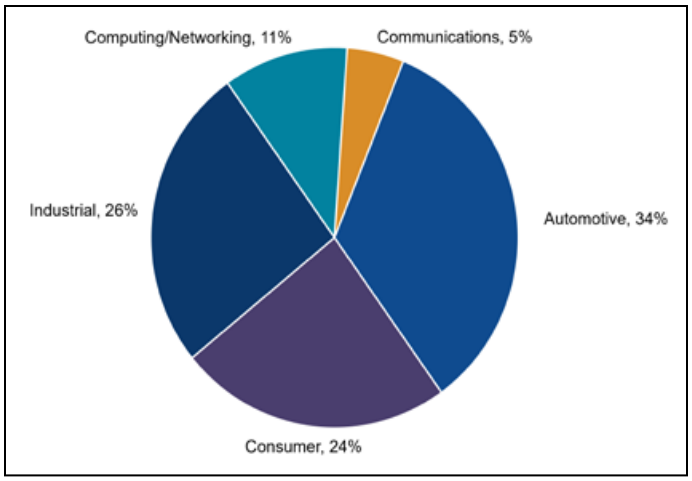

Figure 1: MLF volumes extend across five key market segments.

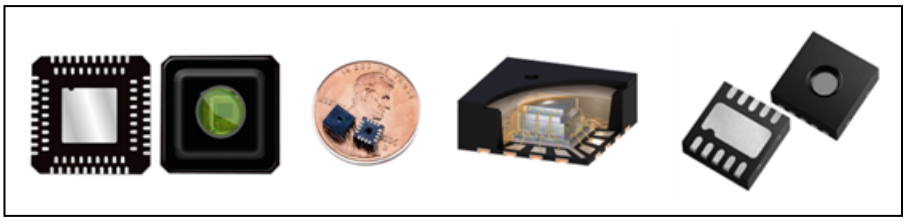

Figure 2: Illustration of the range of body sizes available in MLF packaging.

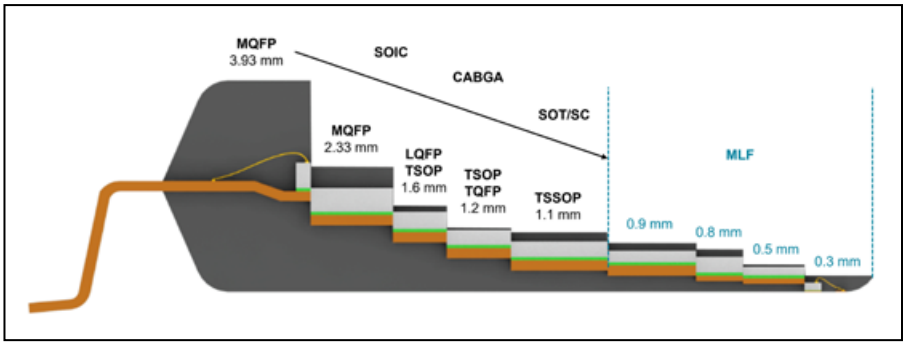

Figure 3: MLF represents the thinnest over molded leadframe technology in the industry.

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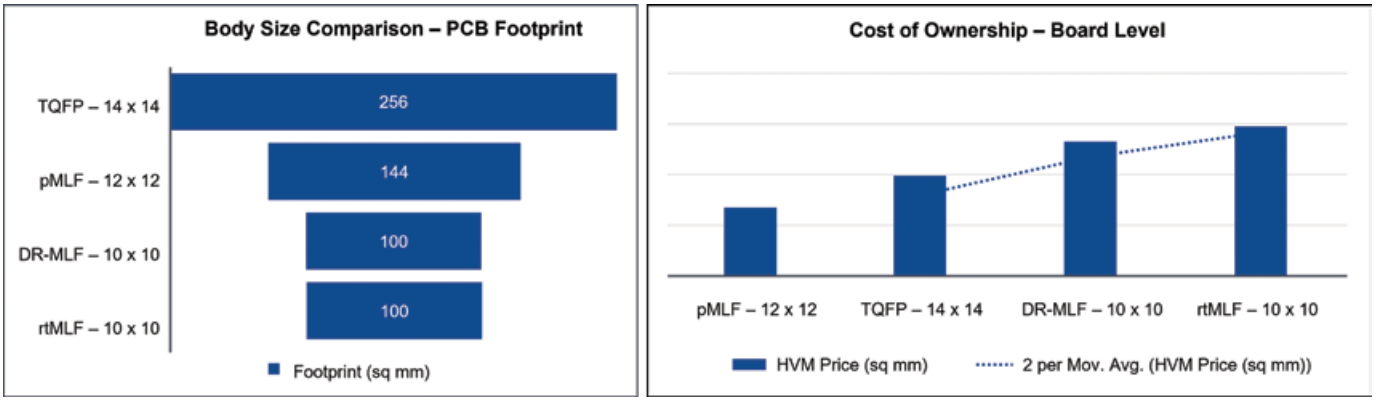

Figure 4: Body size and footprint are critical to application cost.

count, and flexible lead designs are also key attributes that have led to the use of this IC packaging solution in a variety of semiconductor applications.

Cost-effective solutions

Body size or footprint are of equal importance to all applications (Figure 4). Known as the cost of ownership (COO), the amount of area on the printed circuit board (PCB) of a given application is critical to the cost of the application solution. So, it is not only how thick the package is today, but how large it is that can become more of a priority consideration. Migration paths from laminate carrier array ball grid array (CABGA) and quad flat pack (QFP) packages are often driven by these two advantages of the MLF technology. Other COO considerations seen with MLF packaging are the stencil costs, the solder usage, solder joint reliability, and the ability to inspect the solder reflow process by monitoring the lead fillet formation.

Higher pin count requirements are possible for MLF packaging technology by the use of multi-row, interstitial lead designs. Known as the Dual Row MLF (DR-MLF) package, this format can increase the I/O count of a given body size by as much as, or more than, 50%. This enables MLF technology to add functionality within an application while maintaining a small PCB footprint. The DR-MLF is available in both saw and punch formats, with the punch format utilized extensively for body sizes of 8mm x 8mm and greater. Along with the higher I/O density, the DR-MLF also has the advantage of better thermal performance than other equivalent lead solutions such as a laminate CABGA and has demonstrated excellent board-level reliability (BLR) performance. Long a concern with the interior row of leads, data taken to determine solder joint reliability shows that DR-MLF packaging is capable of the same BLR performance as the single-row versions. This has led to the recent adaptation of the DR-MLF technology into automotive applications.

Another way to increase the I/O count of the MLF package is by reducing the lead pitch. Today, the fine-pitch version of the MLF design is available from 0.5mm pitch down to 0.30mm pitch. This enables the package to retain a single-row configuration while increasing the I/O count by more than 30%. Seen as an advantage in computing and consumer electronics applications, the ultra-fine pitch designs at 0.35mm and 0.30mm can be a challenge for electrical test, as well as for the PCB layout and the surface mount technology (SMT) process. Fine-pitch contactor solutions for these pitches are a challenge as is the electrical performance boards required to interface with the automatic test equipment (ATE) tester. High-quality solder stencils and high accuracy of device placement are needed to minimize the incidence of solder shorting during reflow (Figure 5). However, the advantages of these very fine-pitch solutions are seen where size, thermal performance and I/O level are justified by the critical and necessary requirements of the actual application use cases. The use cases in the networking and computer markets are the primary drivers for these fine-pitch solutions. Hard disk drive and solid-state drive (SSD) controllers are primary use cases benefiting from this ultra-fine-pitch version of MLF technology.

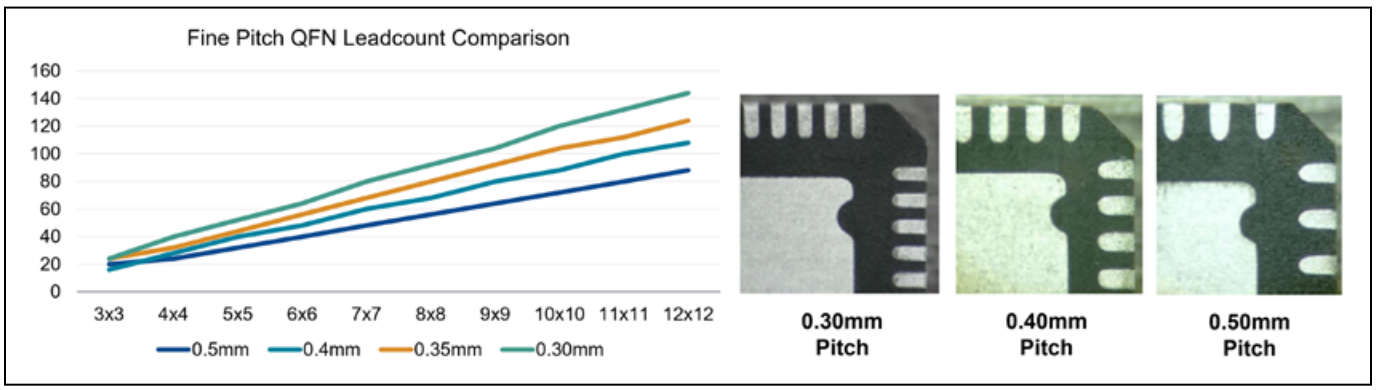

Figure 5: Illustration demonstrating fine-pitch progressions.

Extended electrical and thermal performance

The flexible lead configuration has enabled the MLF packaging technology to extend its capabilities for providing solutions in the power market. The Power QFN (PQFN) is a variant of the saw MLF technology that enables multiple customer exposed pads with multiple fused leads. Combined with the integration capabilities of copper (Cu) clips and heat slugs, the PQFN packaging solution has the thermal capability needed for power metal-oxide semiconductor field-effect transistor (MOSFET) designs while retaining the advantages of size (body thickness and body size). The split exposed pad capability is also a primary reason the MLF is finding success in the GaN market, especially for multi-die solutions where the gallium nitride (GaN) die and an application-specific integrated circuit (ASIC) are integrated into a common package (Figure 6). These solutions are rapidly finding their way into portable, handheld devices and electronic charging devices of all kinds.

Solder die attach, as well as sintering paste, have further extended the thermal performance of PQFN solutions. Even mixed materials such as epoxy die attach for the ASIC controller die and solder paste for the MOSFET attach are common. Isolation of the gates in MOSFETs is also a possibility and an advantage of the split-pad design capability of this packaging technology. Thermal dissipation for properly configured PQFN devices is noted to be extremely robust. With the embedded heat slug and external heat sink, devices capable of a continuous drain current of 15 amps and drain to source voltages of 150 volts can be sustained. The use of Cu leadframes, and lead-free solders are key components of this packaging solution that enable the on-resistance (Rds(ON)) performance required for devices with demanding high-power requirements.

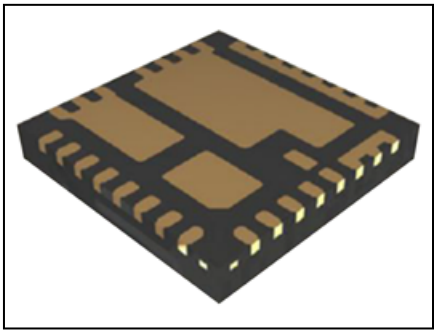

Figure 6: Split die attach pad showing isolation of the ASIC from the GaN.

Adaptable interconnect technology

Further versatility of the MLF technology is demonstrated by the multiple interconnect solutions that have been proven and are available in the market today. These range from traditional wire bond designs to high bump count Cu pillar flip-chip designs. The use of gold (Au), Cu and silver (Ag) wires of various diameters addresses the requirements for performance and cost, while enabling the broad interconnect solutions for a variety of wafer technologies such as silicon, GaN, and silicon on sapphire (SOS), with technology nodes ranging from 120nm to 7nm. Wire diameters range from 0.6mil to 2.0mil. This wide range of wire diameters supports device-level functional performance needs while enabling the right cost point for the solution for the die technology node.

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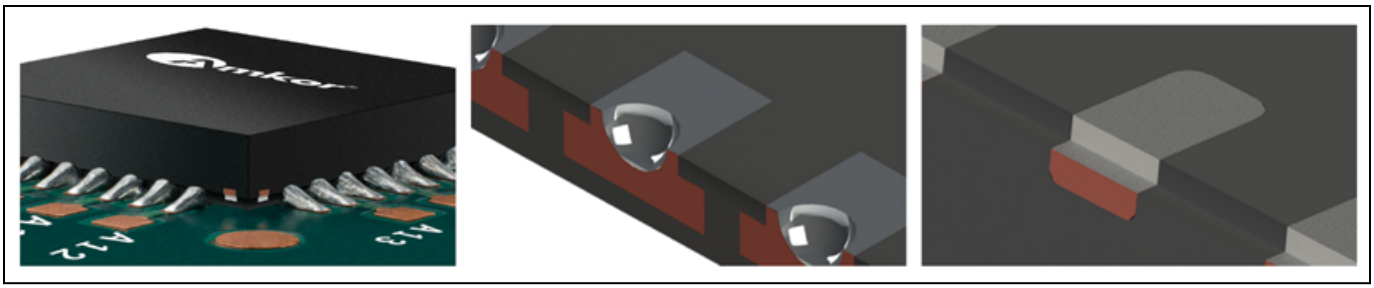

Figure 7: Wettable flank addresses critical needs of the automotive original equipment manufacturers's (OEM's) manufacturing process.

The flip-chip capability of the MLF technology enables size reduction while improving electrical signal integrity and thermal performance. Applications such as power management integrated circuits (PMICs) and radio frequency (RF) are early adopters of the leadframe flip-chip solution. Typical flip-chip MLF technology designs today that utilize Cu pillar bumping can have 160µm bump arrays. RF devices rated up to 40GHz utilize this type of packaging solution in applications ranging from smartphones to high-speed servers. The use of a Cu leadframe enables thermal performance in excess of 4 watts, making this technology ideal for the battery management systems in wireless/handheld applications. Adaptation of the flip-chip MLF is occurring in automotive applications as well. As the battery electric vehicle (BEV) market grows, more focus is being placed on size and weight of the electronics in the vehicles. Battery management controllers today are predominately hard wired into the battery cell. The transition to wireless control solutions will require more devices, so, having small, low weight packaging solutions is of paramount interest.

The exposed die attach pad (either top or bottom, or both) feature enables this packaging technology to meet the thermal needs of high-performance networking devices as well as power devices. The ability to integrate large-diameter bond wires and Cu clips for power field-effect transistors (FETs) has enabled MLF packaging solutions to extend into high-power applications and meet the very demanding market requirements ranging from automotive to consumer gaming products.

New material sets specifically target zero delamination and the demanding automotive reliability requirements of the Automotive Electronics Council's AEC-Q100 and AEC-Q006 standards. These material sets have also extended the use case of this technology to applications previously dominated by leaded-package solutions such as QFPs and small outline integrated circuit (SOIC) designs. Roughened leadframe finishes, improved epoxy die attach materials, film die attach for automotive applications and improved molding compounds to enhance Cu wire performance are only a few of the enhancements that are being applied to extend the value of the MLF packaging technology. Considering the ever-rising increase in the price of Au, more than ever IC packaging solutions need alternatives for interconnects. The automotive industry has been reluctant to adopt Cu wire too quickly primarily due to issues seen regarding long-term latent failures of the wire bonds attributed to interactions of the mold compound and the Cu wire. Innovations in both the wire and mold compounds have resulted in the much-improved performance seen with respect to the reliability requirements and have led to a broader adaptation of Cu wire for automotive ICs.

One of the key recent innovations with respect to MLF technology is the wettable flank (**Figure 7**). Because the MLF is a leadless package and the automotive industry requires a visible indicator of a reliable solder joint post reflow, the need for an inspectable solder fillet on each lead is mandatory. This is especially important in automotive applications where each PCB is inspected using automated optical inspection (AOI) equipment. The formation of a solder fillet on each lead that can be detected by the AOI equipment is critical to the automotive OEM's manufacturing process. MLF packaging solutions form the fillet using a process known as step cut in the saw singulation process, or the dimple when punch singulation is applied. Both processes enable the formation of a fillet necessary for indicating proper wetting of the leads and both processes are widely utilized in the automotive industry today.

Summary

The MLF/QFN technology is a market adaptable and cost-sensitive technology. Utilizing the flexible form factor and adaptable interconnect capabilities in combination positions this packaging technology to meet a multitude of market needs and application requirements.

Acknowledgments

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Biography

Marc Mangrum is Sr. Director for MLF® Products at Amkor Technology, Inc. Tempe, AZ. Prior experience includes more than 30 years at Motorola and Freescale. His capabilities include the development of advanced ATE for digital/analog ICs, and cost-reducing IC package design and assembly processes. He has published over 30 papers and has 33 patents issued, and is a graduate of the U. of Texas at Austin with core competencies in mathematics, electrical engineering, and business administration. Email Marc.Mangrum@Amkor.com

Addressing temperature accuracy and uniformity measurements in wafer probing

By Klemens Reitinger, Bengt Haunerland, Sophia Oldeide [ERS electronic GmbH]

Temperature has always been an important parameter when testing sensor devices, but the trend is moving from simple, functional tests, to calibration at certain temperatures. Consequently, these devices, like temperature, gas, humidity, and pressure sensors, depend not only on highly accurate temperatures, but also must be exposed to a uniform temperature over the whole chuck. This presents new challenges to temperature wafer probing, further exacerbated by broader temperature ranges and tighter accuracy requirements. Some of the challenges include: 1) Validating the long-term performance of the chuck sensors after the first calibration; 2) Verifying the accuracy and uniformity that is specified; 3) Calibrating according to a certain standard. To address these challenges, it is not enough to focus on the thermal chuck system—it is also necessary to look at the calibration tool and method.

Common calibration methods

Today, there are two tools that are commonly used to reliably measure temperature uniformity during wafer test. The first method uses a measurement wafer, i.e., a thin wafer with multiple embedded sensors. Fast test times and instant uniformity data are notable advantages of this type of tool. Because of its multi-sensor design concept, however, there will always be a sensor-to-sensor accuracy deviation. Its operation is also associated with a great deal of effort because the wafer must be manually adjusted and repositioned at low temperatures to ensure an ice-free environment.

The second option is to use a manual drop sensor. Because it's only one sensor, it offers the highest instrument accuracy and is easy to operate. However, this is a very time-consuming method because it relies solely on manual operation, making it difficult to apply repeatably, and it is not applicable at low temperatures.

Both tools described above suffer from a lack of automation and cannot fully reflect the probing conditions because the measurements are taken when the chuck is in a static condition. These issues affect the calibration reliability, which can be calculated using the Guide to the Expression of Uncertainty in Measurement (GUM) standard:

Combined uncertainty: $U_c =$

$$\sqrt{ChuckSystem^2 + CalibrationTool^2 + Method^2}$$

New calibration concept

To tackle the issues noted above and lower the measurement uncertainty, there is a need to eliminate the inherent weaknesses of the tools' designs. ERS's ProbeSense™ is a wafer prober-dedicated tool that offers a new concept for temperature calibration and measurement. As seen in **Figure 1a**, it consists of one sensor jig inside a bell-like cylinder that can be mounted in the probe card position (60) and connected to a calibration instrument (600). The concept takes advantage of the XYZ motion capability of the prober, which allows the sensor to contact the chuck surface (**Figure 1b**) and perform repeatable and automated measurements in the actual probing area.

Our calibration tool addresses some of the key challenges associated with traditional wafer-based calibration by: 1) Addressing the calibration uncertainty through automation; 2) Improving accuracy by using only one calibrated sensor; and 3) Offering an extended calibration range of up to 300°C. The sections below discuss aspects of this technology.

Set up. ProbeSense™ is mounted in the probe card position of the prober. It is compatible with all chuck systems

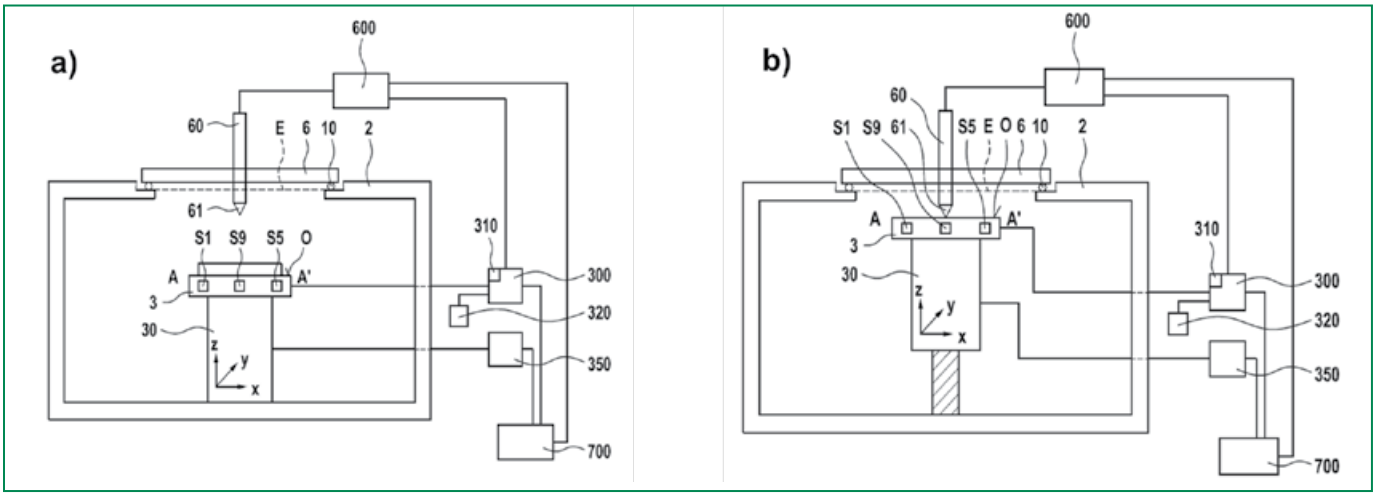

Figure 1: A new temperature measurement concept: a) A calibrated sensor jig attached like a probe card (60); b) Touchdown by chuck motion (as in wafer probing).

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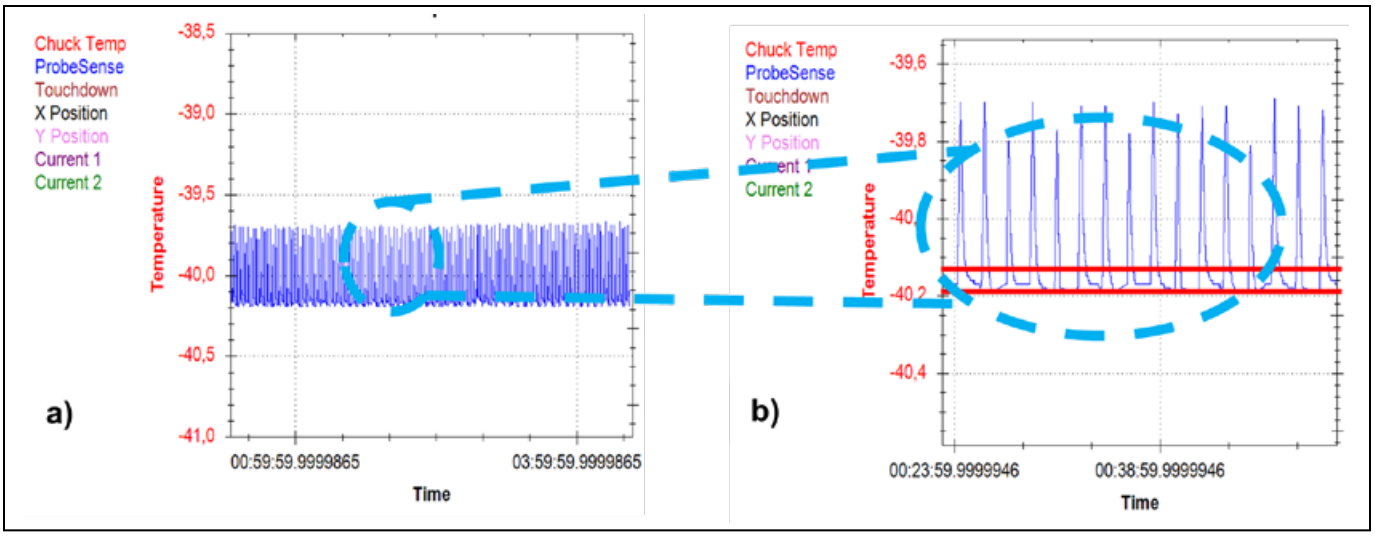

Figure 2: a) 100 touchdowns at -40°C; b) A zoomed-in view showing the temperature reliability of 10mK.

and probers. The tool is connected to a temperature readout device and is controlled with software that communicates with the prober, controller, and readout device. The software allows the user to program the chuck to move to different positions for temperature measurements.

Operation. A fully-automated calibration process is possible, eliminating the problem of loading the measurement wafer and the time-consuming operation of using a manual drop sensor. It also means that no operator skills are required. By using the specially developed software, the user can define each measurement point, start the operation and let it run independently. The automation capability has been thoroughly tested and fully integrated into software provided by Supplier A.

Repeatability tests

To verify the ingenuity of the tool, repeatability tests at various temperatures were carried out on two different probers: a manufacturing probing station from Supplier B and an engineering probing station from Supplier A. The sensor is programmed to make contact with one point on the chuck, separate, and then make contact again, creating multiple, repeated touchdowns. **Figure 2a** shows the test data from 100 touchdowns at -40°C, with a zoomed-in view on the right side (**Figure 2b**). It visualizes the repeated contact between the sensor on the chuck surface and the temperature decrease resulting from their separation. Based on these results, it could be observed that the temperature reliability of the ERS tool at -40°C is approximately 20mK.

At 85°C, the observed temperature reliability increased slightly to around 30mK. This test was also performed with 100 touchdowns, which took approximately five hours to complete. However, when looking at a timeframe of 30 minutes, a temperature reliability of 10mK was recorded.

Temperature drift. When performing the 100 touchdowns at 200°C, a gradual

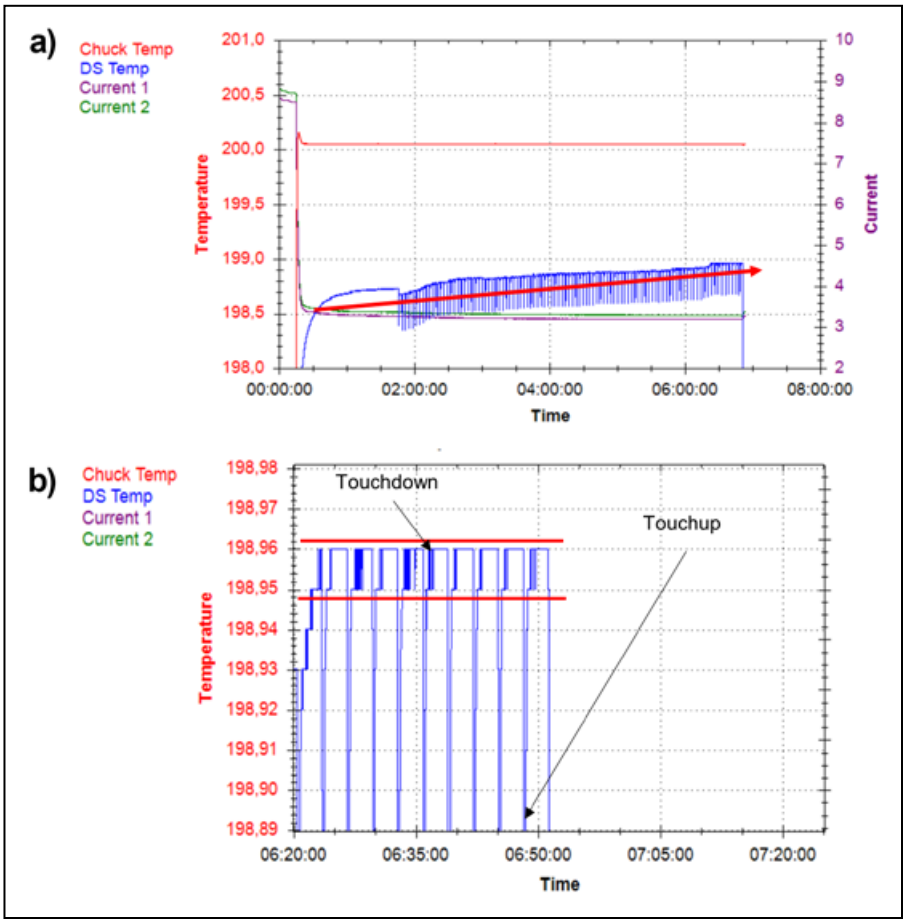

Figure 3: a) A temperature drift was observed at 200°C over five hours; b) Looking closer at a shorter time interval, the reliability remained at 10mK.

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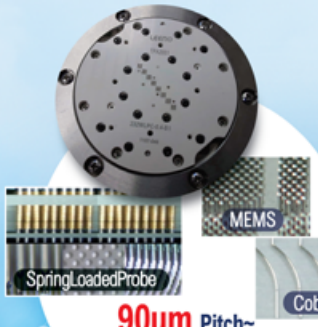
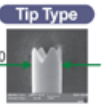
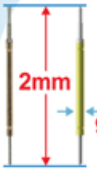


90um Pitch~ Probe Head

Tip Type




Specification
Pitch : Min.120um
Spring Force : 8.0g@ 250um
Current Rating : 1.0A
Inductance : 0.38nH

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RF Coaxial Spring Probe & Impedance Controlled


Logic Test Socket


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Frequency : >20GHz
VSWR : < 1.2
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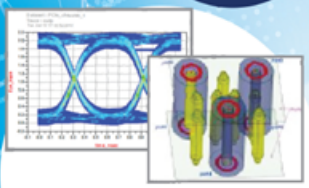
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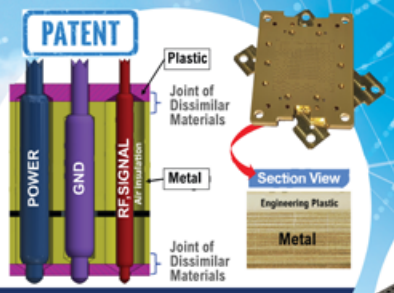
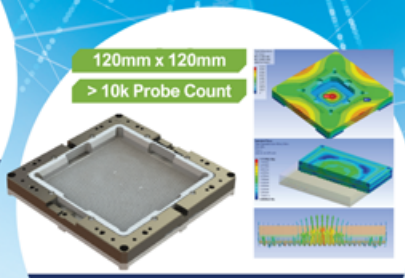
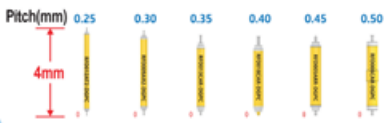


MP Socket



Large Device Socket

Specification
Frequency : 80GHz(BGA),
100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%



Coaxial Probe 100GHz

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CONTACT
USA: hskang@leeno.co.kr / +1 408 313 2964 / +82 10 8737 6561
Korea: sales-leeno@leeno.co.kr / +82 51 792 5639

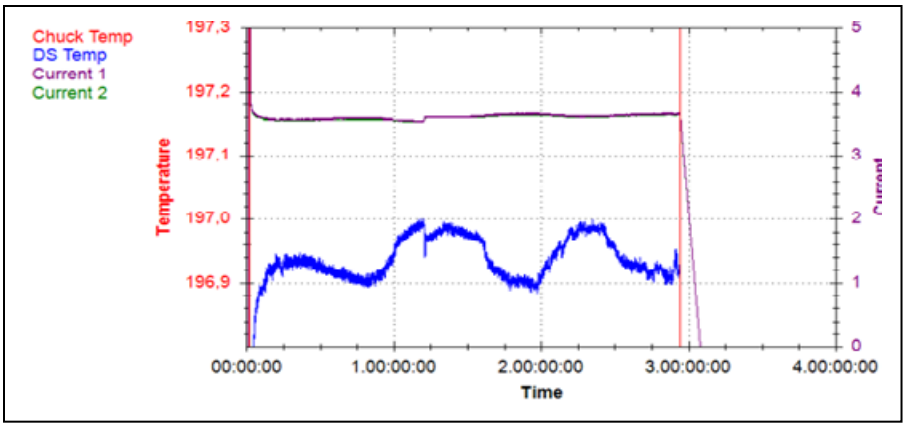

Figure 4: Over the course of three days, the temperature increased and decreased corresponding to the temperature changes in the outside environment.

increase of 0.2°C on the test surface was seen over five hours (**Figure 3a**)—this is called a temperature drift. However, looking again at a 30-minute interval in **Figure 3b**, the observed reliability was 10mK.

To investigate the cause of the temperature drift, an additional test was done at 200°C, but this time a measurement wafer was used. Again, the same gradual heating effect was observed. Following this test result, the ProbeSense™ was again tested in a closed chamber, similar to a sealed prober chamber, over three days. As seen in **Figure 4**, the temperature increased and decreased at regular intervals throughout the days, corresponding with the temperature changes in the environment around the test chamber, which was not air-conditioned. After further tests, it was concluded that the temperature drift does not occur below 100°C and not if the test is performed in a climate-controlled environment.

It was also noted that the chuck construction is an influencing factor. In this case, using an ERS ultra-low noise (ULN) chuck led to a larger deviation than using a low-noise or high-thermal uniformity (HTU) chuck. This is caused by the additional ceramic plate in the ULN chuck, which creates a larger separation between the top plate and the thermal plate.

Measurement wafer vs. single-sensor probing tool

After obtaining and validating the test data, repeatability tests with a measurement wafer were completed to compare the performance of the two devices. Because the measurement wafer requires manual handling, it was placed and removed from the chuck surface multiple times to simulate the touchdowns. Despite trying to realign the wafer the same way, the manual handling leads to an observed repeatability of 0.03°C, compared to the 0.01°C and 0.02°C values recorded with the ProbeSense™.

Calibration reliability. The single sensor in ProbeSense™ is calibrated according to the ISO17025 standard down to 0.01°C between -60°C and 100°C (Range 1) and 0.02°C between 101°C and 230°C (Range 2). The device's uncertainty is, therefore, maximally 0.02°C. A measurement wafer, often consisting of up to 17 sensors, has a significantly higher uncertainty of approximately 0.05°C due to the sensor-to-sensor accuracy deviation. It is also necessary to factor in the absolute accuracy of 0.03°C (taken from the wafer specification sheet), which leaves you with a total device uncertainty of 0.058°C—almost three times more than the maximum uncertainty of the single sensor. To calculate the calibration reliability, the tool's uncertainty is added to the method (repeatability tests) uncertainty. As a result, the calibration reliability of the ERS system is 0.022°C, which is considerably lower than the reliability of the measurement wafer (i.e., 0.065°C).

Single sensor calibration reliability:

$\sqrt{0.02^2 + 0.01^2} = 0.022°C$ (Range 1)

$\sqrt{0.02^2 + 0.02^2} = 0.028°C$ (Range 2)

Measurement wafer calibration reliability:

$\sqrt{0.058^2 + 0.03^2} = 0.065°C$

Uniformity measurements. To compare the uniformity measurements of the wafer and ProbeSense™, it is first necessary to distinguish between static and dynamic measurements. The static measurement was done by placing the wafer on the chuck and then measuring the temperatures without moving the chuck. The dynamic measurement was done by mounting our device and letting the chuck contact the sensor in the same positions as with a wafer on top. **Tables 1a** and **1b** show the static and dynamic measurements on two different probers (Suppliers A and B) at three temperature points.

a) ProbeSense vs. wafer: Engineering prober (Supplier A)

		Max	Min	Total
30°C	Static	30.180	30.036	0.144
	Dynamic	30.080	30.030	0.050
	Variation	0.100	0.006	0.096
85°C	Static	85.167	84.791	0.376
	Dynamic	84.900	84.600	0.300
	Variation	0.267	0.191	0.076
200°C	Static	199.220	197.999	1.221
	Dynamic	198.980	197.960	1.020
	Variation	0.240	0.030	0.201

b) ProbeSense vs. wafer: Manuf. prober (Supplier B)

		Max	Min	Total
30°C	Static	30.34	29.710	0.630
	Dynamic	30.252	29.607	0.645
	Variation	0.088	0.103	0.015
85°C	Static	85.824	85.269	0.432
	Dynamic	85.392	84.814	0.455
	Variation	0.578	0.555	0.023
200°C	Static	198.95	199.6	1.01
	Dynamic	198.02	198.59	0.93
	Variation	0.35	0.43	0.08

Table 1: a) Static vs. dynamic measurements on a prober from Supplier A with a probe card size smaller than the chuck; b) Static vs. dynamic measurements on a prober from Supplier B with a probe card size similar to the chuck.

As seen in **Table 1a**, the static uniformity was notably worse than the dynamic uniformity. However, this can be explained by the size of the probe card. As this is smaller than the chuck itself, there is a smaller shielding effect from the probe card. To verify this, the static and dynamic test was performed on another prober where the probe card is of similar size to the chuck. **Table 1b** shows that this increased shielding effect significantly impacts the uniformity measurements in the static case, which are now closer in value to the dynamic measurements.

A wafer and a single sensor solution do not vary widely in terms of performance when it comes to uniformity measurements. The hot spots and cold spots are generally found in the same area. There is, however, a small deviation in the maximum sensor values, which amounts to 0.070°C when using the GUM standard to calculate. As seen in the previous tables, the uniformity data from the static and dynamic measurements are similar, but our tool offers an advantage when used with the engineering prober from Supplier A. Still, the measurement wafer offers faster test times, as it can measure many points at once, while the ProbeSense™ has longer soaking times and is, therefore, more time-consuming when shifting between different temperatures.

Summary

As temperature testing shifts from final test to wafer probing, it is crucial to have highly accurate tools that can perform measurements that reflect the probing conditions. Sensor devices for electronics, automotive, and industry components have strict temperature requirements, which puts accuracy in the spotlight. It is not enough to only focus on the thermal chuck system when taking on these ever-increasing requirements – continuous improvements to and reassessments of the calibration tool and method are also necessary to better the overall accuracy.

Acknowledgments

For specific information on the performance data described in this article, please contact the lead author.

Biographies

Klemens Reitinger is the CTO at ERS electronic GmbH, Munich, Germany. He holds a Master's degree in Mechanical Engineering from the U. of Applied Science in Vienna, Austria. Over the course of 30 years, he has invented and developed several temperature management solutions for wafer probing, including the thermal chuck family, AirCool®. Email: kreitinger@ers-gmbh.de

Bengt Haunerland is Head of Software and Electronics, at ERS electronic GmbH, Munich, Germany. He has a Master's degree in Electronics Engineering from Simon Fraser U., Canada.

Silver-free AMB and copper bonding for cost-efficient, reliable advanced packaging

By A. Schwöbel, C. Féry, B. Fabian, D. Schnee, M. Rauer, A. Miric, S. Gunst [Heraeus Deutschland GmbH & Co. KG]

High-power electronics have become one of the fastest growing market segments of the semiconductor industry. Major applications include motor drives, hybrid/electric vehicles, rail traction, wind turbines, and photovoltaic inverters. Because the power electronic modules used in these applications operate at high voltage and high current density, they must handle high temperatures and harsh conditions. One of the key components for highly reliable power electronic modules is a reliable metal ceramic substrate. To provide reliable functionality during operation, the substrate materials must provide outstanding electrical, thermal, insulation and mechanical performance. Additionally, they must work with commonly-used assembly and interconnection technologies like soldering, sintering, and wire bonding. Another critical aspect is to ensure a reliable die attachment and interconnection that can transport ever-increasing currents and efficiently take away the generated heat.

Due to cost efficiency, Al_2O_3-based metal ceramic substrates, i.e., direct copper-bonded substrates, are often used for power module manufacturing [1]. However, Al_2O_3-based ceramics cannot fully leverage the potential of wide-band-gap semiconductors. As a result, silicon nitride-based metal ceramic substrates are gaining popularity as materials for power module assembly. Si_3N_4 shows superior mechanical properties combined with high thermal conductivity [2].

Highly reliable Si_3N_4-based substrates are typically manufactured with active metal brazing (AMB) technology that uses Ag-filled and active metal (i.e., titanium) containing brazing pastes [3]. The precious metal content in the brazing paste and a slow vacuum brazing process are the major price drivers for AMB substrates. We have developed a design-to-cost, highly-reliable Ag-free thick-film copper bonding (Condura®.ultra) technology for joining nitride-based ceramics with Cu foils. The paste eliminates the use of an expensive vacuum-based brazing technology. But how does this new bonding technology perform compared to the industry-benchmark AMB substrate? To compare the performance between the two kinds of substrates, various re-liability- and application-related tests such as thermal shock (-65°C/+150°C), peel strength, and high-temperature storage (175°C, 1,000 hours) were conducted. Results of the experiments follow in the first part of this article.

Regarding the attachment of dies to metal ceramic substrates, a clear trend is the replacement of conventional soldering with silver pressure sintering when higher power densities are required. With a melting temperature of 961°C, a sintered silver bonding layer enables operating temperatures above 200°C, whereas a lead-free soldered joint, with a melting temperature of about 230°C, quickly degrades. Furthermore, the heat transport through the joining layer is significantly better with Ag sintering rather than with soldering (>200W/m/K against <65W/m/K) (**Figure 1**) [4].

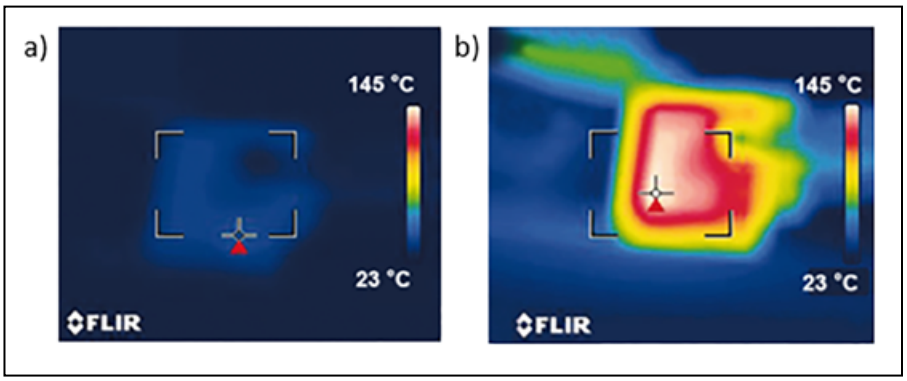

Figure 1: Temperature increase during operation for a die either a) sintered, or b) soldered on metal ceramic substrates.

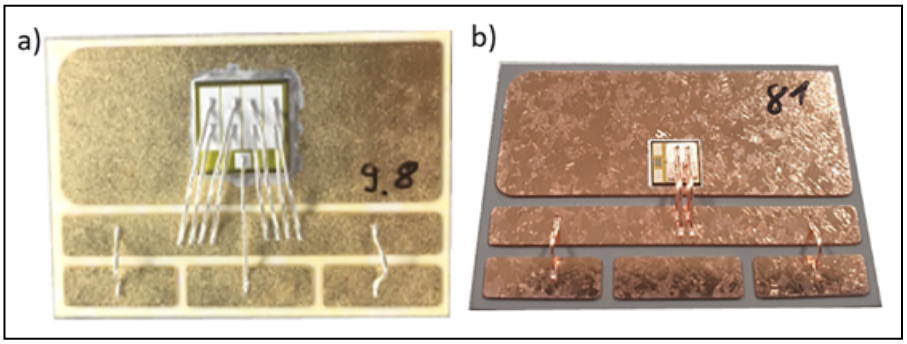

Figure 2: a) Si-IGBT soldered on Al_2O_3-DCB and interconnected with Al wires; and b) SiC-MOSFET sintered on Si_3N_4-AMB with DTS®. Substrate designs from IISB.

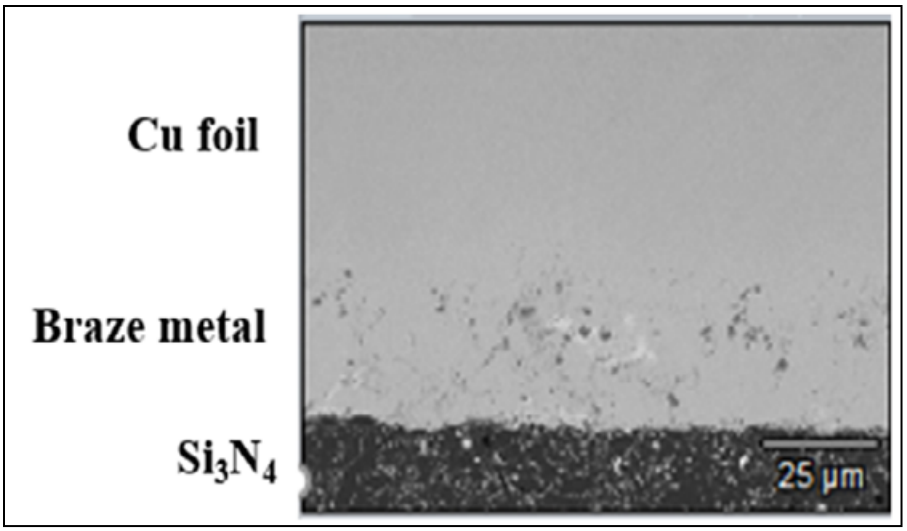

Figure 3: Typical Condura®.ultra microstructure measured by SEM.

Silver pressure sintering can also be used for advanced die frontside interconnections as reported with the attachment of metal clips, flexible printed circuit boards (PCBs), or copper plates. We chose to develop the last one, i.e., copper plates, with our Die Top System (DTS®). It consists of a thin Cu plate (typically 50µm) with pre-applied sinter paste, that is picked from a carrier to be placed on top of the die using a standard die bonder and then pressure-sintered together with the die on the substrate. This way, thick copper wires or ribbons can be wedge bonded without breaking the die (**Figure 2b**). The benefits of copper wire bonding and DTS® are discussed in the second part of the article.

Phase formation

The phase formation and bonding mechanism of our new copper-bonding technology on Si_3N_4 ceramics were characterized by scanning electron microscopy (SEM) as shown in **Figure 3**. The actual bonding mechanism is based on the reaction between the active metal (titanium) and the Si_3N_4 ceramic, forming a stable TiN layer. Because there is no silver in the Condura®.ultra system, typical Ag- and Cu-rich phases are eliminated, which are known from the standard AMB technology as using high Ag-containing brazing filler metal pastes. Nevertheless, the bonding mechanism towards the Si_3N_4 ceramic via a TiN reaction layer is similar.

Thermal shock performance

Si_3N_4-based AMB substrates meet the highest requirements in terms of thermal shock test (TST) performance because of the ceramic's mechanical robustness. To assess resistance vs. the thermomechanical stress of our copper bonding technology on Si_3N_4 ceramics, thermal shock tests were performed using an internal test layout (30.6x29mm^2 with 0.5mm Cu on 0.32mm ceramic) as shown in **Figure 4**. The status of the copper-bonded substrates before testing was characterized by scanning acous-tic microscopy (SAM) and is shown in **Figure 4a**. The red color indicates an etched isolation groove that is part of the used test layout. In case of delamination between copper and braze metal/ceramic because of thermal shock, the red-colored isolation groove will broaden in the SAM picture.

The integrity of the substrates was reassessed by SAM after 3,000 and 5,000 cycles of thermal shock. The results are shown in **Figure 4b** and illustrate no major broadening of the

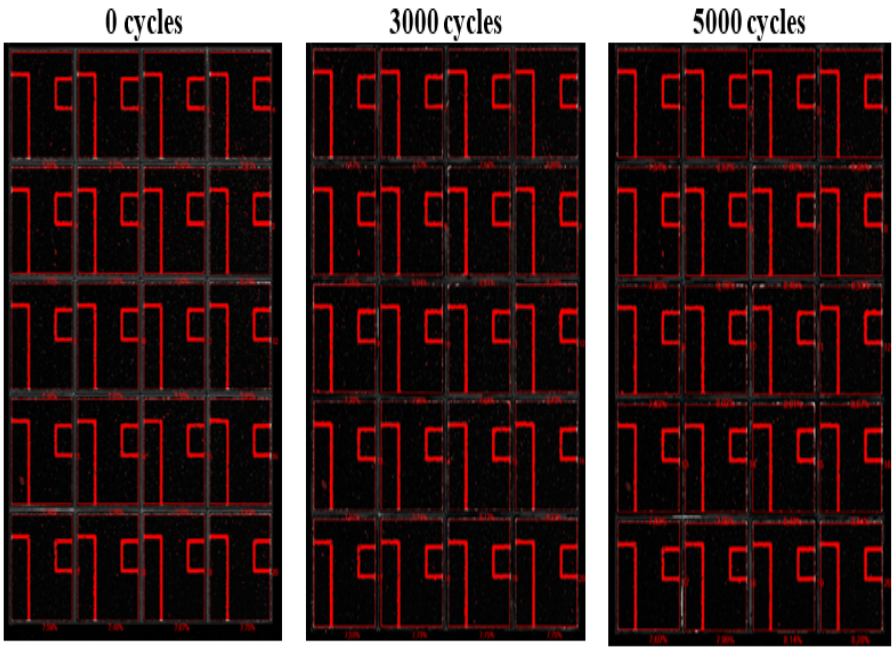

Figure 4: SAM pictures of 20 individual Condura®.ultra test layouts before and after thermal shock tests: a) 0 cycles; b) 3,000 cycles; and c) 5,000 cycles. The test conditions and further details are mentioned in the text. No major degradation is visible after 5,000 cycles.

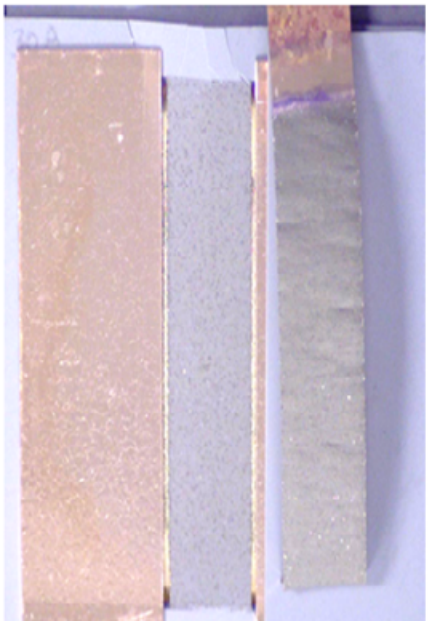

Figure 5: Peel test sample after completion of the peel test. A dark color remains on the peel strip and on the substrate, which indicates Si_3N_4 has been pulled out. The small rectangle indicates the position for the EDS spectroscopy mapping seen in **Figure 6**.

isolation grooves between the initial status of the substrates with the copper-bonding technology and after completing the cycling, proving that no delamination between the ceramic and the braze metal occurred. This indicates that copper-bonded technology can fully leverage the mechanical robustness of the Si_3N_4 ceramics, the same as Ag-containing AMB technology.

Copper peel strength

The copper peel strength characterizes the adhesion strength of the copper (Cu) foil to the ceramic. A simple peel test is used in which a Cu peel strip (10mm wide x 0.3mm thick) is brazed onto a piece of 0.32mm thick Si_3N_4 ceramic using our copper-bonded technology. The Cu is peeled off and the force is measured.

Closer inspection of the failure mode of the peel sample can provide valuable information about the bonding quality. **Figure 5** shows the peeled-off Cu strip after the peel test (right side) and the remaining substrate counterpart. A dark color on the peel strip and on the counterpart is visible, which indicates pulling out Si_3N_4 particles from the ceramic substrate. This

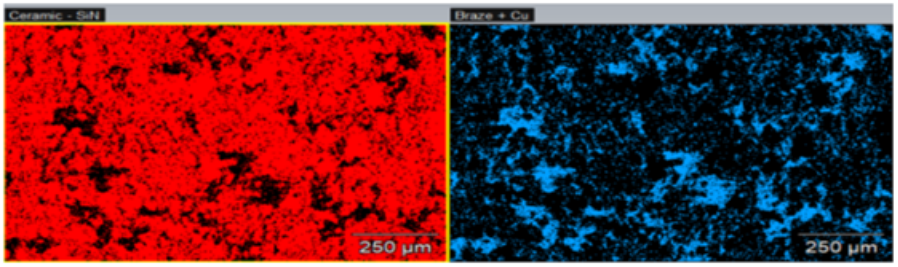

Figure 6: EDS phase mapping of the peeled strip from above: a) (left) The red color indicates the Si_3N_4 phase; and b) the blue color indicates phases from the braze metal.

failure mode is also often observed for Ag-containing AMB substrates. However, there is no failure within the reaction zone of the substrate with the copper-bonded technology. This is proven by energy dispersive spectroscopy (EDS) phase mapping (Figure 6) that shows most of the remaining material on the peel strip originates from the Si_3N_4 ceramic and not from the braze metal, indicating the strong bonding mechanism achieved by the copper bonding process.

Thermal resistance

The thermal resistance (R_{th}) of the metal ceramic substrate is an important factor for the design of the power module. A lower thermal resistance enables a higher power density, allowing reduced chip size. Major contributors to the R_{th} are ceramic thickness as well as ceramic type. Condura®.ultra interface formation is different than Ag-containing AMB and, therefore, it is required to rule out any potential R_{th} contribution from the braze metal or reaction zone itself.

The transient dual interface method was used to assess the thermal resistance of the metal ceramic substrates. Diodes were sintered onto both AMB and the copper-bonded substrates, and the cumulative structure function was calculated from cooling curve measurements after heating the assembly by powering the diode with 40A. The R_{th} of the system was then assessed by detecting the point of divergence of two structure functions measured under different boundary conditions, i.e., the assembly was connected by two different thermal interface materials (TIM) – graphite foil and thermal grease – to the cooling system. The resulting structure functions are shown in Figure 7. The point of divergence is similar for both substrate types, demonstrating that there is no difference in thermal performance between Ag-containing AMB substrates and the copper-bonded substrates in the initial status. Afterwards, the copper-bonded substrates were aged in a high-temperature storage (HTS) test

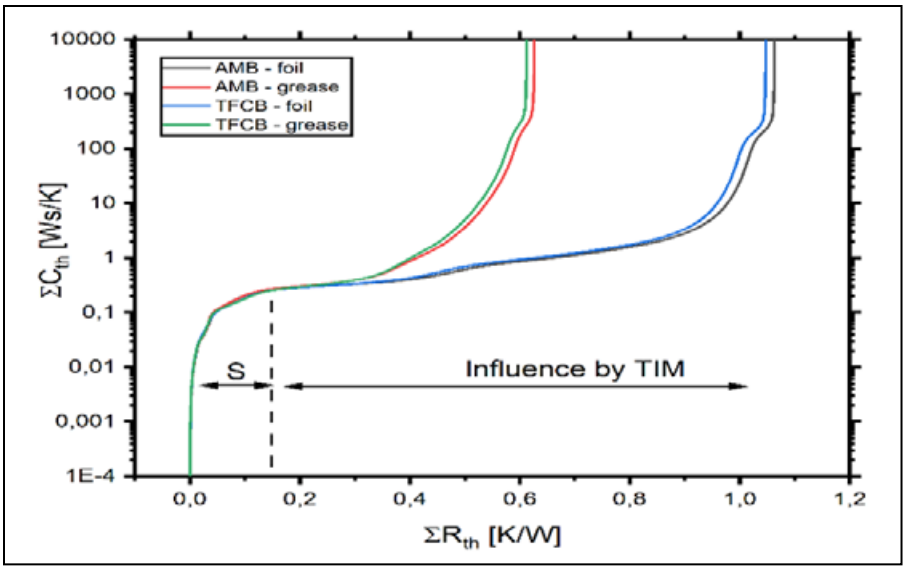

Figure 7: Cumulative structure functions of AMB and Condura®.ultra substrates prior to HTS. "S" shows the region of the system under test.

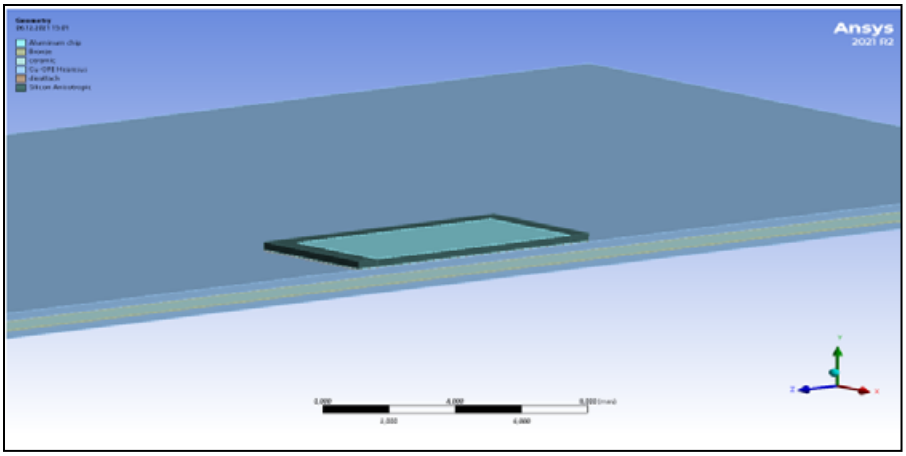

Figure 8: Layout used for FEM simulation.

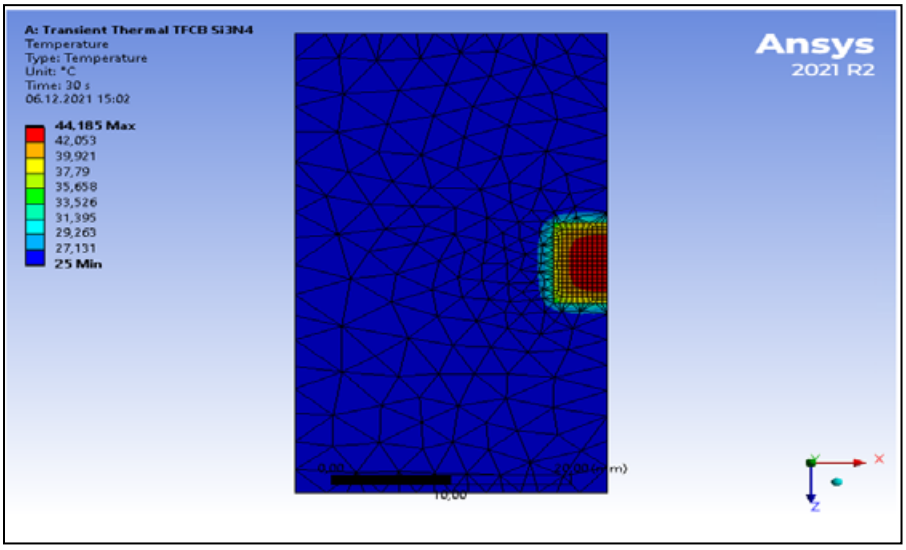

Figure 9: Typical temperature distribution of the Condura®.ultra chip assembly without TIM in a steady state.

for 1,000 hours at 175°C to stress the braze metal and prove that the brazing filler metal system is stable. No difference was observed between the initial status and the aged substrate after HTS, showing that the alloy system displays no degradation and consistent values after 1,000 hours of aging at 175°C.

Thermal resistance simulation

A thermal simulation was performed to assess the influence of thermal conductivity and the thickness of the braze metal layers in the substrate on its total thermal resistance. To include heat spreading and other geometrical effects, a finite element method (FEM) was applied. A simplified geometry of a typical chip-substrate-setup was simulated, including the substrate itself, the braze metal layers on each side of the ceramic/Cu-interfaces, and a silicon chip with a sintered silver die attach (**Figure 8**). In the simulation, the chip is heated by a constant power of 200W in its volume for 30s while the bottom of the substrate is kept at a constant temperature of 25°C. To assess the impact of thermal conductivity and braze metal layer thickness on thermal performance of the Condura®.ultra, both parameters were varied and R_{th} of the chip tracked as a basic result. The R_{th} was calculated based on the simulated maximum chip temperature change dT_J and the applied power. Typically, the region close to the chip is heated up the most while regions further away do not show a significant temperature change (**Figure 9**).

As a next step, a numerical design of experiments (DoE) was conducted. The goal was to identify which of the varied parameters (thermal conductivity and thickness of the braze metal layers) had the highest impact on the R_{th} of the substrate. For this DoE, an OPTISLANG program created 30 simulations distributed across the total design space as defined by the parameter's boundaries. Having calculated these results and determined their R_{th}, a reduced order model was created that allows for a ranking of the influence of the input parameters (thermal

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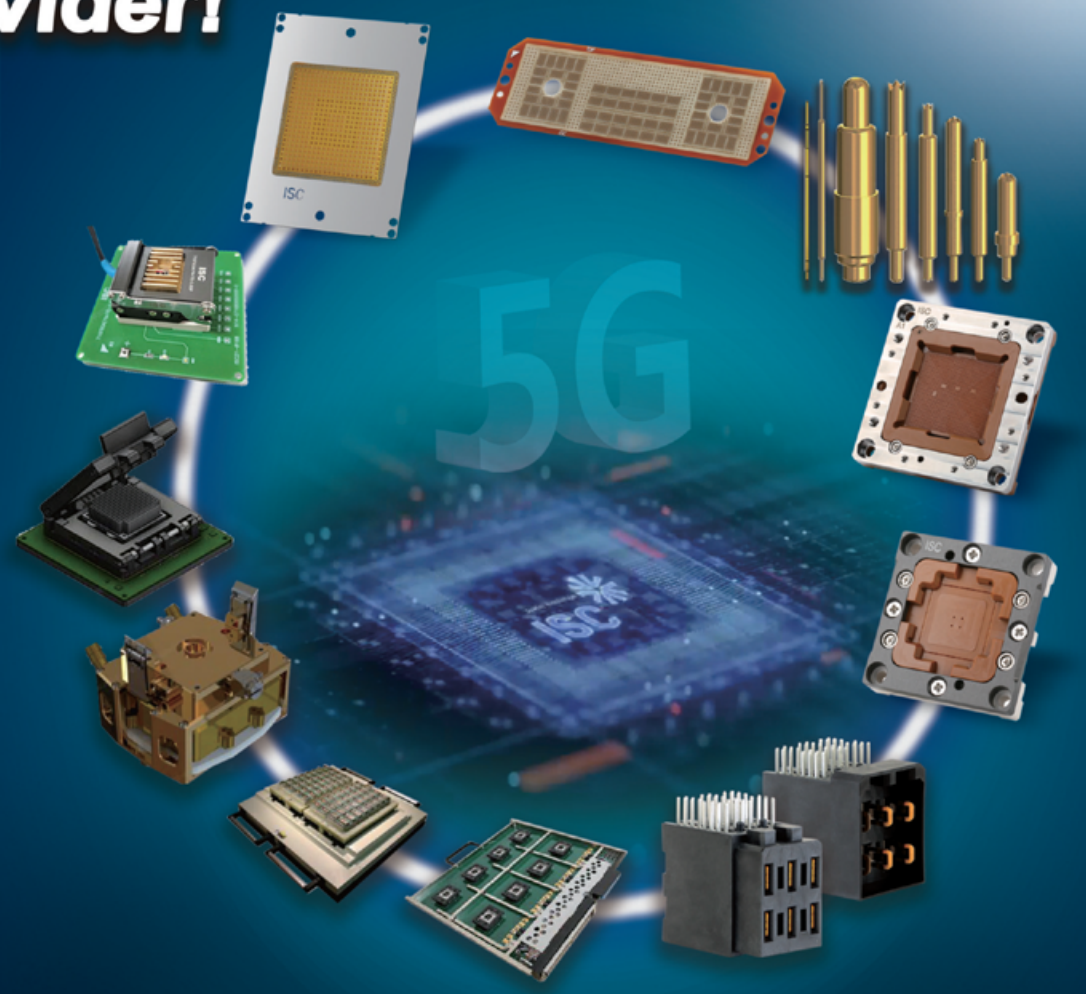

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Overview of properties used for FEM simulation	Min	Max
Thickness of the braze metal layer (µm)	20	60
Thermal conductivity of braze metal (W/mK)	51	140

Table 1: Overview of properties used for FEM simulation.

conductivity and thickness) to the result (thermal resistance). The intervals for the parameters used for simulation are shown in **Table 1**.

The thermal conductivity of the braze metal layer is defined by its composition, which is approximated by a bronze of composition $CuSn_x$ [6]. Typical variations of the braze metal layer thicknesses are on the order of 20 to 60µm and were estimated by cross sections of samples and subsequent secondary electron microscopy analysis.

The correlation between thermal conductivity of the braze metal layer, the thickness of the braze metal layer and the corresponding thermal resistance can be observed in the surface plot in **Figure 10**. The main influencing factor is the thermal conductivity of the braze metal layer. The strongest change of R_{th} is observed in the region towards lower thermal conductivities while the influence is reduced for higher values. The R_{th} values extracted from **Figure 10** vary between 0.088 and 0.104K/W using the input from the table. Comparing this theoretical possible range with the measurement results of (0.13 ± 0.03)K/W shows that experimental and simulated values are in agreement. It can be stated that an overall thermal understanding of the substrate was accomplished.

Challenges of replacing aluminum with copper

Copper is the ideal replacement for aluminum for bonding wires or ribbons. It has higher electrical and thermal conductivities (x1.7 higher for both). It can tolerate more stress in the elastic deformation regime and bears more deformation before breaking. Also, with a lower CTE (~18ppm/K against ~23ppm/K for aluminum) the mismatch with the die is smaller (~2.6ppm/K for silicon). However, because of copper's hardness, it is not possible to directly perform wedge bonding without breaking the die. This last issue is solved with the Die Top System (DTS®), which provides a mechanical protection to increased ultrasonic power and bonding force. It also further benefits from wedge bonding, which is the most

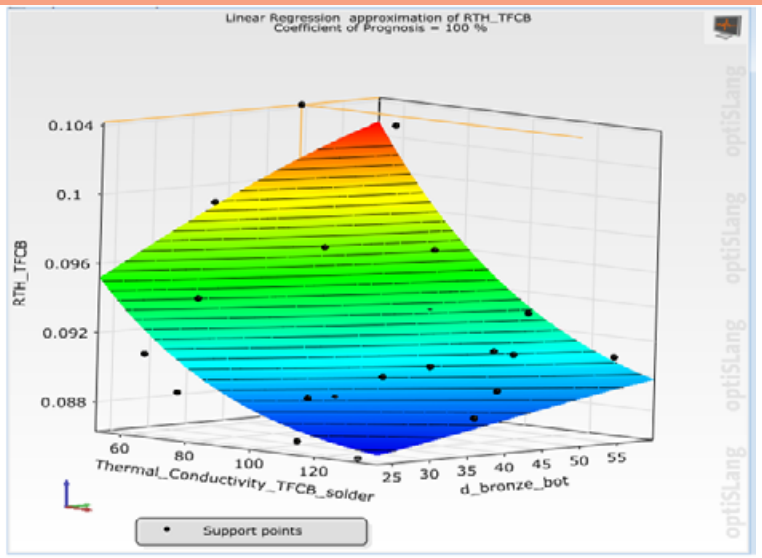

Figure 10: DoE output of FEM simulation showing the influence of the thickness of the brazed metal layer and the thermal conductivity of the brazed metal layer on the thermal resistance.

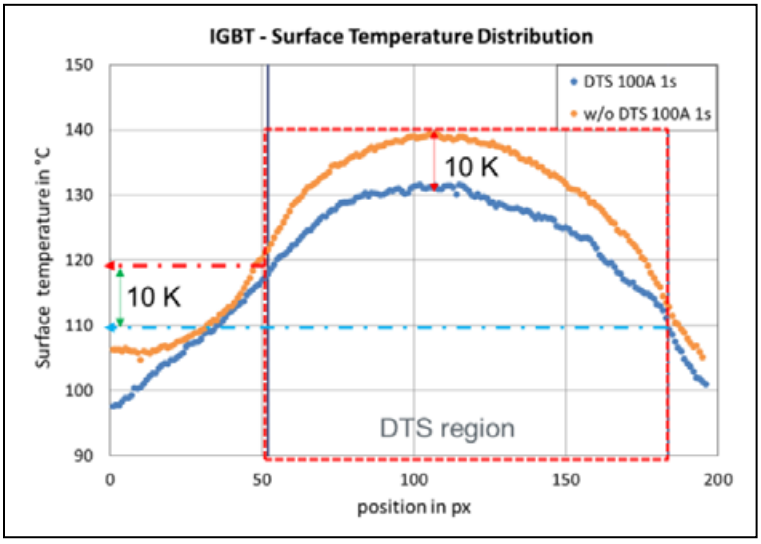

Figure 11: Temperature distribution over a soldered die with Al wires and a sintered die with DTS® and Cu wires during a power cycling test.

widespread interconnection technology in the electronics industry.

A first result of the use of our mechanical protection technology can be readily found by measuring the temperature distribution over a die sintered on a metal ceramic substrate during operation (**Figure 11**). The thermal camera shows a decrease of the temperature possibly due to a more uniform current distribution over the die surface, the lower electrical resistivity of copper and a better thermal dissipation of the material stack. This demonstrates that more current could be switched for the same temperature increase. In fact, this behavior explains why the use of this mechanical protection also improves the surge current capability of a power module as reported elsewhere [7].

Power cycling tests confirm that sintering and DTS® significantly improve the reliability of the die frontside and backside interconnections. **Figure 12** shows the number of cycles until end of life for several sample configurations together with some pictures of cross sections taken after failure. In the case of soldered silicon insulated-gate bipolar transistors (Si IGBT) with Al wires, the failure is clearly related to the lift-off of the bonded wires, accelerated by the increase of the thermal resistance because of solder fatigue [5]. With sintered Si IGBT and DTS®, the lifetime dramatically increases. The main failure is found to be the propagation of cracks in the front metallization of the die [6].

To increase the current density switched by the same Si IGBT, the test vehicle has been soldered to a baseplate that is directly cooled by water (direct cooling) instead of being contacted to the heatsink using a TIM (indirect cooling). A current increase of more than 40% is obtained. However, the lifetime is reduced by a factor of ~5—still significantly higher than for die soldered with Al wires. For indirect cooling, the root cause analysis indicates a break starting from the edge

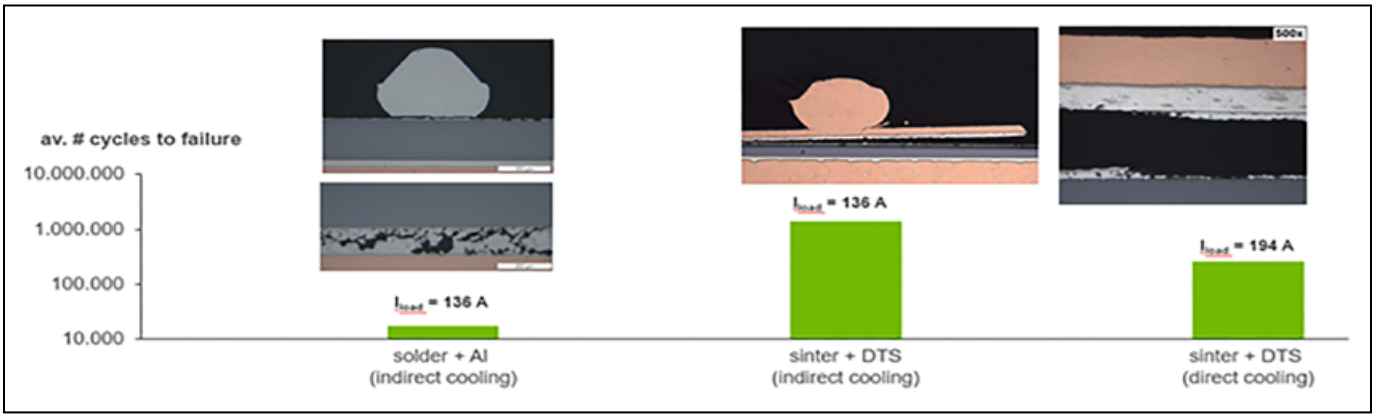

Figure 12: Average number of cycles to failure for several sample configurations tested with power cycling (t_{on}/t_{off} = 1s/2s, $T_{j,max}$ = 175°C, ΔT_j=130K). Soldered Si-IGBT with Al wires have been compared to sintered dies with DTS®. The metal ceramic substrates are either contacted to the heat sink using a TIM (indirect cooling) or soldered to a baseplate that is directly water cooled (direct cooling). Pictures of cross sections show the failure mechanisms for the different sample configurations.

of the mechanical protection layer between the sintered layer and the die, then propagating into the front-side metallization of the die. A degradation of the die attach is also observed. In the case of direct cooling, the same break propagation from the edge of the mechanical protection layer down to the front-side metallization of the die is also observed. However, there's no degradation of the die attach, probably due to the more efficient heat dissipation. Finite element model (FEM) analyses show that the lifetime reduction might be related to an increased plastic strain per cycle into the front-side metallization of the die. This could be due to a higher stiffness of the test vehicle and/or to the temperature being locally higher on the die at higher currents [6].

By enabling higher power densities and higher operating temperatures, our mechanical protection layer turns out to be a suitable solution for the interconnections of SiC metal-oxide semiconductor field-effect transistors (SiC-MOSFETS). Power cycling tests demonstrated a doubling of the lifetime when using DTS® compared to sintered dies with Al interconnections [8]. More recently, power cycling tests up to 200°C have been reported with DTS® and a 1,200V SiC-MOSFET from Wolfspeed [9]. In this case, the failure mechanism is a cohesive break in the sintered layer, although a break in the front-side metallization of the die was expected. However, the number of cycles to failure is in line with results reported at lower operating temperatures, thereby demonstrating the robustness of both die and package at 200°C (**Figure 13**).

Summary

As the semiconductor industry continues seeing high-power electronics applications, there is a need to provide reliable metal ceramic substrates that offer superior electrical, thermal, insulation and mechanical performance while also being able to work with typical assembly and interconnection technologies. Various metal ceramic substrates have been used; however, each provides drawbacks, including precious metal content and a slow vacuum brazing process. We have found a solution that offers a cost-efficient, highly-reliable Ag-free thick-film copper bonding paste that joins nitride-based ceramics with Cu foils and eliminates the need for vacuum-based brazing technology. The technology has been proven by thermal shock, peel strength, thermal measurements and thermal simulations. Numerous studies show that Condura®.ultra enables cost-efficient, but highly-reliable metal ceramic substrate manufacturing using Ag-free paste and a non-vacuum-based brazing process. Additionally, DTS® can

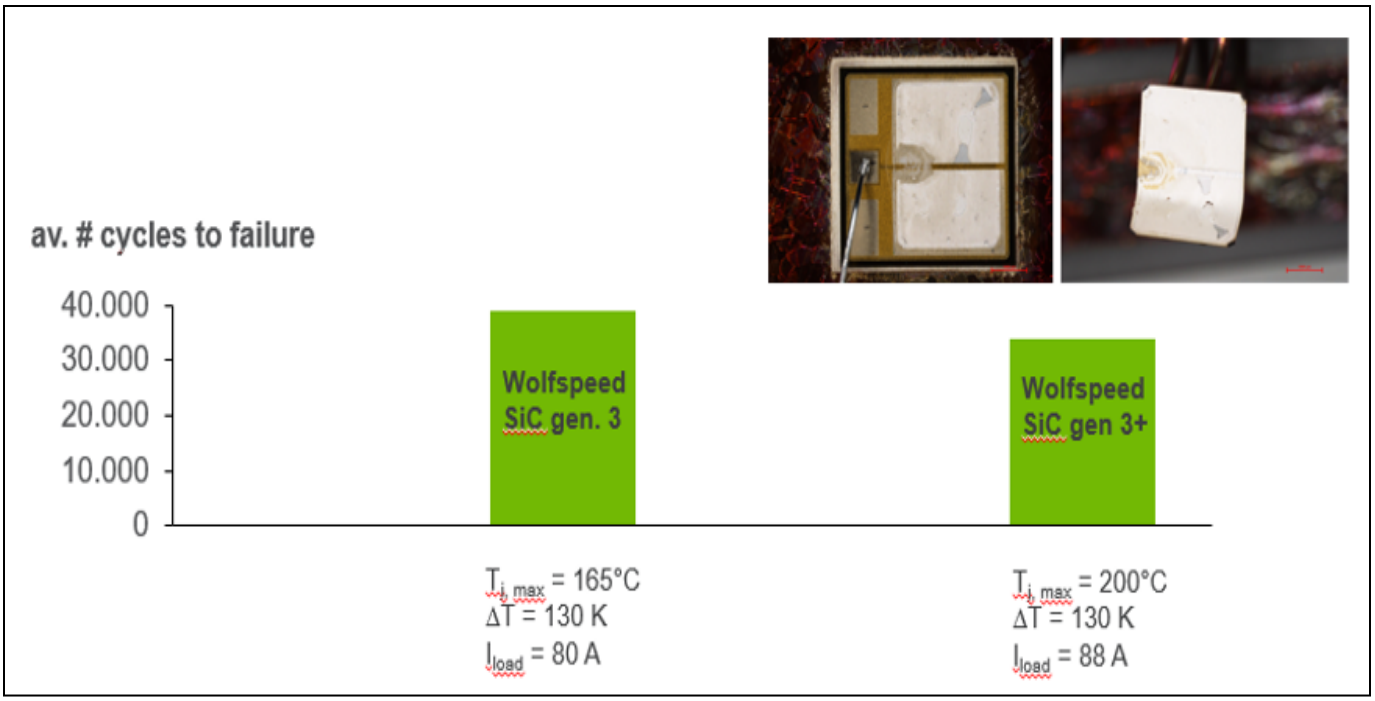

Figure 13: Average number of cycles to failure for sintered SiC-MOSFETs and DTS® tested with power cycling (t_{on}/t_{off} = 1s/2s). The results at $T_{j,max}$ = 165°C are from [8]. The pictures show the fracture surface on the DTS® backside or the die frontside after failure at 200°C.

meet the severe requirements for SiC-MOSFETs and can accelerate its adoption.

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Biographies

André Schwöbel, is a Senior Engineer at Heraeus Deutschland GmbH & Co. KG, Hanau, Germany, focusing on introducing new metal ceramic substrates into the market. He has a PhD in Materials Science from Technical U. Darmstadt, Germany. Email a.schwoebel@heraeus.com

Christophe Féry is a Market Segment Manager for Power Electronics at Heraeus Deutschland GmbH & Co. KG, Hanau, Germany. He works on the development and market introduction of new products. He has a PhD in Materials Sciences from the U. of Lorraine, France.

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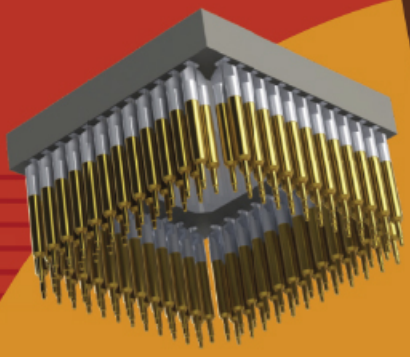

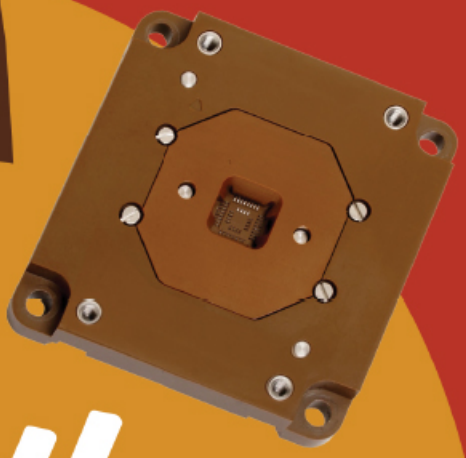

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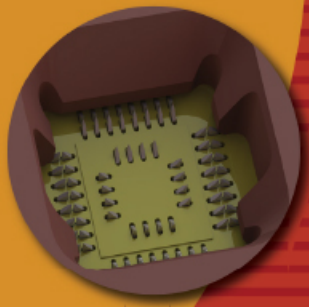

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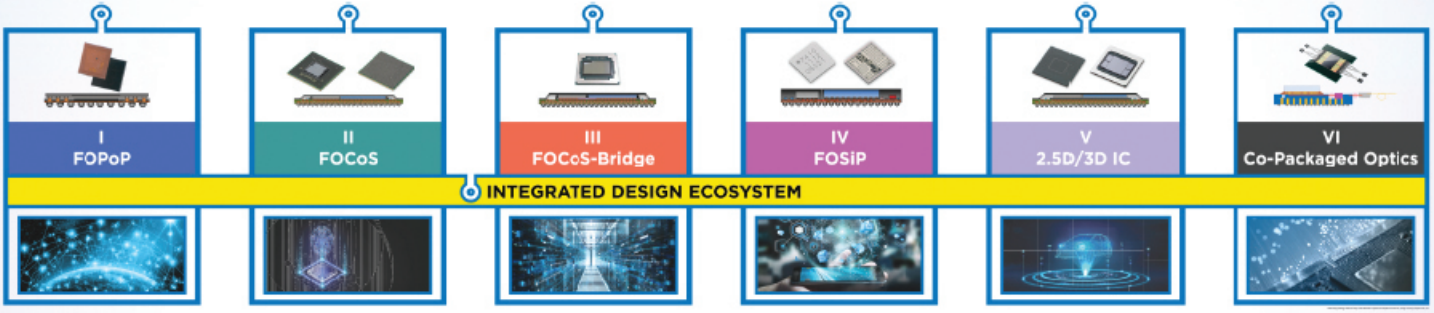

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