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Volume 26, Number 4

July • August 2022

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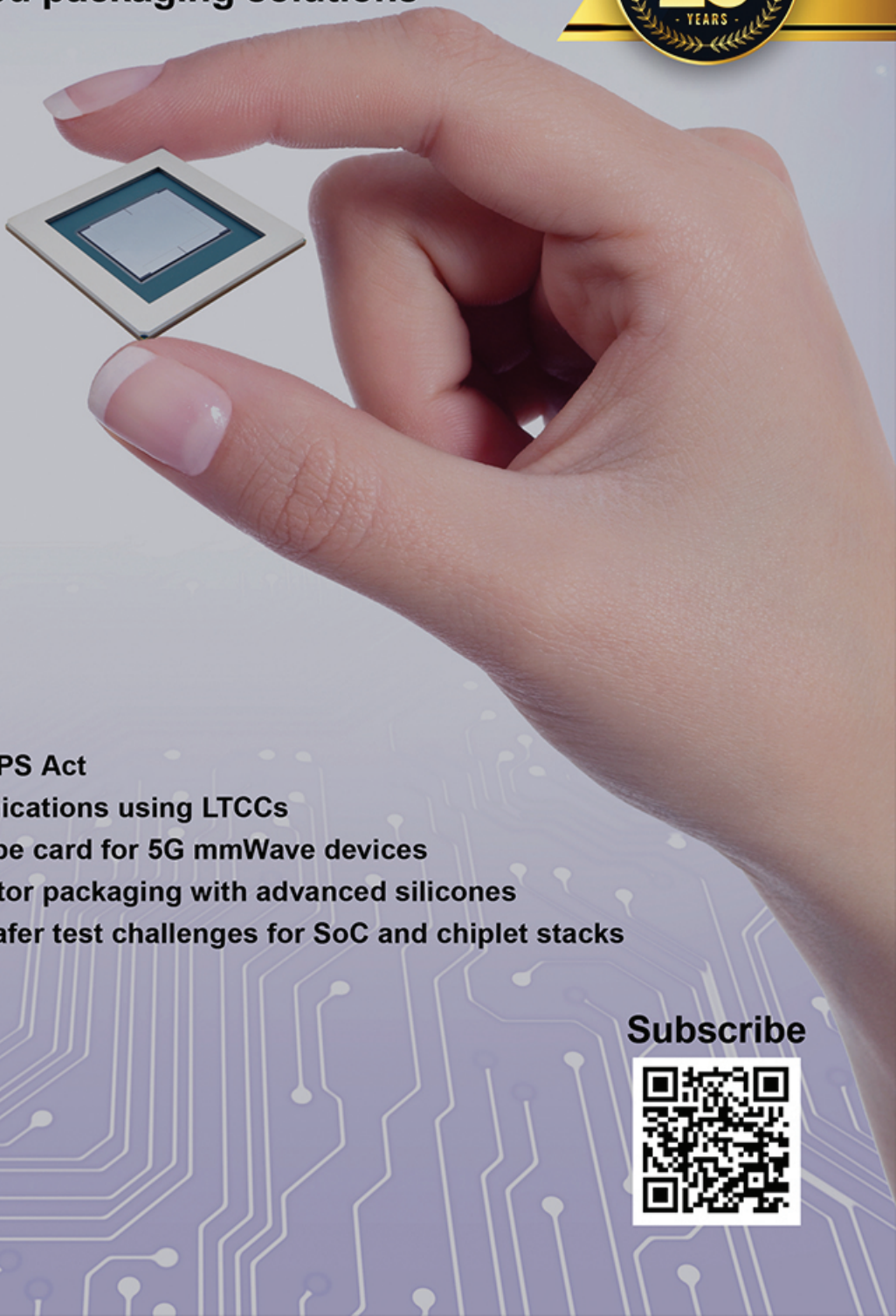

- Perspective on the CHIPS Act
- Advancing 5G communications using LTCCs
- A 55GHz octal-site probe card for 5G mmWave devices
- Improving semiconductor packaging with advanced silicones
- Overcoming thermal wafer test challenges for SoC and chiplet stacks

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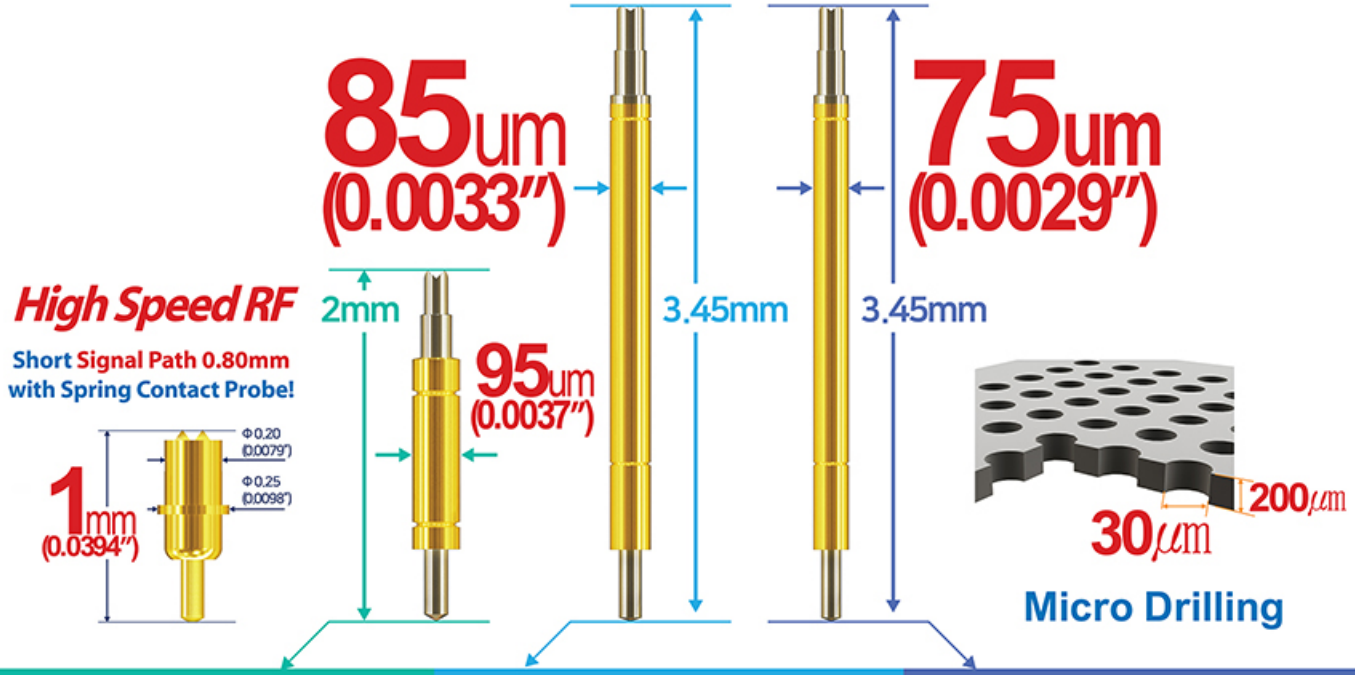


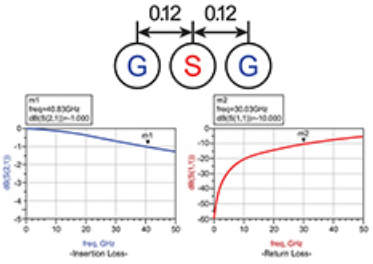
120㎛ Pitch

Mechanical Spec.

- Spring Force : 0.281oz (8.0g) @ .0098 (0.25mm)
- Recommended Travel : .0098 (0.25mm)
- Full Travel : .0118 (0.30mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation Data)

- Current Rating : 1.0A
- Propagation Delay : 20.80ps
- Capacitance : 0.21pF
- Inductance : 0.38nH
- Insertion Loss : 40.83GHz @ -1.000dB
- Return Loss : 30.03GHz @ -10.000dB
  (Dielectric material : CERAMIC)



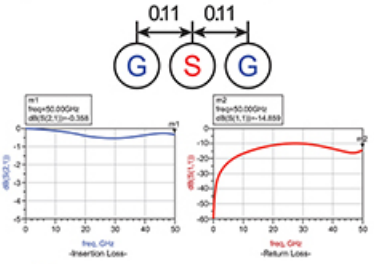
110㎛ Pitch

Mechanical Spec.

- Spring Force : 0.212oz (6.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation Data)

- Current Rating : 0.9A
- Propagation Delay : 38.25ps
- Capacitance : 0.47pF
- Inductance : 0.63nH
- Insertion Loss : > 50.00GHz @ -1.000dB
- Return Loss : > 50.00GHz @ -10.000dB
  (Dielectric material : CERAMIC)



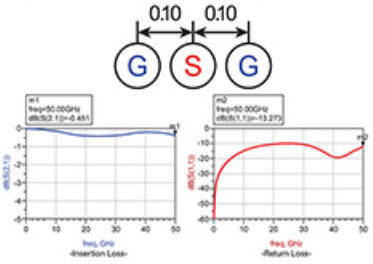
100㎛ Pitch

Mechanical Spec.

- Spring Force : 0.247oz (7.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation Data)

- Current Rating : 0.8A
- Propagation Delay : 35.55ps
- Capacitance : 0.44pF
- Inductance : 0.66nH
- Insertion Loss : > 50.00GHz @ -1.000dB
- Return Loss : > 50.00GHz @ -10.000dB
  (Dielectric material : CERAMIC)



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ASE's advanced packaging is based on six critical packaging technologies. These technologies are built upon an open silicon ecosystem in partnership with foundries, component suppliers, and across the supply chain. Furthermore, these technologies provide the capabilities necessary to enable highly-integrated silicon packaging solutions.

Cover image courtesy of ASE, Inc.

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Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry.
Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at Gilroy, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine
P.O. Box 2165
Morgan Hill, CA 95038
Tel: +1-408-846-8580
E-Mail: subs@chipscalereview.com

Printed in the United States

FEATURE ARTICLES

DEPARTMENTS (continued)

TECHNOLOGY TRENDS

INDUSTRY EVENTS

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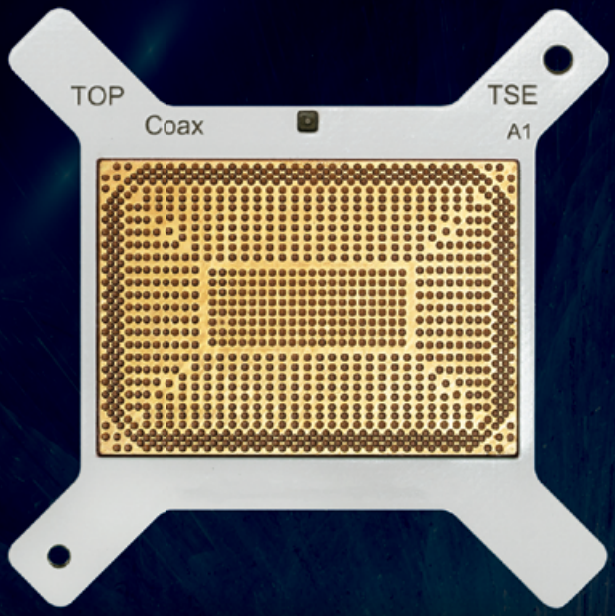
COAXIAL ELASTOMER SOCKET

for >64Gbps ATE/SLT Test
for Crosstalk free Board to Board Connector



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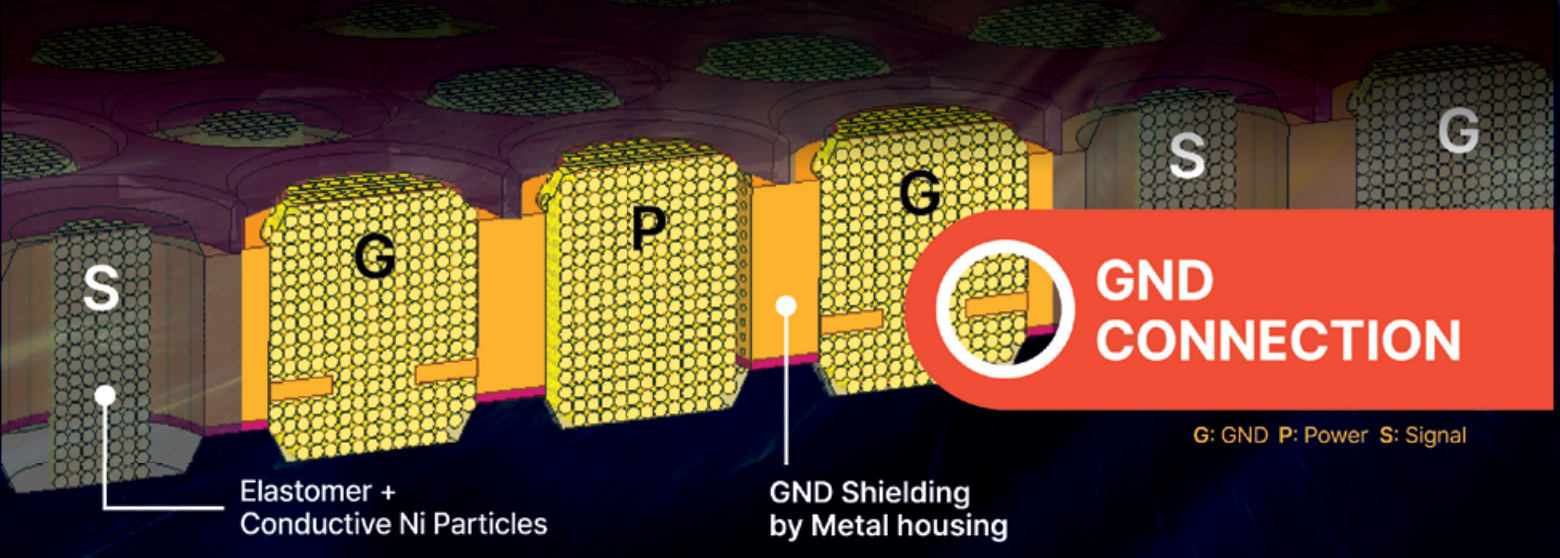
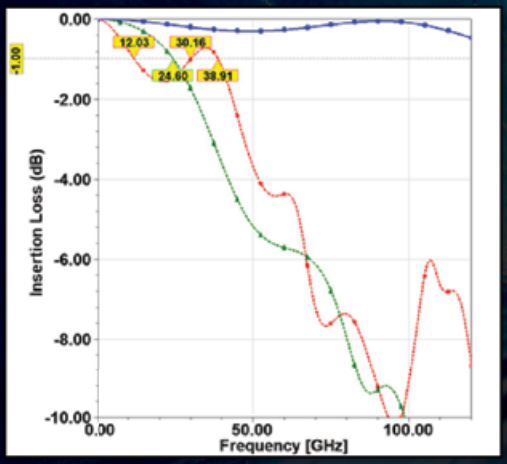


COAXIAL ELASTOMER SOCKET

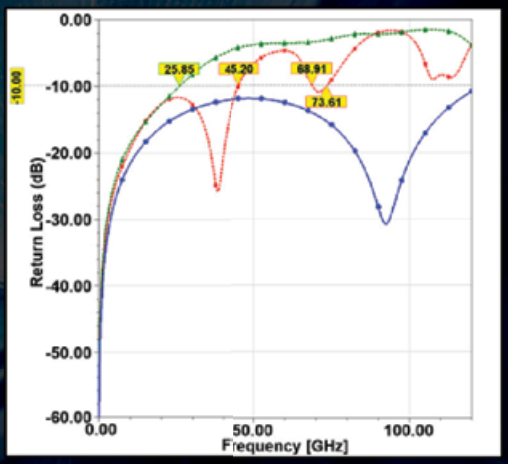
for >64Gbps ATE/SLT Test
for Crosstalk free Board to Board Connector

ELTUNE-coax™

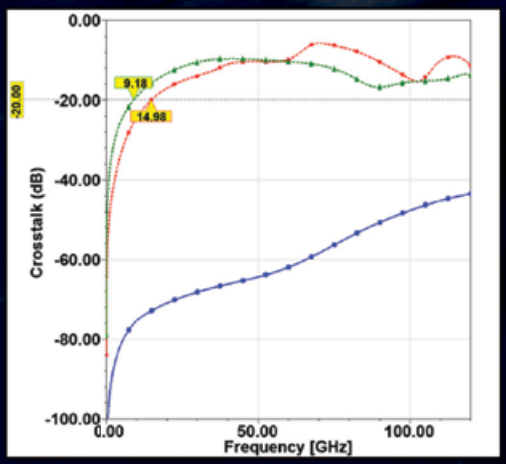
Electrical Specifications (unit: GHz)			
50Ω, 0.80mm pitch	Spring pin	Elastomer	ELTUNE-coax™
Electrical Length(mm)	3.05	0.60	0.60
Insertion Loss(S21) @-1dB	12.03	24.60	>100
Return Loss (S11) @-10dB	45.20	25.85	>100
Crosstalk (S31) @-20dB	14.98	9.18	>100



Insertion Loss



Return Loss



Crosstalk

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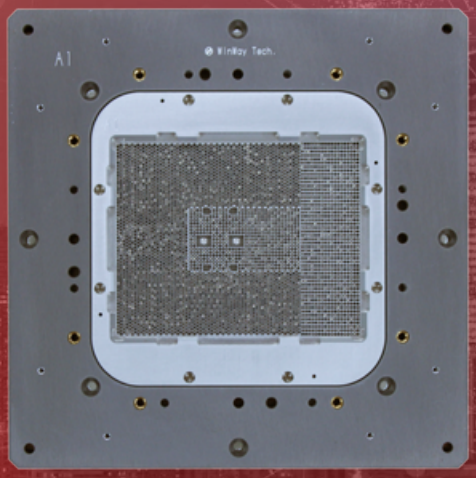
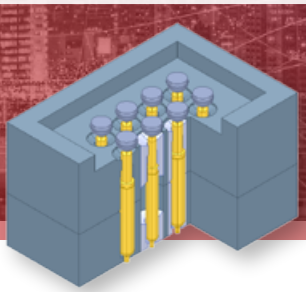
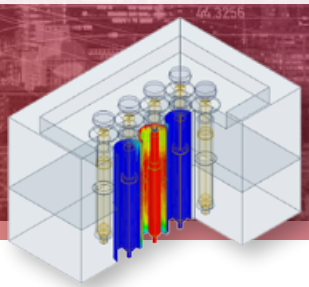


Bandwidth up to 112Gbps

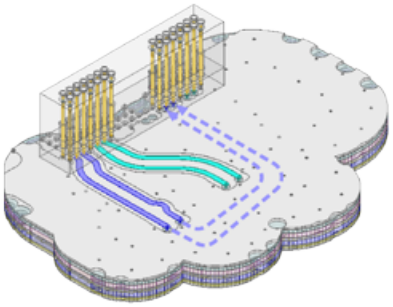


Co-grounding Design



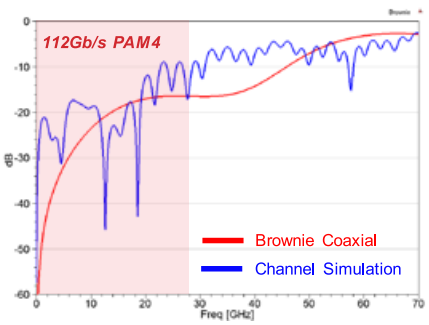
EM Wave

3D Stacking Simulation

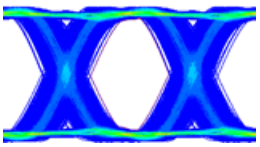
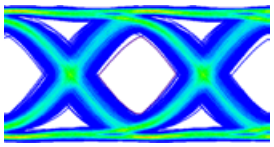
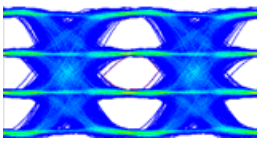
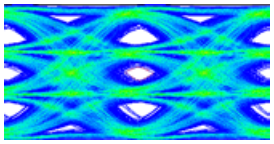


For high speed test application, it's necessary to evaluate the performance of the entire channel at engineering stage to ensure the specifications can be reasonably defined during testing.

Return Loss



Eye Diagram

	Socket Only	Channel Simulation
56Gb/s NRZ		
112Gb/s PAM4		

Solution	Bandwidth	Crosstalk	Impedance (50Ω)
Plastic Socket	<20 GHz	-10 ~ -25 dB	△>10 %
Coaxial Socket	>80 GHz	-50 ~ -70 dB	△3 ~ 5 %

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Overcoming thermal wafer test challenges for SoC and chiplet stacks

By Markus Kindler [ATT-Systems] Amy Leong [FormFactor Inc.]

Leading-edge artificial intelligence (AI)/graphic/mobile processors, dynamic random access memory (DRAM) devices, and heterogeneous integrated IC stacks are all facing the same set of thermal management challenges, i.e., the device under test (DUT) is too hot to test. Even at room temperature wafer chuck settings, a mobile system-on-chip (SoC) device junction temperature can reach between 100°C to 150°C. For full-wafer DRAM testing, up to 2,000W of power may be applied during a single touchdown test. Recent technology roadmaps show even higher heat dissipation requirements ranging up to 3,500W. With the rise of heterogeneous integrated chiplet stacks, test cell thermal management becomes even more complicated. When testing the base die with multiple chips stacked on top, the thermal loading per silicon area is increased by an order of magnitude. If the temperature is not controlled, it can result in burnt probes, damaged devices, and inaccurate test results.

The temperature cannot be controlled unless it is first measured. ATT-Systems' (a FormFactor company) low thermal resistance (LTR) wafer chuck technology applies multiple temperature sensors across the thermal chuck to accurately detect DUT temperature and adjust heat dissipation to achieve the desired test temperature. LTR has shown promising results in production test to address the "too hot to test" challenge.

Selecting the optimal wafer chuck system

A wafer chuck system consists of a wafer chuck, a controller, and depending on the application and temperature range, an air booster, or either a liquid- or air-type chiller. Without a chiller, the thermal chuck systems can control temperatures between +20°C and +200°C. For cold testing, chillers have two options of cooling mediums: air-cooled or liquid-cooled.

Figure 1 compares the maximum cooling capacity of air- and liquid-cooled configurations at a testing temperature of -40°C. The cooling capacity is a function of the specific heat capacity, the thermal mass and the applied ΔT (i.e., the difference between the coolant inflow temperature and the coolant outflow temperature).

The lowest possible coolant temperature in air-cooled chillers available today is limited to around -80°C. The cooling outflow temperature is basically determined by the testing temperature, which is -40°C in this example. Assuming a typical air-flow of 320 l/min, the given ΔT of 40K, and the properties of air, the calculated maximum cooling capacity is nearly 275W. Looking at properties of a thermal fluid, it is obvious the thermal mass of the liquid coolant is >40 times higher than air, resulting in a substantially higher maximum cooling capacity.

The example below is showing an inflow coolant temperature of -50°C. The testing temperature is at -40°C, which results in a ΔT of 10K. Using the same equation as for air-cooled systems and a coolant flow rate of 10 l/min, the calculated maximum cooling capacity is 3,300W, even the ΔT is remarkably lower. A lower ΔT leads to significantly better temperature uniformities, which is equally important for current state technologies. Moreover, the cooling capacity can be scaled up by applying more powerful chillers. In summary, liquid-cooled systems give an order of magnitude higher cooling capacity with better temperature uniformities and are the systems of choice for high-power applications.

After selecting the cooling mechanism, the next critical design consideration is active thermal control (ATC).

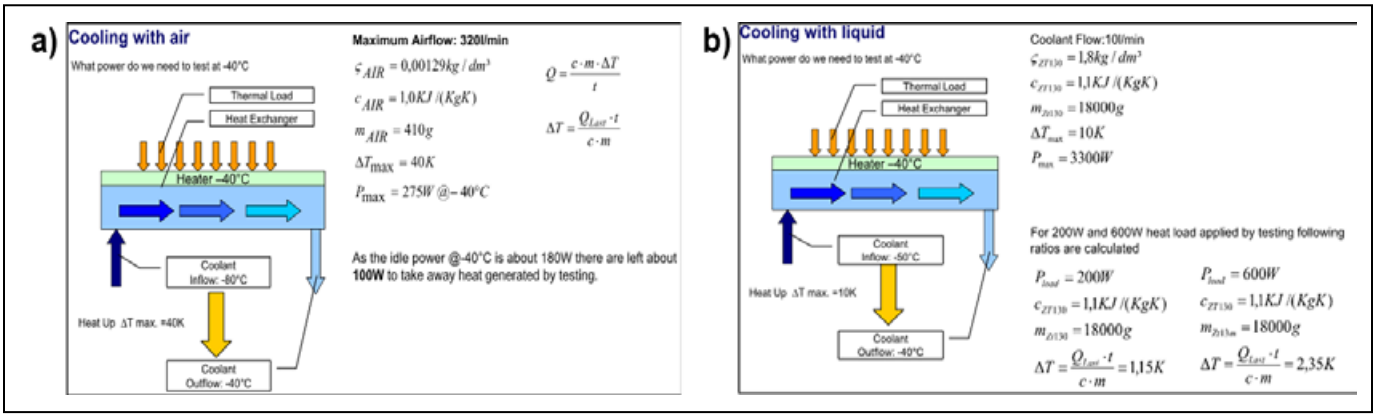

Figure 1: Cooling capacity comparisons between a) air and b) liquid-cooled systems.

Figure 2: Number of sensors scaled to contact area size, ordered from low- to high-sensor array density.

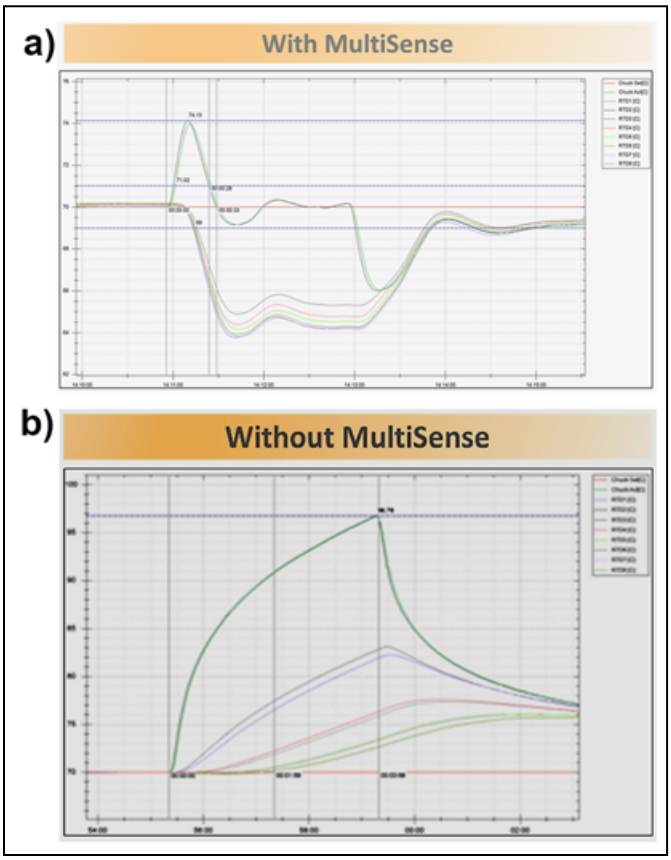

Figure 3: a) Multiple sensors vs. b) single-sensor temperature response and control results.

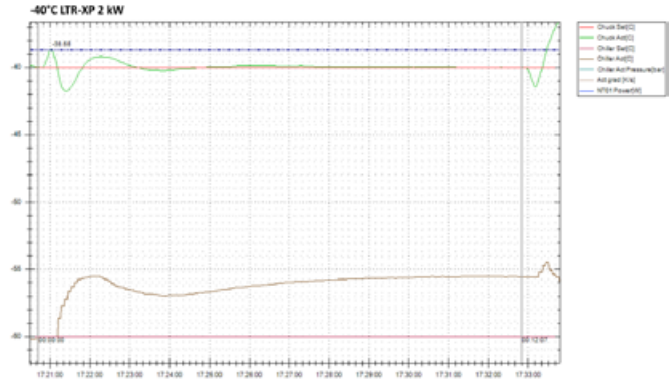

Figure 4: Full-wafer contact test (2000W) with -40°C test temperature.

Detecting the temperature in real time and with accuracy are essential first steps to controlling it. ATT-Systems' low-thermal-resistance (LTR) wafer chucks include a MultiSense option, which places multiple sensors across the chuck to accurately measure the temperature. The number of sensors used varies depending on the application, and is mainly driven by the contact area size. The smaller the contact area, the higher the quantity and array density of sensors. While full-wafer contact applications such as DRAM testing only require one sensor, multi-touchdown devices like automotive microcontrollers or graphics processing units (GPUs) can use up to 21 sensors (**Figure 2**).

Using multiple wafer chuck sensors vs. a single sensor

Let's look at an example of testing with and without our multiple sensor solution. **Figure 3** shows a wafer chuck test setup of a 21 x 22mm contact area with a liquid cooler. In this test, 200W was applied for two minutes with a desired temperature of 70°C. The solution with multiple sensors (**Figure 3a**) shows that the temperature initially jumped to 74.1°C when the power was switched on. After 28s, the temperature was brought back down to +/-1°C of the desired number. At the 33s mark, the 200W of power was completely dissipated. The test using only a single sensor (**Figure 3b**) presents different results. When the power was turned on, the temperature rose past 96°C in the two-minute time frame. The system did not detect a thermal change or implement an active temperature control solution.

With the flexibility of additional sensors, this new LTR wafer chuck technology can be used for a wide variety of high-power applications, including full-wafer contact DRAM testing, automotive microcontrollers, and 5G devices. These active thermal control solutions have proven to be valuable in a series of case studies.

Case studies

The first case study is a full-wafer contact example that is used for high-bandwidth memory (HBM) testing. The setup includes a wafer chuck and 300mm heating plate to simulate the 2,000W wafer test conditions. With a 300 x 300mm contact area, the power will be uniformly distributed throughout the entire chuck area, prompting the need for only one sensor. For this test, the three temperature points were -40°C, 25°C and 125°C. **Figure 4** shows that once the 2,000W of heat was applied, it dissipated within seconds and was brought back down to within +/-2°C of the desired temperature.

The automotive microcontroller case study used a 100 x 100mm contact area with medium parallelism. For these devices, heat transfer can be up to 1000W, with a moderate power density of 10W/cm^2. Nine sensors are recommended for this contact area size to cover all areas of the chuck. During the case study, 400W was applied across the wafer at three temperature points: 0°C, 85°C and 105°C. As seen in **Figure 5**, the correct sensor detected the temperature increase and the chuck system was able to dissipate the 400W within a +/-2°C

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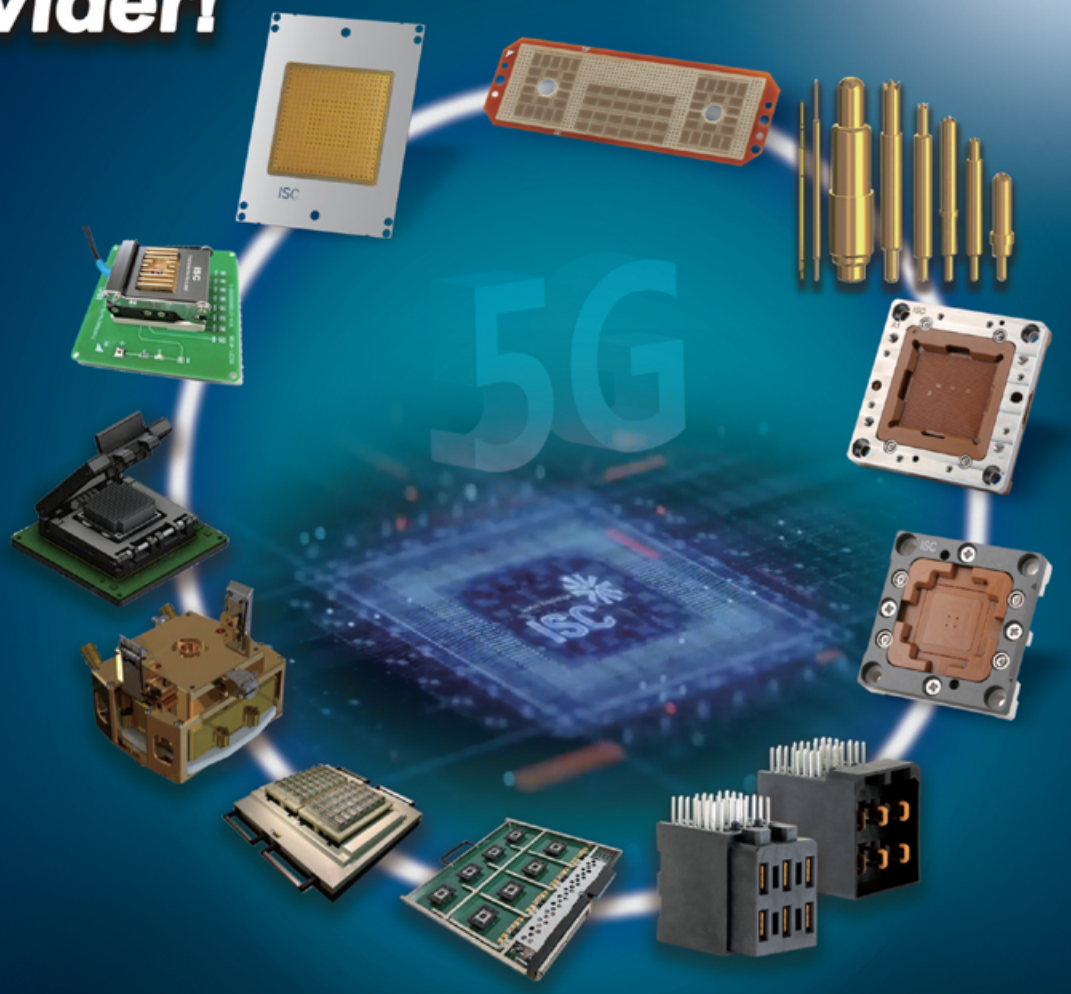

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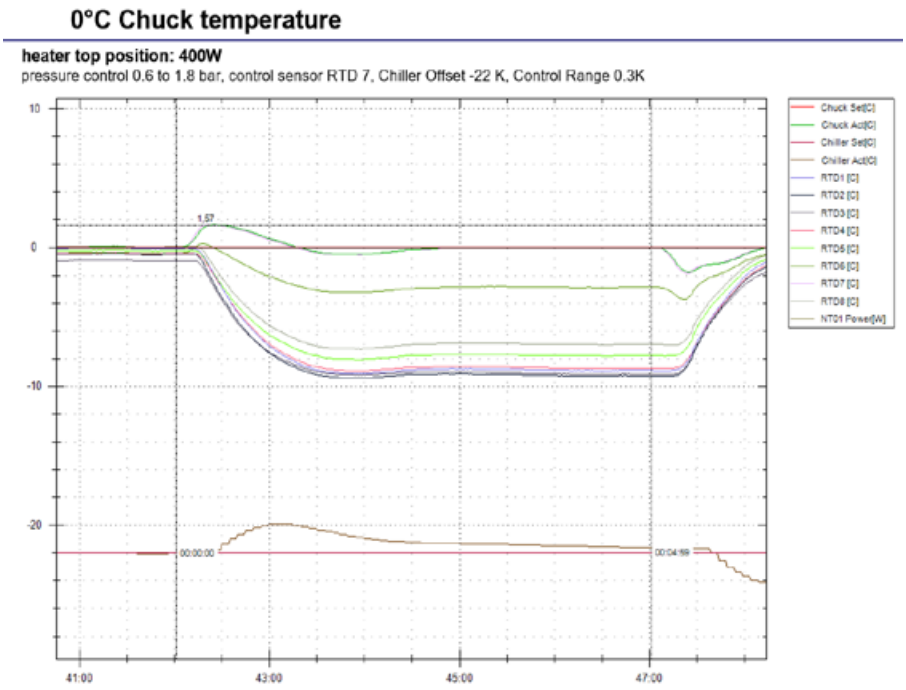

Figure 5: Automotive microcontroller test (400W) with 0°C test temperature.

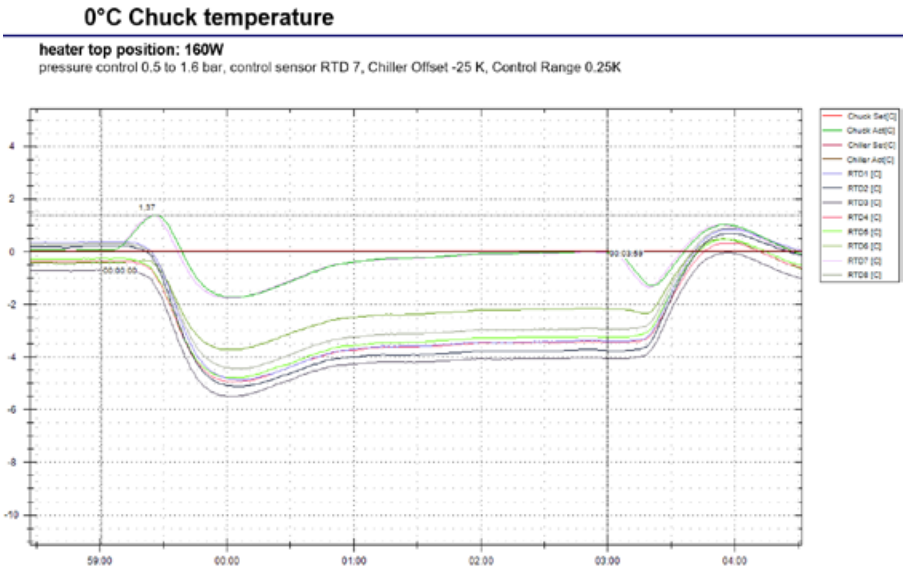

Figure 6: 5G device test (160), with 0°C test temperature.

temperature range for each test.

The last customer study used a small 20 x 21mm contact area, which is representative of applications such as 5G and GPU devices. These examples with low parallelism and small contact areas can have high-power densities up to 125W/cm^2. For these high-power applications, 21 sensors are ideal to reliably detect temperature changes at all touchdown areas. In this customer study with a 5G device, 160W was applied at 0°C and 105°C. As demonstrated in **Figure 6**, the system dissipated the 160W within +/-2°C of the desired temperature.

Summary

Thermal management for wafer test is changing dynamically because of increased parallelism, high-power densities, and complex IC designs. To ensure that a device is tested at the desired temperature, wafer chucks with multiple temperature sensors, as well as liquid-cooled capabilities, are required for timely high-power dissipation. In addition, smart thermal management solutions are crucial for avoiding burnt probes and damaged devices, to ensure high test cell uptime. Various customer production case studies have shown the necessities of using a low thermal resistance wafer chuck systems with multiple temperature sensors, including full-wafer contact memory testing with up to 2000W, medium-contact areas with up to 400W, and small-contact areas of a few DUTs with up to 160W. With leading-edge SoCs, high-bandwidth memory testing, and heterogeneous integrated devices, new thermal testing challenges continue to arise. Our wafer chuck approach is prepared to help overcome future challenges with active thermal control solutions.

Biographies

Markus Kindler is a Managing Director at ATT-Systems, a FormFactor company, Munich Germany. Mr. Kindler is responsible for global sales, marketing, and applications. Prior to ATT-Systems, he held various technical and business leadership roles at Siemens, Hitachi, and KLA. Email: Kindler@att-systems.com

Amy Leong is Senior Vice President, CMO and General Manager at FormFactor Inc., San Jose, California. Ms. Leong has held various management positions at the company including product marketing, product development, business development, and mergers and acquisitions. Prior to FormFactor, Ms. Leong worked in a variety of semiconductor engineering and business roles at Gartner, KLA-Tencor and IBM.

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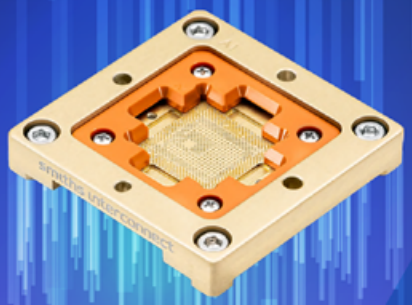

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The coaxial structure of the DaVinci Micro test socket provide ideal pin to pin isolation reducing the effect of cross talk during testing. This allows for at speed functional testing of your IC.

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- Optimized for power integrity of DUT
- Patented insulated metal socket housing provides un-matched mechanical strength
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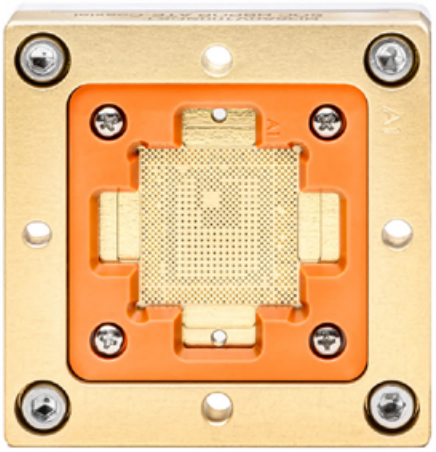

DaVinci Micro inherits the DaVinci coaxial technology for IC applications to 350µm pitch. DaVinci Micro's fully shielded signal path negates the effects of cross-talk during testing, allowing an immediate yield enhancement over non-DaVinci products.

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Vertically-integrated packaging solutions driven by innovations

By Mark Gerber, Lihong Cao, Vikas Gupta, Patricia MacLeod [ASE, Inc.]

As Moore's Law continues to challenge the foundry companies to increase transistor density, new performance and cost challenges are driving the need for heterogeneously integrated (HI) advanced packaging solutions. Advanced silicon node yield attainment is a key driver for looking at ways to approach intellectual property (IP) block integration. The high development cost and lower yields are challenging designers to look for new ways of disaggregating system on chips (SoCs), to reduce the die size, by separating IP blocks that may not need to be in the most advanced silicon node. Creating a SoC-like solution with optimized silicon nodes for different portions of the chip is a new key focus. Advanced redistribution layer (RDL) packaging technologies that add a vertical integration element allow for a denser, 3D approach. At the same time, the traditional packaging components, such as substrates, are also being pushed to limits in which new solutions are needed to extend roadmap requirements. These roadmap requirements are seen across all industry market segments including server, networking, graphics, mobile and telecom infrastructure.

Each market segment has unique requirements to meet its product needs and there are a few common challenges across all of these segments. For example, as advanced silicon nodes continue to shrink the die size and increase the power density per square mm, the challenge of signal noise increases dramatically. In addition, the impedance challenges of connecting one chip to another in a system dramatically reduces the performance that can affect battery life, or power requirements in an array bank of processors. The higher density per area of transistors and reduced line to carry power also challenge the thermal capabilities of the package—and when combined with other areas of impedance in the system, can create larger system-level problems.

ASE has developed a series of RDL-based vertically-integrated packaging solutions that continue to evolve to meet these various challenges. The six pillars underneath the VIPack™ platform include: fan-out system-in-package (FOSiP), fan-out chip-on-substrate (FOCoS), fan-out chip-on-substrate bridge (FOCoS-B) (embedded), fan-out package-on-package (FO-PoP), 2.5D/3D and co-packaged optics (CPO). Each one of these package pillars addresses specific performance and/or form fit challenges and provides advanced solutions that address the market segments listed above. Packaging innovation within these six technology pillars are being evolved by ASE and these will be reviewed in the sections below.

FOPoP

Over the last decade, the trend for most handheld consumer devices development was towards multi-functional, high-definition display, low power consumption, high performance, and thin/light packages, that are now commonly found in smartphones, tablets, and wearables. This trend drove the development of complex 3D or 2.XD integration on integrated circuit (IC) packages. Flip-chip package-on-package (FCPoP), initially with traditional C4 solder bump and later with fine-pitch Cu pillar, was the primary package used because of the inherent low-inductance package interconnect.

The ever-increasing need for higher performance and thinner form factor drove the accelerated implementation of FOPoP in the mobile processor application space. The fundamental high-density, substrate-less configuration of the FOPoP package results in higher package performance because of the elimination of the substrate parasitic inductance along with a thinner package form factor.

Overall, the FOPoP structure provides 1) higher interconnection density and integration through a finer L/S redistribution layer (RDL) as compared to substrates, and 2) a shorter interconnect length resulting in better electrical performance, and 3) a smaller/thinner form factor because the fan-out technology allows die I/O signals to be fanned out to a region larger than the die area without an organic substrate to meet a higher I/O count.

Figure 1 shows a FOPoP package with the cross-section image showing the die, RDLs, and Cu post details. Additional cross-section details are included in **Figure 2**, where the active side of the die utilizes two routing planes to fan out the I/O signals. Fine-pitch Cu posts are used on the periphery to enable electrical connections for the package on top.

The FOPoP package platform is further enhanced for increasing complexity and high-performance needs by enabling RDL on both sides of the die for increased integration and functionality. Furthermore, both land-side caps and near-die deep trench capacitors (DTC) can be implemented to meet the power integrity requirements of advanced nodes. FOPoP is, and will continue to be, a key package platform for application processors, mobile/auto antenna-in-package (AiP), and co-packaged silicon-photonics applications.

FOCoS

The advances in fan-out technology further provided opportunities to address the limitations of traditional flip-chip packages where a single SoC is assembled on a substrate. Two distinct categories are:

1. Utilizing the fan-out RDL process to redistribute the die-level I/Os to a coarser bump pitch to utilize less aggressive substrate design rules and/or to reduce the number of layers on the substrate. This approach also helps with low-k reliability issues related to chip-package interactions.
2. Multi-die and chiplet integration where two or more dies can be reconstituted into a fan-out module and then assembled on a substrate.

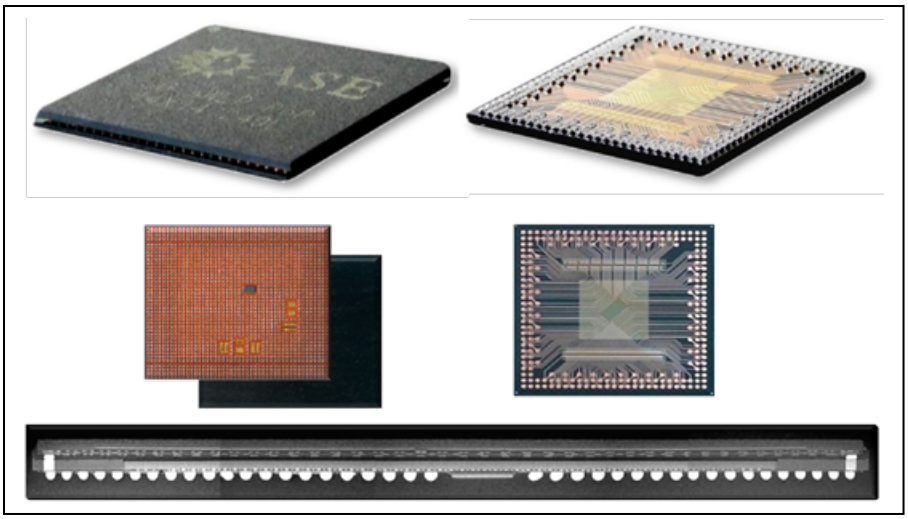

Figure 1: A fan-out package on package (FOPoP).

The FOCoS platform provides versatility in integrating multiple instances of same dies or different dies across digital/analog and other functionalities to provide a highly integrated heterogeneous solution. Chiplet integration offers a compelling value proposition for yield improvement, IP reuse, performance, and cost optimization. Heterogeneous integration through advanced packaging technology enables chiplet integration with separate designs and different manufacturing process nodes within a single package. It has provided advancement for more intelligence, greater connectivity, and higher performance at a more manageable cost.

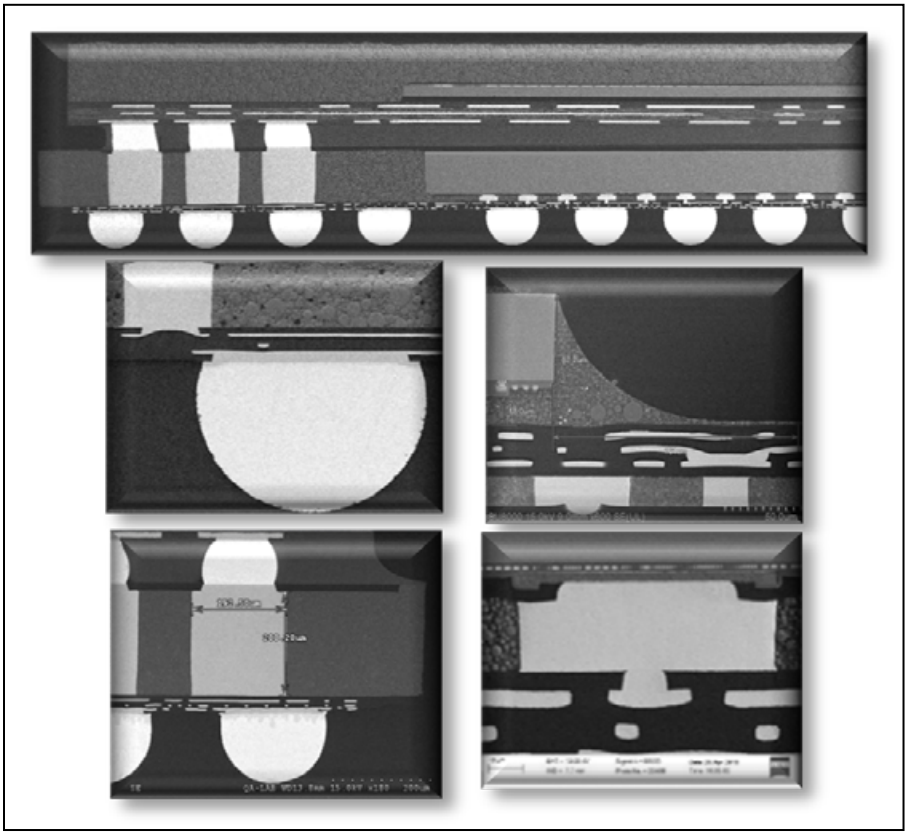

Figure 2: FOPoP cross-section details.

Advanced packaging technologies such as flip-chip ball grid array (FCBGA), multi-chip modules (MCMs), and 2.5D Si through-silicon vias (TSVs) have been widely used for chiplets and die-to-die (D2D) interconnections across various semiconductor segments. However, with increasing demands for high density, high speed and low latency of D2D interconnects, the FC MCM package has reached its limit due to the large Cu interconnect line/space L/S>5/5µm in the substrate, and unsustainable costs related to 2.5D Si TSV with larger interposer size (>2X reticle size). Therefore, alternative packaging solutions such as 2.5D TSV-less and fan-out RDL interposer have been developed in recent years. Three of the six VIPack™ technology pillars namely, FOCoS, FOCoS-Bridge and 2.5D/3D provide chiplet integration options depending on the bandwidth, latency, and other design/performance requirements.

Various FOCoS solutions, e.g., FOCoS chip first (FOCoS-CF) and FOCoS chip last (FOCoS-CL), have been introduced. The schematic structure of FOCoS is shown in **Figure 3** with the cross-section image as shown in **Figure 4**. The FOCoS package contains different chips and flip-chip devices mounted on a high pin count BGA substrate, and Cu RDL replaces the expense of using a Si TSV interposer to provide interconnects.

FOCoS packaging technology has enabled chiplets integration with multiple RDL interconnects up to five layers, a smaller RDL L/S of 1.5/1.5µm and a large fan-out module size of 32x38mm^2. It also provides a wide portfolio integration, such as an application-specific integrated circuit (ASIC) with high-bandwidth memory (HBM) and ASIC with Serdes across many segments of HPC, networking, artificial intelligence/machine learning (AI/ML) and the Cloud. Furthermore, FOCoS has demonstrated better electrical performance and lower cost than 2.5D Si TSV because of the elimination of the Si interposer along with reducing parasitic capacitance.

FOCoS-Bridge

The increasing amount of data from all sectors driven by digital transformation is raising a problem of operational and storage costs. Meanwhile, the exponential cost leaps of silicon scaling and the unaffordable increasing of Si die size over the reticle limit have created an inflection point for the semiconductor industry. It has driven the development of "More-than-Moore"

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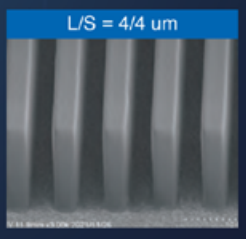

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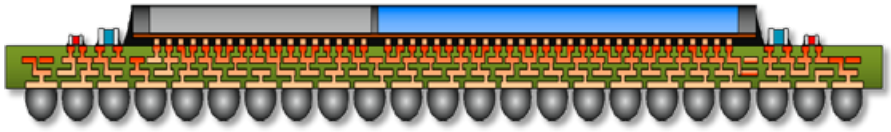

Figure 3: The schematic structure of a FOCoS package.

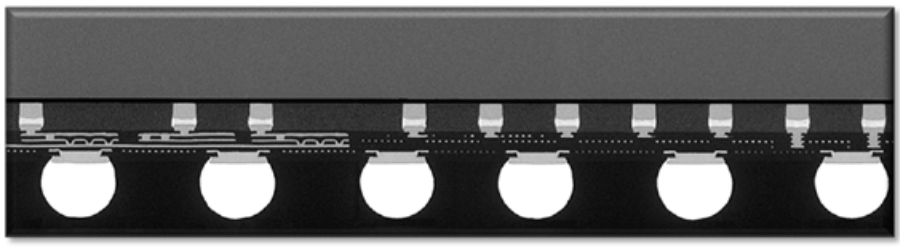

Figure 4: Cross-section image of a FOCoS package.

techniques to augment increased device and system performance. Advanced packaging technologies continue to play critical roles and gain momentum in semiconductor segments across HPC, 5G, automotive, internet of things (IoT) and industrial sectors. Several advanced packaging technologies have been developed and widely used to integrate multi-chips with fine line/space interconnections, such as 2.5D Si TSV interposers, fan-out RDL, and embedded bridge die-in-substrate.

FOCoS-CF and FOCoS-CL technologies have been developed and introduced by using RDL interconnect for chiplets integration at ASE. FOCoS-CF has been in mass production since 2016. Because of the inherent fan-out RDL process limitation, however, it has hit a bottleneck in the manufacture of RDLs with higher layer counts (>6 layers) and finer line/space dimensions (L/S<1µm/1µm) for the applications that require high-density D2D connections, high input/output (I/O) counts, and high-speed signal transmission. To address this, a new technology named as FOCoS embedded Si bridge (FOCoS-B) has been developed to enable ultra-high density D2D interconnection with L/S<1/1µm for high-density chiplets integration. FOCoS-B packaging technology enables D2D interconnect by embedding a small Si die in a fan out RDL interposer. The small Si die plays an interconnection bridge role between chiplets with L/S<0.8µm/0.8µm. **Figure 5** shows the schematic structure of a FOCoS-B package with the optical image. It is composed of two identical fan-out modules that are assembled on one FCBGA substrate in an MCM arrangement. The fan-out module is integrated by 10 chiplets (two ASICs and 8 HBM2e with 8 Si bridge dies). The FOCoS-B package body size is 78x70mm^2 with two fan-out chip modules at a size of 47x31mm^2, respectively. FOCoS-B packages have passed reliability tests and chiplets integration has achieved good integrity. **Figure 6** shows the cross-section of a FOCoS-B package; this package has extensive options and flexibility for multiple bridge die integration for mobile products (AP), HPC, AI/ML and server applications.

FOCoS technology has demonstrated better electrical performance for chiplets integration. The fine-pitch RDL in FOCoS is essential to provide lower insertion loss and better signal integrity (SI) because of the thicker Cu RDL with L/S=2/2µm compared to a thinner Cu RDL with L/

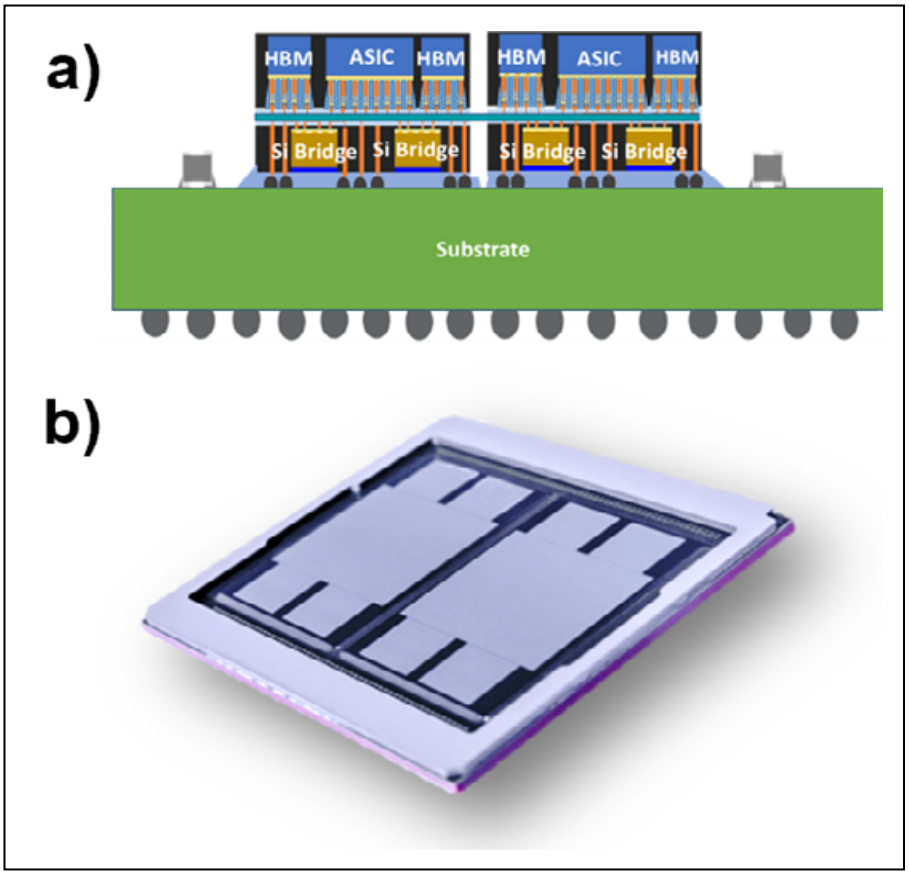

Figure 5: a) (top) Schematic structure and b) (bottom) the optical image for a FOCoS-B package.

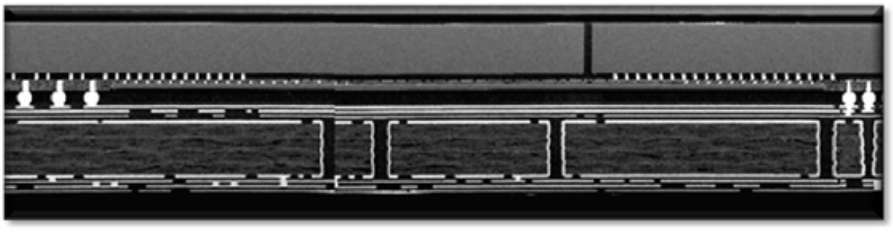

Figure 6: A cross-section of a FOCoS-B package.

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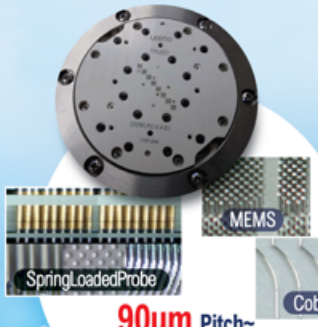
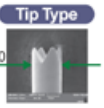
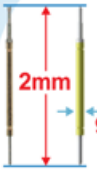
90um Pitch~

Spring Contact Probe



90um Pitch~ Probe Head

Tip Type




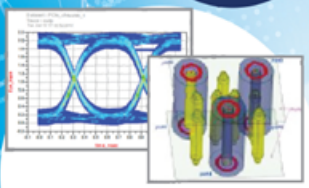
Specification
Pitch : Min.120um
Spring Force : 8.0g@ 250um
Current Rating : 1.0A
Inductance : 0.38nH

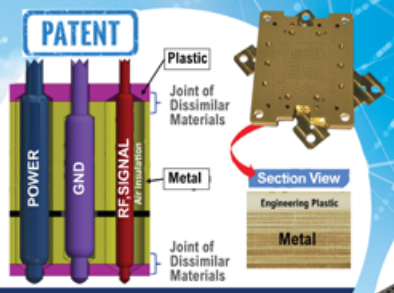
RF Probe for Fine Pitch Probe Head


0.18mm Pitch~
RF Coaxial Spring Probe & Impedance Controlled

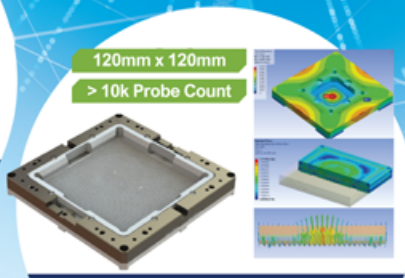

Logic Test Socket


High Speed
Frequency : >20GHz
VSWR : < 1.2
Automatic Coaxial Probe


Electrical Analysis
CCC Test, HFSS, TDR
Eye Diagram
4 Port VNA Test

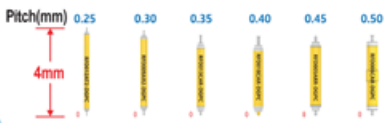


MP Socket



Large Device Socket

Specification
Frequency : 80GHz(BGA),
100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%



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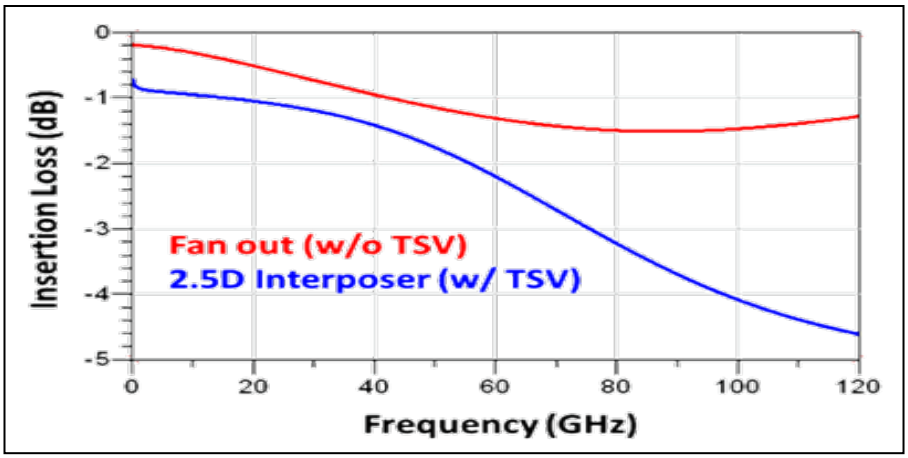

Figure 7: Insertion loss comparison between a FOCoS package and a 2.5D interposer.

S=0.8/0.8µm in a 2.5D Si TSV interposer, which results in lower parasitic capacitance and lower cross talk. **Figure 7** shows the insertion loss comparison between FOCoS and 2.5D Si TSV at different frequencies. The better eye diagram performance is also observed in FOCoS compared to 2.5D SI TSV, which is shown in **Figure 8**.

FOSiP

The term system-in-package (SiP) has had many definitions over the years and as its umbrella has grown across both the low-end and high-end application spaces, the description must allow for advancements. ASE published its formal definition in 2014, which states that an SiP module is a package that contains an electronic system or sub-system and is miniaturized through IC assembly technologies. Although this is a broad definition, it still holds true today, as individual silicon solutions are moving toward highly-integrated system or sub-system level solutions.

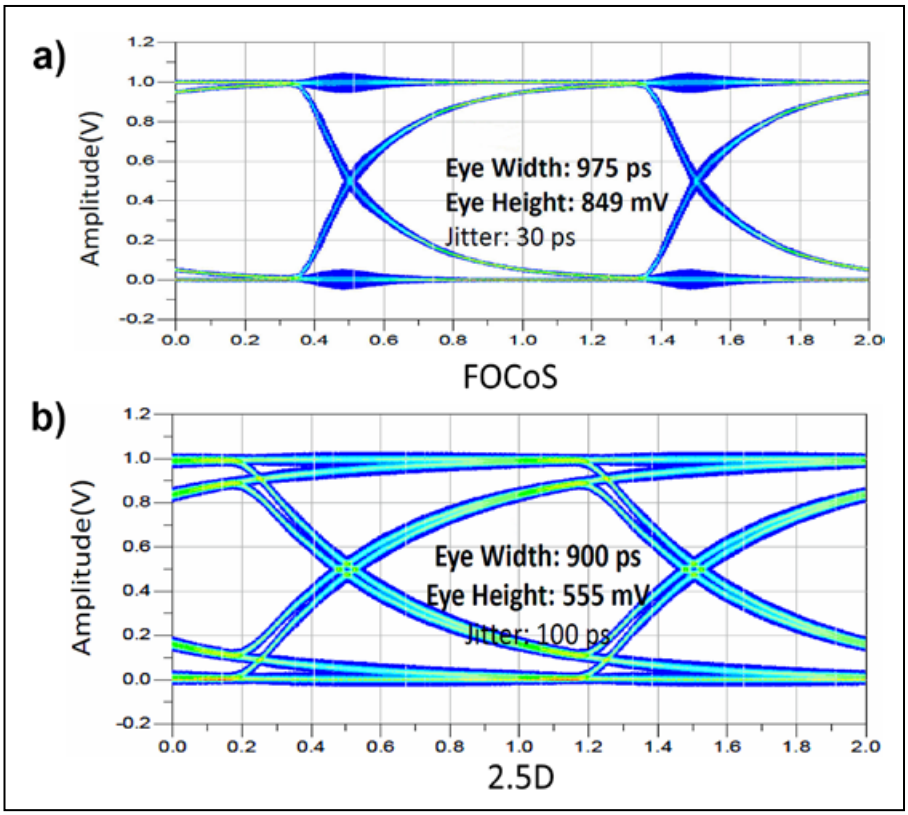

Figure 8: Eye diagram of a) (top) a FOCoS package vs. b) (bottom) a 2.5D interposer.

When we look at the various package platform roadmaps today, we see a trend around miniaturization, not necessarily just for final package size, but also for performance. For the mobile space, the original equipment manufacturer (OEM) suppliers are driving component size reduction or integration across all sub-modules to enable more room for new functionality while managing battery space.

Table 1 by TSR in February 2022 shows the modular adoption rate across various radio frequency (RF) modules. The one reduced adoption is partially due to the exit of LG, shrinkage of Huawei and adoption of the power amplifier module with integrated duplexer (PAMiD). Because of this trend, the need for technology that enables further miniaturization and integration while managing new performance challenges is driving companies to look at fan-out wafer-level packaging (FOWLP) RDL SiP-based technology. Wi-Fi and ultra-wide band (UWB) RF modules are also leveraging the SiP platform. **Figure 9** shows an example of a UWB module in an Apple iPhone 13 Pro with traditional SiP integration tools including packaged IC, discrete and IC components (five die, FC, WLP and shielding).

Specific drivers for FOSiP consideration include substrate thickness reduction, line/space control to minimize RF variation, and tighter component spacing for reduced losses for improved battery life (**Figure 10**). As with most advanced technologies, the key challenge is how to manage cost. When considering SiP, there is the tendency to focus on raw single-package cost vs. the system cost that integrates multiple packages and components. An overall system size reduction is realized by reduced individual component packaging, double-sided RDL for dense component integration (<50µm spacing) and a second RDL stack plane can simplify test, and in some cases, eliminating the substrate can help to enable a more competitive system solution.

Some of the key tools to consider in a fan-out RDL-based SiP may include chip-first discrete passives, but this may require a Cu plating termination for integration into the RDL; or if chip last

Shipment Mu	2020	2021	2022F	2023F	2024F	2025F
% TTL Smartphone						
PAMiD ↑	27%	33%	40%	42%	46%	48%
FEMiD+MMPA ↓	19%	14%	9%	5%	4%	4%
EN-DC Module ↑	0%	8%	19%	20%	21%	21%
5G HB (n41) PAM	12%	17%	14%	12%	12%	12%
5G UHB PAMiF ↑	20%	40%	52%	63%	71%	76%
5G mmWave Module	3%	6%	7%	7%	8%	11%
LMHB DRx Module ↑	61%	67%	76%	77%	78%	79%
5G UHB DRx ↑	15%	39%	52%	63%	71%	76%

Source: TSR, Feb 2022

Table 1: RF front-end module adoption rate. SOURCE: TSR, Feb. 2022

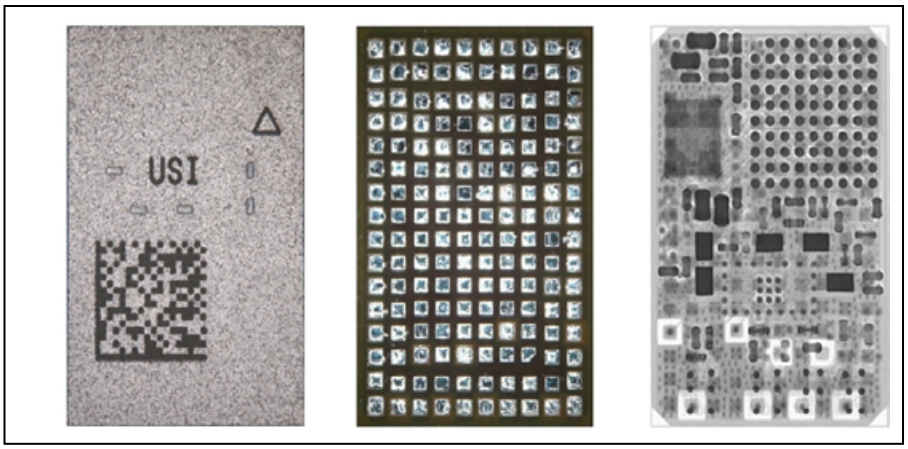

Figure 9: 2021 teardown analysis – USI UWB. SOURCE: TechSearch International

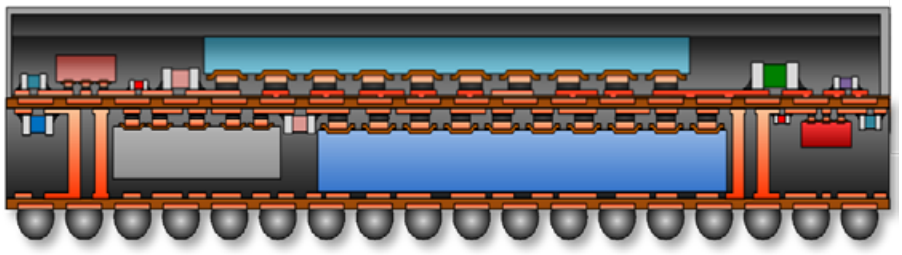

Figure 10: A chip-last double-sided FOSiP.

is used, a standard solder termination can be used. In addition, integrated or created passive components can also be beneficial. Both 2D and 3D spiral inductors, and even new inductor passives are being developed – within the RDL layers – to further improve the performance allowing them to be integrated and further miniaturized (see **Figure 11**).

2.5D/3D

The 2.5D platform with a silicon interposer evolved as a natural progression from MCM on organic substrate because of readily available sub-micron L/S. A 2.5D platform enables a greater than 1X reticle size die, and multi-layer sub-micron L/S for high interconnect density at low latency. The coefficient of thermal expansion (CTE) match between the active die and interposer also helps alleviate chip-package interactions that induce failure modes in flip-chip packages. **Figure 12** shows the 2.5D package in high-volume production at ASE; an ASIC and four HBMs are integrated on a silicon interposer using micro-bumps. The interposer is then assembled on a 70X70mm organic substrate.

Recent advances and ongoing developments in hybrid bonding (combined metal and dielectric bond) provide another step function improvement in interconnect density (**Figure 13**). Hybrid bonding is the ideal candidate to achieve 10µm and sub-micron scale for connectivity as compared to 100µm pitch in advanced flip-chip technology. Both die-to-wafer (D2W) and D2D hybrid solutions address reticle size limitations for manufacturing large dies. The reduction in pitch provides flexibility in SoC portioning. Furthermore, reduction of interconnection lengths from mm length

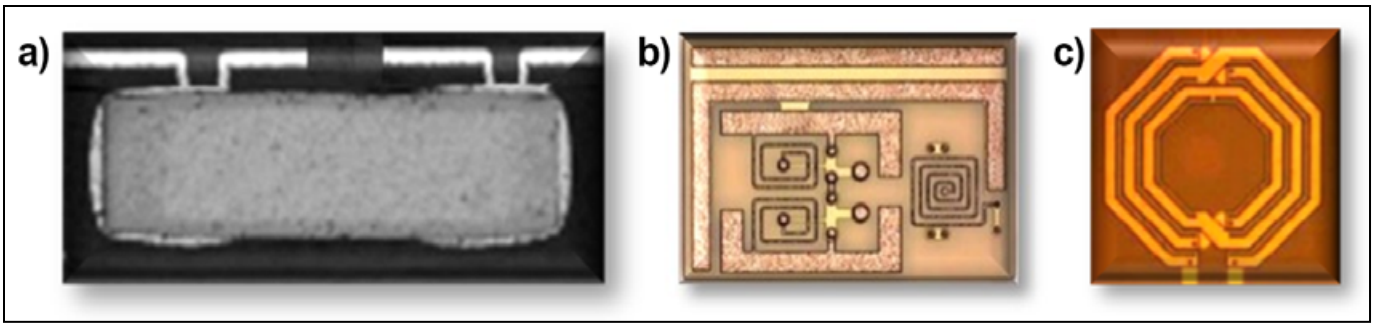

Figure 11: a) (left} Embedded passives in the RDL layers; and b) (middle) discrete and c) (right) created 2D and 3D.

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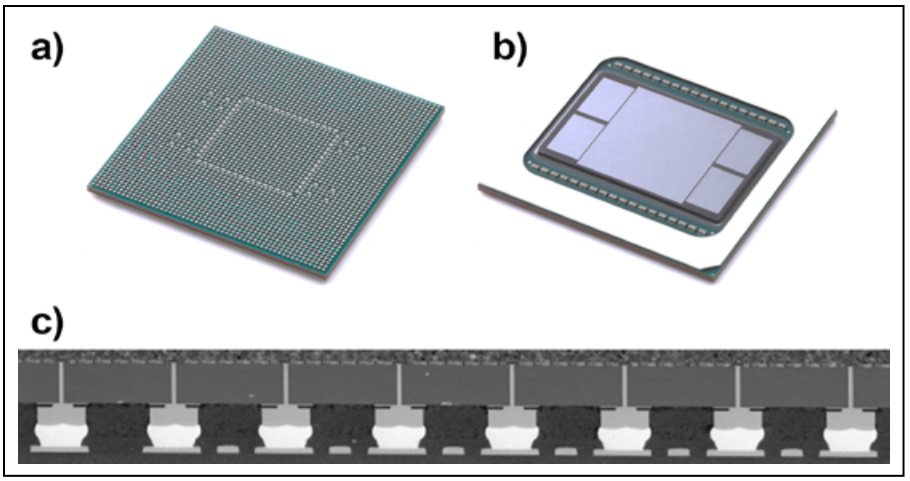

Figure 12: a) BGA side view of the 2.5D package; b) Top view showing ASIC and 4 HBM's; c) Package cross-section with details of TSV in Si interposer and bumps between interposer and substrate.

to micron length, along with high area interconnect densities enabled by finer pitches, enables a true 3D structure with reduced footprint, low latency and high bandwidth while increasing the total SoC area. In addition to packaging portioned SoC dies, hybrid bonding enables stacking of 3D dynamic random access memory (DRAM), heterogeneous integration at high I/O densities, lower power consumption, and form factor reduction.

CPO

The next level of performance packaging for long-distance signal transmission is moving from the traditional copper conductor lines to

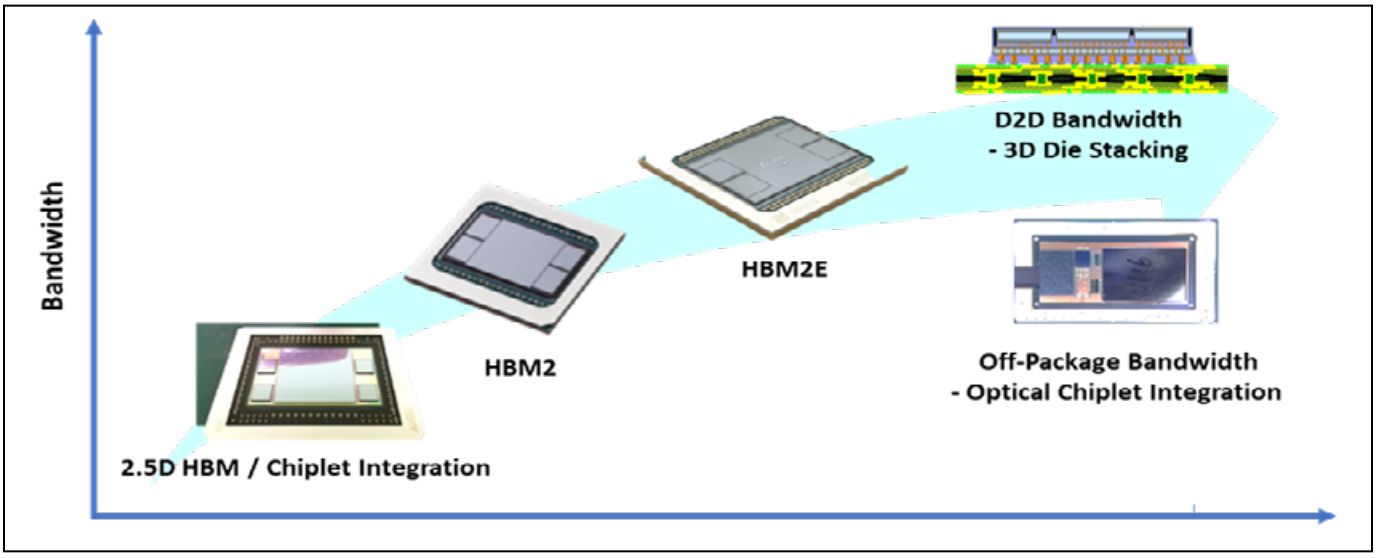

Figure 13: 2.5D to 3D evolution.

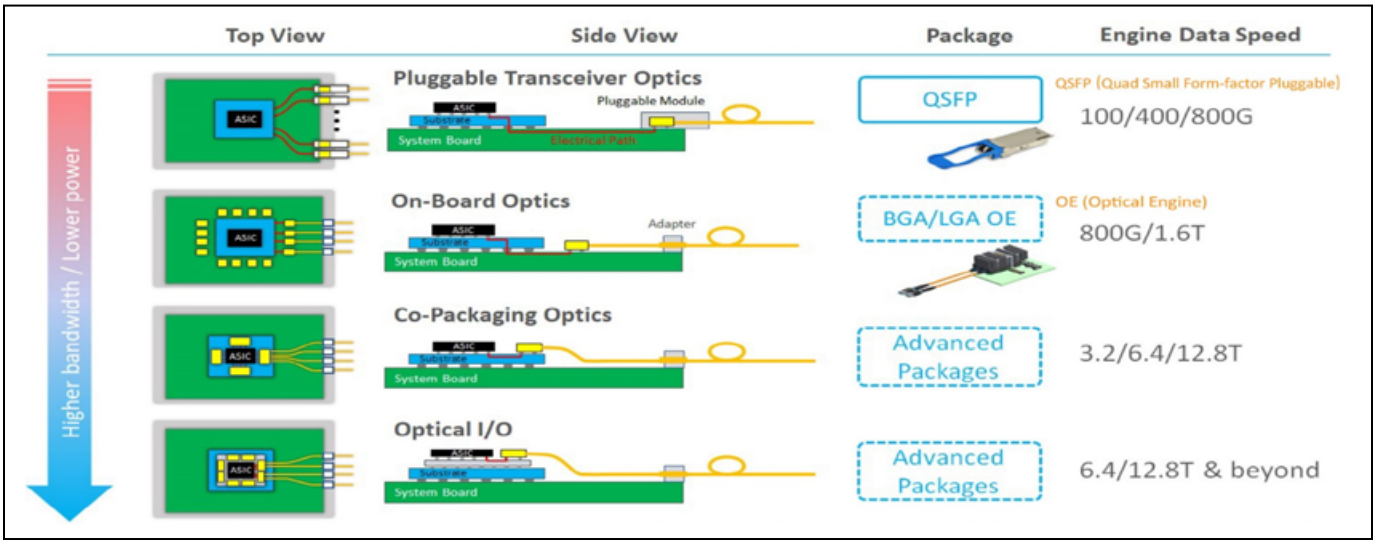

Figure 14: Bandwidth/power vs. integration method.

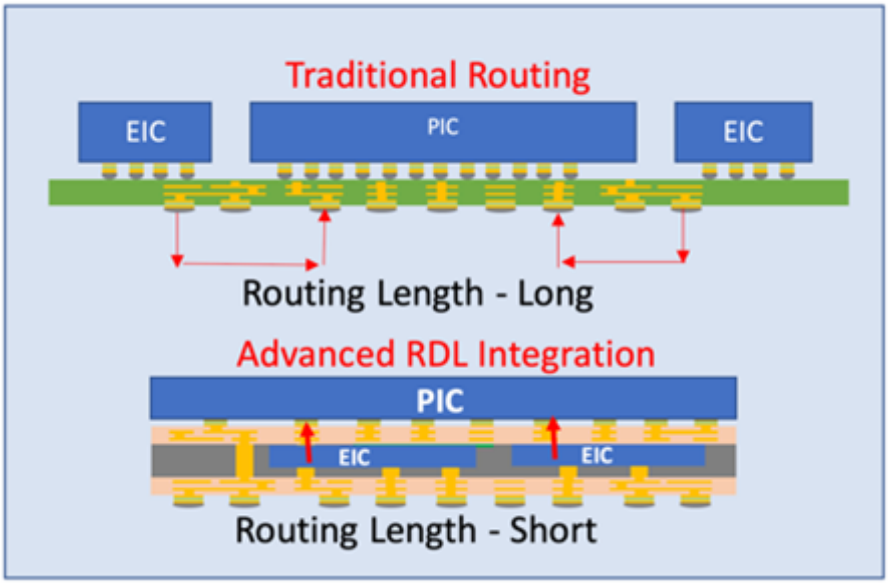

Figure 15: Traditional routing vs. advanced RDL integration.

light-based lines. Silicon photonics has been around since the mid-90s, but has faced technical and cost challenges. Since then, technical improvements and power-hungry scaling bandwidth requirements have driven the industry to accelerate the adoption of silicon photonics. Advances in module-based packaging of both pre-packaged and non-packaged components have helped in the evolution toward CPO. When we look at the various ways network switches can be organized, there is a clear reason why co-packaging the switch die and optics are key. **Figure 14** shows the increasing insertion loss (lower performance) and higher power requirements depending on how the communication is handled between the transmit and receive functions of the backplane.

This co-package configuration improvement reduces the losses between transmission lines and should follow similar rules when looking at IC packaging methodology. Looking at CPO closer, we see that this more integrated packaging methodology is bringing the critical components closer together to minimize losses between the electro-optical conversion process. Because of the custom nature of photonics ICs, CPO generally does not follow any pre-defined packaging rules, which leads to many different types of configurations within the industry. To further improve the CPO area, components must be integrated in the most efficient way while keeping in mind the best way to attach the optical fiber. As mentioned above, when components are placed in a 2D plane, there are longer lines and losses associated with the layout. This can be further enhanced by creative packaging as shown in **Figure 15**. This figure shows a traditional PIC die next to the EIC, side-by side approach, but a more efficient structure is shown by vertical coupling or grading coupling where the EIC die are located directly below the photonic IC. This is enabled by utilizing a double-sided fan-out wafer-level package structure that embeds two driver EIC dies right below the photonic IC die, thereby minimizing the critical length between the dies. This type of sub-module integration can help to enable another level of performance improvement for CPO.

Summary

Six critically important packaging technologies form the pillars of ASE's VIPack™ platform and are supported by a comprehensive and integrated co-design ecosystem. As described in this article, these pillars include ASE's high-density RDL-based FOPoP, FOCoS, FOCoS-Bridge, and FOSiP, as well as TSV-based 2.5D and 3D IC and CPO processing capabilities. The VIPack™ platform provides the capabilities necessary to enable highly-integrated silicon packaging solutions required to optimize clock speed, bandwidth, and power delivery, and to reduce co-design time, product development, and time to market.

These six pillars will help to deliver unique opportunities to those seeking optimum efficiency and performance for their applications. The technology pillars are built upon an open silicon ecosystem in partnership with foundries, component suppliers, and across the supply chain to provide design flexibility required for product realization. A spectrum of new process tools further enhances ASE's current toolbox of capabilities and supports evolving package structures being developed in alignment with industry roadmaps.

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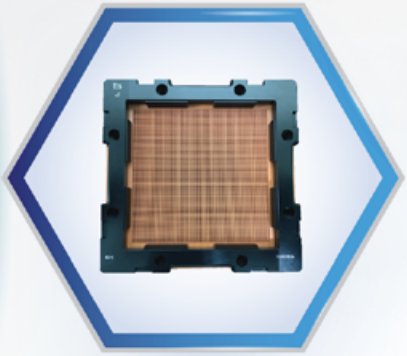
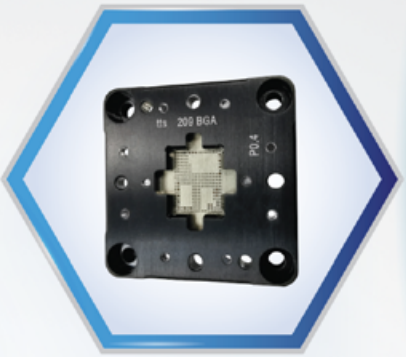


Coaxial

Pitch
≥0.40mm

Insertion Loss
>40GHz@-1dB

Crosstalk
>35GHz@-52dB

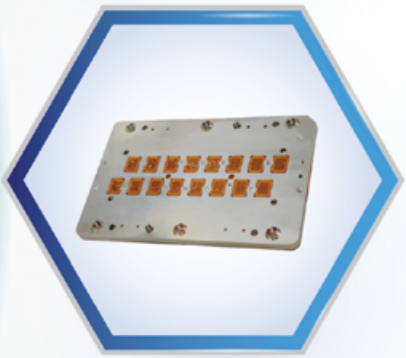


WLCSP Probe Head

Pitch
≥0.15mm

Pin Count
≤6000

Longevity
>1000K

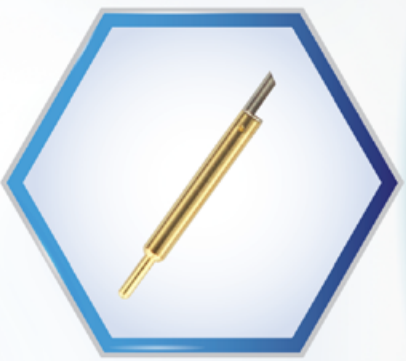


Probe Pin

Pitch
≥0.12mm

Power
≤6.5A

Frequency
>140GHz

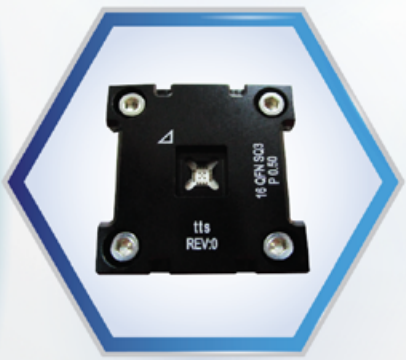


RF

Pitch
≥0.35mm

Insertion Loss
>60GHz@-1dB

Return Loss
>30GHz@-20dB

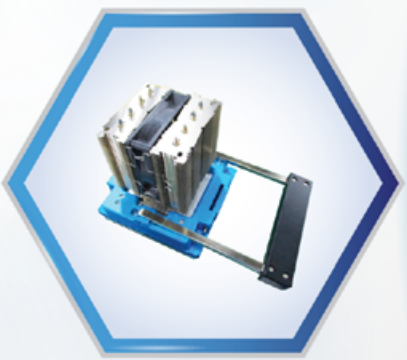


Hand Socket Lid

Heatsink
<100W

Heatpipe
100W - 1000W

Liquid Cooling
300W - 1500W



BROCHURE

A 55GHz octal-site probe card for 5G mmWave devices

By Peter Cockburn [Cohu, Inc.]

To support higher bandwidth 5G connections, suppliers of high-end smartphones are starting to integrate compact antenna modules that support multi-channel, beam-forming mmWave interfaces at frequencies of 24GHz – 48GHz. These rely on complex silicon implemented in fine-pitch, wafer-level packages that need to be comprehensively tested before integration as part of a known good die (KGD) strategy. This in turn puts new challenges on the suppliers of test equipment and test interfaces, namely:

- Automatic test equipment (ATE) systems need to offer cost-effective, mmWave test options with high parallelism; and
- Test interfaces – contactors for package test and probe cards for test of bare die or wafer-level packages (WLPs) – must support the fine pitches and high signal frequencies used.

At SWTest 2021, J. Mroczkowski described a probe card for testing wafer-level chip-scale package (WLCSP) mmWave devices that supported high-bandwidth radio-frequency (RF) connectivity for both direct and loopback testing [1]. This is implemented using a direct-attach printed circuit board (PCB) technology that supports a 150µm-pitch fan out. This method allows a large amount of test functionality to be included in an 8-site layout and minimizes the transitions for mmWave signals that are routed directly from the device under test (DUT) area across the PCB surface via coplanar waveguide (CPW) structures to RF cable connectors.

Each site requires the use of over 600 cViper spring probes at 150µm pitch and the probe head design allows for the attachment of a manual test option that can be used across all eight sites simultaneously to test singulated bumped die (see **Figures 1** and **2**).

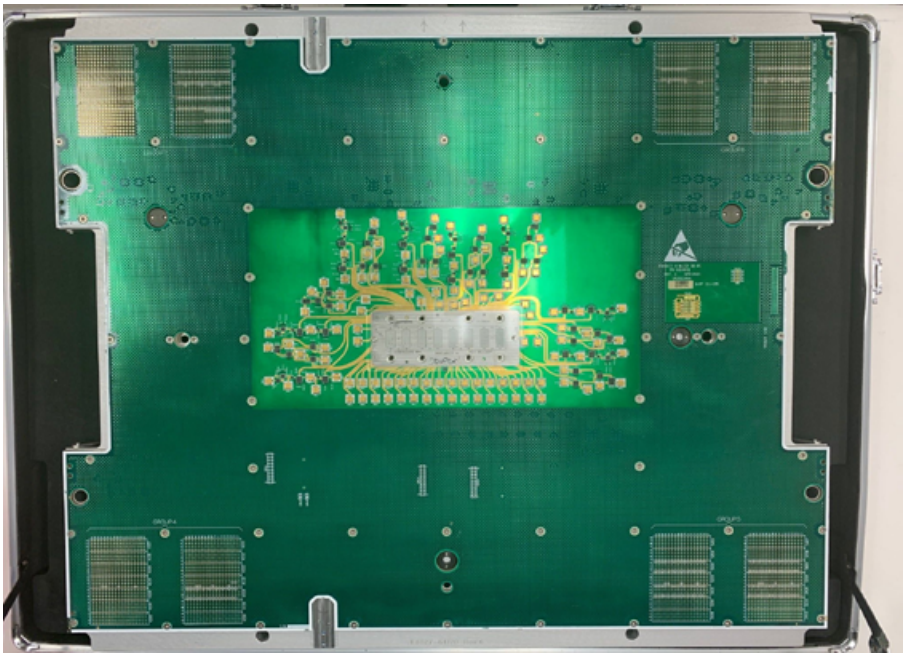


Figure 1: Probe card front.

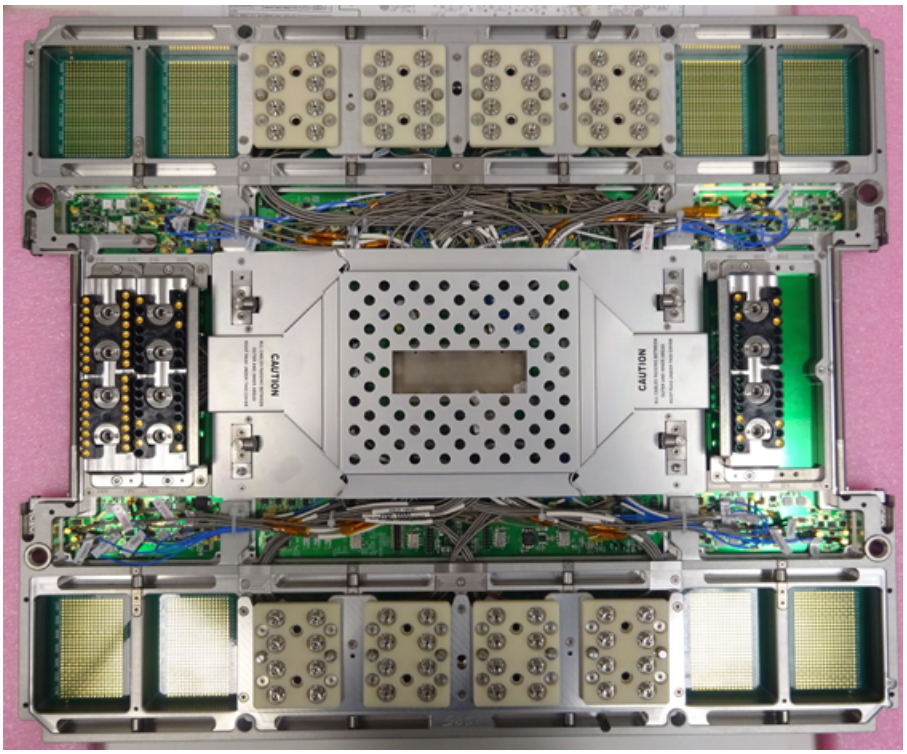


Figure 2: Probe card back.

Since the original deployment of this probe card last year, we have evolved the design in response to changing customer requirements and to improve functionality in several key areas:

- The 55GHz mid-band (MB) RF signals required a change of the matching impedance from 50Ω to 35Ω;
- The alignment mechanism between the probe head and probe card PCB was improved; and
- A feasibility study for implementing denser multi-site test patterns was completed.

35Ω impedance matching

In the original probe card design, all the RF signals required a matching impedance of 50Ω in the interface hardware to achieve the best performance. This required tuning of the cross section of the probe head body and the 150µm pitch cViper spring probes to achieve a 50Ω impedance match. The PCB layout was also simulated and optimized to match the probe head impedance and provide a 50Ω signal path from the DUT ball to tester pin.

In a new customer DUT design, the MB channels operating at up to 55GHz now have an impedance of 35Ω and this required several parts of the interface hardware to be redesigned as follows:

- A new probe card PCB layout is required, with trace geometries for the MB signals matched to 35Ω in the DUT launch area;
- The probe head cross section needs to continue to support 50Ω impedance matching on LB and other RF signals, but also now requires 35Ω impedance matching for the MB signals; and
- As the test equipment used will still be 50Ω, a 35Ω to 50Ω impedance transformer is required, where the signals on the PCB transition from the DUT launch area to RF cable connectors.

Without these changes, test results renormalized to 35Ω would have degraded return loss performance and no longer meet the goal of better than -10dB up to 55GHz.

To evaluate the feasibility of changing the tightly-packed DUT signal layout, a simpler coupon board design was started, which implemented new 35Ω trace geometries for both direct connection paths from DUT to tester instrumentation on the surface layer of the PCB and loopback paths on lower layers of the PCB. The wider trace geometry for 35Ω required the position of several other traces to be adjusted, but overall, the changes could be accommodated without affecting the DUT spacing.

However, if only the PCB traces are changed to 35Ω, this will result in multiple impedance discontinuities as the signal transitions from a 35Ω DUT to a 50Ω probe, then to a 35Ω PCB and finally, back to a 50Ω RF cable connection. This can be simulated and displayed using a time domain reflectometry (TDR) plot (see Figure 3). The resulting return loss performance is even worse than the simple "renormalized" case, so additional design changes are required in the other elements of the signal path.

The probe head and cViper probe cross section also need to match the 35Ω impedance of the DUT MB signals, but the challenge here is to maintain 50Ω impedance for all the other signals in the DUT layout. One approach considered was to reduce the spacing between the 150µm-pitch cViper signal probes and adjacent ground probes by implementing a wider signal probe. This was not possible, as the DUT layout for the

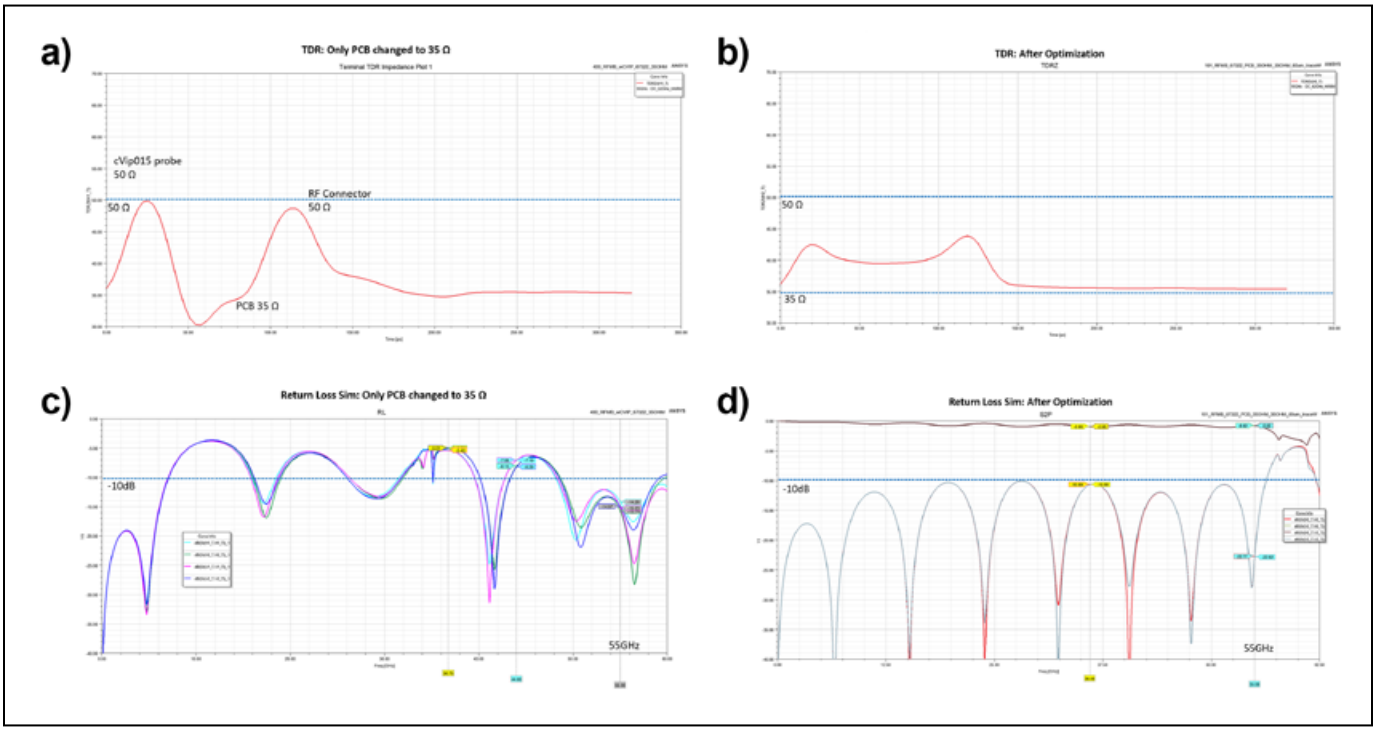


Figure 3: TDR plots a) before and b) after optimization; and RL plots c) before and d) after optimization.

MB signals included some tight signal-ground spacing that would not allow for a wider signal probe. Instead, a wider ground probe was designed that could be used in selected ground locations to reduce the overall impedance of the MB cross section.

A new ground probe was designed and built to match several key parameters of the original signal probe, including test height, spring force at test height and crown tip profile where the probe touches the DUT ball (Figure 4). The new probe is considerably wider to reduce overall impedance in the new cross section, and when tested for contact resistance (Cres) performance over time, it showed stable results out to 1M cycles.

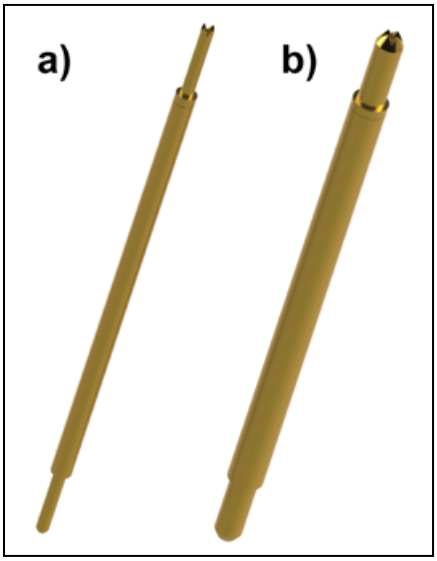


Figure 4: a) A standard cViper015, and b) the new GND probe.

The new probe head cross section in the simulation model showed that return loss is now in the expected range of better than -10dB. As the probe cross-section impedance was not a perfect match to 35Ω, the PCB trace geometry was adjusted to get a closer overall match.

As mentioned earlier, the direct connection RF signals are routed to test equipment via a coaxial connector and RF cable, which are all matched for 50Ω. This requires an impedance transformer to be implemented in the PCB traces that connect from the DUT launch area to the RF connector. The matching of a 35Ω DUT environment to a 50Ω test environment has now been implemented on a cViper probe stack-up and PCB layout and measured after assembly to verify that the targeted performance is being achieved.

Probe head to probe card alignment improvements

When fitting probe heads to probe cards for such fine-pitch applications, there is no margin for error if good alignment and connectivity are to be achieved across all sites. Customers expect to be able to swap out probe heads locally, without requiring a time-consuming realignment process.

The initial probe head and PCB design have evolved in several ways to improve the alignment mechanism. Monte Carlo analysis techniques were used to identify the features of the design that had the greatest impact on

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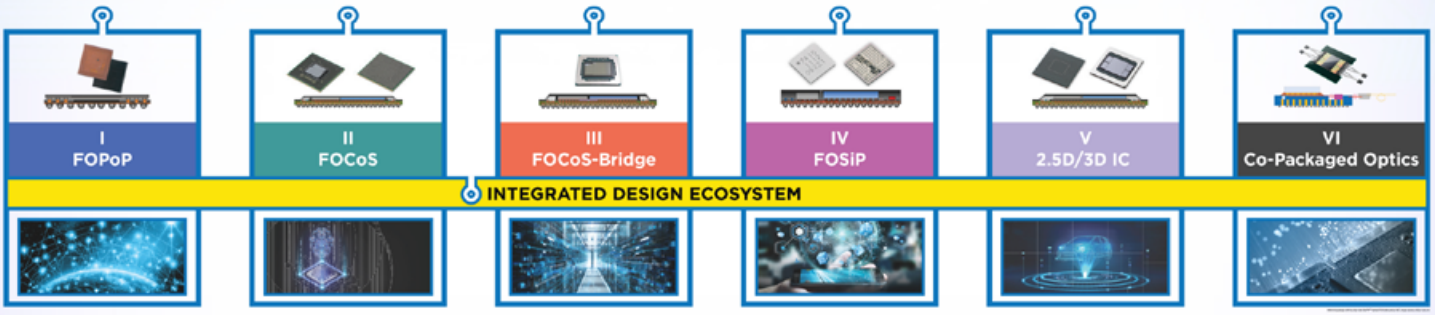

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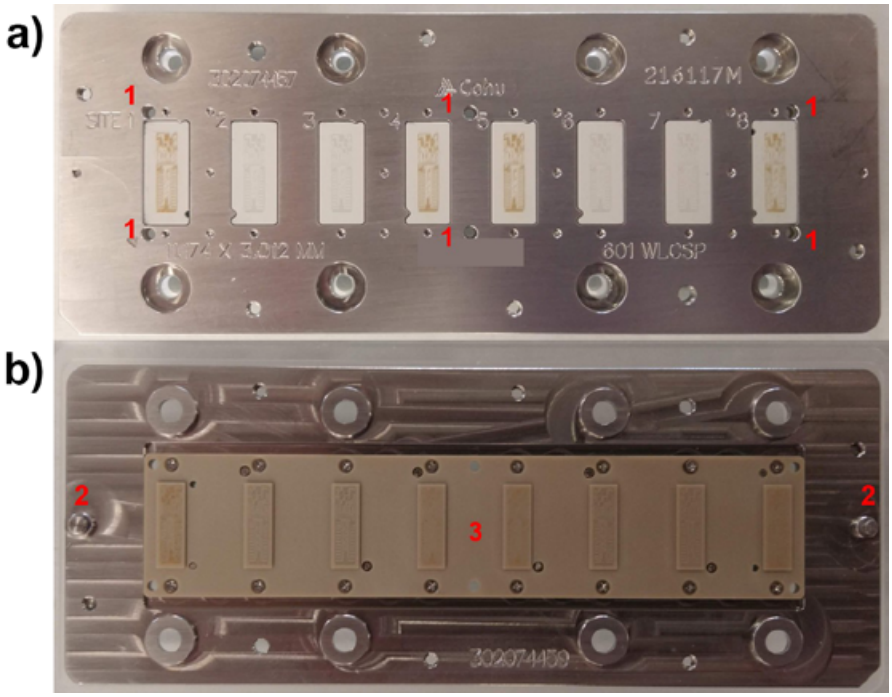

Figure 5: a) (top) Front and b) (bottom) back of the new probe head design.

alignment accuracy. Differences in the new design include a change to the size and position of the alignment pins to make them more robust and accurate. Fiducial features are added on the PCB that provide a high-accuracy reference for drilling alignment holes and a visual reference that can be used to check alignment of the probe head. Some items in the probe head assembly were simplified to reduce stack-up errors across the multi-site layout.

Figure 5 shows the front and back of the new probe head design with the new design features identified in red: 1) Six holes to align with PCB fiducials; 2) More robust and accurate alignment pins; and 3) A single-piece probe retainer plate (PRP). Tighter machining tolerances are also included in the new design, where this improves the alignment accuracy.

To validate the new alignment mechanisms, a simplified version of the probe card PCB was designed and built that duplicates the high-density, fine-pitch DUT layout across eight sites, but fans this out using simpler, low-speed traces to electrical test points, as well as to the normal tester pogo pads. This allows a DUT-pad to test point validation to be performed on the bare PCB, using a flying probe tester (Figure 6), or a DUT probe to tester pad validation to be performed on a complete probe head + PCB assembly, using a probe card analyzer. A design of experiments (DOE) has been defined to assess the variability of the manufacturing processes, using several copies of the probe heads and PCBs, which are manufactured at different times and will be assembled and tested in different combinations.

More efficient multi-site layout

For high-volume production test, a more compact multi-site layout is preferred, as it will typically result in fewer skipped die when testing near the edge of the wafer, thereby translating into higher overall touchdown efficiency, higher throughput, and therefore, a lower cost of test (COT). The original test site layout implemented 8 sites in a 1x8 single row, with three skipped die between each site. This was required to accommodate the large amount of RF test circuitry routed out from each site.

A new design has been proposed that implements the 1x8 layout with only one skipped die between sites, resulting in a 48% reduction in the length of the multi-site test layout (Figure 7). The first step was to confirm that a new PCB layout (Figure 8) could be defined that supported the required level of per-site test functionality within the tighter space restrictions. A new test schematic was defined by the customer that allowed for the removal of some trace structures. Specific RF insertion loss goals were also defined that would influence the overall layout requirements. A new probe head layout was defined and a bowing study performed to confirm that planarity could be maintained across the denser multi-site pattern. After the constraints of the circuit design and probe head were defined, the layout feasibility study could be completed to confirm that the new, denser multi-site pattern was possible.

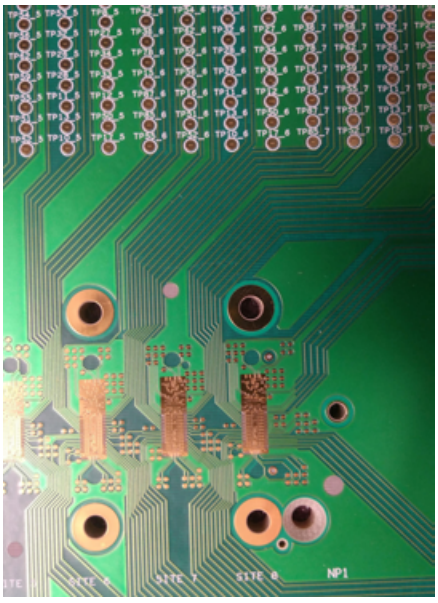

Figure 6: Test PCB layout.

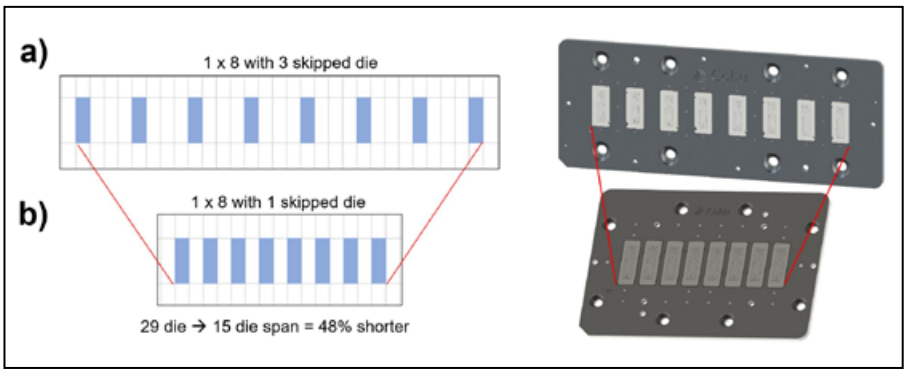

Figure 7: a) (top) Before and b) (bottom) after probe head layouts.

The bowing analysis used ANSYS simulation tools to model the stresses created by the 8 x 600 probes in the probe head design. The design uses a one-piece ceramic body to house the probes, surrounded by a stainless-steel frame, but even with this, the initial analysis indicated that maximum deformation in the center of the test area would exceed a target limit of 50µm. To reduce bowing, the attachment points for the probe head were moved closer to the DUT area (Figure 9). This creates additional challenges for the PCB routing, so it is important to define the two designs in parallel to avoid surprises later! The stainless-steel frame was also extended between each site area and with these changes, the bowing within the DUT area was reduced to less than the 50µm threshold.

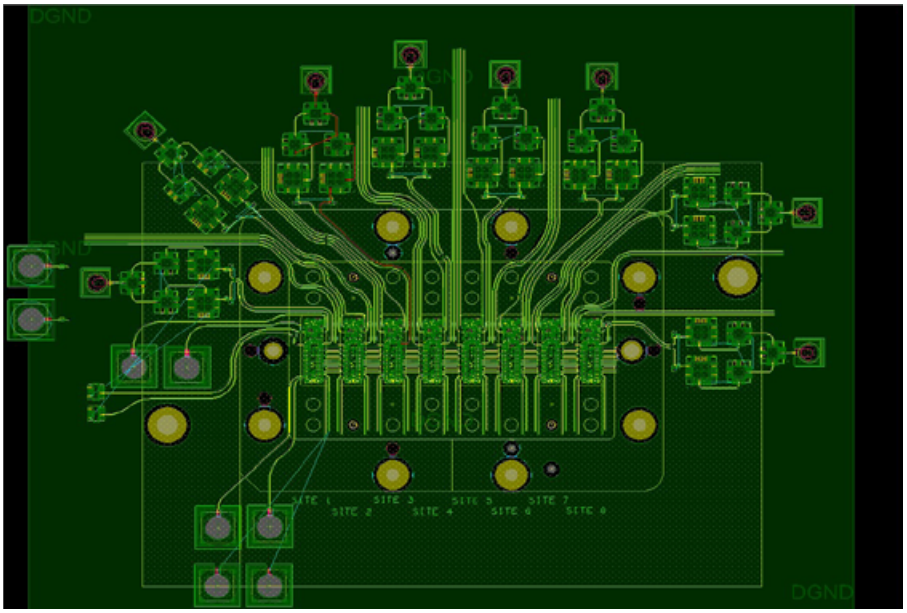

Figure 8: New PCB layout.

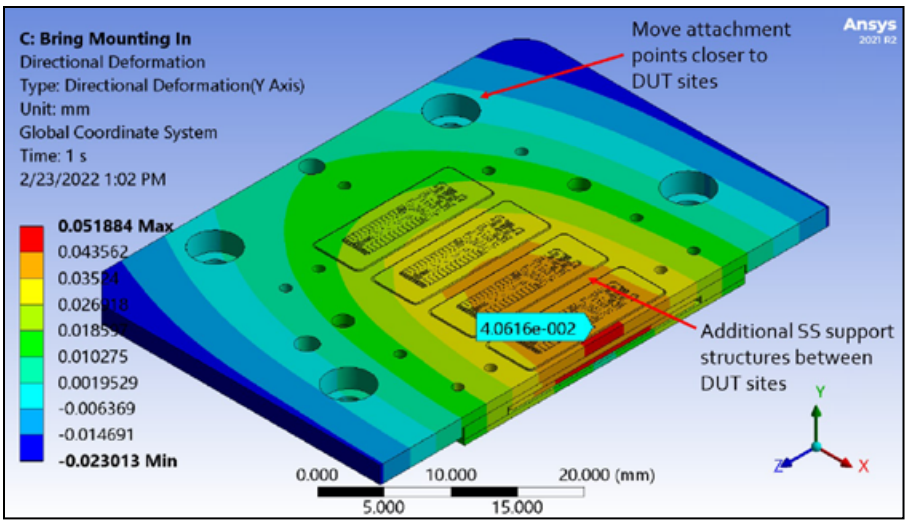

Figure 9: Bowing study results.

Initial feasibility studies for the denser 8-site layout confirm it is possible to include all the required RF functionality and manage the increased bowing stresses on the probe head. Follow-on work can include a complete routing and fabrication of the new design, but the possibility to create a 16-site pattern is also being explored. The final design would need to accommodate all the signal routing requirements and respect the layout restrictions created by the probe head attachment and alignment features. The RF cabling used is being reviewed, to see if shorter lengths will be usable in the new layout to help minimize insertion loss contribution.

Summary

A complex probe card design has been deployed at multiple customer locations and successfully used for validation and test of new mmWave transducers. Because nothing stands still in our technology-driven world, the design has evolved in several areas to meet new customer requirements, improve usability and reduce COT.

Multiple design changes were implemented to match 35Ω impedance of the mmWave MB signals and improve alignment of the probe head and probe card PCB. Options to increase the density of the multi-site test pattern have been validated for feasibility and development has been started.

Acknowledgements

The author thanks the project teams across Cohu and Synergie-CAD for their extensive contributions to this project. This article is based on a presentation originally given at SWTest 2022.

Reference

1. J. Mroczkowski, “55GHz octal-site wafer test probe card for 5G mmWave devices,” SWTest, 2021.

Biography

Peter Cockburn is a Senior Product Marketing Manager at Cohu, Inc., Verwood, UK. He received a BSc from the U. of Southampton in UK. He has over 30 years of experience in the ATE industry, including software development, product marketing and program management. Email: peter.cockburn@cohu.com

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Advancing 5G communications using LTCCs

By Andy Kao [DuPont]

In 5G communication, millimeter wave (mmWave) radio frequencies are used to achieve ultra-high speed, large capacity, and ultra-low latency data transfers. However, mmWave transmissions can't penetrate buildings. To optimize 5G, more and smaller cell antennas are required. Use of low-temperature co-fired ceramic (LTCC) conductive pastes and tapes in radio frequency components (such as those used in band bass filters (BPF), substrates and antenna-in-package (AiP) for radio frequency front-end modules [RF FEM]) can help expand access to 5G mmWave bandwidth devices. Components made with LTCC materials have high reliability, excellent electrical performance, good thermal conductivity, and outstanding environmental resistance. In addition, the physical properties of LTCC materials enable a higher degree of design freedom compared to printed circuit boards because they allow for stacking up to 80 layers while still providing dielectric constant stability and low insertion loss. They have also been proven to enable smooth functioning across a wide frequency range – including high-frequency applications – in challenging environments.

LTCC uses and properties

LTCC material systems combine the benefits of multi-layer ceramic and thick-film technologies used in high-frequency, microwave, and mmWave electronic applications. Most often, these systems are used for high-reliability circuit boards. Recent developments have led to the use of LTCC materials in AiP for RF FEMs.

In the unfired green state, each layer of dielectric can be via punched, filled, and screen-printed with conductor and resistor traces (Figure 1). Up to 80 layers can be stacked together. Compared to traditional printed circuit boards that are limited to a few layers (usually 20 or fewer), LTCC materials allow for the design of more highly integrated circuitry. Plus, these materials are key to achieving high-performance efficiency at low levels of power consumption.

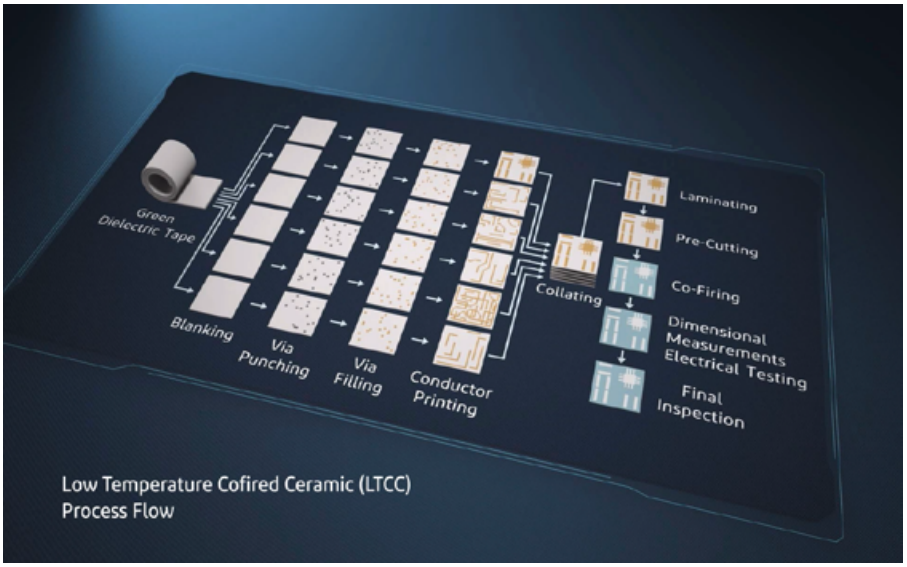


Figure 1: Low-temperature co-fired ceramic (LTCC) process flow.

After layers are stacked and laminated, they are co-fired at 850°C. This is much lower than the >1500°C used in conventional high-temperature co-fired ceramic (HTCC) processing. Circuits made with LTCC materials can also withstand post-firing of thick film, plating, soldering, or brazing to make a fully functional package (Figure 2).

LTCC materials combine the positive attributes of a thick film on a ceramic

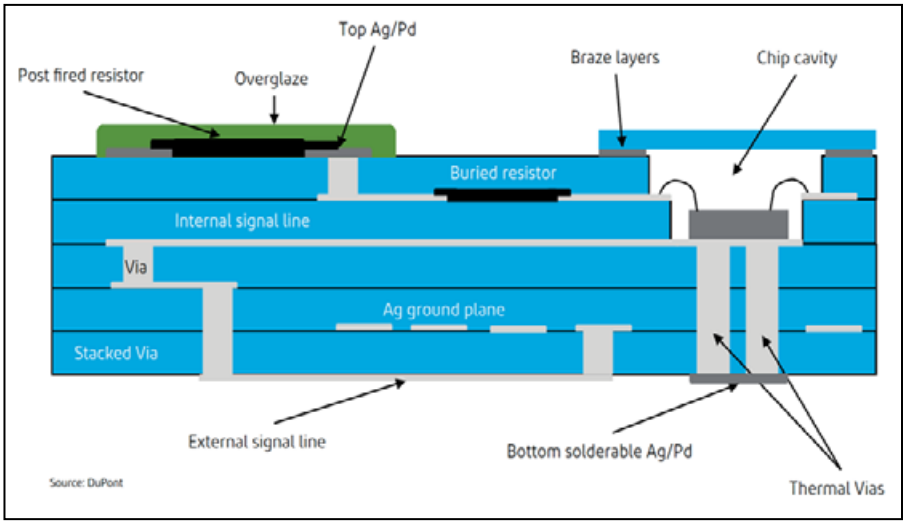
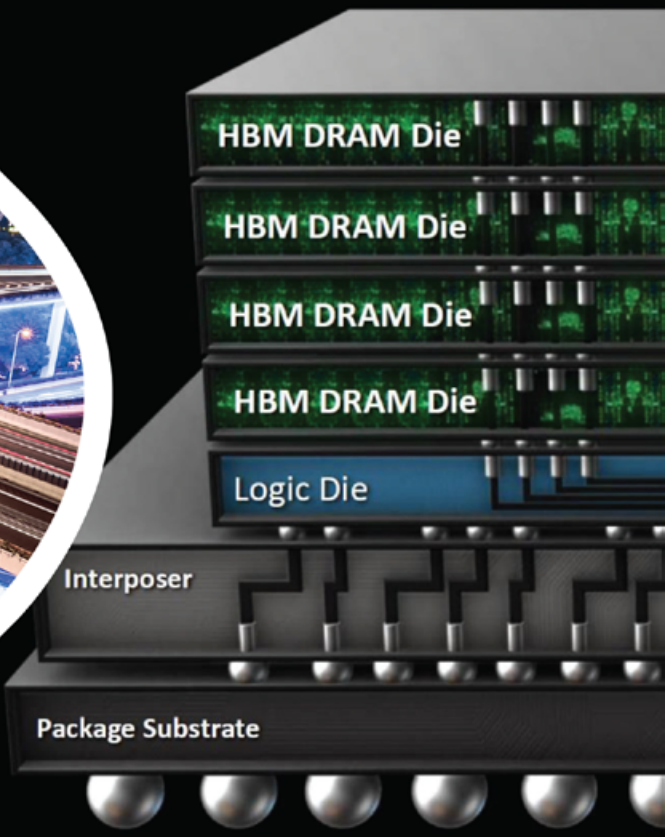


Figure 2: LTCC material systems allow package design flexibility with up to 80 layers for integrating passive components, e.g., capacitors and resistors, as well as the ability to create cavities, and physical properties that withstand post-firing.



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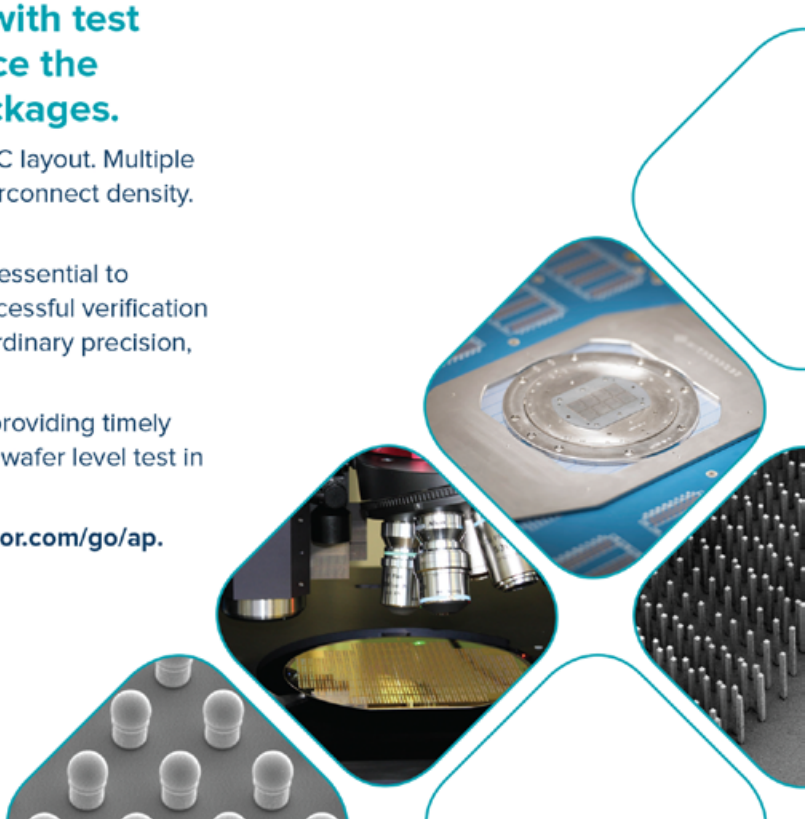

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Coefficient of Thermal Expansion Comparison			
	Printed Circuit Board	Semiconductor	LTCC materials
ppm/K	13-17	4-6.5	5.3

Table 1: CTE of LTCC materials is close to the CTE of a semiconductor material.

Thermal Conductivity Comparison of Various Substrate Materials							
	DuPont™ GreenTape™	General LTCC	LCP	PTFE + Ceramic	FR4	PTFE	PI
W/m-K	4.6	3.3	3	0.5	0.25	0.25	0.12

Table 2: Thermal conductivity comparison among different types of substrates.

substrate and HTCC. Like thick film, LTCC materials can be used with high-conductivity metals (e.g., Au and Ag), have a low dielectric constant (Dk), can be used to print resistors, and are processed at a relatively low temperature. Like HTCC technology, LTCC materials allow high resolution for printed conductors, use a single firing, provide good dielectric thickness control, and multiple layers.

LTCC is inherently hermetic and therefore immune to moisture absorption. The coefficient of thermal expansion (CTE) of certain LTCC materials are much lower than the CTE of printed circuit boards. This allows for a close match to integrated circuit (IC) chips (Table 1). Compared to general LTCC materials and other circuit board materials, DuPont™ MCM GreenTape™ offers better thermal conductivity (Table 2).

With induced low-dissipation factor (Df) degradation, DuPont™ GreenTape™ dielectric properties are very stable with respect to temperature (Figure 3) because of a low CTE, and polarization modes that are not strongly influenced

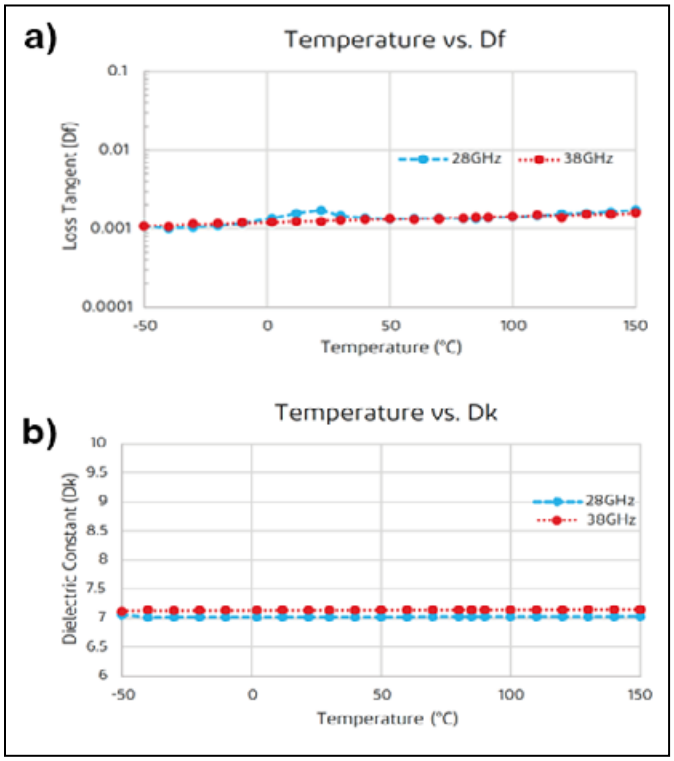

Figure 3: DuPont™ GreenTape™ maintains: a) a low dissipation factor (Df), and b) a low dielectric constant (Dk) in extreme cold and extreme heat.

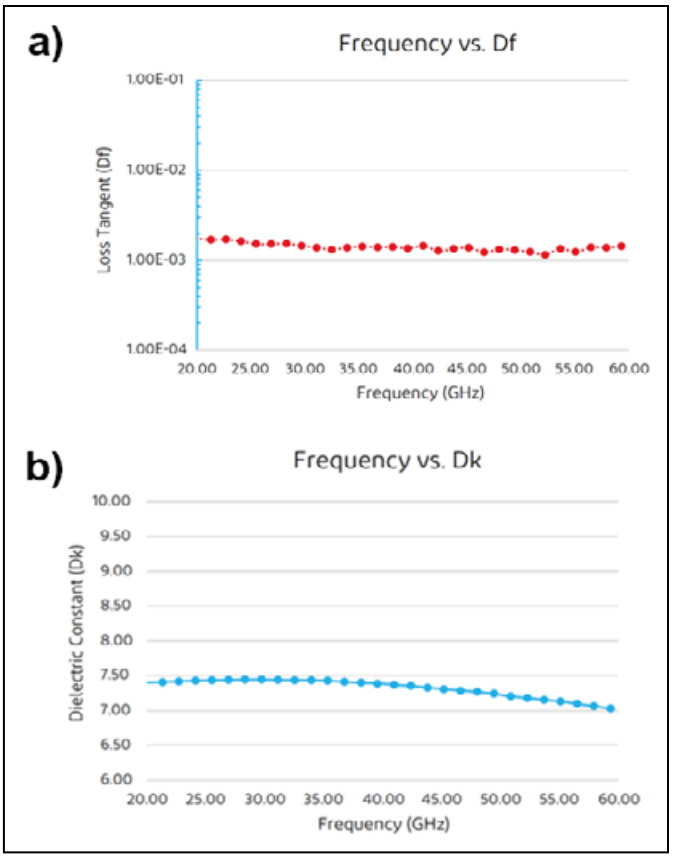

Figure 4: DuPont™ GreenTape™ provides: a) a low loss tangent (Df), and b) a stable dielectric constant (Dk) over a range of mmWave frequencies.

by ambient temperatures. At the same time, the tape has a very low loss tangent of transmissions over mmWave frequencies (Figure 4). For the reasons outlined above, we chose this tape as a test material for AiP applications.

AiP prototyping, testing, and validation

Our Microcircuit and Component Materials team collaborated with the Industrial Technology Research Institute (ITRI) of Taiwan to design and test mmWave AiP prototypes made with DuPont™ GreenTape™. After firing, test results indicate that the electric properties of LTCC substrates perfectly match the design, with an attainable bandwidth of 2GHz and higher as shown in Figure 5. After chips and passive components were packaged onto the substrates (Figure 6), further testing in an anechoic room was used to validate beam-forming properties.

Once installed in the system (Figure 7), the antenna module underwent mmWave signal transmission field testing. Because of its low-loss features, we could validate the quality of signal transmission by using error vector magnitude (EVM) testing (Figure 8). We observed the clean image and audio at the receiving end when a high-resolution video file is transmitted from one device to another (Figure 9). This fully demonstrates the feasibility of using our tape system in AiPs for mmWave applications.

Future development

Using highly-integrated circuitry and exceptionally stable and reliable low-loss LTCC materials in the antennae arrays (or multiple antennae in one or more arrays) and RF

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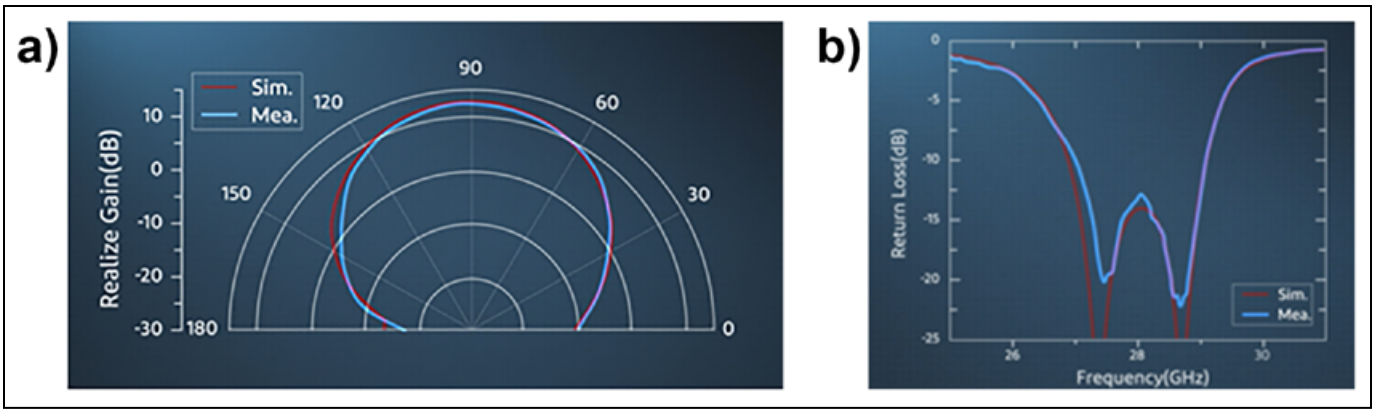

Figure 5: Measurement results a) realized gain, and b) return loss, match simulation results after the LTCC substrate was fired.

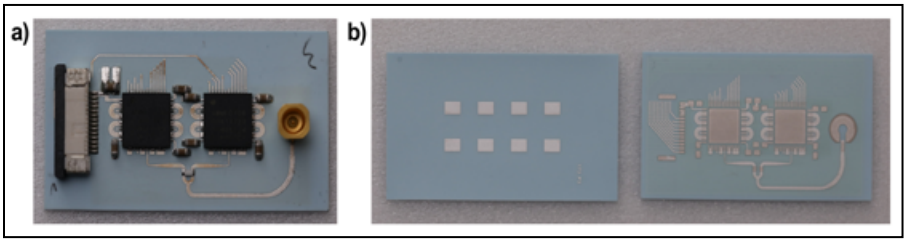

Figure 6: a) (left) Surface-mounted IC chips, and b) fired LTCC substrate.

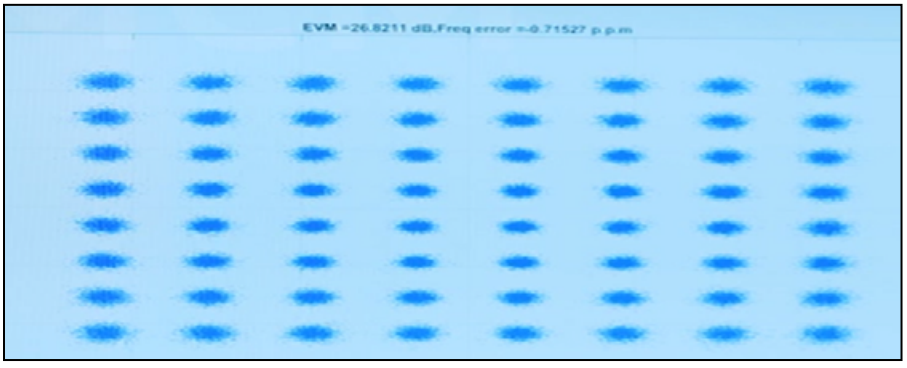

Figure 8: EVM testing result.

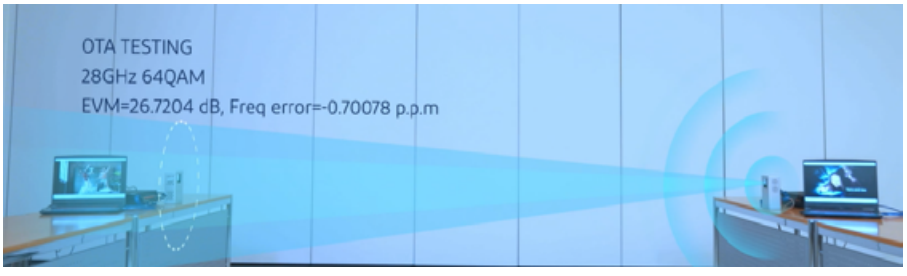

Figure 9: Signal testing showed that antenna prototypes made with DuPont™ GreenTape™ have low loss and provide clean image and audio transmission of high-resolution video files.

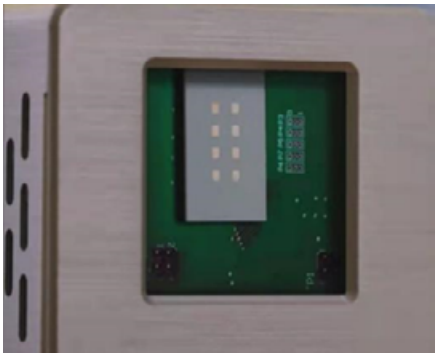

Figure 7: A LTCC AiP module installed into a device.

FEM are key to achieving high 5G performance efficiency at low levels of power consumption. The outcome of our LTCC testing—showing its ability to maintain good thermal stability and heat performance while significantly reducing insertion loss—opens the door to developing new AiP substrates in which their size is reduced along with signal loss.

Summary

LTCC materials deliver both superior environmental tolerance and a high level of design freedom in high-frequency applications. These materials could play an important role in advancing instant communication for autonomous vehicles that talk to each other, as well as for applications for 5G mmWave band communications, military operations, remote surgery, robotics, and more.

Biography

Andy Kao is a Global Telecom Segment Leader at DuPont Microcircuit and Component Materials in Taiwan where he develops new solutions for 5G and high-frequency applications. He received a Master's degree in Material Science from National Taiwan U. Email: Andy.Kao@dupont.com

The American Industrial Compact Consortium seeks to spark innovation and investment

By Brian Long [American Industrial Compact Consortium]

The opinions expressed in this essay are those of the author and not Chip Scale Review.

The American Industrial Compact (AIC) Consortium was announced on July 4, 2019; its purpose is to address the shortfalls in the behavior of American industry toward the communities in which they operate, toward their workforce, and to the nation as a whole. The impetus for forming the AIC was the belief that captains of our flagship industries must not only raise their sails and set course based on achieving purpose and profit, but also accept the responsibility to these communities that comes with their endeavors. This revises Milton Friedman's notion that only shareholders count. Our nation's history offers many lessons from past challenges that can serve as object lessons to enable industry and the private sector to engage responsibly. Interestingly, in October, 2019, the Business Round Table issued its own recommendations to its members calling for greater attention to the needs of the communities in which their member companies operate, and to the interests of workers.

For decades, American policies guaranteed U.S. industries free trade—not just within our nation, but also globally. From that experience, we see how contrasting narratives concerning profits versus other national interests has eroded other national goals and needs, particularly regarding technological primacy, economic equity across all regions of the nation, and resiliency in times of crisis—something that the COVID pandemic demonstrated we had forsaken in the extreme. The use of COVID-induced manufacturing slowdowns is spurring countries to once again make resiliency a priority, spurring on new domestic investments in industrial capacity. The CHIPS for America Act is the first Industrial Policy Act enacted by Congress in 44-years, and may rescue the remaining U.S. companies in the microelectronics arena.

The CHIPS for America Act became law as a part of the 2021 National Defense Authorization Act on January 1, 2021. It is the first Industrial Policy Act enacted by Congress in 44 years. As such, it seeks to strengthen the U.S. industrial base for microelectronics by providing $52.6B in incentives over five-years to industry and academia to expand existing manufacturing capacity, build entirely new capacity, fund the acquisition for new process equipment, and train new workers for fabs as well as in the packaging of microchips, the assembly and testing of devices, and/or research and development. It also puts up guard rails to prevent the further transfer of technology abroad.

The bulk of the funding – $39B – goes toward new facilities, equipment and workforce development activities. Twelve billion goes toward research and development, with the funding split $10B for commercial R&D, and $2B for defense R&D. The remainder of the funds, $1.6B, are earmarked for international collaboration activities involving the U.S. and those allied nations whose export controls are identical to those of the United States. The Act focuses investments on heartland states, and workforce development involving economically disadvantaged individuals (defined as persons considered minorities and/or persons from rural communities whose income [for a family of four] is below the national mean income level).

As you read this article, you must ask yourself, how does this apply to me? Well, from my perspective, microelectronics is the centerpiece of absolutely everything in our lives. It is the central nervous system of our country driving every part of our economy, and ensuring our national defense. Microelectronics is the hub on which every spoke on the wheel of industry revolves, and innovation has been the grease that has lubricated the transformation of our nation from an industrial power to an information power.

To meet the challenges we face with respect to the future of innovation and help achieve the industry goals defined in the proposed legislation, we will need to incorporate new workforce development initiatives that put skills into hands, and those hands into this industry. This means public/private partnerships and elevating our youth into the spotlight. To this end, AIC is engaged with technical trade schools across the country; we are putting the word out on the street, and we intend to use funding from the Act to walk these institutions into the future. There are scores of young people in our nation that are "do it yourself" minded—they procure piece parts and software online to create their own innovations, similar to what we used to do with components from Radio Shack. As the Chairman of the American Industrial Compact, I want to foster this entrepreneurial spirit. I remember my first Radio Shack hobby kit — a radio. I remember the crackle of the speaker powered by a nine-volt battery receiving a radio signal; and I remember the elation I felt from my accomplishment. That same spark of enthusiasm is what I hope we can engender in the young people of today. We have to make the modern equivalent of the "Radio Shack" experience cool again, just as our fathers' generation experienced the space race, and missions to the Moon. We have to put our young "geeks" into the spotlight and set new examples for others to follow. This means that we must also make it exciting again to advance technology.

To meet the above objectives, we must address the issue that most resonates with our nation's youth: climate change. Today, use of microelectronics comprises the fastest growing demand for electricity. The challenge of reducing or eliminating energy demand from this sector, be it from data centers, automobiles, or hand-held devices, is within our reach, but will require that the producers of microelectronic components and systems shift to newer materials and designs in their products. Here is where AIC and the Business Round Table should work together.

The AIC began with a few dozen corporate leaders and now comprises numerous educational and government leaders eager to address the goals I outlined above. The CHIPS for America Act was drafted in the same spirit as the Eisenhower Plan, The Marshal Plan, and the post-Civil War reconstruction effort in the late 1890s. The world has enjoyed free trade for decades, and as countries form new global alignments, there will be occasions for other countries to adopt similar initiatives. I work closely every day with those addressing the legislative outcomes and remain hopeful that more small businesses and investors will come forward to take part in this new initiative.

As we move forward, we must do so with a focus and determination to meet the challenges with more understanding and patience. Eager, yet naive new investors will be coming to the table who do not understand the semiconductor industry. This in no way is their fault, but rather is an opportunity for you as the technology provider to educate your prospects in an easy to understand manner how your capability serves industry needs. The CHIPS for America Act speaks for what it is in form and function—it is intended to bring semiconductor manufacturing back to American shores and close the gap on reliance on foreign suppliers. These efforts will provide for a stable economy and enhanced national security. The language is there in simple form for all to read. The motivation is equally as simple and seen every day in the news. If you are not at this point learning from what you are seeing in your supply chains, then you are simply not paying attention. For additional information, please visit www.Aicamerica.com.

Biography

Brian Long is Chairman and Founder of The American Industrial Compact Consortium, Hazard, Kentucky. He is an American industrialist, designer and inventor with a deep history of providing rapid solutions for various urgent needs of both government and public sectors. He has designed life-saving capabilities that resulted in multi-billion dollar market spaces being created and saved untold numbers of lives. Email Brian_Long@mail.com

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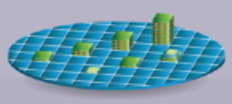

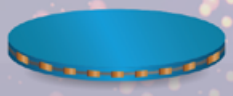

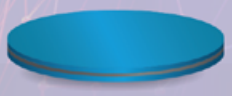

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Improving semiconductor packaging with advanced silicones

By Jayden Cho, Roderick Chen [Dow]

Designers who are familiar with epoxies for chip-level packaging have new options for wafer-level packaging and even panel-level packaging. As 8-inch and 12-inch wafers become increasingly thinner to support new product designs, the challenge of applying epoxies in thicknesses under 10µm requires forward-thinking solutions. Advanced silicones can provide very thin, very uniform coatings for encapsulation along with effective stress management for reduced wafer warpage. Whether alone, or in combination with epoxies to produce novel hybrid materials, advanced silicones are driving packaging innovation.

Epoxies are widely used for chip encapsulation because they combine strong and reliable bonds with low shrinkage and excellent moisture and chemical resistance. Epoxy die attach film (DAF) can be difficult to apply in thicknesses less than 10µm, however, and these organic materials are relatively hard with a high modulus—a measure of resistance to elastic deformation when stress is applied. Because they are less elastic than silicones, epoxies are more prone to cracking when an electronic device encounters physical shock, such as when a smartphone is dropped. The vibrations that industrial and automotive electronics encounter also produce stresses, but the use of thinner wafers in various types of electronics pose special concerns. If stresses on the front and back of a wafer are imbalanced, warpage can break the dies.

Wafer warping can be caused by the formation of intrinsic stresses during thin-film deposition, but mismatches in the coefficients of thermal expansion (CTE) can also cause unwanted dimensional changes. The CTE, a material property that indicates the extent to which a material expands with heat, differs by material type – and today's electronic devices use many different types of materials. Examples include plastic, ceramic or glass for the package; gold or copper for the bonding wires and interconnects; and epoxy, polyimide or phenolic for printed circuit boards (PCBs), which also contain metal heat sinks. Because each of these materials expands and contracts at a different rate, stresses are imparted that can cause fracture. Conversely, advanced silicones are stress-relieving and can help mitigate wafer warpage caused by CTE mismatches.

Chip designers also need to consider the effects of thermal shock, a mechanical load caused by a rapid change in temperature, especially in packages that undergo rapid heating and cooling, such as for electric vehicle (EV) power electronics and 5G communications systems. With 5G devices, resistance to high temperatures is required because there are more heat-generating components packed into very small spaces, such as in smartwatches, or both small and slim spaces, such as in ultra-thin smartphones. Flexible displays can be large, and these devices may be subject to repeated folding and bending along with the high temperatures associated with 5G components. Compared to epoxies, silicones can resist those high levels of heat while withstanding a wide range of temperatures and stresses from CTE mismatches.

Silicone hotmelt solutions

Traditionally, epoxies have offered chip designers advantages in terms of adhesion, hardness and processability. With silicone hotmelt solutions, however, semiconductor manufacturers can achieve excellent adhesion to a variety of substrates while leveraging silicone's fundamental advantages in thermal stability and durability. Compared to liquid silicone, these solid silicone products are easier to handle and cure more quickly for faster processing times and reduced energy costs. Today, chip designers can choose from advanced silicone hotmelts in films, cartridges and tablets. Cured silicone DAF and novel silicone hybrids are also used.

Silicone hotmelt film (SHF) is UV-activated and heat-cured with a thickness between 25µm and 2000µm at room temperature. Products consist of a thin film that is sandwiched between two release liners that are either clear or black in color. Functional fillers can impart thermal or electrical conductivity. When heat is applied, SHF becomes flowable at 90°C and above. After curing, SHF resists the high temperatures associated with today's electronics and provides exceptional stress relaxation. This advanced silicone is designed to simplify package processing and can encapsulate large substrates, even those with uneven surfaces, to a uniform thickness. For cost-effective processing, SHF supports compression molding and vacuum lamination.

The melt viscosity of silicone hotmelt film is a function of temperature. At lower temperatures, SHFs have a higher melt viscosity for less flowability and greater control of bond line thickness (BLT). At higher temperatures, SHFs have lower melt viscosity and are more flowable; however, they offer reduced control of BLT. Flowability, like SHF's gap-filling capabilities, is not just a function of temperature, however. During the compression molding or vacuum lamination processes, pressure and time are also factors. Vacuum lamination is simpler for encapsulating large areas, but compression molding is used to encapsulate chips with flexible, core-less substrates that could easily warp.

Silicone hotmelt films are fabricated as B-stage films, partially-cured products. These advanced silicone products can support both fan-out wafer-level packaging (FOWLP) and fan-out panel-level packaging (FOPLP)—advanced packaging techniques that are designed to meet growing demand for heterogeneous integration in products such as 5G smartphones, data centers, high-performance computing (HPC), artificial intelligence (AI), and Internet of Things (IoT) applications.

FOWLP is an enhanced version of wafer-level packaging (WLP) that packages integrated circuits (ICs) directly on the semiconductor wafer and supports products with smaller footprints and improved thermal and electrical performance. FOPLP can accommodate larger package sizes with finer-pitch chip interconnects on large-format panels for cost reductions. With both FOWLP and FOPLP packages, SHF sheets can encapsulate multiple dies and conform to irregular substrates.

Sometimes, both SHF sheets and cured silicone DAF are used in the same application. For example, SHF may be sandwiched between a die and a non-flat substrate while DAF is sandwiched between two dies of different sizes as die-stacking. Cured silicone DAF (see **Figure 1**) has a three-layer construction with a thin film sandwiched between two release liners and, when applied, a relatively thick bond line (25µm to 300µm) with excellent uniformity. Reliable adhesion and excellent stress decoupling for CTE mismatches are also advantages. In addition, cured silicone DAF eliminates fillet and bleed-out, problems that can interfere with adhesion. To support processing, the product can be diced into small squares with sizes such as 1mm x 1mm.

Silicone hotmelts offer important benefits, but these solid materials are not the only advanced silicones that can address today's semiconductor packaging challenges. Like silicone hot-melt films, silicone hot-melt cartridges (SHC) provide better workability and thermal stability than commercial liquid silicone. Although SHF and SHC are both used for chip encapsulation and over large areas, SHC supports hot dispensing, slit-die coating, and compression molding for processing. SHC can also be used for molded underfill (MUF) encapsulation, filling the narrow gaps under flip-chips and overmolding dies at the same time.

Hot dispensing involves heating the solid contents of a silicone hot-melt cartridge and then dispensing a liquified melt through a syringe. This process fills gaps reliably and supports direct bonding without any

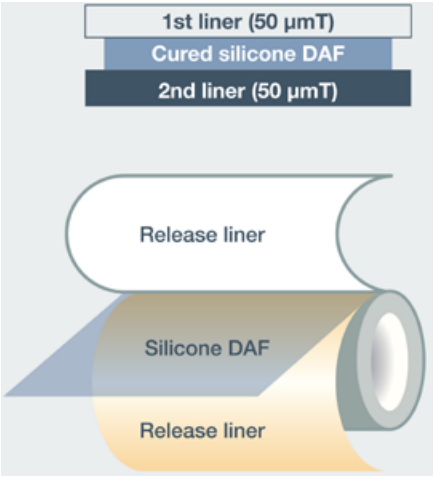

Figure 1: Cured silicone die attached film (DAF).

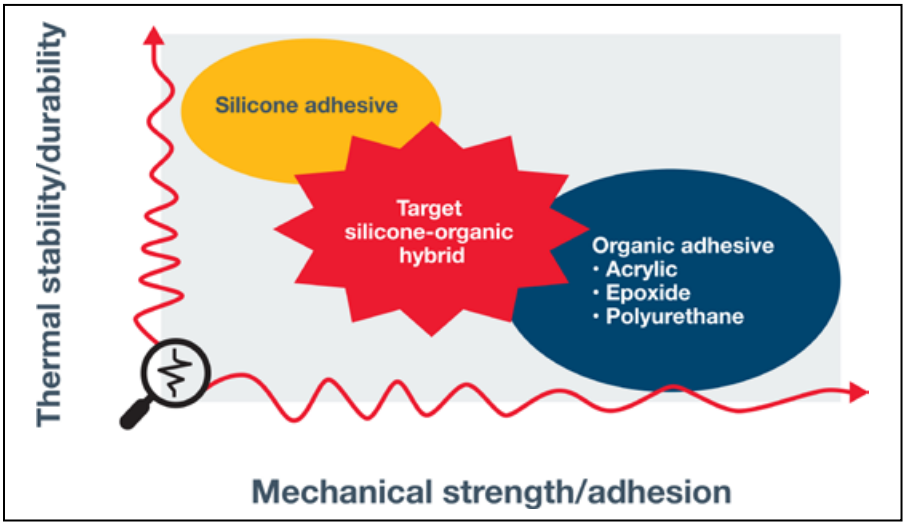

Figure 2: Silicone hybrid options for adhesives, molding and underfill.

substrate size limitations. Although SHC is not flowable at room temperature, heating the material to 100°C supports dispensing for instant bonding and sealing without bleeding. Slit die coating also provides encapsulation across larger surfaces but bonds by lamination instead. Compression molding, the third SHC processing method, encapsulates chips and wafers and is recommended for flat surfaces with a uniform thickness.

Silicone hot-melt tablets (SHT), an advanced silicone alternative to SHF and SHC, are comparable to epoxy molding compounds (EMC) in terms of flowability, moldability, and mechanical strength. SHTs are processed through transfer molding and used in applications such as IoT power modules. Advanced SHT applications include other types of modules that operate at temperatures above 200°C. Silicone hot-melt tablets have a constant CTE up to 250°C and exhibit thermal stability up to this same temperature. Like other advanced silicones, they provide better thermal stability and durability than epoxies.

Through recent developments, novel silicone hybrids are enabling chip designers to choose adhesives, molding and underfill materials with a distinctive balance of properties (**Figure 2**). These innovative materials have a higher modulus than silicones, but with better temperature-related performance than epoxies. Moreover, these new packaging materials are tunable based on application requirements and are available in non-yellowing formulations for displays and optical modules. They cure with ultraviolet (UV) irradiation, heat curing or dual curing that uses both UV lights and thermal ovens.

Summary

Semiconductor manufacturers need packaging materials with better processability, higher-temperature resistance, and improved stress management. They also want to control production costs, promote product reliability and reduce energy consumption, but not at the expense of meeting requirements such as using encapsulants that are very thin and that have a uniform thickness. As chips become thinner, chip designers must also consider challenges posed by putting more electronic content into smaller spaces and supporting the development of flexible electronics, including large-area displays. Recent developments in silicone technology can address these and other packaging challenges, and advanced silicones can complement rather than replace epoxies by providing an effective wafer-level solution.

Biography

Jayden Cho is Global Segment Leader at Dow, Korea. His career spans 18 years in silicones for electronics, acrylic industrial tapes (PSAs) for electronics, and silicones for the building industry. He holds a Bachelor's degree in Polymer Science Engineering from Dankook U., Korea. Email kcho2@dow.com

Roderick Chen is Electronics TS&D Specialist at Dow, Taiwan. His career spans over 13 years working in the chemicals industry for semiconductor packaging applications. He is skilled in materials science, electroplating, soldering technology and silicones.

The 31st Semiconductor Wafer Test (SWTest) Conference

By Jerry Broz [SWTest General Chair, and Advanced Probing Systems Inc]

The Semiconductor Wafer Test (SWTest) Conference was held as a hybrid event June 5–8, 2022, at the Omni La Costa in Carlsbad, CA. The conference was a sold-out, huge success! Now in its 31st year, the conference is an annual event exclusively focused on the complex challenges of wafer-level test and probe technologies. Building off the in-person and virtual conference held in 2021, SWTest 2022 was a two-and-a-half-day hybrid event with more than 525 registered domestic and international attendees. Attending in-person were 480 wafer test professionals, with almost 80 technologists participating via the virtual platform and OnDemand. Benefitting from the relaxation of various COVID travel restrictions, SWTest welcomed approximately 30% of the attendees from the international Asian and European test communities, many of whom had not travelled in more than 18 months. In the grassroots spirit of the conference, attendees were able to have face-to-face discussions with peers, colleagues, and suppliers in a safe environment with ample social distancing.

The conference included two invited, live-streamed visionary keynote presentations that delved into the future needs of test, test development, and the requirements of the advanced packaging roadmap. Starting with the Monday morning plenary session, the first visionary keynote presentation was made by John Yi, who serves as an Engineering Fellow at AMD. Mr. Yi discussed "Architecting Test Solutions for the Next Generation of Compute," and provided deep insights for the general compute roadmap, methods of innovating new test solutions, and the critical solutions that wafer probe test will need going forward. On Tuesday, the second visionary keynote presentation was made by Rebeca Obregon-Jimenez of Amkor Technology. Ms. Obregon-Jimenez focused her presentation on "Advanced Packaging and Test Enabling Our Digital Society." In her presentation, she explored innovations in advanced packaging and test technology that are the key catalysts in our digital society driving 5G, high-performance computing (HPC), Internet of Things (IoT) and automotive applications.

Dr. Jerry Broz, SWTest General Chair, welcomes more than 500 combined on-site and virtual attendees to the sold-out 31st SWTest Conference and Expo that was held at the Omni La Costa in Carlsbad CA, June 5-8, 2022.

The technical program consisted of 9 sessions that included 30 outstanding podium and poster technical presentations addressing the key challenges faced by probe technologists. Monday's session on

John Yi, Engineering Fellow at AMD, made a Visionary Keynote presentation at SWTest 2022 discussing the critical solutions that wafer probe test needs going forward.

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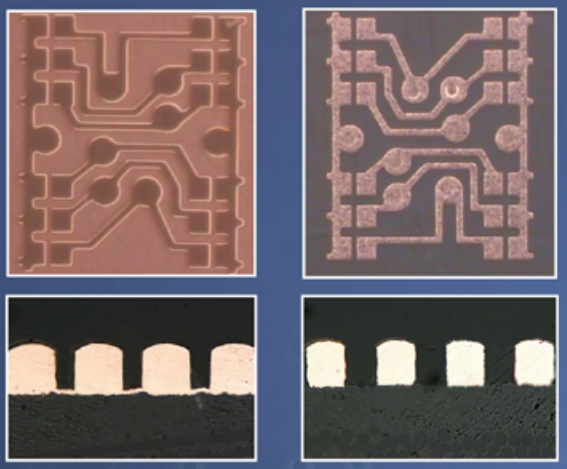

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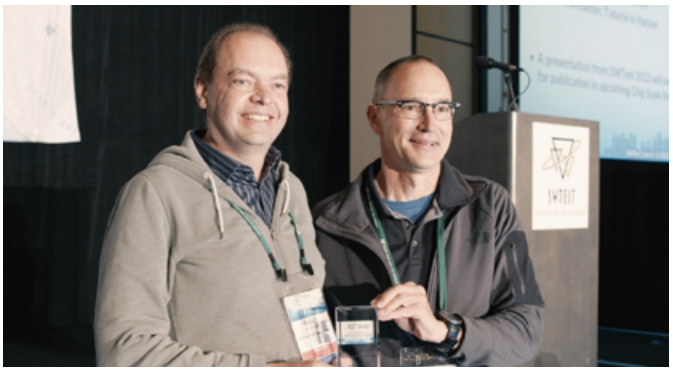
high speed and RF included presentations covering the unique challenges fueling high-speed digital testing and multisite testing for 5GmmWave devices. From this session, the Technical Program Committee awarded the "Best Data Presentation" awards to Daniel Bock, Ph.D. (FormFactor Inc.) for his work on "High Speed Digital: How to Optimize a Probe Card for PAM4 to a Non-50Ω Device," and to Peter Cockburn (Cohu, Inc.), who discussed "55GHz Octal-site Wafer Test Probe Card for 5GmmWave devices."

From Tuesday's session on New Probe Technologies, the "Best Presentation, Tutorial in Nature," was awarded to a hybrid presentation made by Salvatore de Siena (Technoprobe S.p.A. – Italy) and Erwin Verardi and Alberto Pagani, Ph.D. (STMicroelectronics – Italy) who presented on "Copper Pad Probing with Vertical Technologies Featuring Hard Metal Tip: ARIANNA™ Probe Family." From the Pads, Bumps, and Defect session on Wednesday, the "Most Inspirational Presentation" was awarded to Francesco Lorenzelli (imec – KU Leuven, Belgium) who provided key insights on "Shifting Defect Detection in Quantum Chips From Cryogenic to Ambient Temperature." The "People's Choice" was voted on by attendees in real time via the mobile app and was received by David Raschko (FormFactor, Inc.), who discussed the "Advances in Vertical Probing for High-Speed Digital Test at Wafer Sort." From all of the excellent presentations delivered during the conference, the Technical Program Committee was pleased to award the "Best Overall Presentation" to Oliver Nagler, Ph.D. (Infineon Technologies, Germany) for his team's work on "An Advanced Method for Pad Stack Crack Assessment during Probe-Over-Active-Area." *Chip Scale Review*, the SWTest Media Partner, has selected the two Best Data Presentations and the Best Overall Presentation for publication as full articles in upcoming issues.

The SWTest EXPO, which annually attracts key suppliers to the wafer probe industry and support infrastructure, brought together 50 key exhibitors in person and on the virtual platform that play integral roles for the industry. At SWTest, the Expo and the technical program do not compete, so the attendees were easily able to attend both events during the conference and afterwards on the virtual platform. Throughout the schedule, SWTest 2022 attendees had ample time and numerous opportunities for networking and discussions during the long breaks, daily meals, and nightly social and hospitality events. The SWTest Team was excited to continue promotion of the SWTCrew mentor initiative, which is actively connecting women technologists with experienced professionals to support their career development. Additionally, SWTest supported the attendance of four students through the William Mann Student Travel Grant Program that is partially subsidized by the annual fundraising golf tournament.

SWTest 2022 EXPO brought together in-person and virtually 50 key suppliers and service providers that play integral roles for the wafer test industry to have face-to-face discussions and networking with peers, colleagues, and customers.



Dr. Jerry Broz, SWTest General Chair, presents the Best Overall Presentation Award to Dr. Oliver Nagler of Infineon Technologies, Germany, for his team's excellent work that focused on "An Advanced Method for Pad Stack Crack Assessment during Probe-Over-Active-Area."

As the General Chair of this premier conference, I am pleased that our event provides a variety of exciting technical and professional opportunities through the conference and OnDemand. Whether you are an end user, supplier, engineer, sales professional, or marketer, SWTest offers something unique for everyone in the wafer-level test industry. I would also like to take this opportunity to thank the sponsors, exhibitors, authors, speakers, session chairs, committee and the SWTest Team members who helped make the hybrid version of the 31st SWTest Conference such a success.

Mark your calendars for the SWTest Asia 2022 Conference that is currently being planned as an in-person event for October 26–28, 2022, in Hsinchu, Taiwan.

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The 72nd IEEE Electronic Components and Technology Conference (ECTC)

By Rozalia Beica [72nd ECTC General Chair, and AT&S China]

ECTC is the premier international conference on microelectronic packaging, components, and systems technology. The 72nd edition of ECTC was held at Sheraton San Diego Hotel & Marina in San Diego, California, USA, from May 31 to June 3, 2022. It was a resounding success! We had 1,509 attendees from 24 countries. Given the uncertainties with the worldwide pandemic and travel restrictions still in place, the attendance significantly surpassed our expectations. We were glad to bring the conference back to an in-person event and provide our community the opportunity to meet again. Equally important was for us to also provide options to our colleagues who could not travel but were still interested in participating. We organized virtual presentations and special sessions giving our technical speakers and panelists the platform to join us virtually and share with us their expertise, latest developments and industry insights.

Preparation for ECTC 2022 started almost a year ago and was strongly supported by over 250 experts from 15 countries and members of 10 technical committees. There were 489 submitted abstracts – with equal distribution between industry and academia – that were critically reviewed by the technical committees, resulting in 362 technical papers. The papers were organized into 41 sessions that represented speakers from 21 countries, including five interactive presentation sessions. One of the interactive sessions was dedicated to students. The most attended topics reflected interests in heterogeneous integration for high-performance computing, automotive and power electronics, 2.5 and 3D integration, fan-out panel-level packaging, advanced flip-chip and embedded substrate technologies, and hybrid and direct bonding, with multiple sessions getting over 300 attendees. Supplementing the technical program and co-located with the IEEE ITherm Conference, ECTC offered 16 CEU-approved professional development courses (PDCs).

We were honored to have Chris Koopmans, Chief Operations Officer with Marvell Technology (Figure 1), as our keynote speaker. Given the changes happening globally, many enhanced by the growth of digital transformation, the infrastructure to support them is becoming increasingly important. It was a very timely and relevant topic to our industry and a great example of why and how Marvell was able to transform itself from a broad, consumer-oriented company, to an industry-leading data infrastructure semiconductor solutions provider.

Figure 1: Keynote luncheon speaker: Chris Koopmans, COO Marvell Technology.

This year the conference included a record number of on-site editions of 9

Figure 2: Great networking events: it's never too early to start attending ECTC!

special sessions and panel discussions. Very well attended and with international participation by experts and executives across the supply chain, the special sessions and panel discussions featured deep-dive discussions on technology developments, emerging applications, different perspectives, business and industry insights and trends, as well as career, diversity and workplace retention topics, such as:

- ECTC Panel Session
  - Co-chaired by IEEE EPS President Kitty Pearsall of Boss Precision, U.S. and Christopher Riso of Booz Allen Hamilton, U.S. on "State-of-the-Art Heterogeneous Integrated Packaging Program (SHIP – DoD Program);"
- ECTC Plenary Session
  - Co-chaired by Rozalia Beica of AT&S, China, and Jean-Christophe Eloy of Yole Group, France, the session addressed "Digital Transformation – The Cornerstone of Future Semiconductor and Advanced Packaging Growth;"
- IEEE EPS Seminar
  - Co-chaired by Yasumitsu Orii of Nagase, Japan and Shigenori Aoki of Lintec, Japan, on the "Interconnect Technologies for Chiplets;"
- ECTC Emerging Technologies Technical Sub-Committee Special Session
  - Co-chaired by Chukwudi Okoro of Corning and Benson Chan of Binghamton University, U.S. on "Micro-LED Display Technologies High-Volume Manufacturing (HVM) Progress and Challenges;"
- ECTC Assembly & Manufacturing Technologies Technical Sub-Committee Special Session
  - Chaired by Jan Vardaman of TechSearch International, U.S. on "Meeting Next-Generation Packaging Challenges: Chiplets to Co-Packaged Optics;"
- ECTC Heterogeneous Integration Roadmap Special Session
  - Chaired by Amr Helmy of University of Toronto, Canada, that covered "Selected Topics of IEEE EPS Heterogeneous Integration (HIR);"
- ECTC/ITHERM Women's Panel
  - Co-chaired by Kim Yess of Brewer Science and Francoise Von Trapp, of 3D InCites, U.S., and Cristina Amon of University of Toronto, Canada, on "Solving Diversification Challenges and Workforce Retention Issues;"
- ECTC/ITHERM Young Professionals Special Session
  - Chaired by Yan Liu of Medtronic, Inc., and Adeel Bajwa of Kulicke & Soffa, U.S., a networking panel focus on career

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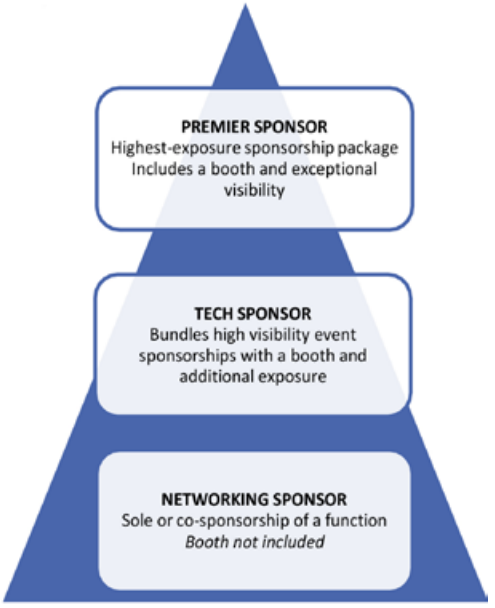

For sponsorship information, contact

Brian Schieman, Executive Director, bschieman@imaps.org

The **55th International Symposium on Microelectronics** is being organized by the International Microelectronics Assembly and Packaging Society (IMAPS) and held at Hynes Convention Center. This year's Symposium will focus on **PACKAGING TECHNOLOGIES ENABLING THE NEW NORMAL**, and will feature 5 technical tracks, plus our Interactive Poster Session. The technical program will span three days of sessions with emphasis on packaging technologies that serve 5G, High Performance Computations, Automotive, Industrial, Defense/ Space, Medical electronics markets, and beyond!

- **TRACK 1: SiP/Design/Manufacturing Optimization**
- **TRACK 2: Wafer Level/Panel Level (Advanced RDL)**
- **TRACK 3: High Performance / High Reliability**
- **TRACK 4: Advanced Package (Flip Chip, 2.5D, 3D, Optical)**
- **TRACK 5: Advanced Process & Materials (Enabling Tech.)**

Figure 3: 2022 ECTC Executive Committee: top row from left to right: Eric Perfecto (Publications Chair), Pat Thompson (Finance Chair), Wolfgang Sauter (Sponsorship Chair), Przemyslaw Gromala (IT Coordinator), Ibrahim Guven (Vice-General Chair), Alan Hufmann (Exhibit Chair), Karlheinz Bock (Program Chair), Florian Herrault (Assistant Program Chair), Tom Reynolds (Treasurer), Michael Mayer (IT Coordinator); front row, from left to right: Annette Teng (EPS Representative), Kitty Pearsall (PDC Chair), Lisa Renzi Ragar (Conference Management), Nancy Stoffel (Jr. Past General Chair), Henning Braunisch (Publications Chair). Missing from the picture are Chris Bower (Sr. Past General Chair) and Rozalia Beica, the 2022 ECTC General Chair.

Figure 4: 2023 ECTC: We are looking forward to seeing you at JW Marriott Orlando, Grande Lakes in Orlando, Florida.

development for young professionals with the participation of IEEE EPS Board of Governors; and

- Heterogeneous Integration Roadmap Workshop
  - Sponsored by the IEEE EPS, EDS and Photonics Societies together with SEMI and ASME EPPD and chaired by William Chen of ASE and Bill Bottoms of MTS, U.S., took place at our conference with another packed audience this year as well. Thank you to the HIR committee for bringing another excellent workshop to ECTC.

The number of the Technology Corner Exhibitors has again crossed the 100 mark with sold-out exhibits and a record level of industry support with 45 sponsorships and 12 media partners. This is a great indication of the growing interest in advanced packaging and the important role ECTC plays in this industry.

ECTC is well known for being a premier, flagship conference of the advanced packaging industry and it has successfully delivered to its name. This year's event delivered even more and diversified content while connecting our community both globally and on site. Besides the highly technical content of this conference and several opportunities to learn and get insights into the latest developments and trends in microelectronics packaging, ECTC is also well known for its great networking events. ECTC 2022 offered over 20 different receptions, the gala, luncheons and various networking events. The feedback was overwhelmingly positive. The entire Executive Committee and I would like to thank all our participants and contributors for their strong and continued support. Special thanks to the Executive Committee and IEEE EPS sponsoring organization for their strong commitment and support in making this year's conference a wonderful event (Figure 3).

Looking forward, the 73rd ECTC will be held at JW Marriott Orlando, Grande Lakes in Orlando, Florida, between May 30 - June 2, 2023 (Figure 4). The Call for Papers can be found at www.ectc.net. Abstract submission will close October 10, 2022. Plan now to attend for in-person sessions, get to know new people, learn where this industry is going, and network with your colleagues!

IMAPS Advanced System-in-Package (SiP) Conference

By Mark Gerber [Advanced SiP 2022 General Chair, and [ASE, Inc.]

On behalf of IMAPS and the SiP Technical Committee we want to thank all the participants, sponsor and exhibitors for supporting the IMAPS 2022 Advanced SiP Conference (held in Sonoma, CA, June 20-23). We received a great deal of positive feedback. A short recap of the event is provided below. Please reach out to IMAPS if you were not able to attend and would like to obtain the presentation materials.

Day 0. We started off with a special heterogeneous integration roadmap (HIR) workshop with an outstanding list of keynotes and invited speakers that covered an intro to HIR, Integrated Photonics, Automotive Electronics, Thermal Management and Supply Chain. This was followed by three professional development courses (PDCs). The pre-conference event was excellent—special thanks go to Bill Chen and Bill Bottoms for the HIR workshop.

Day 1. The first day of the conference kicked off with two keynotes. The first was from Chidi Chidambaram (Qualcomm) on "System-level Optimization Opportunities and Challenges in the Era of Slowing Silicon Process Technology," which provided a look into the next-generation heterogeneous requirements for the next generation of silicon nodes. The second keynote was from Ron Ho (Meta) on the topic of "Silicon SiPs" (system in package) for the Metaverse in which he outlined a number of key miniaturization and performance challenges for the augmented reality (AR)/virtual reality (VR) product space. This was followed by a session of invited speakers, Pouya Talebbeydokhti (Intel), Matthew Poulton (Quoro) and Mohamed Jatlaoui (Murata), who discussed mobile/5G in the morning. In the afternoon session, the topic was wearables/internet of things (IoT) with Curtis Zwenger (Amkor), Mark Poliks (Binghamton University) and Szi Pei Lim (Indium Corp.). The day capped off with a panel session led by Jan Vardaman (TechSearch International) on "Remaining Challenges in the Adoption of 5G," in which several panelists participated including myself, Curtis Zwenger and Matthew Poulton. It was a lively discussion around why there still seems to be some challenges with 5G for both mmWave and sub-6G frequencies.

Day 2. The Khai Nguyen (Nvidia) keynote, "Trends and Reliability Challenges in Advanced Driving Assistance System (ADAS)," provided insight into key considerations for current and next-generation ADAS systems that may use complex modules. Anindya Poddar (Texas Instruments) gave a presentation on "The Automotive Package Ecosystem." This keynote emphasized the need and value of heterogeneous integration and system solutions moving forward, and the key ecosystem players that will be critical to enable. An invited speaker session followed on the topic of high-performance computing (HPC)/co-packaged optics (CPO) with talks covering next-generation advanced fan-out embedded bridge featuring Lihon Cao (ASE), hybrid bonding by Robert Patti (Nhanced Semi), and the path to sub-fJ/Bit interconnect by Daniel Graf (Zero EC). The afternoon focused on automotive and power topics with invited speakers Hongbin Yu (Arizona State University) on "Automotive Power Delivery," Pradeep Lall (Auburn University) on "FCBGA [flip-chip ball grid array] Underfill Materials for Automotive," and Mike Marczi (Marel Power) with a talk on packaging beyond 100kW/L.

The startup company competition had four companies pitching their technology: Averatek, Avicena, Mosaic Microsystems and Sivers Semiconductors (Mixcomm). It was a tough competition and we congratulate the winner, Haris Basit with Averatek. Finally, the day closed with a panel roundtable led by Eelco Bergman (ASE) on "Chiplet Based Architectures – the Road to Mass Adoption," where he hosted four panelists that shared their insights regarding current and future challenges with chiplet integration.

Day 3. The final day began with a keynote from Ming Zhang (Synopsys) who presented on the topic of "Conducting the Semiconductors: The Role of Design in the SysMoore Era," followed by invited speakers John Park (Cadence) and Anthony Mastroianni (Siemens EDA) who provided their insights related to chiplet integration, as well as the ecosystem. The last session featured three speakers on test considerations: Warren Wartel (Amkor), Wei Wang (National Instruments), and Ken Lanier (Teradyne).

The technical program can be viewed at: https://imaps.org/sip_agenda.php

Stay tuned for next year's 2023 IMAPS Advanced SiP Conference and Venue.

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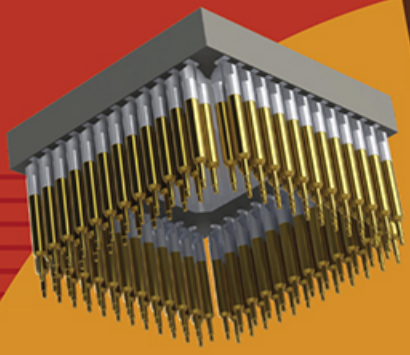

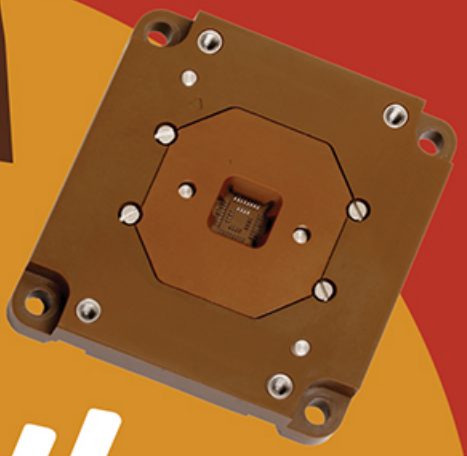

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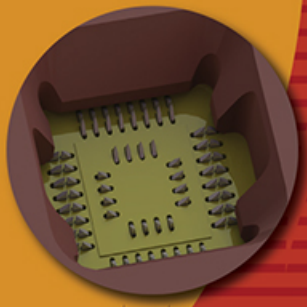

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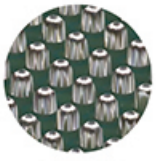
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