Large-size multi-layered fan-out RDL multi-chip module packaging

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Heterogeneous integration is the key technology that is applied in high-performance computing (HPC), artificial intelligence (AI) and cloud computing applications, as well as for die-to-die interconnections, application-specific integrated circuits (ASICs) to high-bandwidth memory (HBM), and ASIC-to-ASIC. The higher I/O density, wider data transmission bandwidth between memory to active die and lower RC delay are required in chiplet integration. Heterogeneous integration between different functional dies, however, leads to various process challenges, such as warpage control for multi-layered redistribution layers (RDLs), surface co-planarization treatment, and solder joint capability during the die bonding (DB) process. Therefore, in this article, we demonstrate a large size fan-out multi-chip module (FO-MCM) package with 6-layers of RDLs that successfully overcomes the non-wetting issue and warpage effects by using optimized RDL technology and compatible glass carrier selection during wafer processing.

In this study, we specifically demonstrate a FO-MCM with 6 layers of RDLs with 2/2µm line/spacing using chip-last technology. As a result, the warpage effect was decreased 39% by a particular glass, which has a compatible coefficient of thermal expansion (CTE) parameter and thickness. Additionally, we assess chip module warpage performance during reflow at a high temperature of 245ºC of chip-last FO-MCM, which is important for addressing C4 bump non-wetting phenomenon during the chip module bonding to substrate process.

The multi-layered RDL with the compatible glass technology described above brings a potential benefit to improve the warpage effect on the RDL surface. The results of the reliability tests, which are qualified in the experiment, include: 1) temperature cycling testing (TCT) for 1000 cycles; 2) unbiased highly-accelerated stress testing (u-HAST) for 192 hours; and 3) high-temperature storage life (HTSL) testing for 1000 hours. Undoubtedly, heterogeneous integration with multi-layer fan-out RDL is the mainstream for AI, cloud computing and HBM integration in the IC package industry. By utilizing this multi-layer RDL with compatible glass technology, the stability and yield of the fine-pitch die bond will be improved.

Background

Over the last decade, the semiconductor industry has demonstrated the incredible possibilities for revolutionary technologies. For example, several advanced packaging technologies have been developed to accelerate machine learning (ML), AI and HPC applications, such as 2.5D/3D, FO-MCM, fan-out embedded bridge (FO-EB), and fan-out package-on-package (FO-PoP). These packaging technologies enable heterogeneous integration scaling, which drives interconnect density with an increased bandwidth requirement, while also enabling more effective die partitioning to shorten the time to market [1-5]. However, the traditional monolithic die design in which a multi-core is integrated into one system on chip (SoC) die architecture is facing many challenges, such as increasing wafer cost, limited die size, and high power consumption. Consequently, fan-out packaging was proposed and developed as the robust solution to reduce packaging costs and provide a more flexible chiplet combination by using die partition methodology. The resulting fan-out redistribution layer (FO-RDL) technology became an essential routing technology between the die to die interconnect area. Additionally, finer line/space (L/S) values of metal trace and multi-layer RDL routing are required in order to enhance the high-speed and demands for large-volume data processing.

Fan-out technology has been developed into a variety of structures for particular applications or purposes. **Figure 1** shows the main platforms and their names, which are classified by the relevant RDL interconnect technique. The first type is called FO-EB, or

Interconnect	Structure	3D Drawing	Platform
Bridge Die + RDL			FO-EB / FO-EB-T
RDL			FO-PoP
RDL			FO-MCM

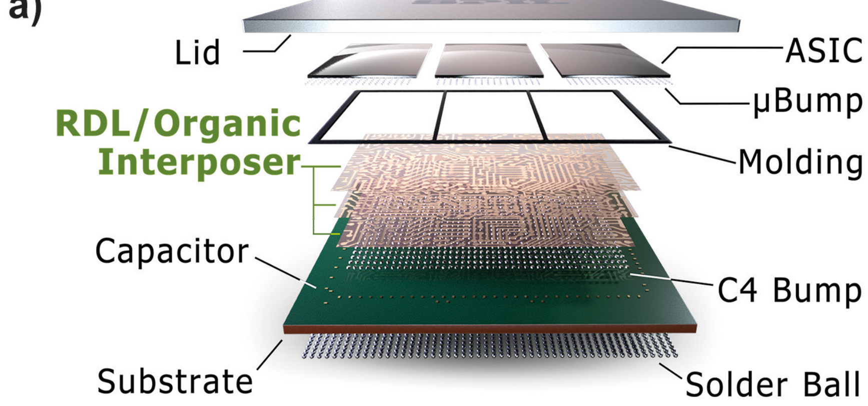
Figure 1: Fan-out technology platforms.

FO-EB-T (where "T" represents through-silicon via); in these structures, the top dies are connected by a silicon bridge die and a RDL. The bridge die plays the main role with respect to communicating in the high-speed area between the die-to-die structure. Because of the fine-pitch and small L/S design, the metal L/S on the bridge die is normally smaller than 0.56µm. Therefore, compared to 2.5D, FO-EB only requires a small silicon die size at the interconnect area, which reduces the interposer cost by reducing the gross die size and raising the yield performance for each interposer wafer. Furthermore, FO-EB-T (which is designed using TSV structures) inside the bridge die is the next cutting-edge packaging technology. Using a TSV design in the FO-EB-T structure, the electrical performance is enhanced by shortening the signal or power delivery path between the top die and the bottom substrate.

FO-PoP is also a very popular platform for mobile processor applications in which the dies are vertically interconnected. It is generally used to connect the top low-power double data rate (LPDDR) memory with the bottom system on chip (SoC) die. Therefore, the small form factor, thin package height and low power consumption are the key design factors for FO-PoP. Finally, FO-MCM is another main platform that is widely applied in advanced packaging. In FO-MCM, the RDL connects the top dies horizontally using multi-layers of RDL; and the L/S is generally scalable between 2/2µm~10/10µm. This flexible routing design is better for power and signal integrity. On the other hand, FO-MCM is the ideal structure to achieve a lower cost than 2.5D because the costly silicon interposer is not required [6-9].

Fan-out multi-chip module (FO-MCM) package technology

The FO-MCM architecture is shown in **Figure 2a**. Three ASIC dies are integrated on a 2,000mm^2 large chip module, the metal routing applies 6 layers of RDL with 2/2µm L/S, and the package size is 6,000mm^2, which is covered by a lid-type heat sink on the top. **Figure 2b** shows that 6L RDLs are built up with C4 bumps for the vertical transmission of signal and power from active dies to the substrate. The FO-MCM structure is highly flexible for advanced package design in terms of the Cu wire inside the RDL layers. FO-MCM is, therefore, also a robust platform for both homogeneous and heterogeneous integration, owing to the advantages of known-good RDL before die attaching and a competitive manufacturing cost. Additionally, FO-MCM has a shorter development cycle time than 2.5D and FO-EB because the RDL interposer can be grown before the wafer arrives at the outsourced assembly and test (OSAT) site for chip-last processing. Therefore, FO-MCM is widely applied in chiplet integration because it can be performed as an assembly turnkey service provided by the OSAT supplier. Moreover, the heterogeneous integration of ASIC to HBM memory has also been investigated in advanced packaging and it further proves out the advantages of having known-good RDL before die attaching is done in the chip-last process flow. This means that HBM memory yield won't be impacted (lost) during assembly, which again demonstrates the high yield performance of the FO-MCM platform. We will introduce both chip-first and chip-last process flows in this article.



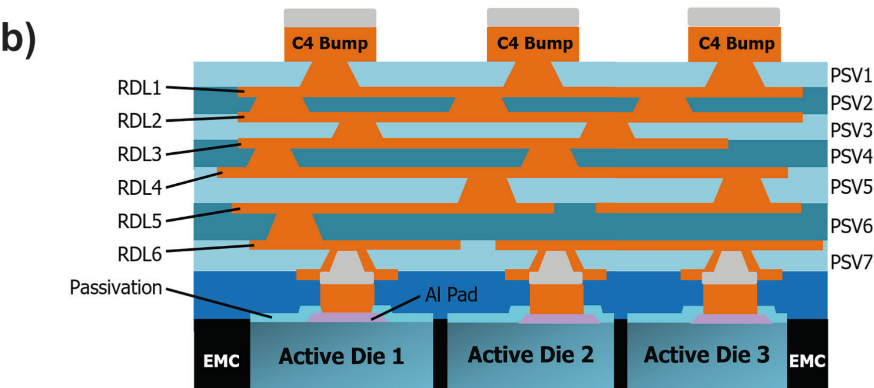


Figure 2: a) FO-MCM architecture—ASIC dies are integrated on a 2000mm^2 large chip module, the metal routing applies 6 layers (RDL) with 2/2µm L/S, and the package size is 6,000mm^2; b) 6 layers (RDL) are built up with C4 bumps for the vertical transmission of signal and power from active dies to the substrate.

Chip-first and chip-last process flows for FO-MCM

Generally, FO-MCM has two major process flows: chip first and chip last [10-11]. A brief introduction to each is provided below.

Chip-first process flow. The chip-first process flow is shown in **Figure 3a**. Silicon dies are applied onto a glass carrier with release tape; molding compound is then added to build a "reconditioned wafer." Then, a lapping process is done to expose the die. Multi-RDL layers are then deposited on the die surface. C4 bumps are then built on the RDL module, followed by a second lapping to expose the back side and reduce the molding thickness to

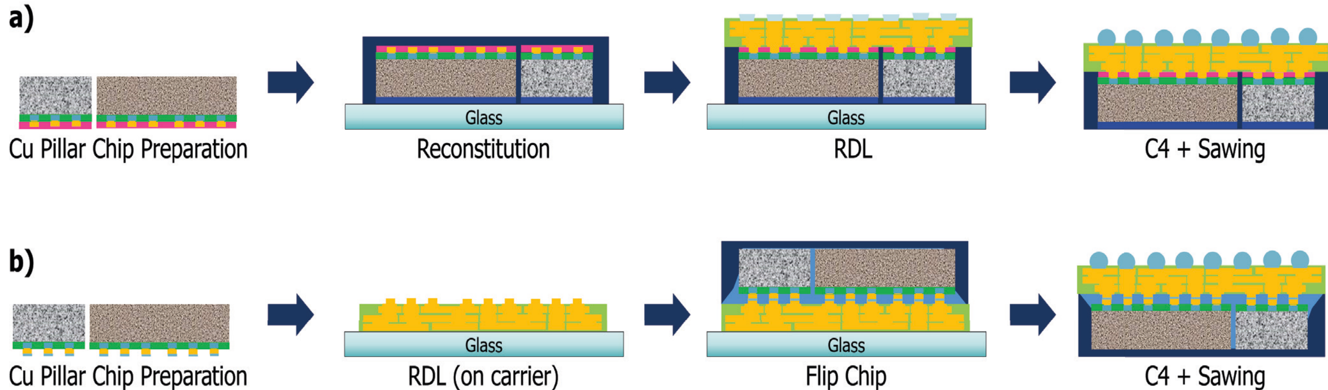


Figure 3: FO-MCM process flows for a) chip-first, and b) chip-last approaches.

the target thickness. Finally, sawing is done to form chip module units.

Chip-last process flow. The chip-last process flow is shown in Figure 3b. In the first step, RDL layers are grown on a flat glass carrier, and then a die attach process is used to attach dies to the Cu pillar bump on the RDL carrier. Under fill is then added into the micro-bump space to protect the interconnect area. Next, the RDL module is covered with molding compound. And lastly, the carrier is removed and C4 bumps are grown on the opposite RDL surface.

Compared to the chip-first process, however, the chip-last process has a more complicated process flow. Still, the chip-last process shows several obvious advantages when either the chip module size or the number of RDL layers number is increasing. Those advantages are as follows. First of all, there is no loss of KGD because the RDL yield and quality can be inspected before the die bond process, so the die loss risk can be avoided. In particular, this is a benefit because a costly wafer comprising dies at advanced nodes (e.g., 7nm, 5nm, 3nm and below) can be used. Secondly, higher yield performance is achieved compared to the chip-first process because the non-coplanarity risk is higher for the chip-first process than for the chip-last process. The risk is higher because of the grinding tolerance that is needed when multi-die surfaces are being worked on simultaneously. The end result is a lower module yield while stacking the RDL on the die's face. Lastly, the chip-last process flow makes embedding of die easier because the thickness of the die is not an issue.

Stress simulation results

In this simulation study, the stress ratios are investigated for both chip-first and chip-last structures, which are designed by 6L, 2L and 1L RDL layers individually as shown in Figure 4. As we can see from the simulation result in Figure 4a, the stress effects on the top RDL layer of the chip-first structure are 90%, 119% and 127% higher than for the chip-last case of 6L, 2L and 1L RDL structures shown in Figure 4b. Additionally, the stress ratio is 12% from 6L to 2L RDL, and 18% higher from the 6L to the 1L RDL structure individually on the top RDL of the chip-last structure. Conversely, compared to the chip-last case, the stress on the chip-first structure increases to 29% comparing the 6L RDL structure to the 2L RDL structure; and the stress increases

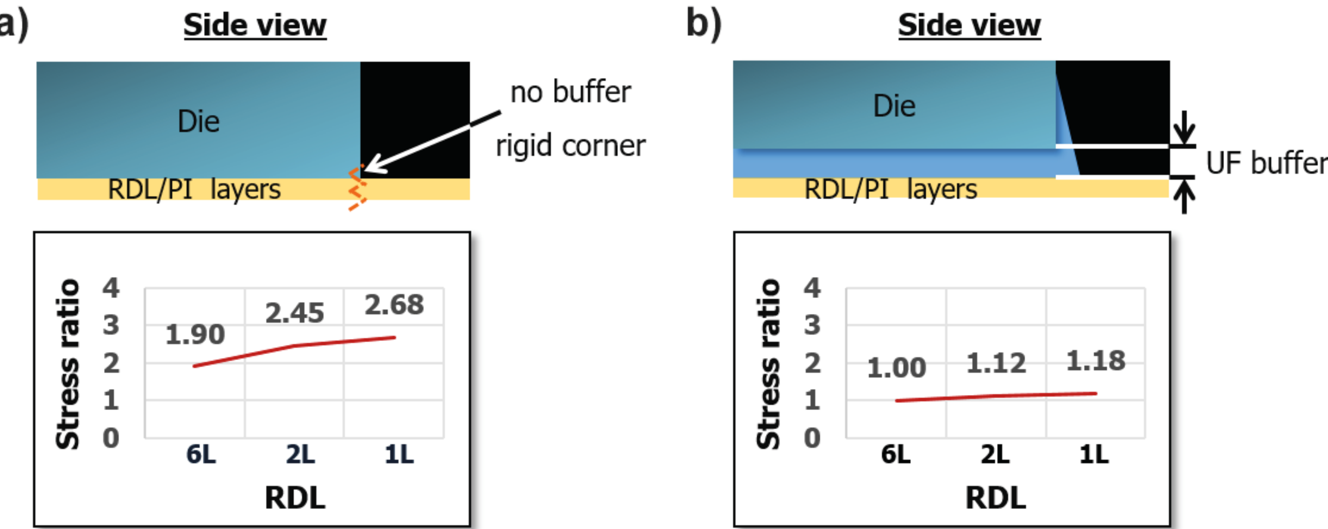


Figure 4: a) Stress simulation results of 6L, 2L and 1L RDL in the chip-first case; and b) The stress simulation results of 6L, 2L and 1L RDL in the chip-last case.

41% from the 6L RDL to the 1L RDL case, individually. Therefore, the simulation result shows that the chip-last structure has a lower stress effect on the top RDL layer because the under fill functions as a strong buffer layer that absorbs the stress from the corner area of the top die. What this means is, the FO-MCM structure — by using the chip-last process — has a lower risk of RDL cracking because of the protection provided by the under-fill layer.

Warpage measurement results

Generally, the biggest challenge for FO packaging is warpage control because if mismanaged, it can be an interruption. This situation is particularly challenging for finer high-density FO-RDL used in multi-die integration. A larger package size and more RDL layers are the factors that result in severe warpage and yield loss. In this study, we obtained yield results using a wafer with 2/2µm L/S RDL in chip-first and chip-last structures, individually. As shown in Figure 5a, the chip-last structure shows better RDL quality than the chip-first structure on the whole wafer area because of its better warpage performance. The chip-first structure also has an issue with a missing copper trace on the wafer edge side. As shown in Figure 5b, the missing copper trace was caused by the fact that the chip-first structure experienced a worse warpage effect (see Figure 5c). As a result, the material CTE mismatch between the RDL layers and the molding compound interface is the key factor to cause this convex-shaped warpage in the chip-first structure. Therefore, in order to achieve better RDL topography and quality, the glass carrier was optimized for different thicknesses and CTE parameters to try and reduce the wafer warpage effect during the inline process. Table 1 shows the warpage effect on glass types A and B by 3L and 6L RDL designs, individually. Comparing the results, it can be seen that glass B has the smaller CTE value and a 30% thicker thickness than the type A glass carrier. Therefore, by using glass B in the FO process, the wafer warpage effect was dramatically improved 39% in the 6L RDL FO-MCM chip-last structure.

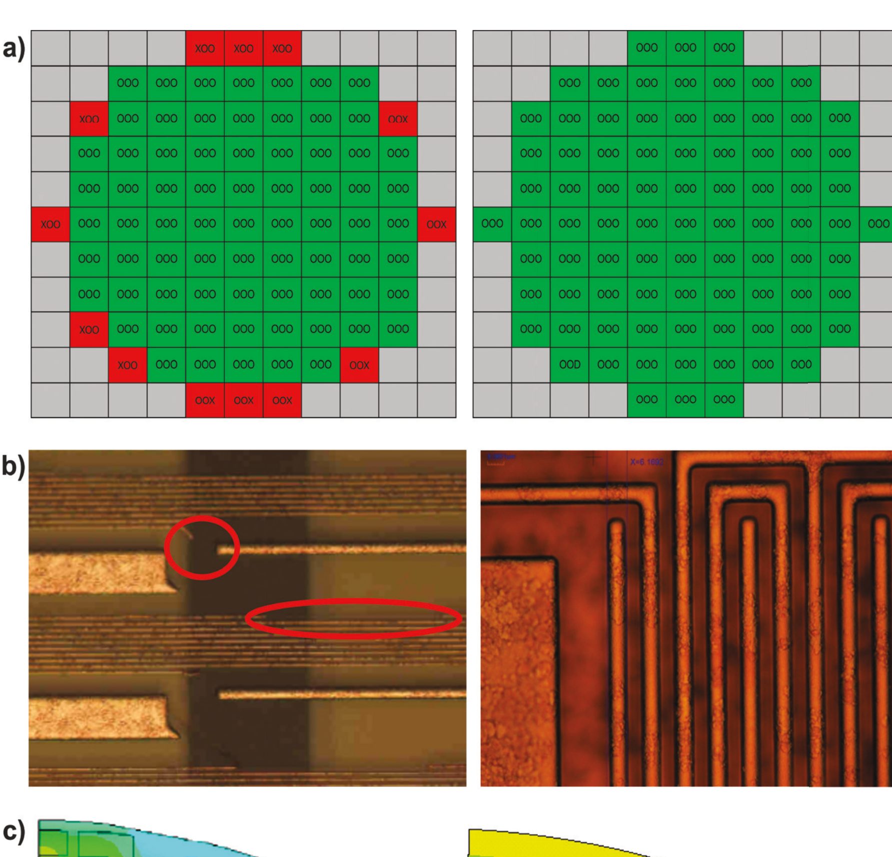


Figure 5: a) Chip-last structure showing better RDL quality than the chip-first structure on the whole wafer; b) Chip-first structure with a copper trace missing on the wafer's edge; and c) Worst warpage effect on the chip-first structure.

Leg	Structure	Wafer Form Warpage (mm)					
		RDL 1	RDL 2	RDL 3	RDL 4	RDL 5	RDL 6
Glass A	3 layers RDL	+0.24	+0.49	+0.8			
	6 layers RDL	+0.24	+0.51	+0.78	+1.07	+1.29	+1.65
Glass B	3 layers RDL	+0.16	+0.41	+0.65			
	6 layers RDL	+0.18	+0.41	+0.61	+0.82	+0.95	+1.01

Table 1: Warpage effect on glass types A and B for 3L and 6L RDL designs, individually.

Yield performance vs. FO size and RDL layers results

The diagram of fan-out size versus yield performance is plotted in Figure 6a. The blue line represents the chip-first (CF) structure. The red line represents the chip-last (CL) structure—it shows that the package yield performance of CF decreased more than that of the CL structure as the fan-out module size increases. RDL yield performance is compared between CF and CL in Figure 6b. The RDL yield was analyzed for different RDL layers of a certain package size. As can be seen, the CL structure had an over 98.5% yield performance—this is because the known good RDL feature is set before the die bond process. However, the yield of the CF case

is getting worse when the number of RDL layers is raised from 2L to 5L. This study shows that the CL design has the better yield control capability in both the large module size and high RDL layers design.

This indicates that the CL structure has the potential to show a better cost benefit than the CF structure once either the FO size or the number of RDL layers exceed a particular range.

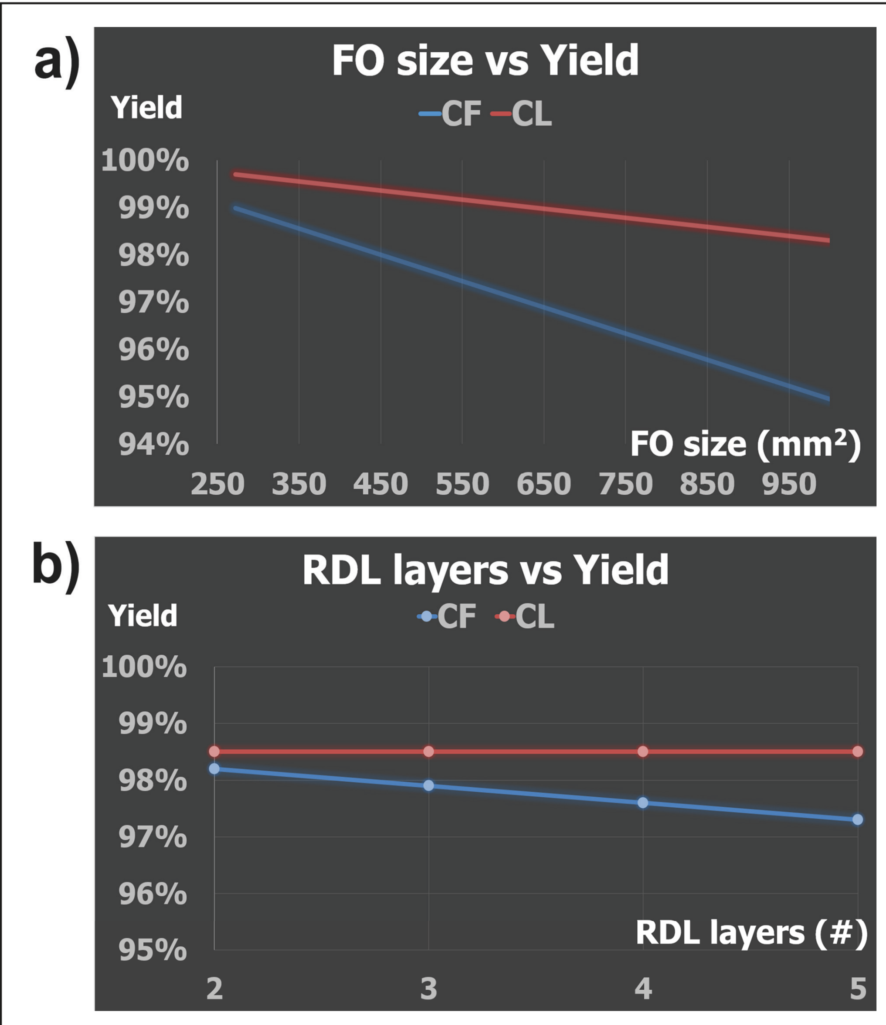


Figure 6: a) Fan-out size versus yield performance; and b) Analysis of the RDL yield by different RDL layers.

Summary

FO-MCM using the chip-last technique has been demonstrated as a robust package paradigm. It provides less stress effect, better warpage control and high yield performance. **Figure 7** shows the SEM cross-section image of a FO-MCM with 6L RDL. The micro-bump height and diameter are 8µm and 25µm in this design, and the top coplanarity is controlled within 4µm, which ensures the quality of the micro-bump joint after the reflow process. In addition, the 6-via stacking structure was demonstrated in this experiment through the use of an optimized glass design. The top total thickness variation (TTV) was shown to be under control such that excellent joint quality was achieved in both the via stacking and non-via stacking areas.

Additionally, reliability tests were verified in this study. All reliability conditions received a "pass" result for MSL3, TCT1000, u-HAST192, and HTSL1000 conditions. Furthermore, the cross-section of the micro-bump joint area (after completing the reliability tests) as shown in **Figure 8**, indicates perfect joint quality without any non-wetting, void or solder creeping issues. In this investigation, the FO-MCM package not only provides an alternative solution from a cost-benefit standpoint, but also results in less warpage during chiplet integration when using an optimized glass carrier design. With the advantages of being able to control the warpage and have less internal stress, FO-MCM is the proper platform to build up a much larger package size for the integration of even more dies.

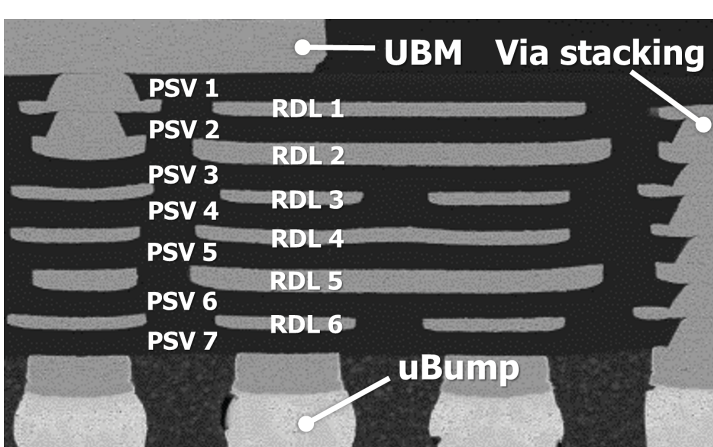


Figure 7: SEM cross-section image of an FO-MCM structure with 6L RDLs.

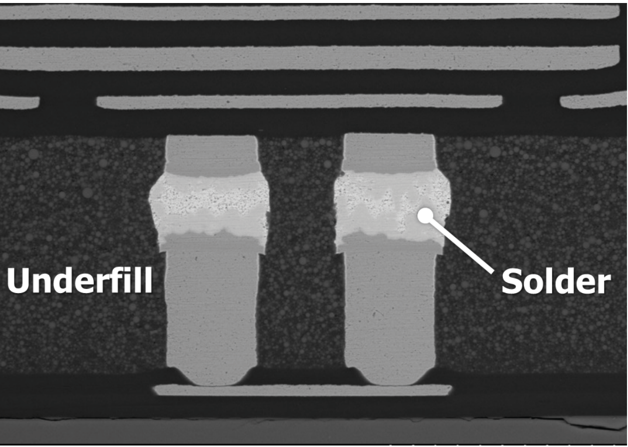


Figure 8: Micro-bump joint cross-section SEM result.

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