Sustaining Moore's Law with graphene

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Since the invention of metal-oxide-semiconductor (MOS) integrated circuits in the early 1960s, the speed, capacity, and complexity of the chips have increased dramatically, roughly following Moore's Law, owing to various technological and process breakthroughs that doubled the transistor count per chip area every two to three years. Along with the advancement in transistor technology, the wires (or interconnects) that connect these billions of transistors have also evolved tremendously. **Figure 1** provides a snapshot of the evolution of the interconnect and intra/inter-layer dielectric (ILD) technology, also known as back-end-of-line (BEOL) technology. The aluminum (Al) wires used initially during 1960-1980 were replaced by better performing aluminum-copper (Al-Cu) wires, which were followed up in 1997 by the currently employed dual-damascene (DD) wiring scheme utilizing electroplated Cu, resulting in denser, faster, and more reliable wiring solutions.

Scaling limitations of conventional interconnect materials

Even though cobalt (Co) has recently been introduced as a possible substitute for the narrowest Cu lines to keep Moore's Law alive, these technologies will eventually run out of steam when wiring dimensions approach sub-20nm. At these critical dimensions, conventional technologies such as Cu, Co, and noble metals such as ruthenium (Ru) suffer from significant size effects, mainly due to a nonlinear increase in resistivity, and resulting wire and via resistances, which increases RC-delay and self-heating, degrades electromigration reliability, and thereby limits their current-carrying capacity and performance (**Figure 2a-c**) [1,2]. Additionally, void formation during metal fills in highly scaled (and high aspect ratio [AR]) trenches and via holes during the DD process exacerbates the reliability and variability problems, thereby making further increase in the aspect ratio difficult. Traditional solutions will fail to meet the performance-based current density requirements set forth by the International Roadmap for Devices and Systems (IRDS) beyond 15nm wiring dimensions, as shown in **Figure 2d**, necessitating an urgent need to identify alternative metallization strategies to keep Moore's Law alive.

What is so exciting about graphene interconnects?

Since its discovery in 2004 [4], graphene has been proposed as a potential material for future electronics because of its unique electrical, optical, and mechanical properties. Initially derived from its 3D layered allotrope-graphite (**Figure 3a**), graphene is a single atomic-layer-thick sheet of carbon atoms (**Figure 3b**). A hexagonal honeycomb crystal structure of graphene (**Figure 3c**) is formed by the sp^2 hybridized in-plane bonding arising from the electron sharing of each carbon atom with three nearest carbon atoms (**Figure 3d**) with exceptionally high mechanical strength. This results in a unique electronic band-structure shown in **Figure 3e** where the conduction and valence bands precisely

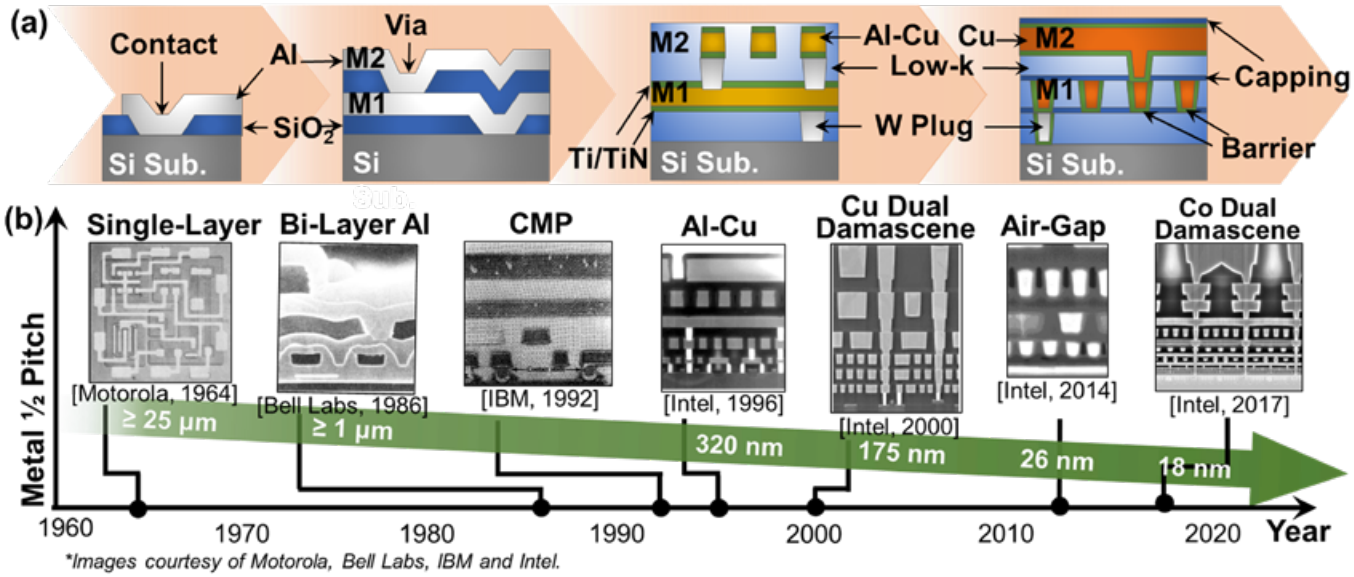


Figure 1: Evolution and scaling of BEOL technology—from the use of Al wires and SiO_2 dielectric to the current state-of-the-art dual-damascene technology based on Cu and low-k dielectrics: a) A cross-sectional view of the various metallization technologies adopted by the semiconductor industry. b) Scaling of the metal-1 ½ pitch along with the cross-sectional scanning electron microscope (SEM) images corresponding to each new technological evolution.

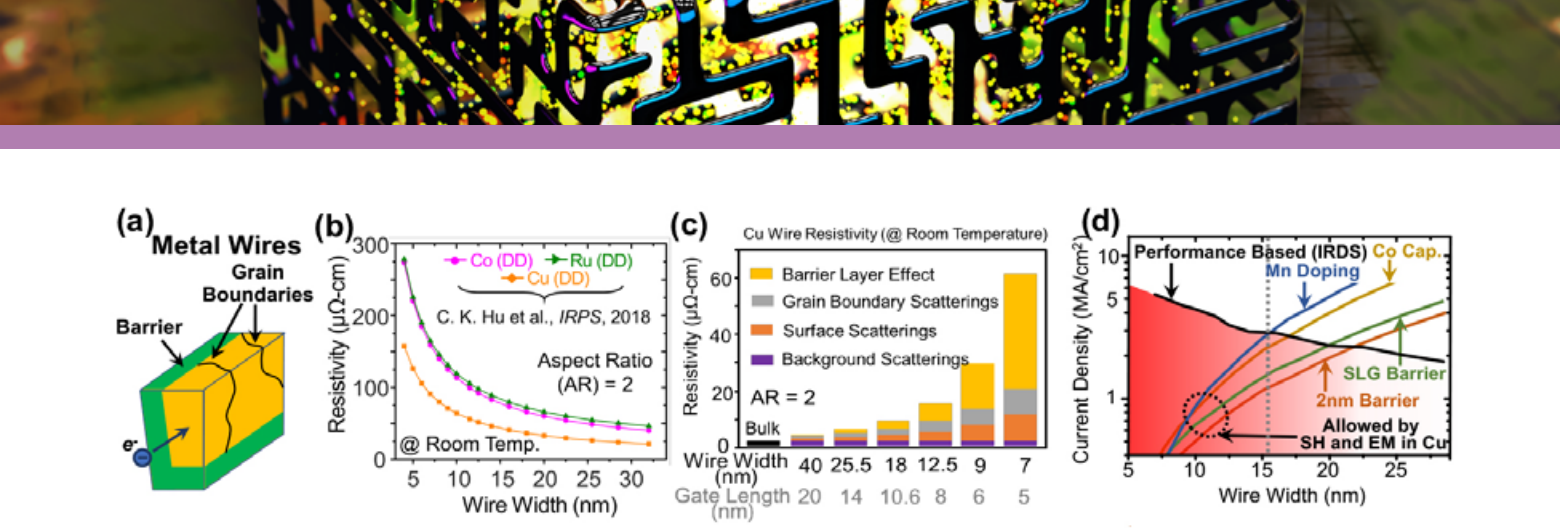


Figure 2: Challenges of the current BEOL technology: a) Schematic of the typical interconnect structure used in current CMOS technology with the barrier layer (in green) and the metal (in yellow). b) Resistivity vs. wire width for conventional metal interconnects as a function of wire width. The significant resistivity/resistance increase for sub-20nm critical dimensions is primarily due to the inability of the barrier layer to be scaled down at the same rate as the actual metal itself, which is shown in (c) to contribute more than 50% of the total wire resistivity at sub-10nm wire widths. d) Circuit-performance required current density for integrated circuit interconnects and the maximum allowed current density for Cu interconnects with TaN and single-layer graphene (SLG) barrier, Co capping, and Mn doping (from electromigration (EM) reliability and self-heating). While Mn doping and Co capping help in increasing the current-carrying capacity by restricting the diffusion (and hence, EM) of Cu atoms, it severely increases the wire resistance. The maximum current density allowed by self-heating and EM for Mn doping and Co capping are estimated from Black's equation by using the experimentally obtained activation energy and the time to fail data. More information is available in [3].

cross at Dirac points, thereby making graphene a zero-bandgap semimetal. Moreover, the linear energy dispersion (E-k relation) of electrons around Dirac points (**Figure 3e**) makes graphene different from other materials like silicon with parabolic electron dispersion. By patterning graphene into nanoribbons (**Figure 3f**), a bandgap can be opened (**Figure 3g**) because of the confinement of carriers in such materials; the magnitude of this bandgap is a critical function of the graphene nanoribbon (GNR) width and thickness [5] (**Figure 3f**). Furthermore, this bandgap is an indication of the highly nonlinear effects that occur at sub-50nm wire dimensions in these materials [6]. These nonlinearities can be alleviated by introducing foreign atoms/molecules between the layers of graphene, also called intercalation doping, offering high flexibility in designing systems using graphene [7-9].

Multiple layers of graphene (also called multilayer graphene (MLG)) are preferred for designing interconnects and systems as compared to monolayer graphene. This is primarily because of its lower contact resistance and higher density of states compared to monolayer graphene. Unlike monolayer graphene, MLG has a parabolic band structure, which, after intercalation, significantly shifts the Fermi level and restores the linear band structure of monolayer graphene, offering a dual benefit of not only tackling the nonlinearities, but also significantly modulating its conductivity [9]. Moreover, the strong sp^2 hybridized bonds in graphene/MLG offer a substantially higher melting point than conventional metals (**Figure 4a**), and significantly higher mechanical strength (stronger than steel) and in-plane thermal conductivity. On the other hand, graphene's extraordinary electrical conductivity is due to the π band (**Figure 3d, e**). These unique traits, in conjunction with low $\rho_0\lambda$ product (**Figure 4a**) (which signifies lesser electron scatterings at the surfaces and grain boundaries at ultra-scaled dimensions, and hence reduced resistivity size effect, **Figure 4b**), high carrier mobility, and high carbon abundance (inset of **Figure 4a**) make graphene (or more specifically, doped multi-layer graphene (DMLG)) an ideal candidate for next-generation on-chip interconnects [7,8]. Apart from Cu, Co, and the noble metal Ru, several other noble metals (Pt, Ag, Au) and layered materials (MoS_2, WTe_2) have been considered as potential interconnect candidates, however, they either cannot match the performance-based current density requirements, or suffer from poor carrier concentration, thereby restricting their use in upcoming BEOL technology nodes [7].

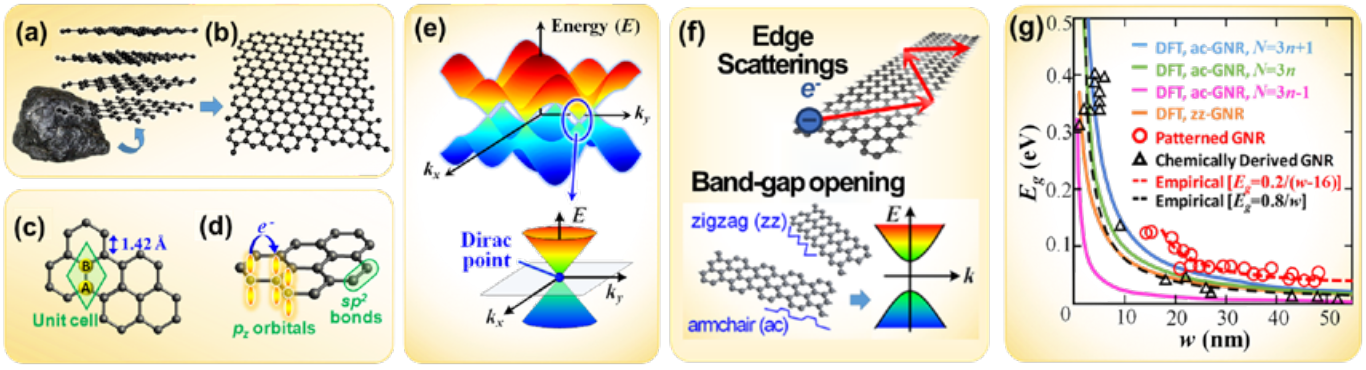
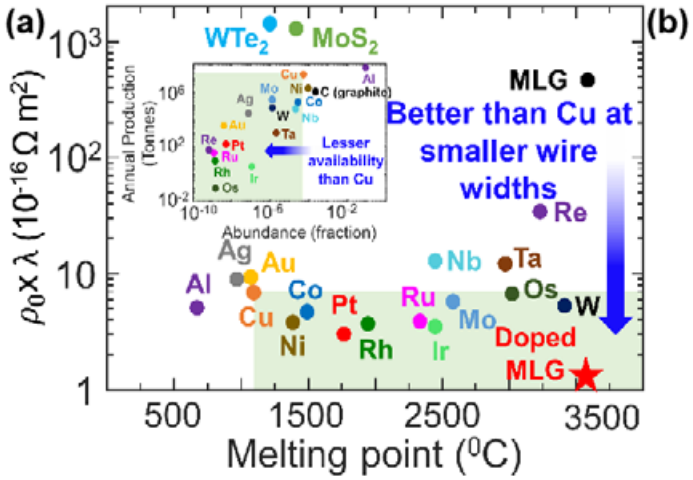


Figure 3: Fundamentals of graphene and GNR. a-b) Graphite to graphene transition; c) Crystal structure of graphene showing the unit cell. d) sp^2 bonding of graphene forming in-plane σ band, and origin of the π bands (from the out-of-plane p_z orbitals) that are responsible for its amazing electrical conductivity. e) Electronic band-structure of the π band of graphene displaying linear E-k dispersion of electrons and zero bandgap with the conduction and valence band edges meeting at the Dirac point. f) Various nonlinear effects (edge scatterings and bandgap opening) in graphene as its width is scaled down to sub-50nm critical dimensions. g) Bandgap (E_g) tunability of GNR, where N is the number of carbon atoms along the width (w) of GNR and n is a natural number [5].



Interconnect Candidates	Resistivity (μΩ-cm) @ 20 nm wire width		
	AR = 2	AR = 1	AR = 0.5
Cu	32.91	45.8	62.03
Co	59.88	82	113.27
W	34.04	36.864	42.517
Ru	66.033	88	119.06
Pt	30.93	34.69	42.23
Undoped MLG	543.37	543.37	543.37
Doped MLG	15.17	15.17	15.17
Metallic WTe_2 (Experimental) (2 μm width, ~10 nm thick)	~8x10^3		
Semiconducting MoS_2 (Experimental) (2 μm width, ~0.5 nm thick)	~5x10^3		

Figure 4: Advantages of graphene as a prospective interconnect technology can be seen in the following: a) Product of bulk resistivity (ρ_0) and mean free path (λ) vs. the melting point of various conventional interconnect candidates in comparison to that of MLG, used for identifying the best interconnect candidate for advanced technology nodes. The conductivity of bulk MLG can be significantly modulated by doping to bring it inside the desired green corner, making it the best interconnect candidate for replacing Cu. The inset figure shows the annual production of various metals used in (or considered for) the BEOL technology. b) Table showing the resistivity of various metal candidates and two-dimensional (2D) van der Waals materials in comparison with doped (E_F = ±0.6eV) and undoped MLG at a wire width of 20nm and aspect ratios of 0.5, 1, and 2, indicative of the resistivity size effect for the conventional metals as compared to graphene.

Integrating graphene interconnects in CMOS

Micromechanical (or liquid) exfoliation of graphene from bulk graphite yields relatively small (micron sized) flakes that are not suitable for a complementary metal-oxide semiconductor (CMOS) process. The most common approach for growing relatively large-area graphene is to use chemical vapor deposition (CVD), which is based on the thermal decomposition of its gas-based precursors on a metal catalyst substrate such as Cu or Ni. While this approach yields high-quality graphene/MLG, it not only requires temperatures that are far higher than the BEOL thermal budget (<450°C), but also requires a transfer from the metallic growth substrate to the desired substrate, making it unsuitable for direct application in the BEOL CMOS process. Other techniques to grow graphene, such as epitaxial growth, or solid-phase growth, also require much higher temperatures than the allowed thermal budget and the resulting MLG quality is not sufficient for interconnect application (see **Table 1** for a summary of various growth methods). Recently, the Nanoelectronics Research Lab (NRL) at UC Santa Barbara devised a new approach for growing high-quality multi-layer graphene at significantly lower temperatures (~300°C), by a pressure-assisted solid-phase diffusion of carbon atoms through the bulk and grain-boundaries of a sacrificial catalyst metal (Ni) [8]. Approximately 20nm-thick MLG can be grown using ~65-80psi of mechanical pressure and ~30-60min of growth time.

Figure 5a shows the cross-sectional schematic of the wafer/chip during the growth process. This technique is highly versatile and possesses the capability to be engineered to directly grow high-quality low-temperature graphene/MLG with varying thicknesses on arbitrary substrates [10]. The quality of graphene/MLG developed using this technique is equivalent to that produced using traditional methods (**Figure 5b**), making

Graphene Synthesis Technique	Pros	Cons	CMOS-Compatible?
Mechanical Exfoliation	• Excellent quality (high crystallinity) • Room temperature process	• Requires transfer • Difficult to control the number of layers • Small area flakes	No
Liquid Exfoliation	• Good growth quality • Room temperature process • Large-area flakes (~50-100 μm)	• Non-uniform area coverage • Difficult to precisely control thickness • Low-crystallinity • Requires transfer	No
Chemical Vapor Deposition (CVD)	• Excellent growth quality • N/P doping possible	• High growth temperature (~1000 °C) • Requires transfer • Difficult to control the number of layers and area coverage	No
Plasma-Enhanced CVD (PECVD)	• Excellent growth quality • Direct growth on dielectric substrates • N/P doping possible	• High growth temperature (~600 °C) • Non-uniform area coverage • Non-uniform doping	No
Epitaxial Growth on SiC/Ru	• Direct growth on SiC/Ru • Excellent growth quality • Wafer-scale area coverage	• Very high growth temperature (~1100 °C) • Thickness restricted to 1-2 layers • Need UHV environment	No
Solid-Phase Epitaxy (using amorphous carbon)	• Good growth quality • Direct growth below catalyst metal (no transfer)	• High growth temperature (~900 °C) • Non-uniform growth quality	No
Solid-phase Segregation and Precipitation	• Good growth quality • Wafer-scale coverage	• High growth temperature (~1000 °C) • Difficult to control the number of layers • Graphene growth on catalyst metal	No
Catalyst Metal Agglomeration	• Good growth quality • Direct growth on multiple substrates • Controllable thickness	• High growth temperature (~800 °C) • Non-uniform growth • Small area coverage	No
Pressure and Temperature Assisted Solid-Phase Growth (NRL-UCSB)	• Low-temperature (~300-350 °C) • High quality growth • Direct growth (no transfer) • Wafer-scale coverage • Controllable thickness • N/P doping possible	• Needs specialized tool – commercially unavailable • Graphite powder may require specialized processing/handling	Yes

Table 1: Summary of various graphene/MLG growth techniques reported in the literature. The growth method developed in NRL-UCSB is the only method capable of satisfying the crucial CMOS-compatibility criterion.

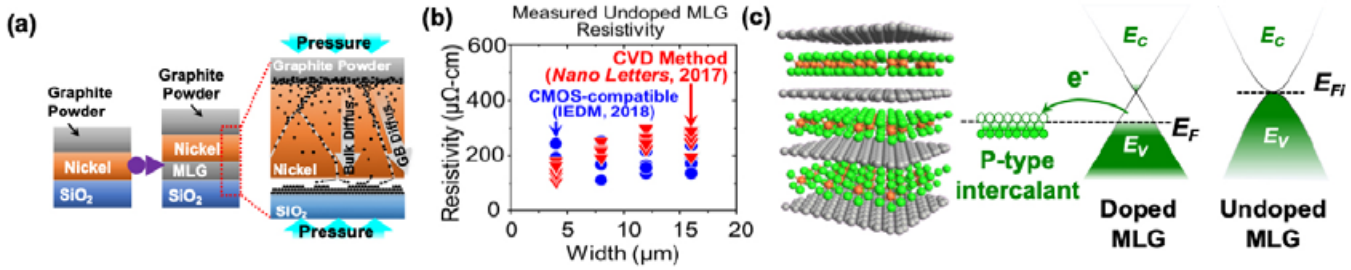


Figure 5: CMOS-compatible multilayer graphene (MLG) growth. a) Cross-sectional view of the wafer during the pressure-assisted CMOS-compatible solid-phase graphene growth technique. The growth occurs through the diffusion of carbon atoms through the grains (bulk) and grain boundaries of the sacrificial catalyst metal, Ni. b) Resistivity vs. wire width of undoped MLG using the CMOS-compatible growth technique in comparison with the conventional CVD method [7]. c) Schematic of $FeCl_3$ intercalation-doped MLG structure, and the corresponding band-diagram of MLG before (undoped) and after (doped) intercalation.

it a viable option for BEOL integration [8,11]. Additionally, the introduction of suitable intercalants/dopants between the layers of MLG (**Figure 5c**) can lead up to ~5x improvement in resistivity, ~4x improvement in RC-delay, and ~80%/72% benefit in switching energy at the local/global level wires as compared to conventional interconnect materials (**Figure 6a-d**) [7], respectively. Furthermore, DMLG interconnects provide 100-fold higher current-carrying capacity with respect to conventional metals, making them an ideal material for next-generation interconnect technology. While the above-mentioned demonstration has opened a clear pathway for the integration of graphene/MLG in CMOS technologies, it is worth noting that the idea of DMLG was first proposed by NRL [13], followed by various other important technological innovations relevant to graphene/MLG interconnects. **Figure 7** provides a snapshot of the evolution of the key achievements in graphene/MLG interconnect technology at NRL including its robustness under high-current/electrostatic discharge (ESD), which is a major reliability issue [14].

While the reliability and performance of single-level MLG wires have been studied in detail, a key remaining requirement in the application of MLG as interconnects in today's semiconductor technologies is the demonstration of a multi-tier MLG wire/via system incorporating low-resistance contacts. This is crucial for demonstrating the benefit of MLG wires in contacting the transistors at the local level. The primary step for achieving this is to first grow high-quality MLG reliably on multiple levels. **Figure 8a-b** shows the demonstration of large-area multi-level graphene (separated by a 200nm ILD) using the CMOS-compatible growth technique. Almost identical characteristics as compared to the bottom MLG are also observed for the top MLG, as evidenced by the various structural and optical characterizations for both top and bottom levels (**Figure 8a-b**). The layered structures at both the top and bottom levels confirm the versatility of the growth technique for arbitrary surface topologies. Because of the difficulty of graphene/MLG to be grown vertically in trenches, we employed the age-old subtractive etching (SE) technique, which was initially used for Al interconnects, to join multi-level MLG interconnects with metal vias in an edge-configuration [10], which is the preferred method of contacting MLG while simultaneously minimizing the additional contact resistance. Rigorous scaling analyses indicate that the increase in the total via resistance in the case of the MLG/metal-via multi-level structure is more than compensated by the reduced MLG wire resistance (for a fixed AR = 2), resulting in ~2-fold improvement in the overall circuit performance at sub-10nm critical dimensions.

It is worth observing that the CMOS-compatible growth process can be extended to grow MLG on arbitrary substrates if the growth conditions do not result in the thermal degradation of the substrate [10]. Because of the inability of the conventional barrier/capping layer materials (TaN/Si_3N_4) to be scaled down below ~0.5nm (as it could otherwise lead to the diffusion of Cu into the surrounding dielectric), graphene-based capping to conventional metal

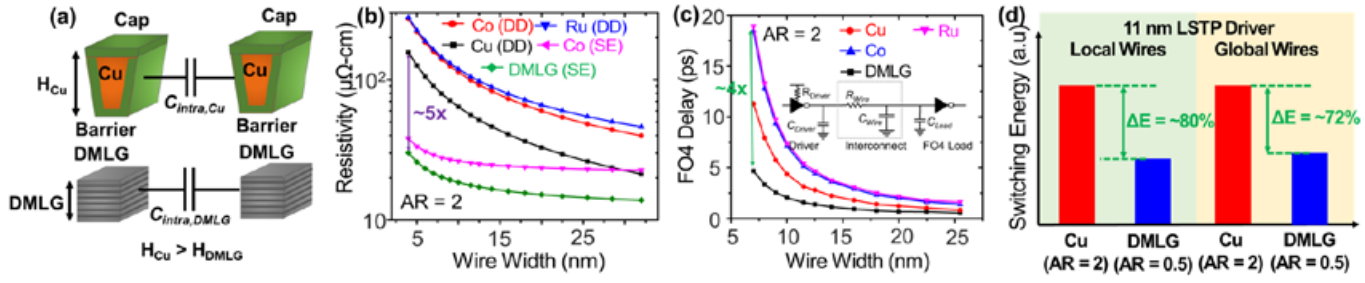


Figure 6: Performance analyses of CMOS-compatible single-level MLG interconnects: a) Schematic of two parallel copper wires of thickness H_{Cu} with barrier layer, in comparison with two adjacent doped-MLG wires, with a height of H_{DMLG}; significant reduction in intra-layer parasitic capacitance can be obtained for DMLG wires, as compared to copper ($C_{intra,Cu}$>>$C_{intra,DMLG}$). b) Resistivity vs. wire width for conventional metal interconnects in comparison with DMLG. c) Delay for a unit-sized inverter driving a FO4 load via 100x minimum gate pitch local interconnects, as a function of wire width. d) Switching energy comparison between Cu and DMLG interconnects connecting 11nm multi-gate LSTP driver, showing ~80%/72% benefits in energy savings for local/global wires, respectively, assuming the same delay penalty of ~5% for both local/global wires. A power-optimal repeater insertion methodology [12] has been assumed for global wire simulations.

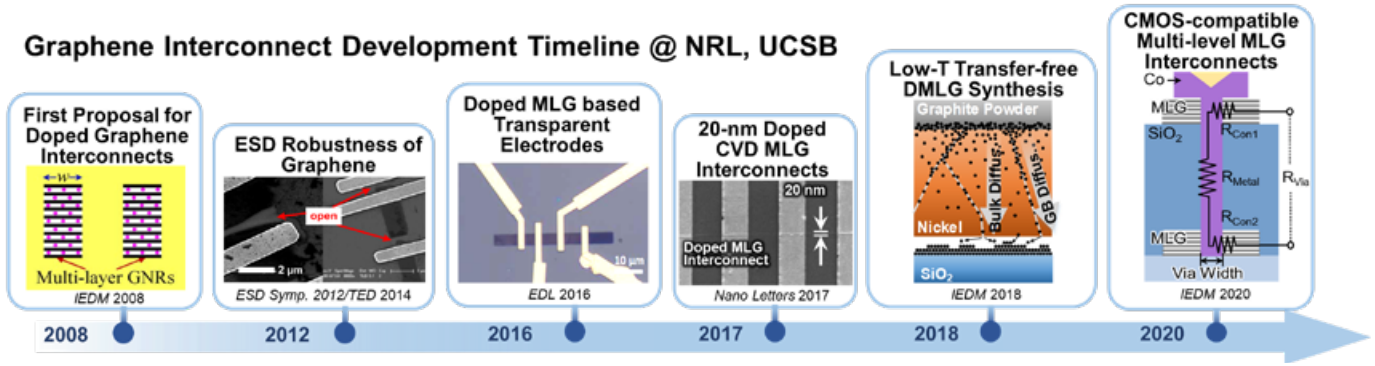


Figure 7: Graphene interconnect technology development timeline at NRL, UCSB: Evolution of graphene as an interconnect technology from the first proposal of doped graphene interconnects in 2008 to the demonstration of CMOS-compatible multi-level graphene interconnects in 2020.

interconnects is being actively evaluated, and has been demonstrated to reduce overall resistance by 15% [15]. With that in mind, NRL recently demonstrated BEOL-compatible growth of high-quality MLG directly on Cu by inserting ~2nm amorphous carbon layer between Ni and Cu [10]. In principle, with a smart choice of the overall growth conditions, and a thorough knowledge of the relative diffusion coefficients of carbon in the growth catalyst and growth substrate, this technique can be engineered to grow MLG on various metallic (Co, Ru, W, Pt, etc.) and dielectric surface topologies. Moreover, the current wafer coverage of ~10mm^2 can be expanded to directly grow high-quality MLG on 300mm industry standard wafers, making this technique extremely versatile and industry friendly.

Intercalated MLG inductors overcome a 200-year-old limit

On-chip inductors are essential components in almost all modern electronic gadgets such as smartphones and computers and can occupy up to 50% of the total chip area. However, unlike all other IC components that shrink with each technology node, inductors are hard to scale down as they solely rely on their magnetic inductance (**Figure 9a**). Therefore, the design of inductors has remained basically unchanged since their invention almost two centuries ago. NRL at UCSB overcame this fundamental scaling challenge by evoking sizable "kinetic inductance (KI)" (**Figure 9b**) in intercalation-doped MLG inductors at room temperature, leading to materials with the highest inductance densities ever created [9]. In contrast to conventional magnetic inductance, kinetic inductance arises from the intrinsic inertia of the charge carriers and appears in series with magnetic inductance, hence increasing the overall inductance for a given inductor footprint (**Figure 9b**). Intercalation

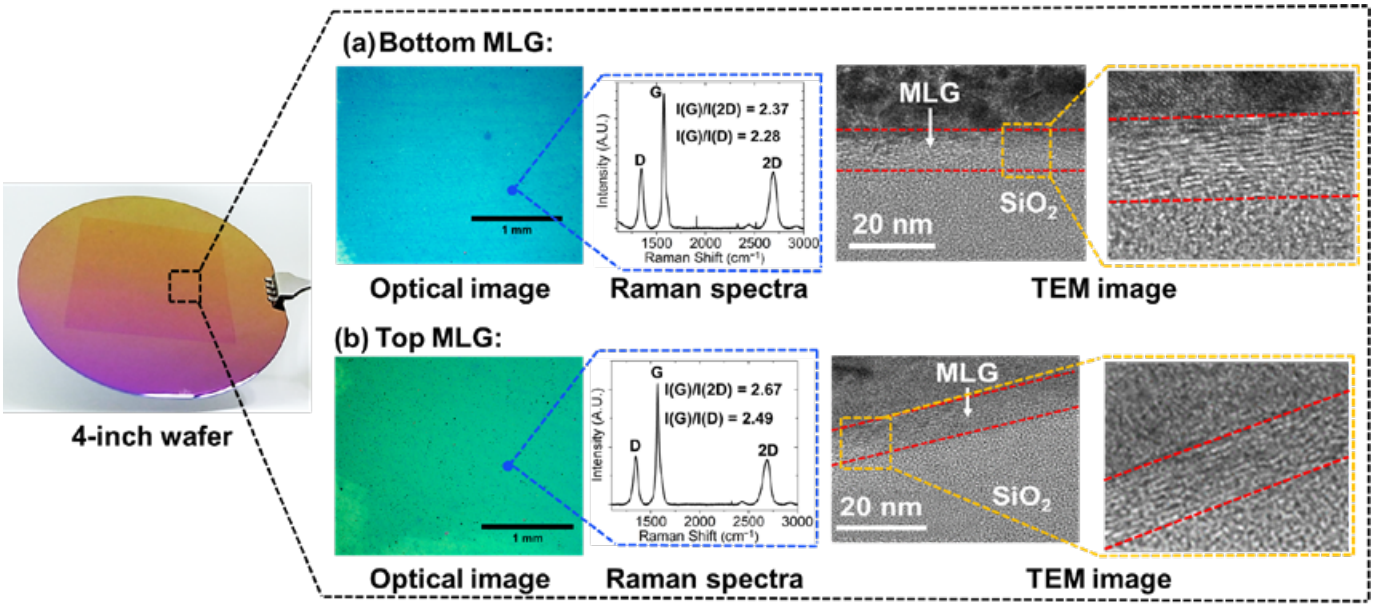


Figure 8: CMOS-compatible multi-level MLG interconnects (separated by 200nm ILD) grown on a 4-inch silicon wafer. a) Optical image of a large-area MLG (bottom level) grown using the solid-phase growth technique. The sharp G and 2D peaks in the single-point Raman spectrum confirm the uniform high-quality growth. Cross-sectional transmission electron microscope (TEM) images clearly show the layered structure of graphene, once again confirming the high growth quality. b) Similar to the bottom-level, the top MLG (optical image) is fabricated under the same conditions and exhibits almost comparable quality and thickness, as evidenced from the large area optical image, single-point Raman spectra and cross-sectional TEM image. The electrical properties of the bottom MLG before and after the fabrication of the top MLG (and Co-via) yielded nearly identical resistances.

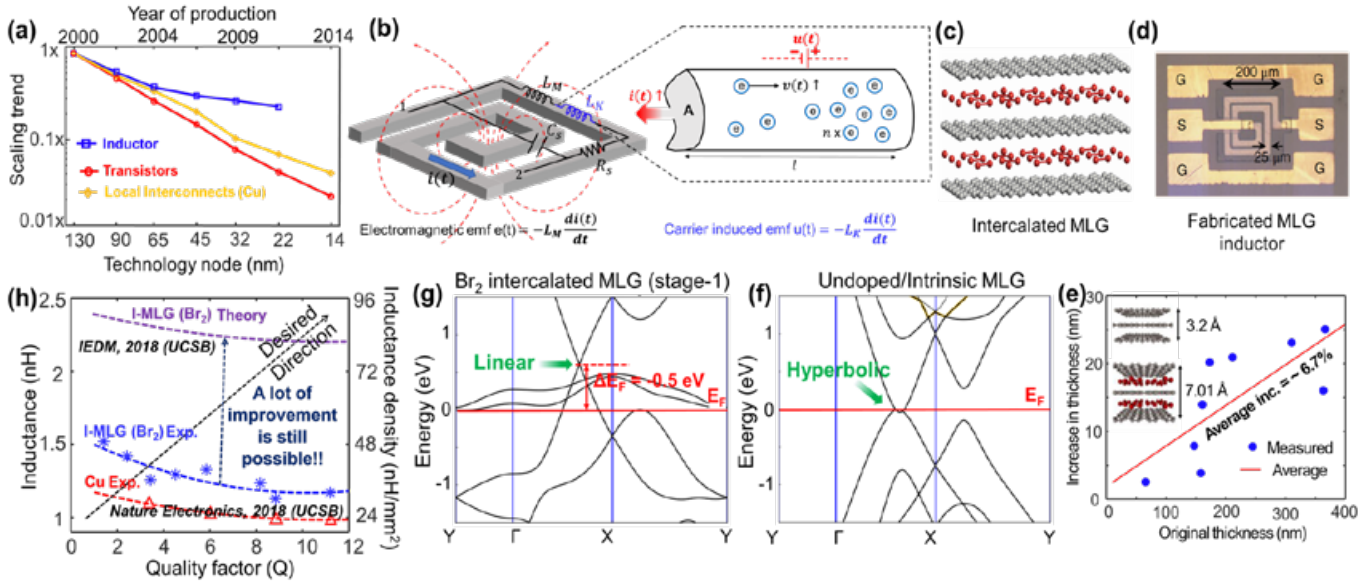


Figure 9: High-performance intercalation-doped MLG inductors exhibiting kinetic inductance: a) Comparison of scaling trends: required area of a typical on-chip inductor vs. area of a single logic transistor (= gate pitch × metal pitch) and width of M1 interconnect. All the data were normalized with respect to the 130nm node. b) Schematic showing the difference between the conventional magnetic and kinetic inductance. c) Schematic of an intercalation-doped MLG. Intercalation doping introduces foreign atoms (Br_2) between the layers of MLG. d) Optical image of a Br_2 intercalation-doped MLG inductor. e) Thickness increment after doping for MLG ribbons with various initial thicknesses. f) Hyperbolic band structure of intrinsic/undoped MLG. g) Linear band structure of intercalation-doped MLG showing the doping effect, as evident from the shift in the fermi level. h) Inductance and corresponding inductance density versus quality factor for the spiral square inductor fabricated in (d).

doping provides high Q-factors of up to 12, while the KI increases the total inductance-density by ~1.5-fold and thereby allows inductor scaling for the very first time. This development is crucial for the Internet of Things (IoT) industry and has been justifiably touted as a "trillion-dollar breakthrough" by Forbes magazine [16] (**Figure 9b-g**). Intercalation doping essentially increases layer separation in MLG that leads to recovery of the linear band structure of monolayer graphene, which possesses the highest KI (**Figure 9e-g**). Further process and doping optimization can provide up to 10-fold higher inductance densities [17] and pave the way for next-generation IoT and wireless applications (**Figure 9h**).

Wafer-scale integration and manufacturing challenges for graphene

One of the main challenges for the large-scale integration of MLG/DMLG into CMOS processes is the absence of a wafer-scale MLG growth tool satisfying the BEOL thermal budget and process requirements. The graphene synthesis technology pioneered by NRL presents a comprehensive solution to the various challenges of integrating MLG into large-scale manufacturing of not only interconnects and inductors, but also graphene-based transparent electrodes [14,18], RFIDs and solar cells (**Figure 10a**), and therefore, warrants the need for more sophisticated temperature and pressure controllers to precisely deposit a desired thickness of graphene/MLG on a given substrate over a large area.

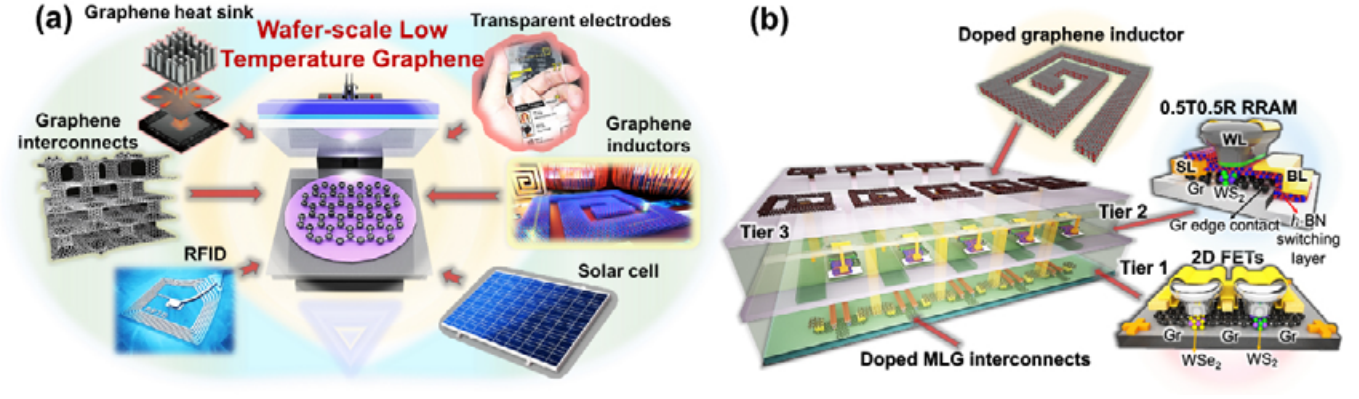


Figure 10: Applications of MLG in electronics: a) Schematic illustrating the various applications where the wafer-scale low-temperature graphene growth developed by UCSB NRL can be utilized. b) Schematic showing the prospects of monolithic 3D integration using 2D materials, where each tier consists of an active layer, a BEOL layer and an ILD. At the first level, 2D field-effect transistors (FETs) are connected via graphene (Gr) and DMLG interconnects and inter-tier metal vias are used for establishing connection between the two tiers. The second tier consists of the recently demonstrated 0.5T-0.5R RRAM cells, which are connected by DMLG interconnects. The top tier consists of doped MLG inductors, which are connected to both the bottom tiers 1 and 2 using monolithic inter-tier vias.

Apart from conventional transistor and interconnect scaling, the massive computing requirements for future generations necessitate the need for alternative architectures. One such approach is 3D integration, or the sequential stacking of chips—including front-end-of-line (FEOL) and BEOL materials, devices, and interconnects in the vertical direction, which can not only reduce the interconnect delay, but also improve the bandwidth and energy-efficiency of the entire chip. Various approaches such as through-silicon via (TSV), flip-chip or wire bonding, have been used for interconnecting multiple levels in a 3D-IC for a long time. However, their large parasitic capacitances and severe electrical, thermal, mechanical reliability, and adhesion challenges, as well as increasing costs and complexity with each generation, severely restrict their use for future technology nodes. Monolithic-3D (M3D) integration is another type of 3D integration scheme, where multiple stacked tiers are fabricated sequentially on the same wafer via deposition/recrystallization of the upper tiers (**Figure 10b**).

Theoretical studies have demonstrated that graphene-based interconnects, inductors, and shielding layers in conjunction with 2D semiconductor material-based transistors can improve the integration density by more than 10-fold when compared to TSV-based 3D integration density, and by more than 1.5-fold when compared to conventional monolithic 3D integration [19]. Additionally, the integration of logic and memory levels (**Figure 10b**) using M3D integration can alleviate the memory wall problem for today's computing architecture, paving the way for high-speed data transfer and computation. Consider, for example, the recently demonstrated 0.5T0.5R ultra-compact hybrid memory cell that reduces the device count by half for the very first time in resistive random-access memory (RRAM) technology history. It also simultaneously allows for higher lateral and vertical (3D) integration density with respect to the conventional 1T1R architecture, and can be monolithically 3D-stacked to build the ultimate high-density nonvolatile memory arrays and neuromorphic/in-memory computing systems, with significantly higher vertical density than the conventional 1T1R architecture (with RRAM on top of the transistor). These attributes enable unprecedented performance and energy-efficiency to emulate the workings of the human brain in the near future [20]. Therefore, effective methods for the seamless integration of graphene/MLG, and/or other 2D materials with mainstream CMOS could lead to revolutionary new devices, circuits, and beyond-Moore architectures to fuel next-generation electronics.

Summary

BEOL passive devices including metal interconnects and inductors are facing fundamental scaling limitations that threaten to derail Moore's Law. Pioneering inventions led by Professor Kaustav Banerjee at UC Santa Barbara have revealed that judiciously engineered

graphene, and synthesized in a CMOS-compatible manner, can not only help overcome such major bottlenecks in CMOS technologies, but also bring unprecedented energy-efficiency and performance gain in next-generation IC products. Thereby, these inventions have established a revolutionary new BEOL technology platform for future ICs and paved the way for graphene's entry into mainstream electronics.

Acknowledgement

The research summarized in this article was conducted in the Nanoelectronics Research Lab at UC Santa Barbara and was supported over the years by the DoD (AFOSR and ARO), DoE, NIST, NSF, and SRC.

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