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Volume 26, Number 2

March • April 2022

Large-size multi-layered FO RDL MCM packaging
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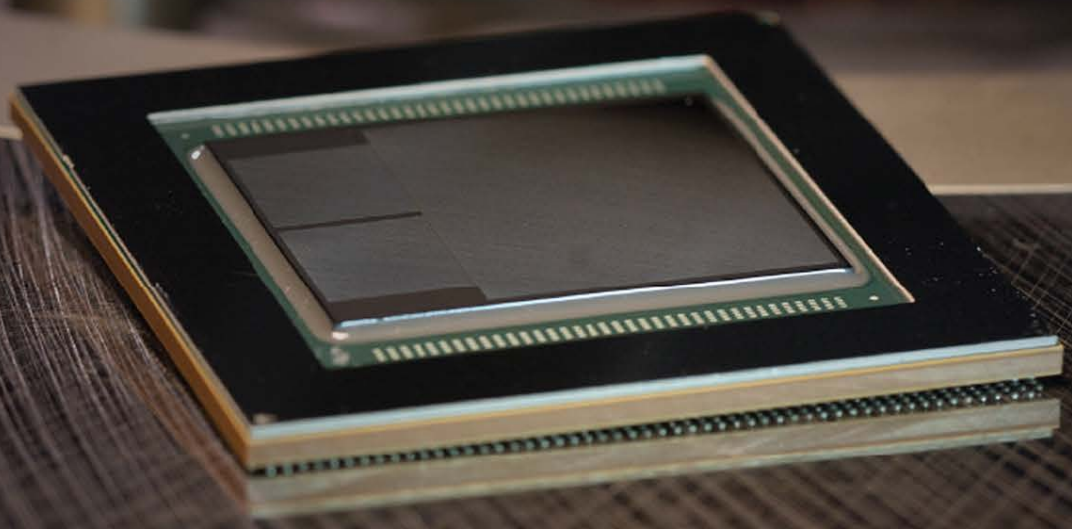

- Embedded chip packaging
- A new and historic packaging era
- Enabling low-profile LSCs for automotive flip-chip packaging
- Heterogeneous integration for AI applications: status and future needs
- Wafer-level polymer/metal hybrid bonding using a photosensitive permanent bonding material

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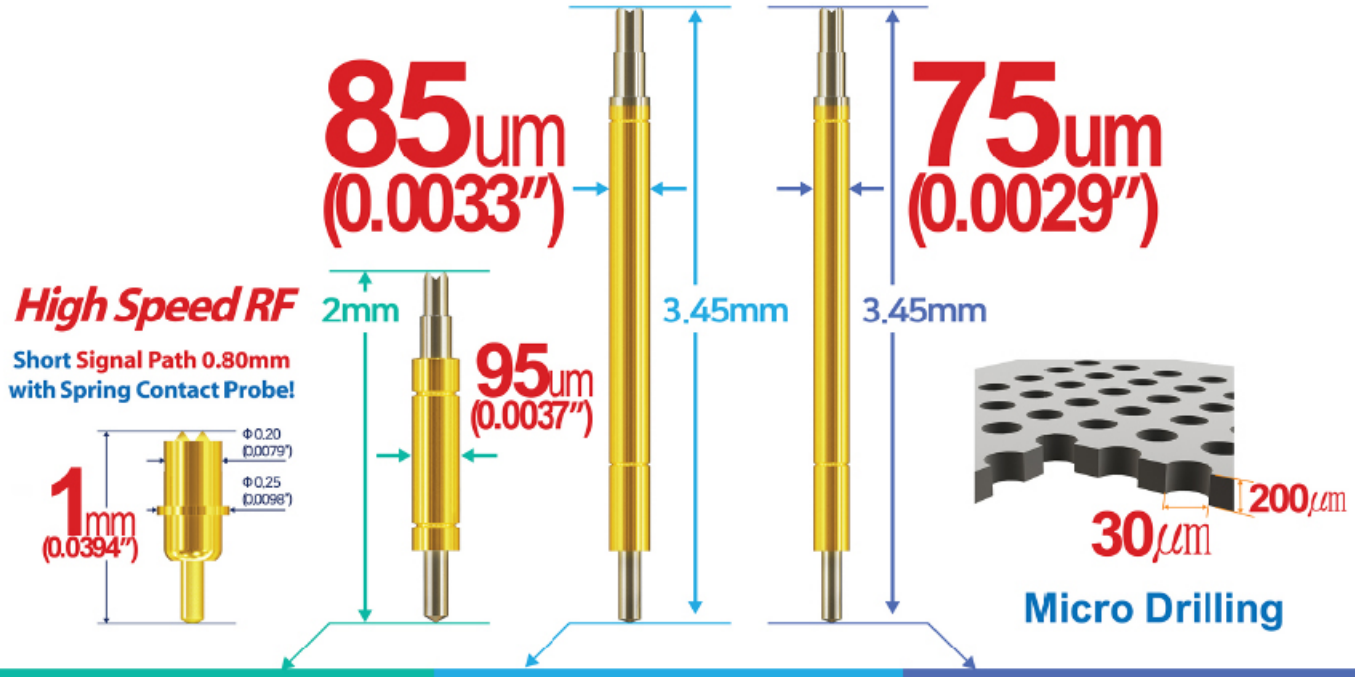


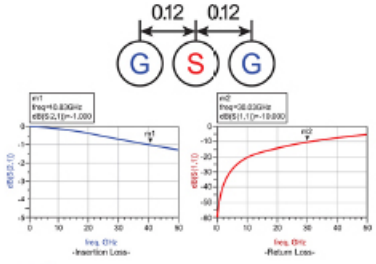
120㎛ Pitch

Mechanical Spec.

- Spring Force : 0.281oz (8.0g) @ .0098 (0.25mm)
- Recommended Travel : .0098 (0.25mm)
- Full Travel : .0118 (0.30mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation Data)

- Current Rating : 1.0A
- Propagation Delay : 20.80ps
- Capacitance : 0.21pF
- Inductance : 0.38nH
- Insertion Loss : 40.83GHz @ -1.000dB
- Return Loss : 30.03GHz @ -10.000dB
  (Dielectric material : CERAMIC)



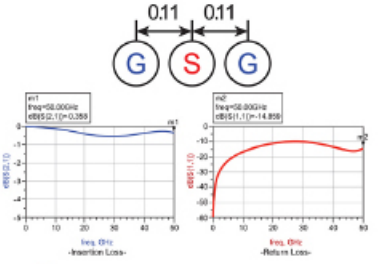
110㎛ Pitch

Mechanical Spec.

- Spring Force : 0.212oz (6.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation Data)

- Current Rating : 0.9A
- Propagation Delay : 38.25ps
- Capacitance : 0.47pF
- Inductance : 0.63nH
- Insertion Loss : > 50.00GHz @ -1.000dB
- Return Loss : > 50.00GHz @ -10.000dB
  (Dielectric material : CERAMIC)



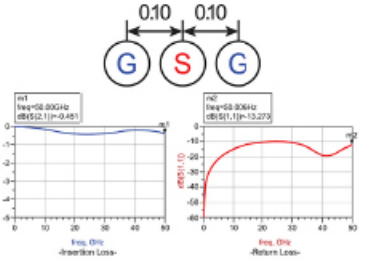
100㎛ Pitch

Mechanical Spec.

- Spring Force : 0.247oz (7.0g) @ .0118 (0.30mm)
- Recommended Travel : .0118 (0.30mm)
- Full Travel : .0138 (0.35mm)
- Material : Terminal – Pd Alloy / No plated
  Plunger – Pd Alloy / No plated
  Barrel – Ni-Au Alloy / Au plated
  Spring – Music Wire / Au plated

Electrical Spec. (Simulation Data)

- Current Rating : 0.8A
- Propagation Delay : 35.55ps
- Capacitance : 0.44pF
- Inductance : 0.66nH
- Insertion Loss : > 50.00GHz @ -1.000dB
- Return Loss : > 50.00GHz @ -10.000dB
  (Dielectric material : CERAMIC)



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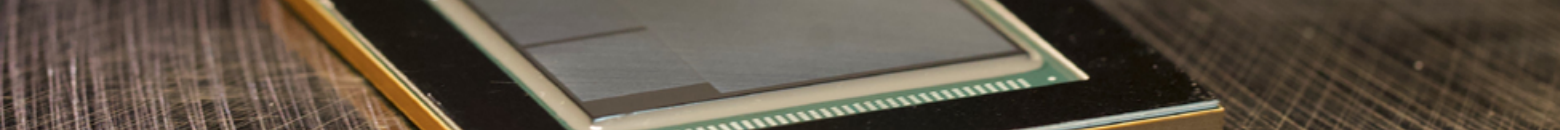

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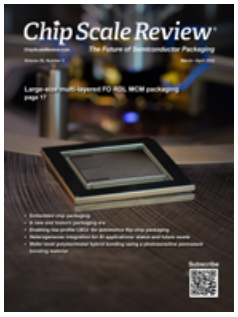

The chip shown in the picture is a fan-out multi-chip module (FO-MCM). It's an example of heterogeneous integration fabrication with optimized 2/2µm line/spacing, multi-layers of redistribution layers (RDLs) and chip-last technology to supply interconnects between die to die and die to high-bandwidth memories. This becomes a potential platform for applications such as HPC, AI accelerator and cloud computing. Scalable routing capability makes this type of package competitive with respect to one using a conventional silicon interposer.

Cover image courtesy of SPIL

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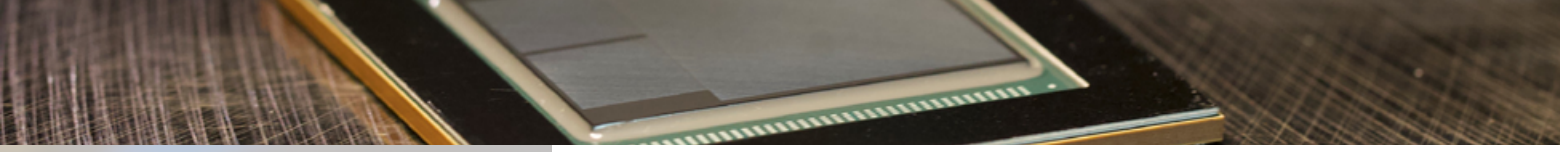

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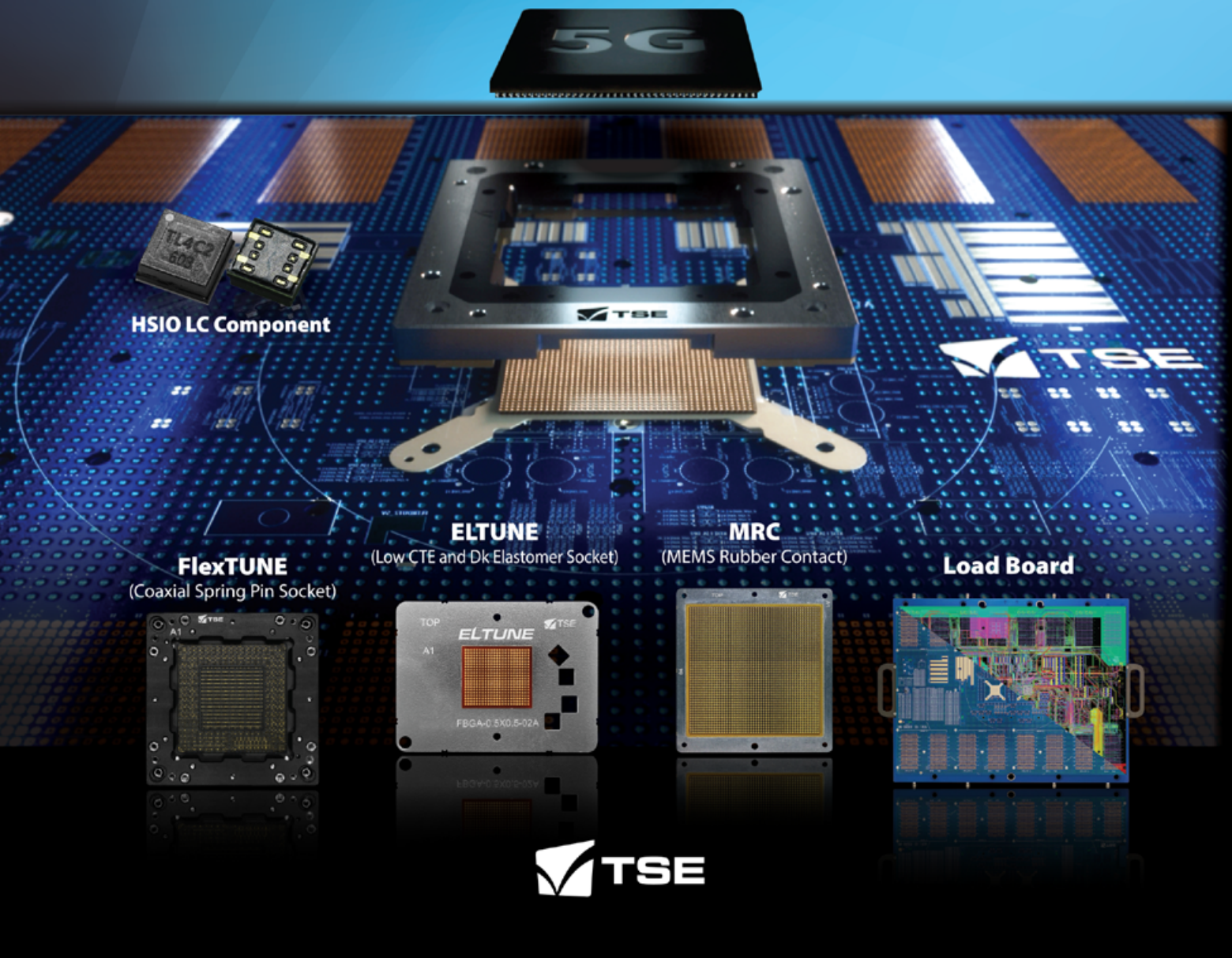

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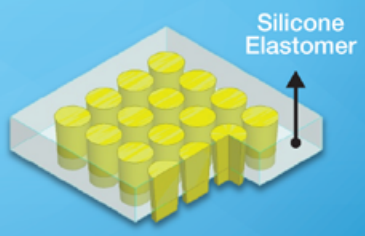
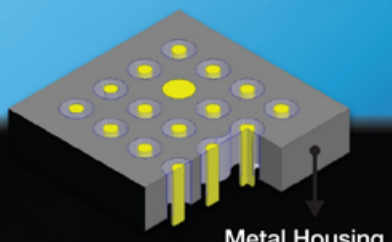
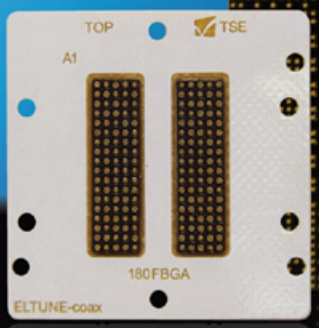


Conventional Elastomer Socket



ELTUNE-coax



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Test height	3.50	0.60	0.60

• Electrical Specification

(unit: GHz)

42.5Ω, 0.80mm pitch		Spring Pin	Elastomer	ELTUNE-coax
Insertion Loss S_{21} @-1dB	Single Ended (G-S-G)	13.93	27.81	>100
	Differential (G-S-S-G)	25.39	28.94	>100
Return Loss S_{11} @-10dB	Single Ended (G-S-G)	10.98	15.89	>100
	Differential (G-S-S-G)	20.77	25.20	48.21
Crosstalk S_{21} @-20dB	G-S-S-G	8.50	9.43	>100

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A new and historic packaging era

By Rao Tummala, Madhavan Swaminathan, Pratik Nimbalkar [Georgia Institute of Technology]

A new, historic, and transformative packaging era has begun starting with high-performance computing electronics. This transformation is due to many reasons that include the transistor speed slowing down from node to node, thereby contributing to slowdown in computing performance, and the increase in chip size along with an increase in the number of transistors to more than 50 billion with the concurrent increase in their cost. The slowdown in transistor speed is driving the development of new, non-traditional complementary metal-oxide semiconductor (CMOS) devices. But the need for faster computing speed requires more than transistors. Packaging or interconnections, therefore, became strategic, value-add and differentiators for many applications such as artificial intelligence (AI), cloud computing, virtual reality (VR), 5G and mm-wave communications, the Internet of Things (IoT) and self-driving cars. The industry focus, accordingly, began to shift from transistor scaling to system-on-chip (SoC), to system scaling and integration, to system-on-package (SoP). This is one historic transformation.

The second historic milestone has to do with packaging or interconnection developments. While wafer back-end-of-line (BEOL) packaging has always been below 1µm, package foundries always produced packages with much larger wiring—typically 10-20µm. The reason for this is the use of laminate or build-up organic packaging technologies, using low temperature and soft organic composite cores with layers of polymer redistribution layers (RDLs) on top of these to form high-density interconnections. These packages, however, offered the single largest benefit: the lower cost for large packages, produced from large organic panels. So, while wafer technologies produced the highest inputs and outputs (IOs) at a high cost, the panel laminate packages produced lower IOs at a lower cost. What is needed, therefore, is a panel technology that addresses both. This is the reason for the development of inorganic panel packages such as glass panel packaging, which has started a historic era of panel packaging reaching wafer BEOL IO density starting at 1µm lithography. Asian and American companies are gearing up to manufacture these latest panels starting in 2022. This is the third historic development. The fourth historic development is IC assembly pitch that, for the first time is below 10µm using direct Cu-to-Cu or hybrid bonding, replacing solder. This article describes these historic packaging developments in more detail.

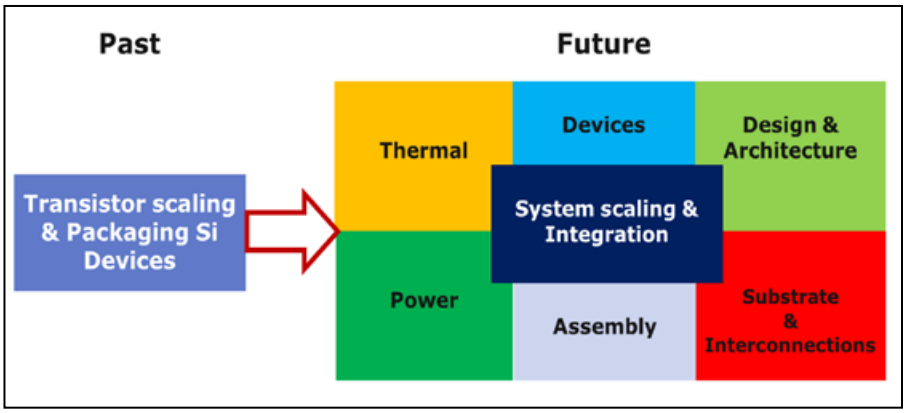

Figure 1: Transistor scaling and packaging Si in the past vs. packaging a system with system scaling and integration.

System-scaling and integration as the new frontier

In the past five decades, the number of transistors on an integrated circuit (IC) has increased exponentially, following Moore's Law—reaching tens of billions of transistors on a single chip. The current maximum transistor count is 57 billion metal-oxide field-effect transistors (MOSFETs) on the M1 Max SoC by Apple [1]. However, as transistor speed slows down from node to node and computing systems demand higher and higher performances, packaging or interconnections are viewed as a potential solution. Computing applications drive workloads and workloads drive systems technologies that include all the devices, interconnections, power and thermal components, assembly, and the integration of all these at the package level, leading to the system-on-package concept. **Figure 1** depicts this new system era in contrast to transistor scaling and packaging of Si devices era in the past.

Panel packaging reaching BEOL IO-density

The enormous increase in transistor count necessitates a proportional increase in IOs, which requires ultra-high density RDL wiring layers on the substrate. **Figure 2** shows how the wiring or IO pitch has evolved from package and wafer foundries. The mother of package foundry technologies has been laminated printed wiring boards, initially at more than 100µm. Over the years, this technology has

begun to be applied for package substrates using build-up polymer dielectrics, large-area photolithography and semi-additive processes, leading to about 10µm wiring widths, currently. Wafer–based BEOL packaging has always been below 1µm using dry processes for inorganic dielectrics and the dual-damascene processes. The lithography gap, as shown in **Figure 2**, has always existed between packaging or interconnections from wafer and package foundries. Over the last few years, package RDLs have made tremendous progress either in chip-first fan-out or chip-last substrate architectures. RDL IO densities have increased significantly faster in the last few years than in the previous few decades (**Figure 3**) for wafer and panel sizes. As shown in this figure, only wafer packages have been developed so far with RDL wiring at or below 1µm. These are developed either as fan-out packages or as silicon interposers. Package RDLs have scaled from 10µm a few years ago, to less than 5µm now. Mediatek and SPIL have fan-out packages at 5µm RDL [2,3]. Amkor (SWIFT®), ASE (FOCoS) and JCET have also developed 2µm RDLs for high-density fan-outs [4-6]. TSMC (InFO) and Amkor's Silicon-less Integrated Module (SLIM™) have demonstrated sub-micron RDL with 0.8µm dimensions for their respective fan-out platforms [7,8].

Silicon interposers such as TSMC's CoWoS®, or embedded bridges such as Intel's embedded multi-die interconnect bridge (EMIB), or TSMC's local Si interconnect (LSI), are more popular packages for high-performance computing with high-density RDLs smaller than 2µm up to 0.4µm [9-11]. All these packages are at the wafer-scale level. Panel-scale RDLs have also shown outstanding progress over the past few years. Organic packages from Semco, Kyocera, Cisco and Shinko are the leaders in panel packaging [12-15]. High-density panels approaching the wafer RDL wiring at or below 1µm have been the holy grail of the industry that has not been realized until now. The main limiting factor to panel RDL scaling has been the use of

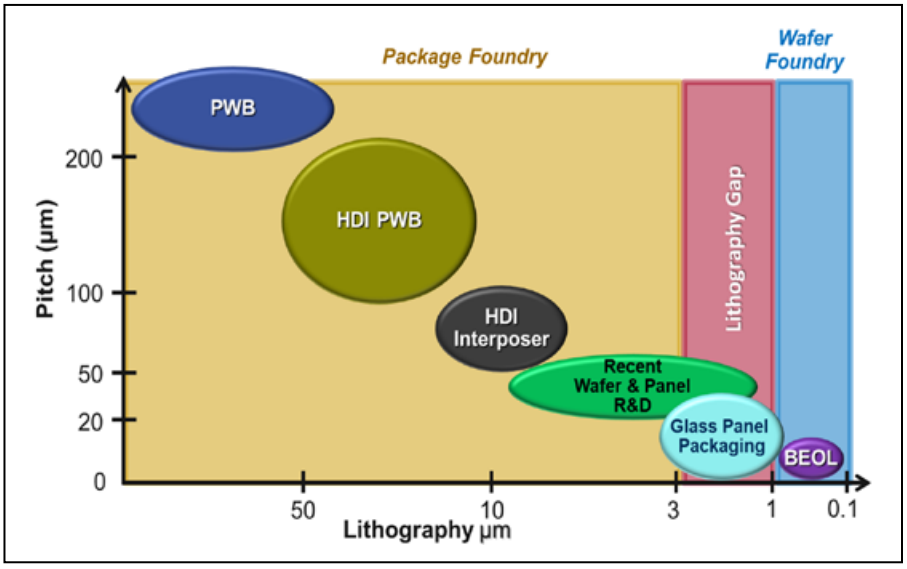

Figure 2: Package foundry bump pitch and lithography reaching Si wafer BEOL.

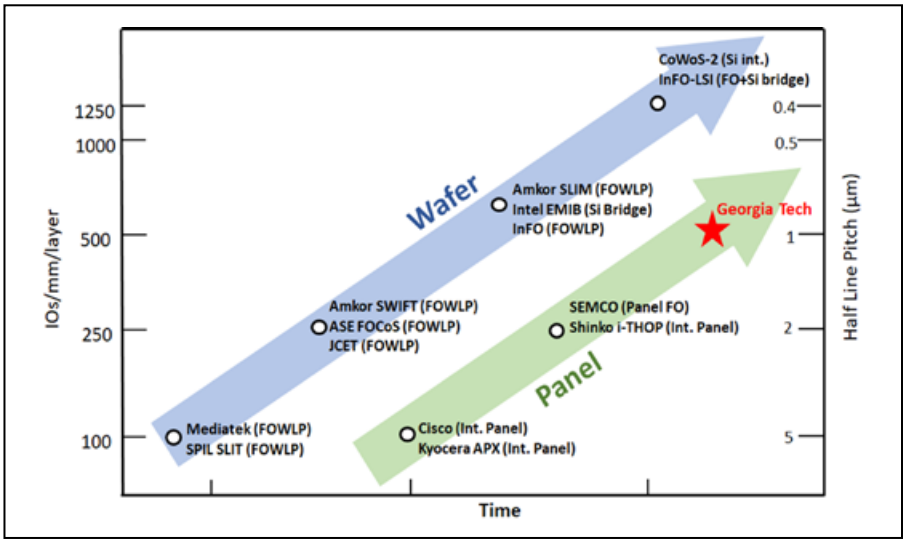

Figure 3: Evolution of wafer and panel package RDLs over time.

low modulus organic core substrates that are not dimensionally stable for 1µm lithography and warp during RDL fabrication and IC assembly. This is the reason for glass panel R&D activities at Georgia Tech. The advantages of glass are several: 1) a higher modulus; 2) a thermal coefficient of expansion (TCE) that is optimized for IC and board assembly; 3) ultra-low roughness and surface uniformity without having to grind and polish as with silicon interposers and therefore, results in lower warpage. Georgia Tech, with its global supply-chain manufacturers, has been developing the glass panel technology systematically for a decade starting with 5µm RDL in 2012. As shown in **Figure 3**, it has achieved a historic milestone of 1µm panel RDL overcoming many challenges in ultra-low-K dielectrics and their deposition, as well as overcoming challenges with large-area lithography and semi-additive and laser via processes to form 1µm lines and 2µm micro-vias. These advances led to the elimination of the lithography gap between wafers and panels, as shown in **Figure 2**.

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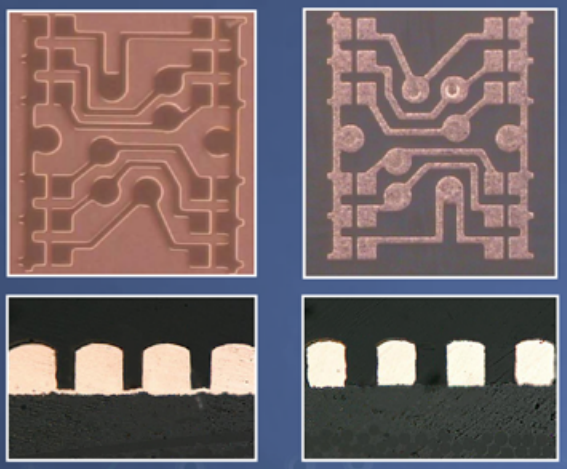

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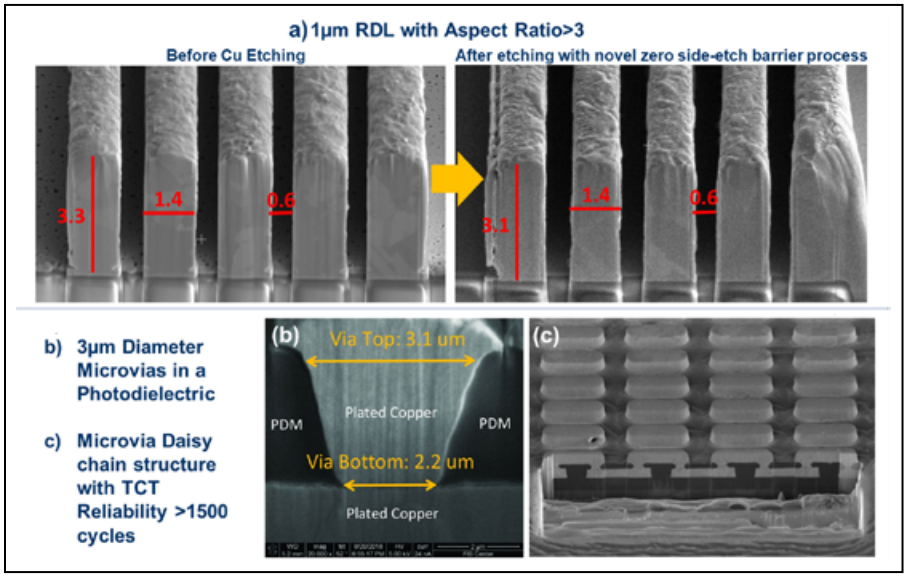

Figure 4: Recent advances at Georgia Tech enable high aspect ratio 1µm RDL on glass panels.

Glass panel reaches 1µm RDL

Georgia Tech began to pioneer glass packaging in 2010. The effort began by setting up panel facilities for substrates and assembly and forming partnerships with global supply chain companies for materials and tools. These activities, pursued systematically over a decade, led to a historic milestone of 1µm RDL in 2021. **Figure 4** shows the high aspect ratio of 1.4µm Cu traces with 3.3µm height resulting in lower resistance. This is an outstanding achievement in two ways. For the first time, industry reached 1µm RDL on a panel. Such an RDL also solves the problem with wafer-based RDLs having higher resistances. This solution was made possible by advances in advanced positive-tone dry-film photoresists, large-area lithography tools with high depth-of-focus, and advanced seed-layer etching. With a novel zero-side etch process that Georgia Tech team demonstrated, Cu line etching with zero changes in RDL dimensions was achieved for the first time, as shown in **Figure 4a**. This etching process allows one to potentially scale RDLs below 1µm to 0.1µm using the advanced semi-additive process (SAP) that was recently invented. Micro-vias with diameters <3µm (**Figures 4b** and **c**) have also been demonstrated using advanced photo-dielectrics along with their thermal cycling reliability [16], thereby enabling the entire stack of 1µm multi-layer RDL. Research is currently ongoing at Georgia Tech to further scale RDL dimensions below 1µm using advances in SAP on glass panels. Simultaneously, glass panel packaging is also gaining momentum in the industry with Asian and American companies gearing up to manufacture these latest panels, starting in 2022.

IC assembly reaches 10µm pitch

The need for smaller bump pitch has led to continual progress in chip bonding and assembly technologies as shown in **Figure 5**. In the early years of packaging – since the 1960s – wire bonding provided the needed interconnections. As the number of transistors grew on the chip, flip-chip technology was developed by IBM as an area array assembly technology, initially at >200µm pitch, and more recently to 100µm. As solder bridging began to occur between solder bumps below 100µm, copper pillar with solder cap technology was developed by APS in Singapore. This technology is further miniaturized, and thermocompression-bonded, leading to the so called "micro-bumps" at about 40µm pitch.

There are many R&D activities currently ongoing to reduce the assembly pitch to 10µm by improving materials, processes, and tools.

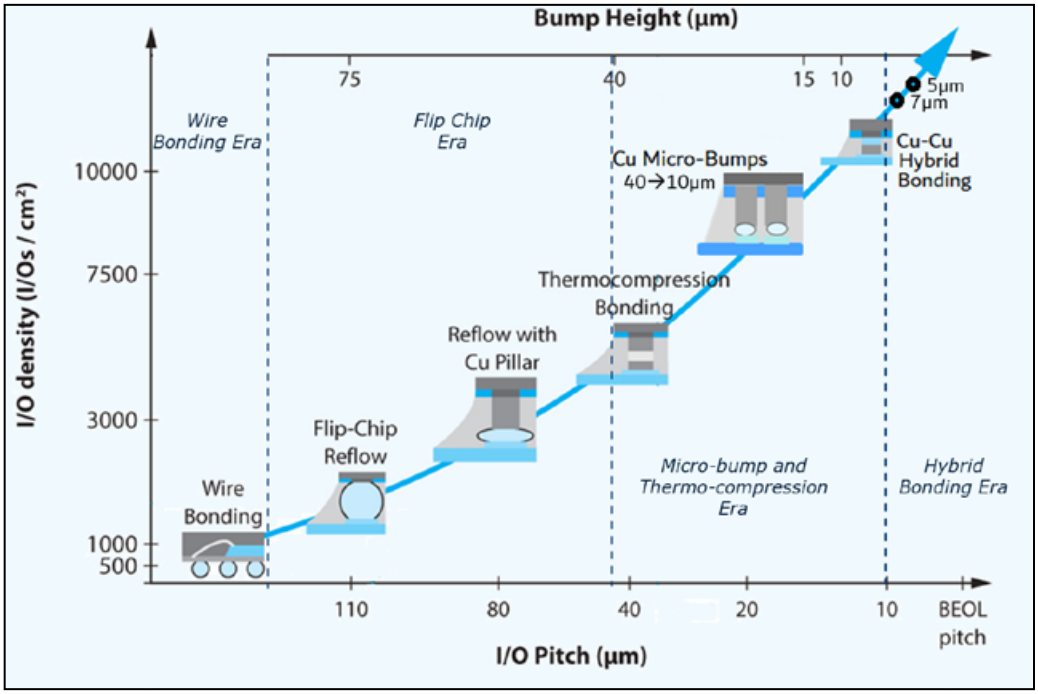

Figure 5: Evolution of chip-level assembly technologies.

This may be the end of solder-based assembly. Direct bonding of copper to copper has been pursued for more than a decade using advanced thermocompression bonding technologies. While the progress has been outstanding, these assembly technologies tend to be slow and difficult for high-volume production. It is because of this reason that hybrid bonding became a very popular technology, originally invented by Ziptronix about 15 years ago, and currently licensed to Xperi. Both TSMC and Intel are pursuing this technology very aggressively showing plans for 10µm pitch in the short term, and 1µm pitch within a decade. Simultaneously, tool makers like Applied Materials are developing the necessary production tools.

Summary

In summary, a historic shift from transistor scaling to system scaling and integration has begun, leading to many other shifts such as glass panel packaging, reaching 1µm lithography, and IC assembly reaching 1µm pitch within a decade—two historical milestones. The current panel technology is based on laminate or build-up organic technology, which has been known to be incapable of 1µm lithography. In parallel, IC assembly is being advanced with micro-bumps to 10µm pitch in the short term, and later, towards a 1µm pitch using direct Cu-Cu bonding (also known as hybrid bonding) to replace solder.

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Biographies

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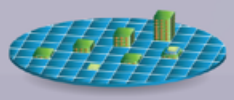

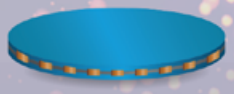

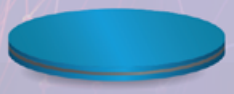

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Operating in the eye of the COVID-19 storm

By Asif R. Chowdhury [UTAC Group]

In these past 18 months or so, the semiconductor sector has been put to the test by unprecedented supply constraints and logistical disruption. This has been across the supply chain spectrum — from material shortages, to material cost increases, to significant increases in new equipment cycle time — all resulting in historic component shortages. Some industries, such as automotive, have suffered, and continue to suffer, the worst. The COVID-19 pandemic has meant that long-established methods of working are no longer applicable and need to be adapted accordingly. We are constantly looking at innovative ways to navigate through this crisis so that we can service all our customers' demands.

Further complicating the challenges noted above are the higher demands for semiconductor products that came about because of the pandemic, thereby placing the semiconductor manufacturing industry under extreme pressure. To meet this demand, we have been running at full capacity and managed to achieve an impressive 70% growth during 2021. In addition, for the first time in its history, the company reached the milestone of US$1Bn in revenue in the third quarter of 2021.

The pandemic has also reinforced the importance of the well-being of our employees to the success of our company. At UTAC, we are taking this responsibility very seriously by making certain that our staff are safe and healthy. We continue to invest in employees by creating a safe environment that is conducive to business.

By observing strict guidelines about how members of our staff interact with one another, we have been able to work in a safe environment. The implementation of a system of safe management measures through the assignment of safety officers has proved itself to be highly effective. The use of safety officers has provided the necessary structure for continued safe operation across the entire business—taking care of the workplace, the employees located there, and tending to the needs of those who become unwell. To enhance safety, new technology and processes have been installed at all UTAC facilities. These include thermal temperature scanning terminals (TTSTs), along with a regular antigen rapid test (ART) program. Safe distancing measures are implemented throughout each site, with check-in and check-out systems installed at all access points.

Some measures have included, where possible, letting a sizable portion of employees conduct their work from home. We have supplied them with the necessary IT support to enable this to be done, so that there has been no unwanted impact on the smooth running of the business. In most cases, meetings have been carried out via online conference platforms.

We have also implemented a complete range of measures that rigorously follow official COVID-19 guidelines. By doing so, we have been able to maintain continued operations at our sites across Asia—in Singapore, Malaysia, Indonesia, Thailand, and China. Despite all the precautions, some of our facilities, unfortunately, had to face dealing with the pandemic. But because of our stringent mitigation plan, we have been able to recover in a short period of time. Where possible, we have been actively working with local governments and the private sector to provide free COVID vaccinations to our employees This has meant that business continuity has been upheld, and we are now reaping the rewards.

Although it may be too early to see the full impact of the COVID-19 crisis

Figure 1: UTAC smart factory summary.

on long-term trends, projections from leading market analysts, such as Gartner, WSTS and IC Insights, all anticipate double-digit year-on-year (YoY) growth to be experienced in both 2021 and 2022. The momentum surge in 5G mobile connectivity, artificial intelligence (AI), virtual reality (VR), data and cloud computing servers, plus advances in industrial and automotive technologies, all seem certain to continue.

To take advantage of these trends there will be a need to continue increasing the degrees of automation incorporated into our test and assembly operations. Figure 1 shows a summary of UTAC's automation project, which utilizes key technologies such as robotics, artificial intelligence, augmented reality (AR)/VR technology and application specific softwares. Almost 100% of assembly and test for automotive products are utilizing these automation technologies. These technologies, combined with a highly trained and up-skilled local workforce, along with continued access to a robust supply chain, have improved overall factory productivity and efficiency. We have invested in state-of-the-art industry 4.0 Internet of Things (IoT) devices and robotic systems, as well as leveraged the latest AI technology, in order to increase the levels of automation at our facilities. Figure 2 shows the increase of overall CapEx spent by UTAC in the last three years as a percentage of revenue, which includes CapEx spent for factory automation. These expenditures have resulted in heightened machine efficiencies, greater throughput, improved cycle time, reduced cost and most importantly, improved quality. All these initiatives have significantly enhanced our quality, which is currently in the low single-digit parts-per-billion (PPB) with automotive products at a high single-digit PPB level.

Though business conditions are starting to improve, it would be unwise for our industry to assume that we are now fully through the storm. There may yet be further problems ahead. All the indicators and forecasts-to-date suggest that 2022 should be a good year for the semiconductor industry, with demand driving strong revenue growth. But it is too early to tell. If indeed demand

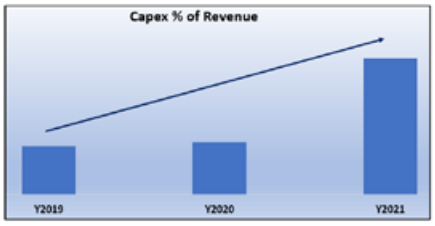

Figure 2: CapEx spent by UTAC as a percentage of revenue.

remains strong, it will be of paramount importance that we remain vigilant, and mitigate any remaining threat posed by COVID-19. If demand starts to weaken, which, invariably it will at some point due to the cyclic nature of the semiconductor market, that will add another layer of complexity with which to be reckoned.

Despite all the challenges that the pandemic has presented, and the repercussions that we are facing in its aftermath, UTAC is in a very strong position moving forward. At the same time, we are vigilant and looking at all options to ensure our future success.

Acknowledgment

This article originally appeared in the *SSIA VOICE* magazine and was updated and edited for *Chip Scale Review*.

Biography

Asif R. Chowdhury is SVP at UTAC Group, Singapore. He has over 30 years of experience in the semiconductor industry. Before joining UTAC, he held senior positions at Amkor Technology, Chandler, AZ, and Analog Devices, Wilmington, MA. He holds a BS in Mechanical Engineering from U. of Texas at Arlington, an MS in Mechanical Engineering from Southern Methodist U., and an MS in Finance and an MBA from Northeastern U. Email asif_chowdhury@utacgroup.com

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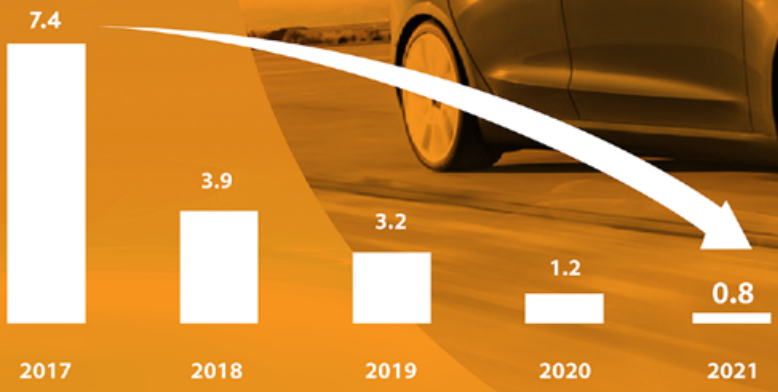

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ECTC 2022 will bring key technologists/ scientists together – in-person!

By Karlheinz Bock, TU Dresden, 72nd ECTC Program Chair

On behalf of the Program and Executive Committees, it is my pleasure to invite you to IEEE's 72nd Electronic Components and Technology Conference (ECTC). We are very excited about the ECTC 2022 program and welcome our colleagues from all over the world to join us. The 72nd edition of ECTC, sponsored by IEEE/EPS, will take place in San Diego, CA, U.S.A., from May 31-June 3, 2022.

Considered the premier electronic packaging conference of the industry, ECTC is continuing its tradition of bringing the latest developments in integrated circuit (IC) packaging, components, and microelectronic system technologies. This annual international conference brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses and foundries, outsourced semiconductor assembly and test (OSAT) service providers, substrate makers, equipment manufacturers, material suppliers, research institutions, and universities—all under one roof. ECTC typically attracts more than 1,500 attendees from over 25 countries. Last year's 71st ECTC, was held virtually on the Engagez platform of MCE because of the pandemic. The virtual conference had 1,380 attendees from more than 55 countries around the world with 350 video presentations featured in 46 technical and interactive presentation sessions. The virtual ECTC 2021 event also presented virtual exhibitions on the Engagez platform. Furthermore, 14 special sessions were organized with a broad spectrum of electronics packaging-related hot topics based on more than 50 invited expert presentations for the virtual ECTC 2021 event.

The 72nd ECTC in-person conference will continue with the same tradition of being the premium venue to showcase all the latest developments in the electronic components industry where packaging has become a way to achieve device and system performance scaling. More than 200 experts from broad ranging technical areas have put together an exceptional program consisting of more than 350 technical papers in 41 technical sessions, 14 Professional Development Courses and several panels, special sessions, and networking opportunities. The conference will address various important topics and industry trends, from mobile, 5G, medical wearables and automotive applications including autonomous driving, flexible and printed electronics, to high-speed communications, wireless, LiFi, photonics, high-performance and quantum computing, and artificial intelligence (AI) hardware. The technical presentations and panel discussions will feature a wide range of packaging technologies, from wire bonding, wafer- and panel-level packaging, flip chip, 2.5D and 3D integration, to advanced substrates and interposers, embedded technologies, system in package and heterogeneous integration. New ideas, designs, characterizations, simulations and reliability studies will bring new perspectives and challenges with respect to materials and processing, integration, interconnections, assembly and manufacturing. More than 350 authors from over 25 countries have already submitted their abstracts and are now getting ready to submit their completed manuscripts. These submissions for the 72nd ECTC cover ongoing technology developments within established disciplines, or emerging topics of interest for our industry.

Chris Koopmans – Chief Operations Officer of Marvell – will deliver the invited keynote speech entitled, "Accelerating the power of data infrastructure with cloud-optimized silicon." The keynote will share insights into how data infrastructure is converging into the cloud, the emerging cloud-optimized silicon era, and the technology areas the industry must tackle to accelerate the power of data infrastructure with cloud-optimized silicon.

The in-person conference has been extended to 9 special sessions (see **Table 1**) with invited industry experts that will cover emerging technologies and applications as noted below.

Session #5 (IEEE EPS President's Panel) will address the "State-of-the-Art Heterogeneous Integrated Packaging Program - SHIP Projekt with DoD," and will be chaired by EPS president Kitty Pearsall (Boss Precision, Inc.) and Chris Riso (Booz Allan Hamilton).

Session #	Special Session Topics	Chair/Co-Chair/Moderator
1	ECTC Special Session - Micro-LED Display Technologies	Chukwudi Okoro (Corning, Inc.) and Benson Chan (Binghamton University)
2	ECTC Special Session - Selected Topics of IEEE EPS Heterointegration Road Map	Amr Helmy (Univ. of Toronto) and Tom Salmon (VP at SEMI)
3	ECTC Special Session - Meeting Next Generation Packaging Challenges: Chiplets to Co-Packaged Optics.	E. Jan Vardaman (TechSearch International, Inc.)
4	ECTC Special Session - How will IC substrate technology evolve to enable next generation Heterogeneous Integration schemes for high performance applications?	Kuldip Johal (Atotech Group) and Bora Baloglu (Amkor)
5	IEEE EPS President's Panel - State-of-the-Art Heterogeneous Integrated Packaging Program - SHIP Projekt with DoD	Kitty Pearsall (Boss Precision, Inc.) and Chris Riso (Booz Allan Hamilton)
6	ECTC/ iTherm Diversity Panel - Solving Diversification Challenges and Workforce Retention Issues	Kim Yess (Brewer Science), Christina Amon (iTherm), Francoise Von Trapp (3D InCites)
7	2022 ECTC Plenary Session - Digital Transformation - The Cornerstone of Future Semiconductor and Advanced Packaging Growth	Rozalia Beica, (AT&S) and Ed Sperling (Semiconductor Engineering)
8	IEEE EPS Seminar - Interconnect Technologies for Chiplets	Yasumitsu Orii (NAGASE) and Shigenori Aoki (Fujitsu)
9	ECTC Young Professionals Network Panel	Yan Liu (Medtronic) and Adeel Bajwa (Kulicke and Soffa)

Table 1: ECTC 2022 special sessions topics.

Session #7 (ECTC Plenary Session) will focus on the important topic of "Digital Transformation - The Cornerstone of Future Semiconductor and Advanced Packaging Growth." The session will be chaired by the IEEE ECTC 2022 general chair, Rozalia Beica (AT&S), and Ed Sperling (Semiconductor Engineering).

We are continuing our tradition and bringing back the young professionals networking event (Session #9). This is a great networking opportunity for young engineers, researchers, and students, to meet senior EPS members and professionals, learn more about industry activities, receive career guidance, and engage through a series of activities.

The ECTC Diversity Panel (Session #6) – started a few years ago as a women-focused panel – has now evolved into a Diversity and Career Panel. Its focus will be on "Solving Diversification Challenges and Workforce Retention Issues." Our colleagues from Japan will be chairing this year's IEEE EPS seminar Session #4, which will focus on "Interconnect Technologies for Chiplets."

Following the industry trends and a growing interest in Micro-LED, ECTC 2022 will feature a special session (Session #1) on "Micro-LED Display Technologies." ECTC Special Session #2 will highlight the IEEE EPS Hetero Integration Roadmap and will present special topics from the HIR working groups.

ECTC Special Session #3 will focus on "Meeting Next Generation Packaging Challenges: Chiplets to Co-Packaged Optics." ECTC Special Session #4 will cover the topic, "How will IC substrate technology evolve to enable next generation Heterogeneous Integration schemes for high performance applications?" In addition to the technical and special sessions and panels, the 72nd ECTC event will again offer the professional development courses (PDCs) and the Technology Corner exhibits. This year, 14 PDCs organized by PDC Committee chairs, Kitty Pearsall and Jeffrey Suhling, will be offered. The return to a live event also means that our Technology Corner will return to a newly renovated exhibition space with over 100 companies representing the full spectrum of materials, services, equipment, and products for the electronic packaging industry. Remaining exhibit space is currently very limited, but there is still time to reserve a booth for 2022.

Whether you are an engineer, a manager, a student, or a business and marketing professional or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. As the Program Chair, I invite you to make your plans now to join us and be a part of all the exciting technical and professional opportunities offered at this event. I would also like to take this opportunity to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 72nd ECTC a success. I look forward to meeting all of you again in person on May 31, 2022 in San Diego.

Large-size multi-layered fan-out RDL multi-chip module packaging

By Nicholas Kao, Jay Li, Jackson Li, Yu-Po Wang [Siliconware Precision Industries Co., Ltd]

Heterogeneous integration is the key technology that is applied in high-performance computing (HPC), artificial intelligence (AI) and cloud computing applications, as well as for die-to-die interconnections, application-specific integrated circuits (ASICs) to high-bandwidth memory (HBM), and ASIC-to-ASIC. The higher I/O density, wider data transmission bandwidth between memory to active die and lower RC delay are required in chiplet integration. Heterogeneous integration between different functional dies, however, leads to various process challenges, such as warpage control for multi-layered redistribution layers (RDLs), surface co-planarization treatment, and solder joint capability during the die bonding (DB) process. Therefore, in this article, we demonstrate a large size fan-out multi-chip module (FO-MCM) package with 6-layers of RDLs that successfully overcomes the non-wetting issue and warpage effects by using optimized RDL technology and compatible glass carrier selection during wafer processing.

In this study, we specifically demonstrate a FO-MCM with 6 layers of RDLs with 2/2µm line/spacing using chip-last technology. As a result, the warpage effect was decreased 39% by a particular glass, which has a compatible coefficient of thermal expansion (CTE) parameter and thickness. Additionally, we assess chip module warpage performance during reflow at a high temperature of 245ºC of chip-last FO-MCM, which is important for addressing C4 bump non-wetting phenomenon during the chip module bonding to substrate process.

The multi-layered RDL with the compatible glass technology described above brings a potential benefit to improve the warpage effect on the RDL surface. The results of the reliability tests, which are qualified in the experiment, include: 1) temperature cycling testing (TCT) for 1000 cycles; 2) unbiased highly-accelerated stress testing (u-HAST) for 192 hours; and 3) high-temperature storage life (HTSL) testing for 1000 hours. Undoubtedly, heterogeneous integration with multi-layer fan-out RDL is the mainstream for AI, cloud computing and HBM integration in the IC package industry. By utilizing this multi-layer RDL with compatible glass technology, the stability and yield of the fine-pitch die bond will be improved.

Background

Over the last decade, the semiconductor industry has demonstrated the incredible possibilities for revolutionary technologies. For example, several advanced packaging technologies have been developed to accelerate machine learning (ML), AI and HPC applications, such as 2.5D/3D, FO-MCM, fan-out embedded bridge (FO-EB), and fan-out package-on-package (FO-PoP). These packaging technologies enable heterogeneous integration scaling, which drives interconnect density with an increased bandwidth requirement, while also enabling more effective die partitioning to shorten the time to market [1-5]. However, the traditional monolithic die design in which a multi-core is integrated into one system on chip (SoC) die architecture is facing many challenges, such as increasing wafer cost, limited die size, and high power consumption. Consequently, fan-out packaging was proposed and developed as the robust solution to reduce packaging costs and provide a more flexible chiplet combination by using die partition methodology. The resulting fan-out redistribution layer (FO-RDL) technology became an essential routing technology between the die to die interconnect area. Additionally, finer line/space (L/S) values of metal trace and multi-layer RDL routing are required in order to enhance the high-speed and demands for large-volume data processing.

Fan-out technology has been developed into a variety of structures for particular applications or purposes. Figure 1 shows the main platforms and their names, which are classified by the relevant RDL interconnect technique. The first type is called FO-EB, or

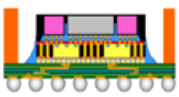
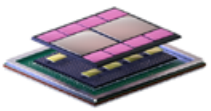
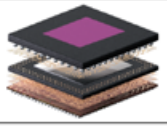
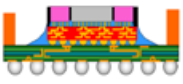
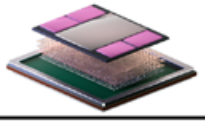
Interconnect	Structure	3D Drawing	Platform
Bridge Die + RDL			FO-EB / FO-EB-T
RDL			FO-PoP
RDL			FO-MCM

Figure 1: Fan-out technology platforms.

FO-EB-T (where "T" represents through-silicon via); in these structures, the top dies are connected by a silicon bridge die and a RDL. The bridge die plays the main role with respect to communicating in the high-speed area between the die-to-die structure. Because of the fine-pitch and small L/S design, the metal L/S on the bridge die is normally smaller than 0.56µm. Therefore, compared to 2.5D, FO-EB only requires a small silicon die size at the interconnect area, which reduces the interposer cost by reducing the gross die size and raising the yield performance for each interposer wafer. Furthermore, FO-EB-T (which is designed using TSV structures) inside the bridge die is the next cutting-edge packaging technology. Using a TSV design in the FO-EB-T structure, the electrical performance is enhanced by shortening the signal or power delivery path between the top die and the bottom substrate.

FO-PoP is also a very popular platform for mobile processor applications in which the dies are vertically interconnected. It is generally used to connect the top low-power double data rate (LPDDR) memory with the bottom system on chip (SoC) die. Therefore, the small form factor, thin package height and low power consumption are the key design factors for FO-PoP. Finally, FO-MCM is another main platform that is widely applied in advanced packaging. In FO-MCM, the RDL connects the top dies horizontally using multi-layers of RDL; and the L/S is generally scalable between 2/2µm~10/10µm. This flexible routing design is better for power and signal integrity. On the other hand, FO-MCM is the ideal structure to achieve a lower cost than 2.5D because the costly silicon interposer is not required [6-9].

Fan-out multi-chip module (FO-MCM) package technology

The FO-MCM architecture is shown in **Figure 2a**. Three ASIC dies are integrated on a 2,000mm^2 large chip module, the metal routing applies 6 layers of RDL with 2/2µm L/S, and the package size is 6,000mm^2, which is covered by a lid-type heat sink on the top. **Figure 2b** shows that 6L RDLs are built up with C4 bumps for the vertical transmission of signal and power from active dies to the substrate. The FO-MCM structure is highly flexible for advanced package design in terms of the Cu wire inside the RDL layers. FO-MCM is, therefore, also a robust platform for both homogeneous and heterogeneous integration, owing to the advantages of known-good RDL before die attaching and a competitive manufacturing cost. Additionally, FO-MCM has a shorter development cycle time than 2.5D and FO-EB because the RDL interposer can be grown before the wafer arrives at the outsourced assembly and test (OSAT) site for chip-last processing. Therefore, FO-MCM is widely applied in chiplet integration because it can be performed as an assembly turnkey service provided by the OSAT supplier. Moreover, the heterogeneous integration of ASIC to HBM memory has also been investigated in advanced packaging and it further proves out the advantages of having known-good RDL before die attaching is done in the chip-last process flow. This means that HBM memory yield won't be impacted (lost) during assembly, which again demonstrates the high yield performance of the FO-MCM platform. We will introduce both chip-first and chip-last process flows in this article.

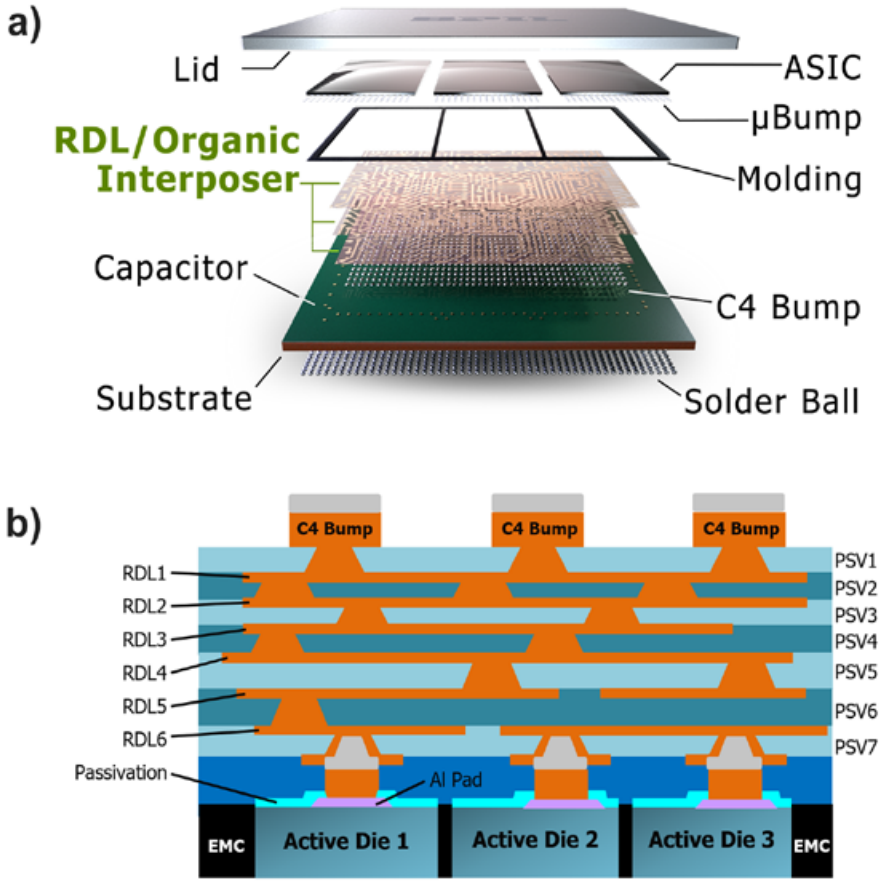


Figure 2: a) FO-MCM architecture—ASIC dies are integrated on a 2000mm^2 large chip module, the metal routing applies 6 layers (RDL) with 2/2µm L/S, and the package size is 6,000mm^2; b) 6 layers (RDL) are built up with C4 bumps for the vertical transmission of signal and power from active dies to the substrate.

Chip-first and chip-last process flows for FO-MCM

Generally, FO-MCM has two major process flows: chip first and chip last [10-11]. A brief introduction to each is provided below.

Chip-first process flow. The chip-first process flow is shown in **Figure 3a**. Silicon dies are applied onto a glass carrier with release tape; molding compound is then added to build a "reconditioned wafer." Then, a lapping process is done to expose the die. Multi-RDL layers are then deposited on the die surface. C4 bumps are then built on the RDL module, followed by a second lapping to expose the back side and reduce the molding thickness to

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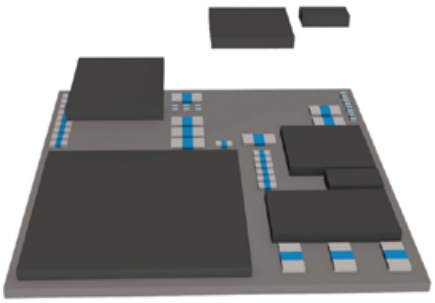

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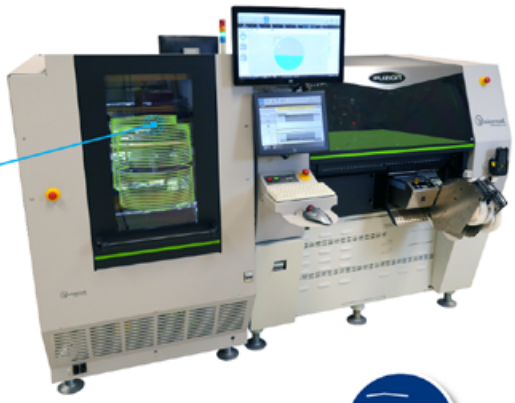

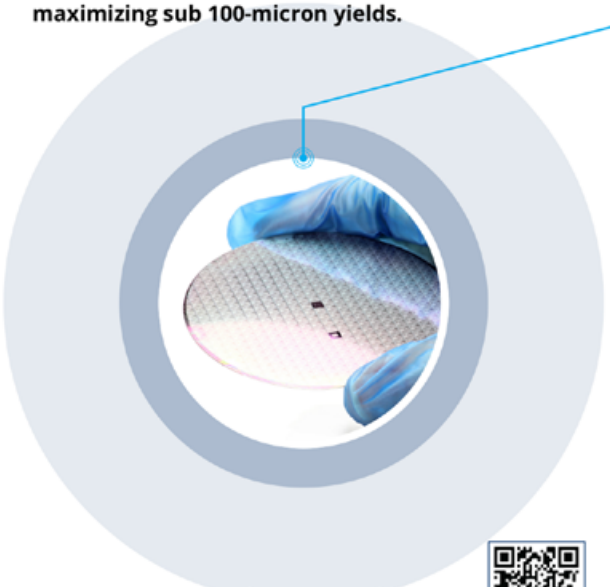

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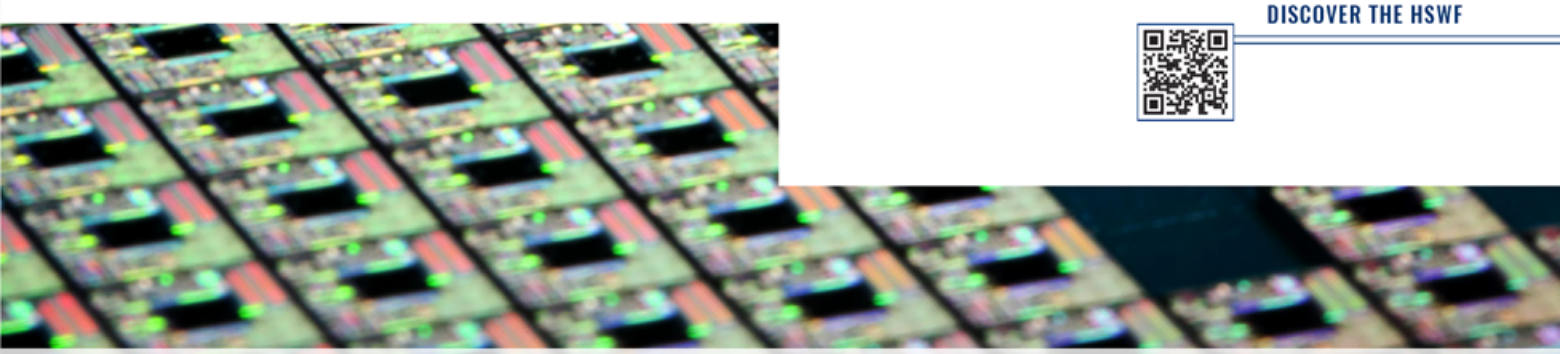

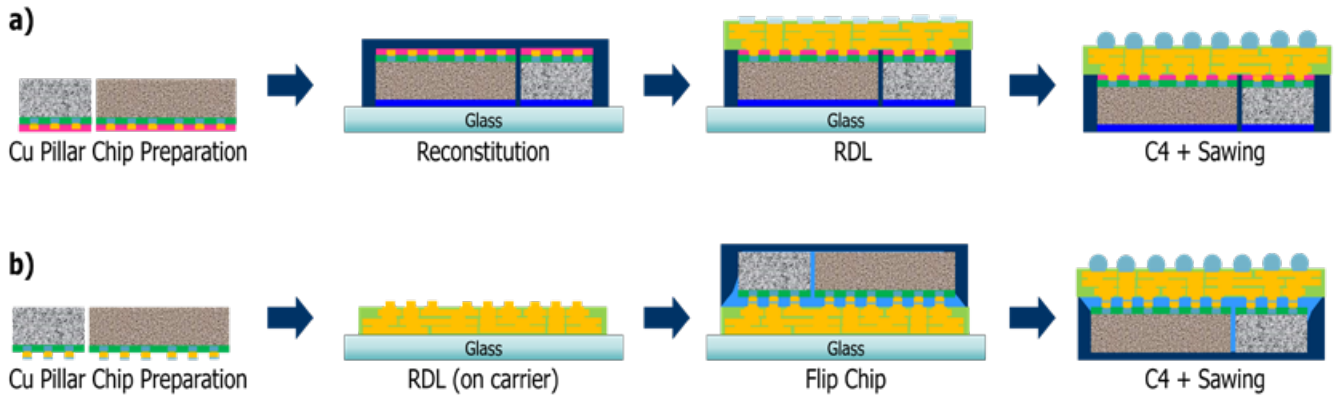

Figure 3: FO-MCM process flows for a) chip-first, and b) chip-last approaches.

the target thickness. Finally, sawing is done to form chip module units.

Chip-last process flow. The chip-last process flow is shown in Figure 3b. In the first step, RDL layers are grown on a flat glass carrier, and then a die attach process is used to attach dies to the Cu pillar bump on the RDL carrier. Under fill is then added into the micro-bump space to protect the interconnect area. Next, the RDL module is covered with molding compound. And lastly, the carrier is removed and C4 bumps are grown on the opposite RDL surface.

Compared to the chip-first process, however, the chip-last process has a more complicated process flow. Still, the chip-last process shows several obvious advantages when either the chip module size or the number of RDL layers number is increasing. Those advantages are as follows. First of all, there is no loss of KGD because the RDL yield and quality can be inspected before the die bond process, so the die loss risk can be avoided. In particular, this is a benefit because a costly wafer comprising dies at advanced nodes (e.g., 7nm, 5nm, 3nm and below) can be used. Secondly, higher yield performance is achieved compared to the chip-first process because the non-coplanarity risk is higher for the chip-first process than for the chip-last process. The risk is higher because of the grinding tolerance that is needed when multi-die surfaces are being worked on simultaneously. The end result is a lower module yield while stacking the RDL on the die's face. Lastly, the chip-last process flow makes embedding of die easier because the thickness of the die is not an issue.

Stress simulation results

In this simulation study, the stress ratios are investigated for both chip-first and chip-last structures, which are designed by 6L, 2L and 1L RDL layers individually as shown in Figure 4. As we can see from the simulation result in Figure 4a, the stress effects on the top RDL layer of the chip-first structure are 90%, 119% and 127% higher than for the chip-last case of 6L, 2L and 1L RDL structures shown in Figure 4b. Additionally, the stress ratio is 12% from 6L to 2L RDL, and 18% higher from the 6L to the 1L RDL structure individually on the top RDL of the chip-last structure. Conversely, compared to the chip-last case, the stress on the chip-first structure increases to 29% comparing the 6L RDL structure to the 2L RDL structure; and the stress increases

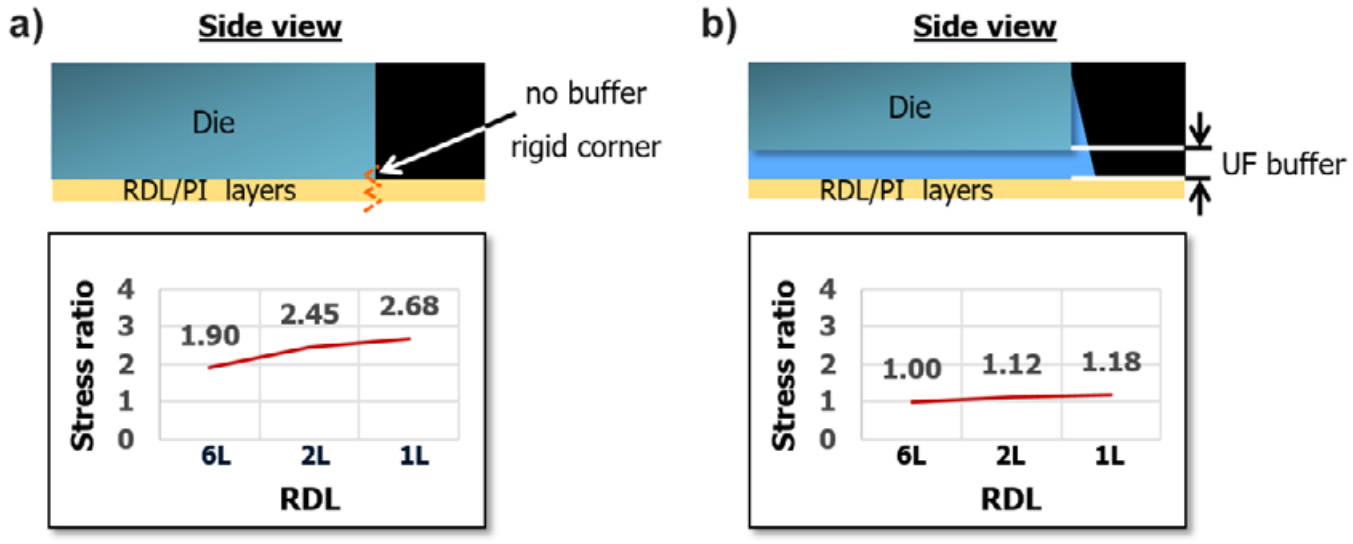

Figure 4: a) Stress simulation results of 6L, 2L and 1L RDL in the chip-first case; and b) The stress simulation results of 6L, 2L and 1L RDL in the chip-last case.

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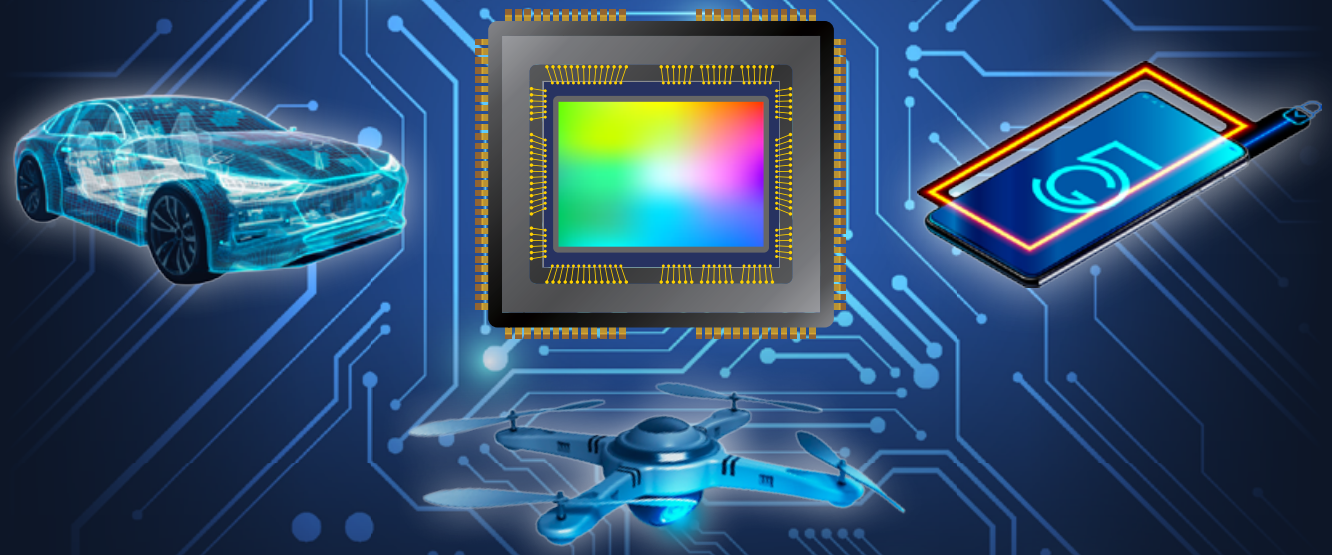

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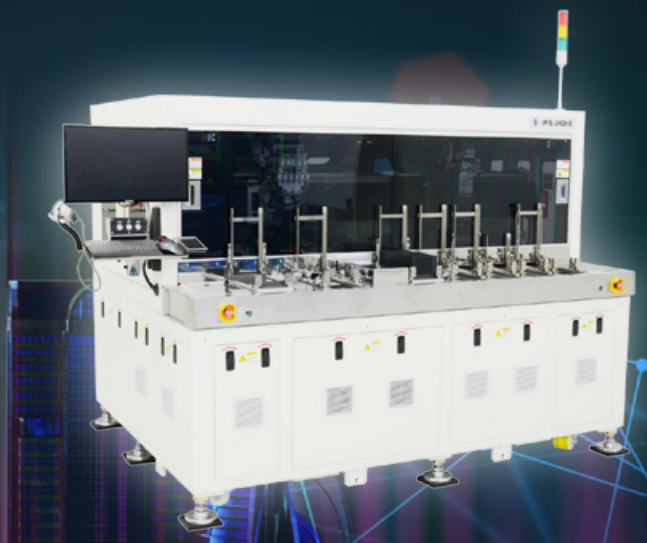

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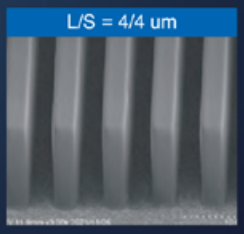

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41% from the 6L RDL to the 1L RDL case, individually. Therefore, the simulation result shows that the chip-last structure has a lower stress effect on the top RDL layer because the under fill functions as a strong buffer layer that absorbs the stress from the corner area of the top die. What this means is, the FO-MCM structure — by using the chip-last process — has a lower risk of RDL cracking because of the protection provided by the under-fill layer.

Warpage measurement results

Generally, the biggest challenge for FO packaging is warpage control because if mismanaged, it can be an interruption. This situation is particularly challenging for finer high-density FO-RDL used in multi-die integration. A larger package size and more RDL layers are the factors that result in severe warpage and yield loss. In this study, we obtained yield results using a wafer with 2/2µm L/S RDL in chip-first and chip-last structures, individually. As shown in **Figure 5a**, the chip-last structure shows better RDL quality than the chip-first structure on the whole wafer area because of its better warpage performance. The chip-first structure also has an issue with a missing copper trace on the wafer edge side. As shown in **Figure 5b**, the missing copper trace was caused by the fact that the chip-first structure experienced a worse warpage effect (see **Figure 5c**). As a result, the material CTE mismatch between the RDL layers and the molding compound interface is the key factor to cause this convex-shaped warpage in the chip-first structure. Therefore, in order to achieve better RDL topography and quality, the glass carrier was optimized for different thicknesses and CTE parameters to try and reduce the wafer warpage effect during the inline process. **Table 1** shows the warpage effect on glass types A and B by 3L and 6L RDL designs, individually. Comparing the results, it can be seen that glass B has the smaller CTE value and a 30% thicker thickness than the type A glass carrier. Therefore, by using glass B in the FO process, the wafer warpage effect was dramatically improved 39% in the 6L RDL FO-MCM chip-last structure.

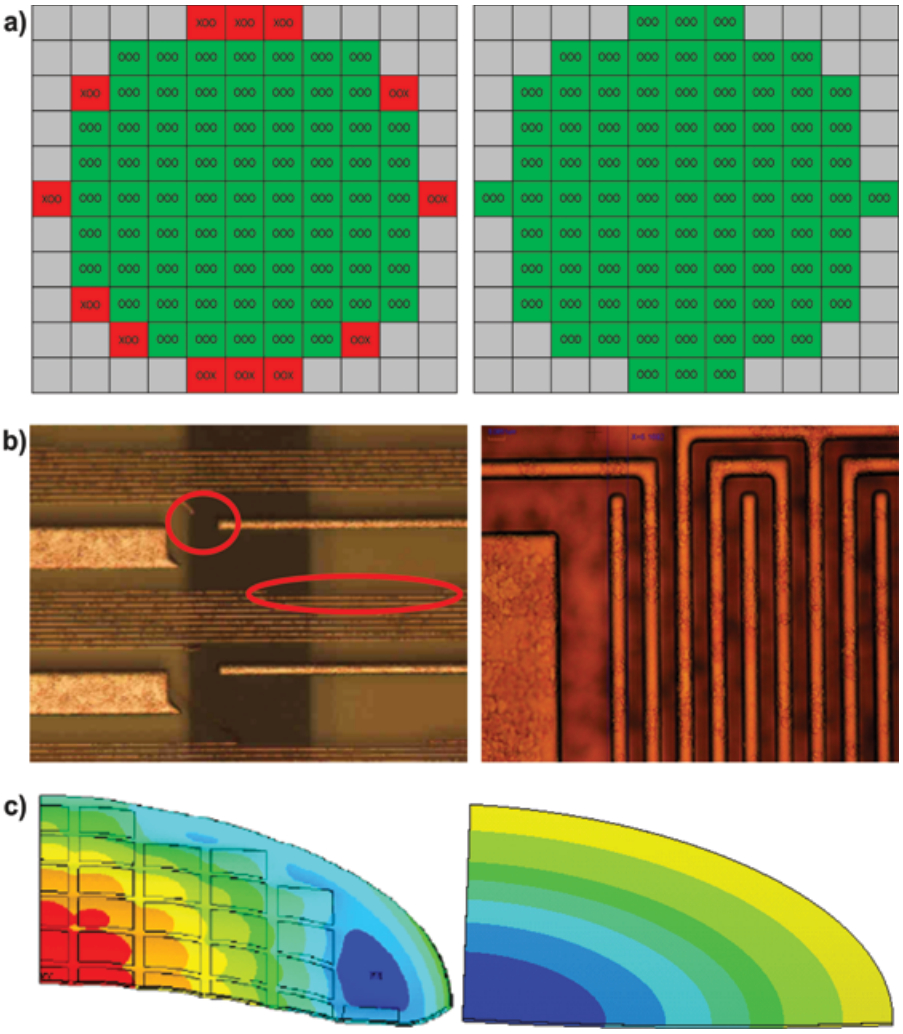

Figure 5: a) Chip-last structure showing better RDL quality than the chip-first structure on the whole wafer; b) Chip-first structure with a copper trace missing on the wafer's edge; and c) Worst warpage effect on the chip-first structure.

Leg	Structure	Wafer Form Warpage (mm)					
		RDL 1	RDL 2	RDL 3	RDL 4	RDL 5	RDL 6
Glass A	3 layers RDL	+0.24	+0.49	+0.8			
	6 layers RDL	+0.24	+0.51	+0.78	+1.07	+1.29	+1.65
Glass B	3 layers RDL	+0.16	+0.41	+0.65			
	6 layers RDL	+0.18	+0.41	+0.61	+0.82	+0.95	+1.01

Table 1: Warpage effect on glass types A and B for 3L and 6L RDL designs, individually.

Yield performance vs. FO size and RDL layers results

The diagram of fan-out size versus yield performance is plotted in **Figure 6a**. The blue line represents the chip-first (CF) structure. The red line represents the chip-last (CL) structure—it shows that the package yield performance of CF decreased more than that of the CL structure as the fan-out module size increases. RDL yield performance is compared between CF and CL in **Figure 6b**. The RDL yield was analyzed for different RDL layers of a certain package size. As can be seen, the CL structure had an over 98.5% yield performance—this is because the known good RDL feature is set before the die bond process. However, the yield of the CF case

is getting worse when the number of RDL layers is raised from 2L to 5L. This study shows that the CL design has the better yield control capability in both the large module size and high RDL layers design. This indicates that the CL structure has the potential to show a better cost benefit than the CF structure once either the FO size or the number of RDL layers exceed a particular range.

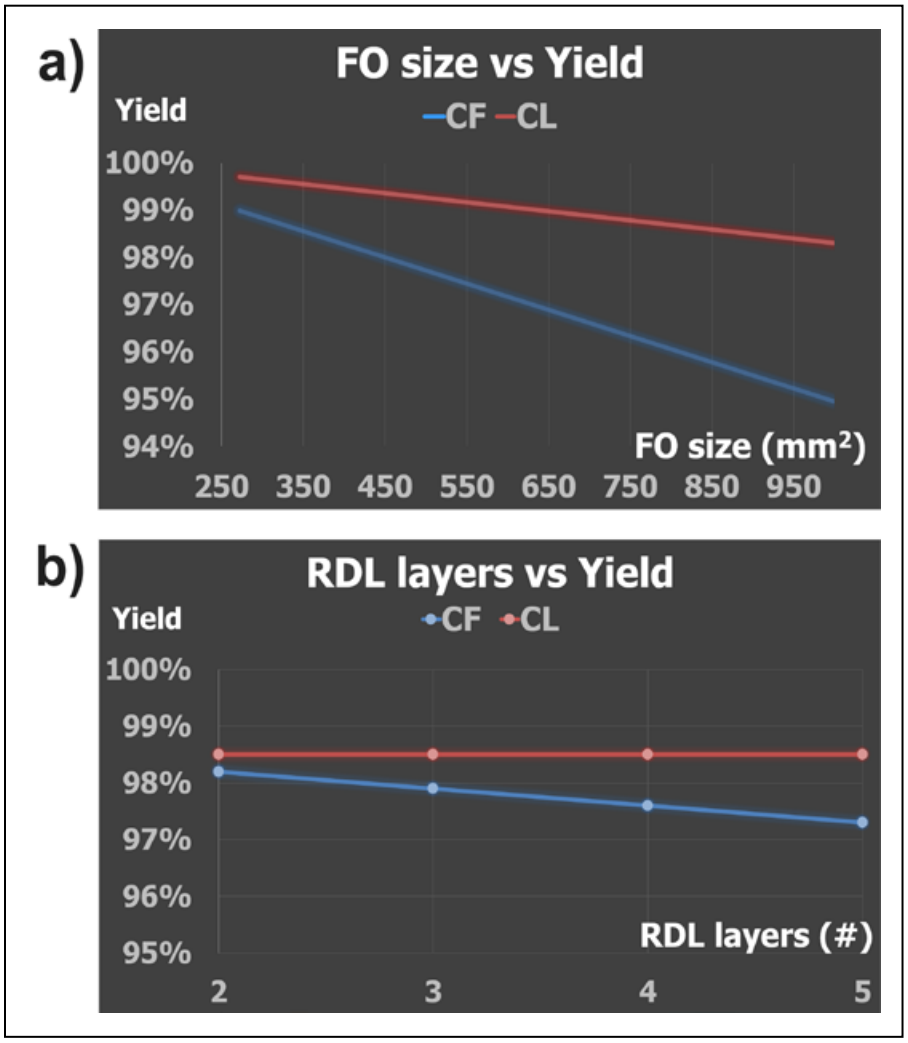

Figure 6: a) Fan-out size versus yield performance; and b) Analysis of the RDL yield by different RDL layers.

Summary

FO-MCM using the chip-last technique has been demonstrated as a robust package paradigm. It provides less stress effect, better warpage control and high yield performance. Figure 7 shows the SEM cross-section image of a FO-MCM with 6L RDL. The micro-bump height and diameter are 8µm and 25µm in this design, and the top coplanarity is controlled within 4µm, which ensures the quality of the micro-bump joint after the reflow process. In addition, the 6-via stacking structure was demonstrated in this experiment through the use of an optimized glass design. The top total thickness variation (TTV) was shown to be under control such that excellent joint quality was achieved in both the via stacking and non-via stacking areas.

Additionally, reliability tests were verified in this study. All reliability conditions received a "pass" result for MSL3, TCT1000, u-HAST192, and HTSL1000 conditions. Furthermore, the cross-section of the micro-bump joint area (after completing the reliability tests) as shown in Figure 8, indicates perfect joint quality without any non-wetting, void or solder creeping issues. In this investigation, the FO-MCM package not only provides an alternative solution from a cost-benefit standpoint, but also results in less warpage during chiplet integration when using an optimized glass carrier design. With the advantages of being able to control the warpage and have less internal stress, FO-MCM is the proper platform to build up a much larger package size for the integration of even more dies.

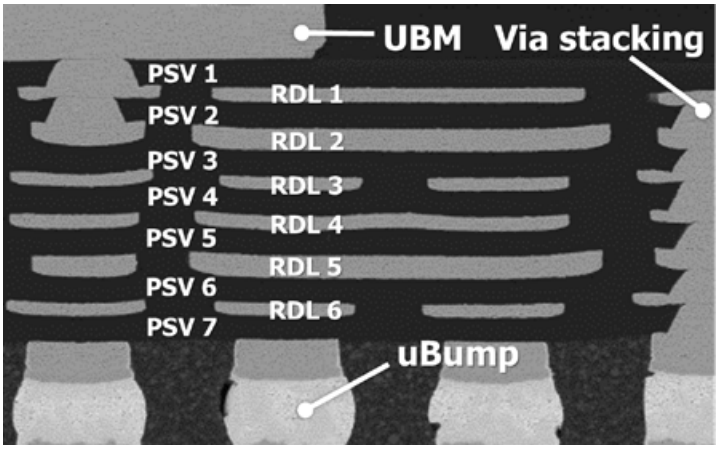

Figure 7: SEM cross-section image of an FO-MCM structure with 6L RDLs.

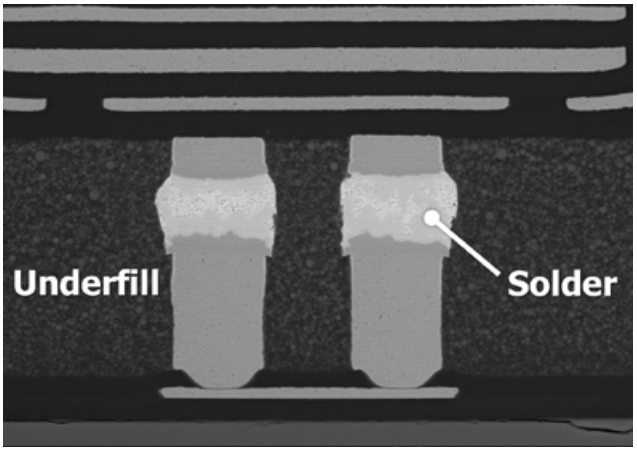

Figure 8: Micro-bump joint cross-section SEM result.

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Embedded chip packaging

By Ray Fillion [Fillion Consulting]

In the November/December 2021 issue of *Chip Scale Review*, seven advanced packaging technologies were described [1]. The article covered embedded chip packaging (ECP), fan-in wafer-level packaging (FIWLP), fan-out wafer-level and panel-level packaging (FOWLP, FOPLP), 3D packaging and system-in-package (SiP) and compared how well each meets the basic functions of microelectronics packaging. In this article, we will go into a more in-depth look at ECP, detailing the structures, processes and materials used in the various versions of ECP technologies and look at some of the unusual application areas where ECP is being applied.

Multichip modules (MCMs)

An ECP module typically includes multiple chips embedded in or under an organic interconnect structure. ECP modules with more than one chip are an advanced form of a multichip module (MCM). Traditional MCMs have multiple bare chips mounted on top of a pre-fabricated and fully-tested interconnect structure, such as a multilayer organic or ceramic substrate. Each chip is interconnected to the substrate using wire bonds or flip-chip solder bumps. The completed MCM would be mounted in a large package or over molded with a thermoset resin, creating a molded package. In traditional MCMs, the substrate is fabricated and tested first, and then the chips are placed on the substrate, making it a "chips-last" approach.

ECP technologies

As the term implies, ECP is a semiconductor chip packaging technology in which bare chips are embedded in organic material and electrically connected using an overlying interconnect structure. ECP MCMs differ from traditional MCMs in that the chips have direct metallurgical connects to the overlay interconnect structure in place of wire bond or flip-chip connections to the substrate. ECP also reverses the basic MCM fabrication processing sequence by mounting the chips prior to fabricating the interconnection structure, making ECP a "chips-first" approach.

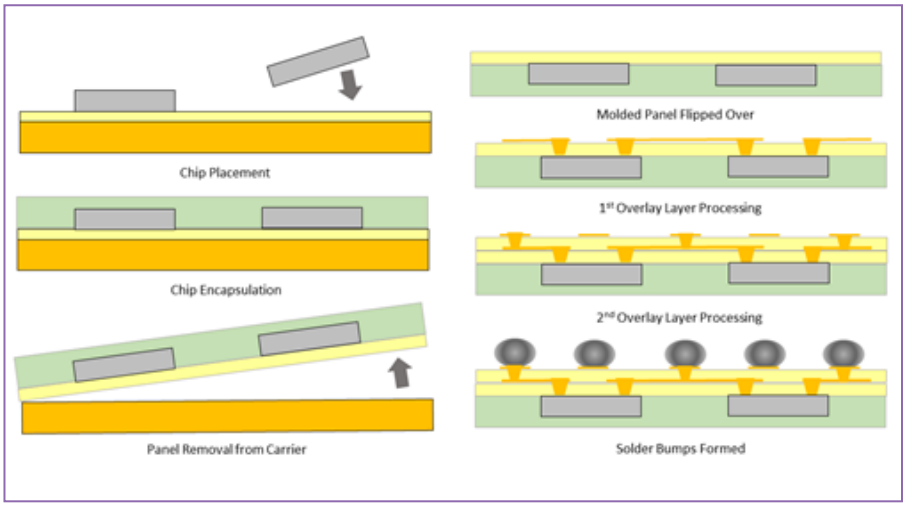

Figure 1: Basic COF ECP processing steps with two overlay layers interconnecting the chips.

Early ECP development

The first ECP development was the GE high-density interconnect (HDI) technology developed in the late 1980s at the GE Global Research Center in Niskayuna, NY. It was developed as a high-performance MCM technology for aerospace electronics. The HDI process started by forming cavities in a ceramic substrate, attaching multiple bare chips face up into cavities using an organic adhesive. A dielectric film was laminated over the chips and microvias were laser-formed to the chip pads and a fine-line interconnect was formed on the surface of the film and into the microvias. Additional interconnect layers were formed by repeating these steps [2]. A completed HDI module would be assembled in a large hermetic package. HDI modules had high silicon density and very low interconnect parasitics, but it also was a high-cost packaging technology.

GE chip-on-flex (COF) ECP technology

Because of the high cost of HDI, the team that I led at GE developed a new ECP technology in the mid-1990s with modifications targeting lower costs while maintaining HDI's low interconnect parasitics and high silicon density. This effort led to the development of the GE COF technology, targeting less complex modules and later, the power overlay (POL) embedded power module technology. Figure 1 depicts the basic processing steps for the COF ECP technology. Bare chips are placed face down onto a B-staged (partially-cured) adhesive coated on a polyimide film on a processing platen. Molding material is dispensed to encapsulate the chips and form a molded carrier in a wafer or panel format. The molded carrier is removed from the processing platen and flipped over for front-side processing. Microvias are formed to the chip pads and to component contacts using laser ablation. The same metallization and pattern processes developed with HDI are used to form the first interconnect layer. Additional interconnect layers can be formed by applying another dielectric layer, laser-forming microvias, metallizing and patterning. As with most

ECP approaches, other component types, including passive devices and sensors, could be embedded along with the semiconductor chips. Figure 2 depicts a cross-sectional view of a typical COF ECP module showing two bare chips of differing thicknesses and a passive device, all interconnected with a two-layer overlay interconnection structure and topside area array I/Os [3].

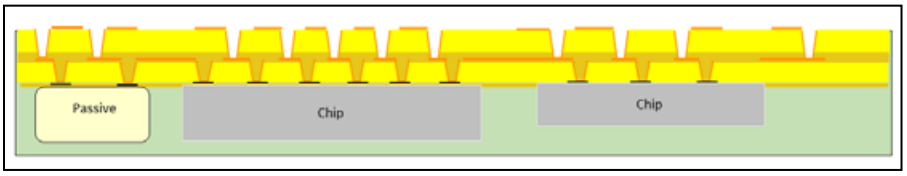

Figure 2: Cross-sectional view of a typical COF ECP module with two overlay layers connecting two chips and one passive device.

The COF technology has several key advantages over the HDI technology. The most important advantage was the elimination of excessive chip movement during chip placement and chip adhesive cure, eliminating the need to adapt to the locations of the microvias and metal patterning. This feature makes it fully compatible with mask-based photo-patterning and volume scaled up to large-panel processing. Another advantage was the elimination of the custom and costly ceramic carrier with its mechanically-machined chip cavities. The COF structure had a much flatter top surface that allowed fine interconnections and a much thinner structure that enabled the mounting of other components on the top surface while also allowing the stacking of multiple COF substrates into 3D modules. Finally, the molded substrate readily accommodated thermal structures under high-power dissipation chips [4].

ECP structures

All ECP modules have a number of common structural features. First, bare chips and other devices are encased in organic material covering the four sides and generally, the back surface of each device forming the ECP substrate. A low dielectric constant polymer overlays the components and the molded substrate and forms the first dielectric layer. Microvias are formed through the dielectric to the chip pads and to other component contacts. A thin, patterned metal layer is formed on the top surface and into the microvias to the chip pads. A typical ECP module would have at least one additional interconnect layer. The key feature of all ECP structures is the direct metallurgical connection of the interconnect metallization to the chip pads, thereby eliminating the parasitics associated with wire bonds and solder bumps.

ECP advantages

As mentioned above, a key advantage of ECP is its low interconnection parasitics. ECP structures lower chip-to-chip parasitics by an order of magnitude

verses flip-chip structures, and by two orders of magnitude verses wire bonds use in traditional MCMs. As shown in Table 1, the interconnection parasitics of ECP microvias that connect directly to the chip pads are less than 0.01nH of inductance, less than 0.001pF of capacitance, and less than 1.0mohms of resistance [5]. These low parasitics permit faster clock rates, faster switching, reduced line noise, and lower interconnect losses.

ECP processes and materials

Although many of the ECP structures, process steps and materials described above relative to the COF technology are also used by many high-volume ECP fabricators today, there are a number of variations in these across the industry. These variations include: 1) chip placement orientation; 2) encapsulation materials and processes; 3) microvia processes; and 4) dielectric materials and processes.

Chip placement orientation. An alternative method of chip placement in some ECP technologies is placing the chip face up prior to molding. One face-up chip placement approach is depicted in Figure 3. Chips with different thicknesses are placed face up on a processing platen and a molding compound embeds the chips, forming a molded carrier with the molding compound forming both the molded substrate and the first dielectric layer. Because of differing chip thicknesses, the dielectric layer over thin chips is thick, while the dielectric layer that is over the thick chips is thin. This results in some deep microvias and some shallow microvias making the microvia processing more complicated. It also complicates the choice of molding material because it cannot be optimized for both the best molding material, i.e., lowest coefficient of thermal expansion (CTE), and the best dielectric material, i.e., low dielectric constant.

Chip encapsulation. Although most ECP approaches embed chips using molding compound or resin, there are alternate methods used to embed the chips including film laminate using thermal plastic polymer sheets and within a cavity formed within a printed circuit board (PCB). Figure 4 depicts a lamination-based embedding process used by AT&S and TDK. It uses multiple layers of thermoplastic or thermoset films, each with cutouts to form chip cavities [6]. The

Parameter	Wire Bond	Flip Chip	ECP Micro-Via
Inductance (nH)	1.0 -3.0	0.05 - 0.1	0.005 - 0.01
Capacitance (pF)	0.01 -0.05	0.002 - 0.01	0.0002 – 0.001
Resistance (mΩ)	30-100	2.0 - 6.0	0.2 - 1.0
Transmission Line Capability	None	To bump pad	All the way to the chip pad

Table 1: Comparisons of interconnect parasitics for ECP modules with microvias verses MCMs with wire bonds and flip-chip solder bumps.

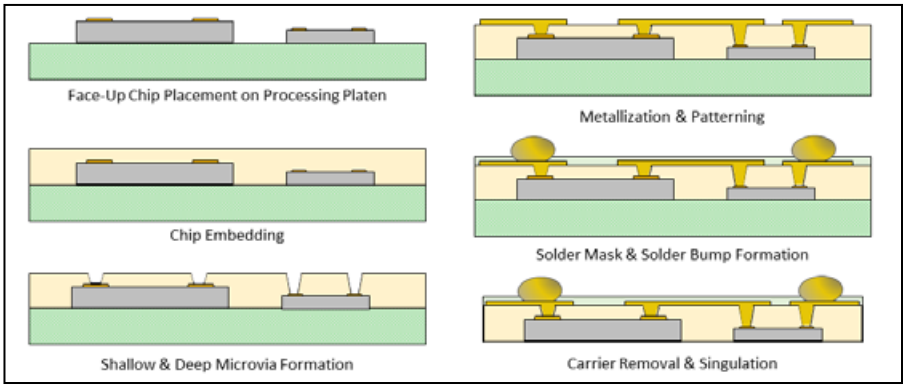

Figure 3: ECP face-up chip placement processing steps with both deep and shallow microvias to chips with differing thicknesses.

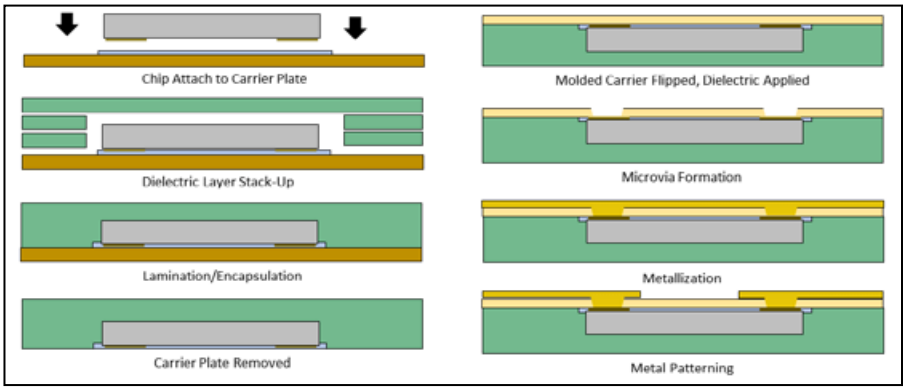

Figure 4: ECP process steps for a multilayer laminate process to encapsulate chips.

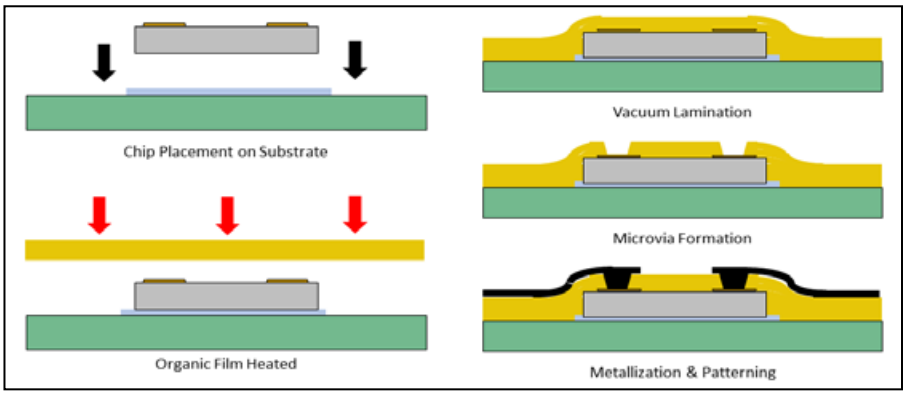

Figure 5: Processing steps for a one-layer, ECP overlay lamination process.

chips are placed face down in the cavities and a top film without cutouts is applied over the stack-up covering the chips in the cavities. Standard lamination processing steps with heat and pressure are used to soften the dielectric layers and reflow the resin around the chips, embedding them and bonding the layers together. Another laminate-based process utilizes one thick flowable thermoplastic organic film to embed thinned chips. Figure 5 depicts a simple lamination process where one thermoplastic film is draped over the chips. Then, a vacuum is pulled below the film and heat and pressure are applied to the top of the film, which causes the organic film to encase the chips and form the first dielectric layer. This process is generally applicable to low I/O modules. Finally, chips can also be embedded within a multilayer PCB. As depicted in Figure 6, a chip cavity is formed in a double-sided PCB with plated through-holes (PTHs). A bare chip is placed face down in the cavity and the cavity is filled with molding material. Then, thin dielectric layers are applied to both sides of the PCB and standard via formation, metallization and patterning form double-sided fine-line interconnect structures directly connecting to the chip pads.

Via formation. The predominant method used to form ECP microvias in the overlay dielectric layers is by laser ablation—effectively vaporizing the dielectric material and forming microvias with sloped sidewalls, optimized for microvia metallization. In some ECP technologies, in order to avoid using a high-cost laser to ablate microvias, a photo-definable overlay dielectric is used that can be photo-defined by mask-based photo-processing. Another approach is to apply and photo-pattern a hard mask forming openings at the microvias' locations and form the microvias by chemical etch or plasma etch.

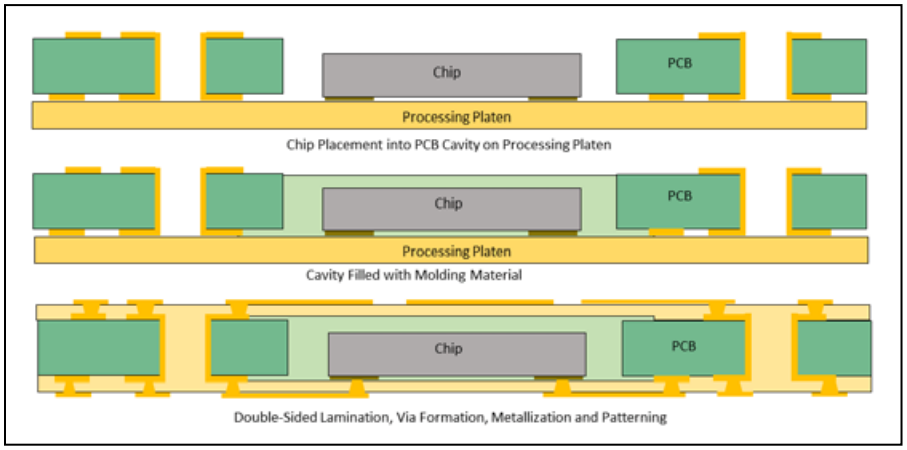

Figure 6: Process steps for embedding chips inside a PCB.

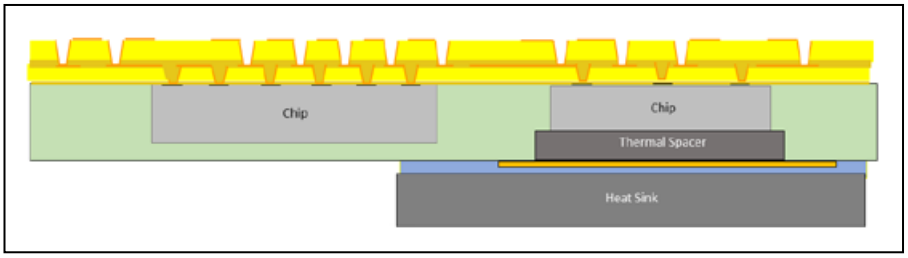

Figure 7: ECP module with thermal spacer directly attached to the back surface of a high-power dissipation chip and backside heat sink.

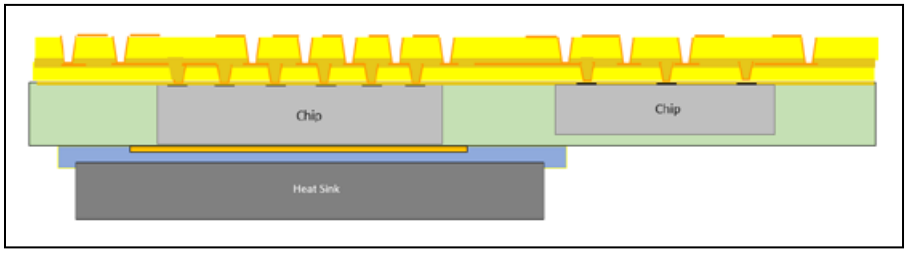

Figure 8: EP module with one high-dissipation chip with its back surface exposed by back grinding and with an attached heat sink.

Thermal performance. Because all ECPs are essentially a molded plastic package, it might be assumed that ECPs would inherently have poor thermal performance. That is generally true for a fully-encapsulated module without a direct high thermal conduction pathway to a heat sink. ECP fabricators have addressed the issue of thermal performance of their processes by providing a low thermal resistance path for higher power dissipation chips. There are two main approaches to improve ECP thermal performance. The first approach is to attach a thermally-conductive structure to the back surface of a high-power dissipation chip prior to molding and then use a thermal interface material (TIM) to attach a heat sink as depicted in Figure 7. The second approach is to thin the module by back grinding to expose the chip's back surface and attach a heat sink using a TIM (Figure 8). This method, however, does have drawbacks if the high-power dissipation chip has an active backside contact. In vertical power and microwave devices, the chip's electrical ground contact is on the chip's back surface. Back grinding to expose the chip could damage the backside contact.

ECP application areas

Although ECPs are generally targeted for use in those modules that have only a few chips (say, 3-5, or so), their high density, low interconnect parasitics and low processing costs have led ECP fabricators and users to apply the technology to a wide array of application areas. These include mixed analog/digital modules, sensors, control electronics, power electronics, photonics, microwave, single-chip packages and thin, flexible modules. Examples of some of these application areas are discussed below.

Mixed analog/digital. All ECP structures that we reviewed have very low interconnect parasitics and can bring a matched transmission line all the way to the chip pads as shown earlier in Table 1. Because of this, ECP

is ideal for analog circuitry including low-voltage sensors and high-frequency circuits. Either full or partial ground planes can be fabricated in the overlay structures for switching noise isolation or transmission line impedance control. Figure 9 depicts a mixed analog/digital control module processed in the COF ECP technology.

Figure 9: Mixed analog/digital COF module with embedded chips and passive devices.

High-power modules. Although most ECP technologies were developed with interconnect structures featuring thin metallizations (5-10µm), small microvias (15-25µm), narrow lines (10-25µm) and thin dielectric layers (15-25µm) targeting lower power digital circuits, these technologies can be easily beefed up to handle power circuits. These features could not support the high voltages, high currents and high power dissipation of a high-power circuit. One example of a high-power ECP is the GE power overlay (POL) ECP technology. The COF process was modified using thicker interconnect metal (25-50µm), microvias were replaced with large diameter vias (100-200µm), line widths were increased (100-1000µm), and dielectric thickness was increased (50-100µm) for higher breakdown capability. A high-power POL module is shown in Figure 10. It depicts an 800A, 600V switch with eight insulated-gate bipolar transistors (IGBTs) embedded under one overlay interconnect layer with arrays of large vias to the power contact pads to handle the high current [7]. Another example of a low-power ECP process being extended into high power is Infineon's Blade technology.

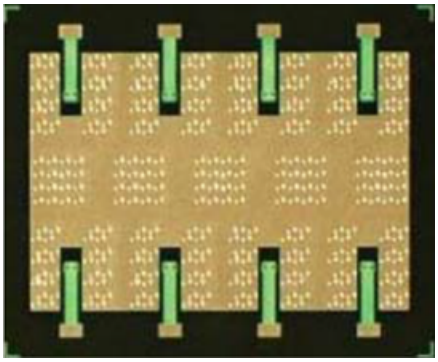

Figure 10: High-power, 800A, 600V, switch module with eight IGBT chips fabricated with the GE POL ECP process.

Figure 11 shows a cross-section of a typical embedded power module available from Infineon, TDK, ASE and others. It has a thick copper base plate, a power diode and a power transistor solder attached to the base plate, arrays

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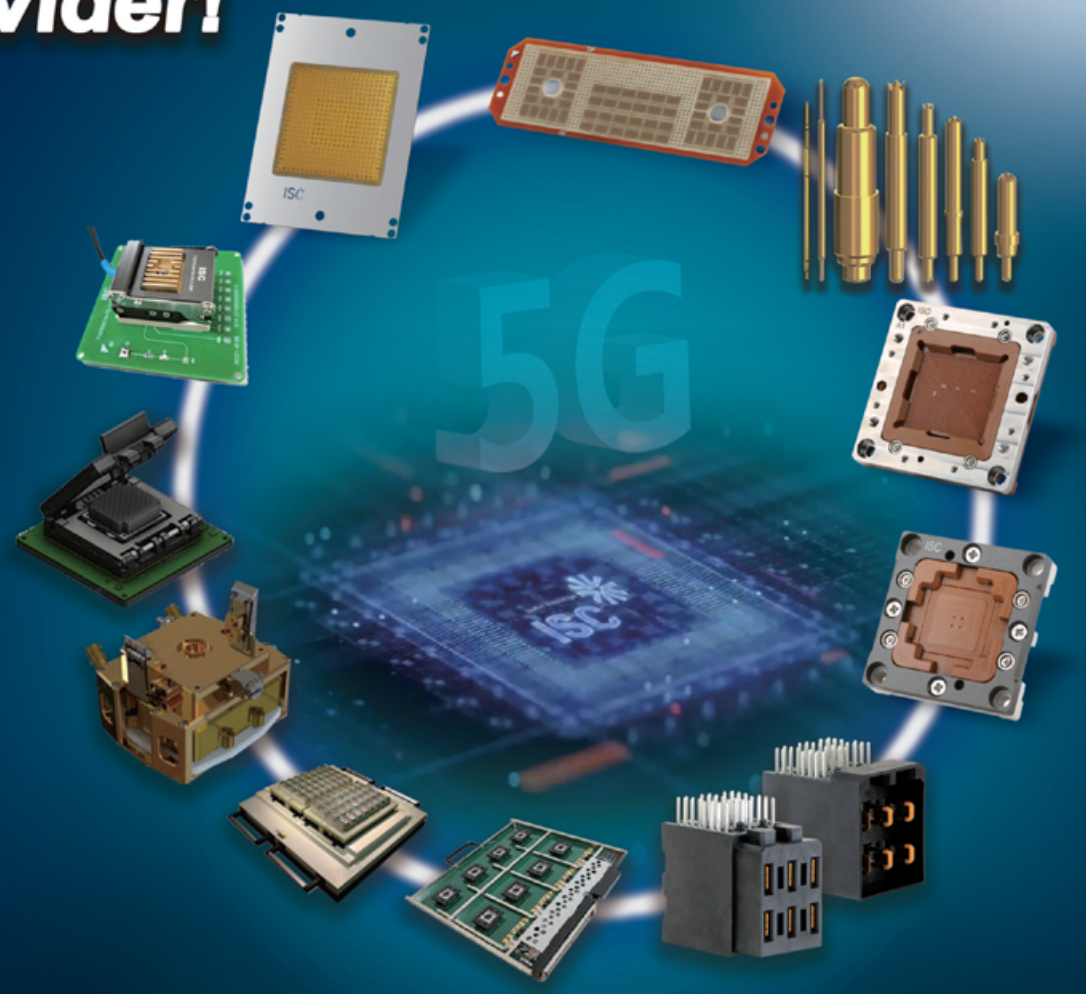

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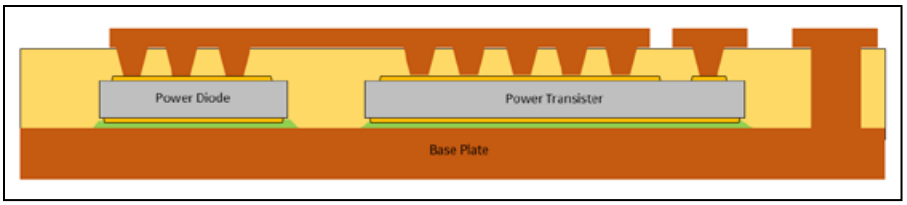

Figure 11: Infineon high-power, Blade ECP module with thick metal traces, solid post vias, and a bottom metal plate.

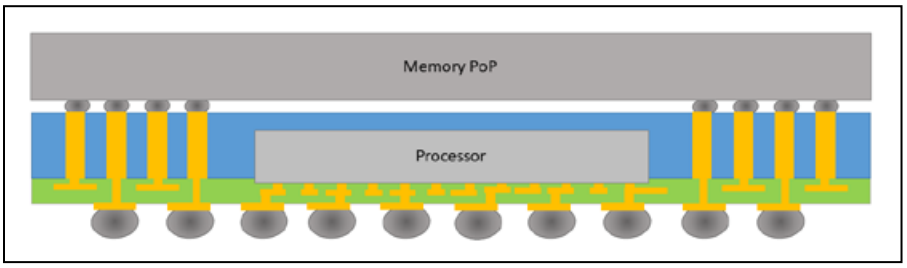

Figure 12: TSMC PoP with bottom package containing an InFO-embedded processor chip and the top package containing a memory stack.

of large, solid post vias connecting through the overlying dielectric and thick topside metal interconnecting the chips and the backside through the post. It has a direct through-the-base thermal cooling path. In both of these high-power applications, backside electrical contacts were required to connect to the vertical power chips.

Single-chip ECP modules. Although most ECP modules have multiple chips, ECP has also been used to fabricate modules with only one chip, such as a high-performance, high-I/O count processor chip. Figure 12 illustrates a package-on-package (PoP) module with a lower package featuring an application processor that is packaged using the TSMC InFO ECP technology. Through-molding vias (TMVs) interconnect the lower BGA pads to the topside small BGA pads that, in turn, connect to the top memory package [8]. TSMC used the InFO ECP technology to package the Apple applications processor for iPhone 10–12 smartphones. This eliminated solder bumps from the processor to a substrate, thereby enabling lower interconnect parasitics and a reduction in the thickness of the processor package that was used in a PoP configuration [9].

Summary

ECP technologies are in broad use across the microelectronics industry from "few-chip" MCMs to single-chip FOPLPs. Processes vary generally based on the technical background of the fabricators. PCB manufacturers often use PCB processes, materials and equipment, such as lamination, epoxy glass prepregs, double-sided interconnect structures and large-area panels. Fine-line substrate manufacturers tend to use unfilled dielectrics such as polyimide and fabricate single-sided interconnect structures. Wafer fabricators tend to use back-end of the line (BEOL), wafer-level processing, spin-coated dielectrics and finer interconnect lines and spaces. All of these versions of ECP feature low cost, high silicon density and low interconnect parasitics. Applications of ECP technologies range from single-chip fan-out devices, to complex multichip logic circuits, to very high-power circuits.

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Biography

Ray Fillion is Managing Director at Fillion Consulting, Schenectady, NY. He retired after 40 years from the GE Global Research Center where he worked in various engineering, management, business development and licensing positions in embedded chip, MCMs, 3D modules and power electronics. He has over 100 publications, has 45 issued U.S. patents and was the lead inventor on the GE Embedded Chip Build-Up and the GE Power Overlay technologies. Email fillion.consulting@gmail.com

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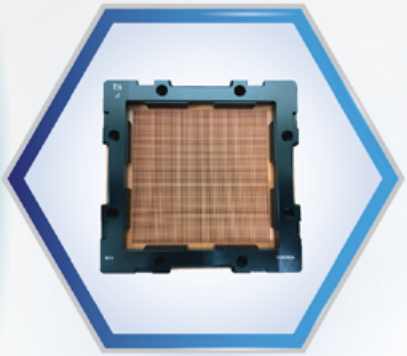

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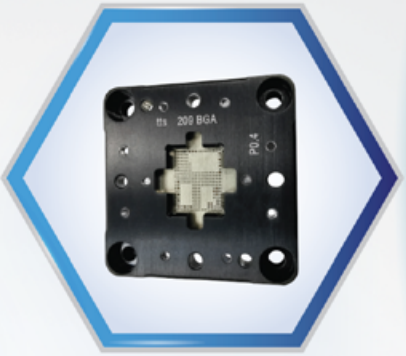

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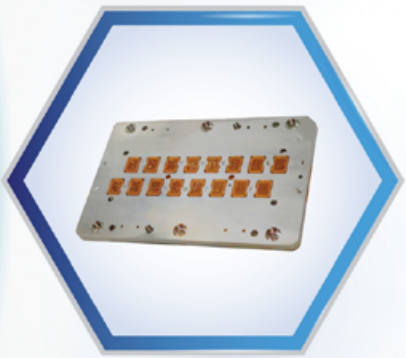

Probe Pin

Pitch
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Power
≤6.5A

Frequency
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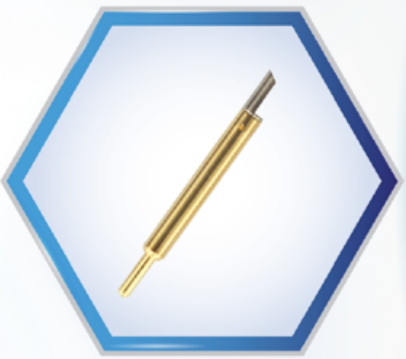

RF

Pitch
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Insertion Loss
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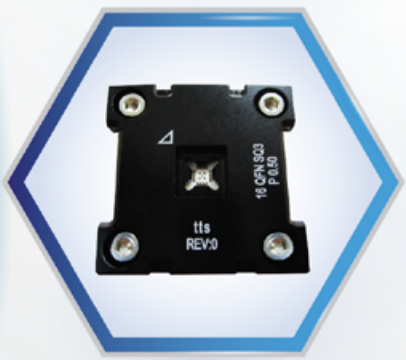

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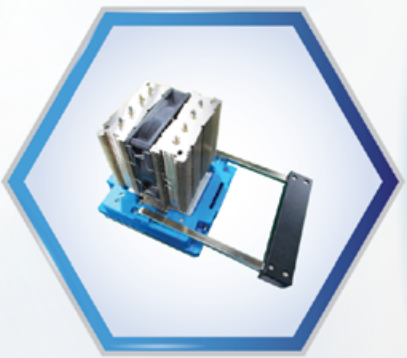

BROCHURE

Heterogeneous integration for AI applications: status and future needs (part 2)

By Madhavan Swaminathan, Siddharth Ravichandran [Georgia Institute of Technology]

Part 1 of this article was published in the January/February 2022 issue of Chip Scale Review.

In part 1 of this article, the emerging artificial intelligence (AI) system needs that are driving various packaging architectures were discussed along with 7 metrics driving new technologies. These metrics include interconnect density, interconnect length, data rate, bandwidth density, energy per bit, power delivery, and thermal design power. In part 2, we compare the state-of-the-art (SOTA) packaging technologies based on these metrics along with future requirements. [Note to readers: figure and reference numbers start where numbering left off in part 1.]

Packaging, interposers, and 3D stacking options

In this section we refer to high-density interconnect (HDI) packaging as 2D, interposers supporting higher density wiring as 2.5D, and stacking of dies as 3D. In the 2D approach, bare dies are placed side-by-side and connected to each other through interconnections in the package substrate. Interposers can be viewed as a large chip that contains several smaller dies that are connected and that serves the role of a conduit between the dies on top and the package substrate at the bottom. In contrast, in the 3D approach, dies are vertically stacked and connected to each other using through-silicon vias (TSVs) and chip bonding technologies. **Figure 5** shows the classification of the various die connectivity approaches for heterogeneous integration along with their schematics in **Figure 6**. We describe and compare the different options available both commercially and under development that can support heterogeneity.

2D architectures. Based on the core material used we can further classify the approaches as silicon based, organic based, and glass based. **Table 1** compares the different core materials used based on the raw material properties and physical

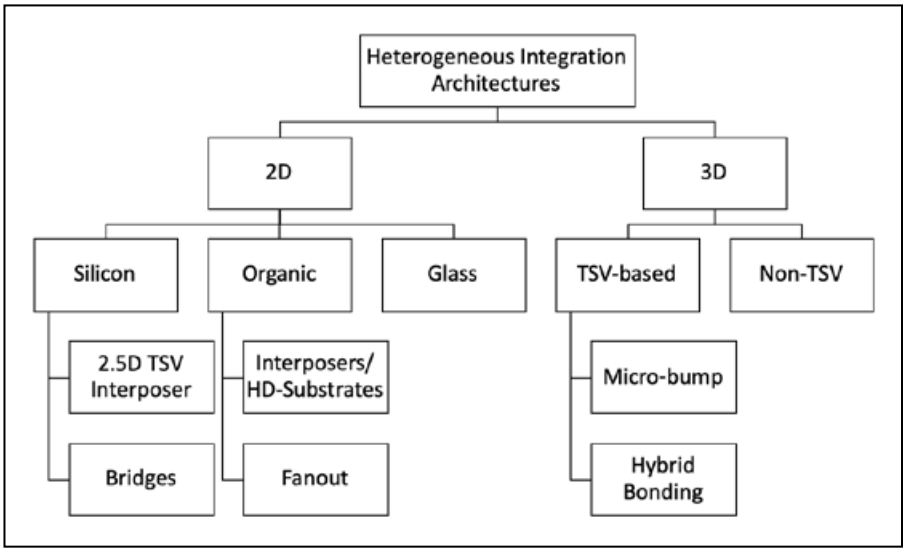

Figure 5: Classification of 2D, 2.5D and 3D approaches for heterogeneous integration.

requirements for current and future AI applications. Achieving high IO densities require smooth surfaces (tens of nm) to ensure lithography yields are high. The coefficient of thermal expansion (CTE) of the core material is a key determinant of the reliability of the system. Mismatch in CTE between chip, package, and printed wiring board (PWB) builds up stresses on the assembly joints during the operational lifetime of the system—eventually leading to failures. Therefore, it becomes critical to understand the thermo-mechanical properties and interactions of the different layers and components to ensure reliability of the overall system.

Another important property is the Young's modulus, which is a measure of the dimensional stability of the core. Better dimensional stability (or a higher Young's modulus) helps in lowering warpage both during redistribution layer (RDL) formation and assembly. In multi-layer package cores with poor dimensional stability, the dimensional shifts that occur from one layer to another during processing need to be compensated with larger pad diameters (D from Figure 3 in part 1), thereby impacting IO density. Moisture absorption impacts the performance degradation over time due to increasing D_k (dielectric constant) and D_f (dissipation factor) while also impacting system reliability. This may not be critical in modern data centers, but it is increasingly important as AI hardware gets deployed in uncontrolled environments, for example, in self-driving cars. Although the dominant heat path is through the backside of the die [14], the thermal conductivity of the core material is worth noting and shown in **Table 1**.

Package sizes are limited by two key factors: 1) reliability concerns with increased stresses on assembly joints; and 2) cost, arising from the larger substrate. Today, advanced integration is largely at wafer scale owing to the existing 300mm-wafer infrastructure, but with increasing package sizes, panel scalability becomes an important issue for lowering costs [15].

Substrate Core	Silicon	Organic		Glass
		Laminates	Fanout (Epoxy Mold Compound)	
Material properties				
Surface roughness (nm)	<10	400-600	> 1000	<10
CTE (ppm/K)	2.9-4	3-17	16-30	3-9
Young's modulus (GPa)	165	10-40	22	50-90
Moisture absorption	0	0.04%	1-2.5%	0
Thermal conductivity (W/m.K)	148	0.9	0.5-0.75	1.1
Physical Dimensions				
Package size (mm)	35x35	70x70	50x50	100x100
Panel/Wafer size	300 mm	710 mm^2	300 mm / 510 mm^2	710 mm^2

Table 1: Comparison of material properties and physical dimensions of different core material options.

Silicon-based approach

In silicon-based interposers, traditional complementary metal-oxide semiconductor (CMOS) processes are used to form the high-density wiring to interconnect dies to each other. Variations of this approach include interposers with TSVs or the use of bridge chips without TSVs to establish connectivity.

An example of a 2.5D TSV-based silicon interposer is the Chip on Wafer on Substrate (CoWoS®) process from TSMC [16] as shown in **Figure 6a**. This process connects multiple fine-pitch bare dies to a coarser-pitch package substrate, along with high-density wiring on either side of the silicon core to connect the dies to each other. Two critical technologies that enable this are: 1) TSV, and 2) RDL. The advances in Bosch processing have scaled the dimensions of TSVs to <20µm diameter in high-volume manufacturing. The RDL layers, however, are re-engineered from 65nm-CMOS back end of line (BEOL) processing. This allows for lithography ground rules ranging from 1µm to <0.5µm [17,18]. The dielectric used for the interconnections is SiO_2. While extreme-low-K (ELK) dielectrics with D_k<3 are available for advanced CMOS processes on silicon, they are not commonly used. The silicon interposer is matched in coefficient of thermal expansion (CTE) with the die, thereby enabling fine assembly pitches of 35µm using micro-bumps while attaching to a ball grid array (BGA) substrate using C4 at ~130µm pitch. Because of the use of traditional CMOS processes, the size of silicon interposers are often limited by the reticle size supported by the semiconductor foundry. So, even though a 300mm-diameter silicon wafer is available, the interposer size is limited to areas less than 1600mm^2 unless nontraditional approaches like reticle stitching are used, which adds to the cost of silicon fabrication making large-size TSV interposers very expensive.

In contrast, the TSV-less embedded multi-die interconnect bridge (EMIB) from Intel shown in **Figure 6b** addresses the interposer size issue by utilizing smaller bridge dies embedded in an organic package to provide localized high-density wiring to connect dies together [8]. Though this approach reduces cost while increasing interposer size, only adjacent dies can be connected to each other through the edges facing each other and requires two bump pitches for assembly (coarse- and fine-pitch at the center and edge of the die, respectively). In EMIB, the bridges range in size from 2x2mm^2 to 8x8mm^2 using 4 metal layers with 2µm lines and spaces for the RDL.

Organic-based approach

Organic substrates can be further classified into interposers (**Figure 6c**) and fan-out (**Figure 6d**) packages. Although both these types use organic material as the core, there are significant differences in their structure and manufacturing processes. While organic interposers and high-density substrates follow a more conventional approach of chip assembly after package construction, in fan-out packages, the RDL and IOs are formed over the molded, or fanout, region of a reconstituted die.

Organic laminates are extensively used as package substrates today because of their electrical properties and low cost. Laminate packages are typically fabricated in large panels by sequentially processing each layer of thin-film polymer dielectric

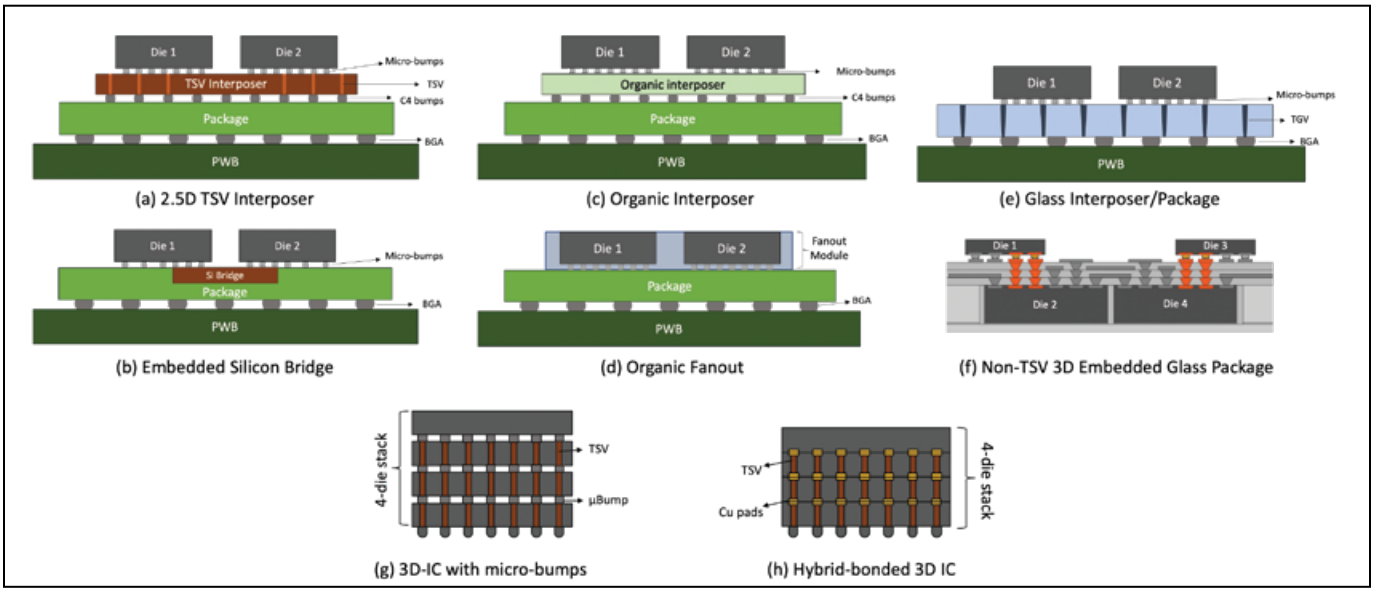

Figure 6: Schematics of various approaches for heterogeneous integration.

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and conductor using photolithographic processes. While these processes are well-known, their use in advanced HDI packaging is limited because of two main challenges: 1) Large total thickness variation (TTV) leading to nonplanar surfaces; and 2) Dimensional instability due to a decrease in elastic modulus with temperature. Nevertheless, there is a continuous push towards advancing the scope of laminates in advanced packaging for cost reasons, which has led to significant advances in materials for core and dielectric, along with process advances in micro-via technology, and lithography. The most advanced BT-epoxy laminate core today has a CTE of 3ppm/K, a T_g of 300°C, and an elastic modulus of 34GPa measured at 25°C [19]. The assembly bump pitch today is as low as 80µm in production and <55µm in research and development [20,21]. The smallest line, via and capture pad reported to date by Shinko are 2µm line width, 10µm via diameter with a 25µm capture pad, leading to a wiring density of 145 IO/mm/layer [22].

In wafer-level fan-out (WFO), or fan-out packages, the redistribution wiring and IOs extend outside of the die footprint onto the molded fan-out region where the packages are balled for assembly. Infineon was the first company to introduce WFO packages for radio frequency (RF) and analog applications [23]. The first high-volume production of embedded fan-out packages (WFO) occurred when TSMC manufactured these for the Apple iPhone 7 in 2016, using integrated fan-out (InFO) technology [24]. Although fan-out packaging has only been applied to mobile applications today with a die size of 13x13mm^2 and an assembly pitch of 80µm, several fan-out packages are being developed for larger ICs with a <40µm assembly pitch tailored for high-performance computing (HPC) applications. Based on the manufacturing process flow, they can be grouped into chip-first and chip-last fan-out approaches.

In chip-first fan-out packages [25], dies are reconstituted into 300mm round wafers and molded with epoxy-based molding compounds before fabricating the RDL on these molded wafers. On the other hand, in chip-last fan-out packages, the RDL is fabricated on a temporary carrier upon which the ICs are assembled and then molded. The fan-out module is then released from the carrier for package substrate attachment. Chip-first packages enable ultra-thin form factors, avoid the need for chip-level assembly, and provide a way to further scale IO count beyond assembly limits. Because these interposers do not have chip-level bumps, they do not suffer from electrical parasitics arising from solder-based interconnects. This can result in improved signal integrity (SI) and better power delivery to the dies [26]. As we move to finer IO pitches, an important consideration for the selection of process technology is the testability for known-good-die (KGD). Yield and cycle time are also important differentiators for both these technologies. While in chip-last packages, the KGDs are assembled after substrate manufacturing and therefore enable testing. In chip-first packages, however, the dies are committed to the package prior to interconnect formation and therefore, "lost" in the event of wiring yield loss. Today, chip-last packages support 2/2µm L/S using 3-4 wiring layers and 40µm assembly pitch, while chip-first packages are at 5/5µm L/S with 3 layers and 80µm IO pitch [27].

Glass-based approach

Glass has been in consideration as a core material for interposer substrates because of the following advantages [28,29]: 1) glass is available in large panels (used in displays like organic laminate panels today) unlike the wafer forms of silicon; 2) glass is a low-loss, insulating material compared to CMOS-grade silicon, which is a lossy semiconducting material; 3) the ultra-smooth surface of glass – like a silicon wafer – is ideal for fine-pitch, high-density RDL fabrication processes using photolithography and planarization; and 4) glass has good dimensional stability with a high Young's modulus of 70GPa like silicon (120GPa) and, therefore, shows lower warpage as compared to organic laminate substrates (that have a modulus between 20–35GPa). The CTE of glass can be tailored between 3–10ppm/K. This property, combined with the high Young's modulus of glass, is ideal for direct assembly of a glass interposer to a PWB. This is shown in **Figure 6e**, which uses a glass CTE of 7–9ppm/K. This packaging architecture of a 2.5D glass interposer that is also the BGA package module (the package substrate can be removed), can be directly assembled onto a PWB, mitigating the parasitics arising from bulky BGA organic packages. In research, glass interposers have been demonstrated with 2/2µm L/S with 4-8 layers of wiring, 40µm assembly pitch and 800µm BGA pitch. As interposer sizes grow towards 100x100mm^2 and beyond, glass interposers can become an ideal candidate provided the throughput of through-glass via (TGV) drilling and thin-glass handling in manufacturing lines can be improved.

In **Table 2** we provide a comparison between the various 2D approaches considered based on the metrics discussed earlier [30,8,31,32,33,29]. In the table we also include silicon interconnect fabric (silicon IF), an approach being developed where dies are assembled onto a 300mm silicon wafer with RDL layers, where the wafer forms the system akin to wafer-scale integration [31]. The dielectric constant (D_k) shown in the table corresponds to the dielectric material used for the interconnections and does not represent that of the core material. For example, in silicon-based approaches, the dielectric used is SiO_2 with a D_k of 3.9. Apart from lowering the standalone interconnect loss, a lower dielectric constant can also help reduce channel-to-channel crosstalk. In chip-first fan-out, [31] shows superior bandwidth density because of the lower dielectric constant of the material.

3D architectures. 3D stacking, is one of the best approaches for achieving ultra-high die-to-die bandwidth because the transistors are in close proximity to each other. While such approaches support short interconnect lengths, they are often times limited by: 1) area occupied by TSVs because they are much larger than the transistors; 2) challenges associated with power delivery through multiple stacks; and 3) poor thermal dissipation for dies at the bottom of the stack. There have also been a few non-TSV based 3D approaches as an alternative to foundry-only 3D stacking options. While these solutions address the drawbacks of TSVs, they are often limited by the number of dies connected in 3D form and therefore, a hybrid combination of 2D and 3D solutions is necessary for scaling the performance of a system.

TSV-based 3D

Because 3D stacking is largely a semiconductor foundry-based process, it requires a combination of many key technologies. First of all, TSVs are formed in the dies typically using the Bosch process, where the barrier layers are insulated and metallized. The second key technology is in wafer thinning (die thickness <100µm) that enables die stacking with reasonable

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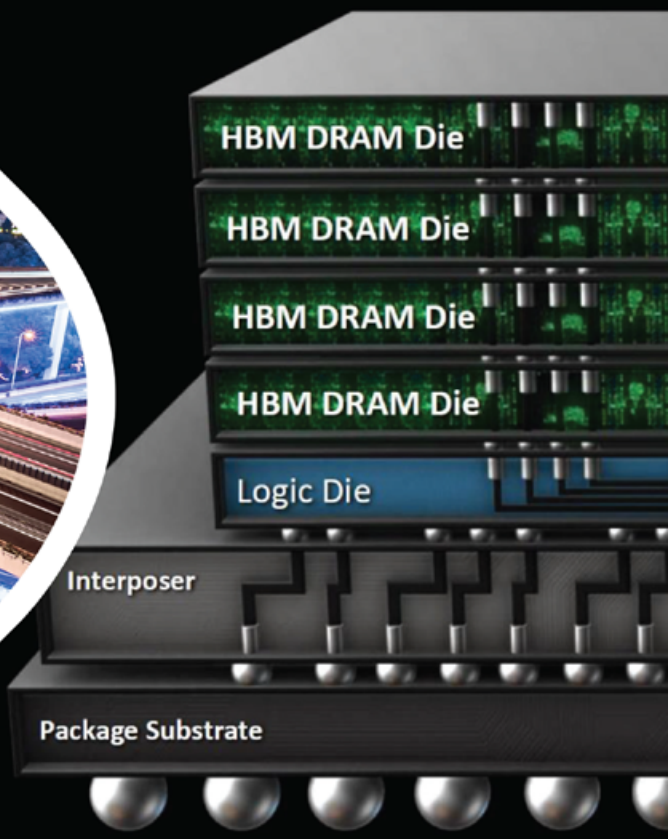

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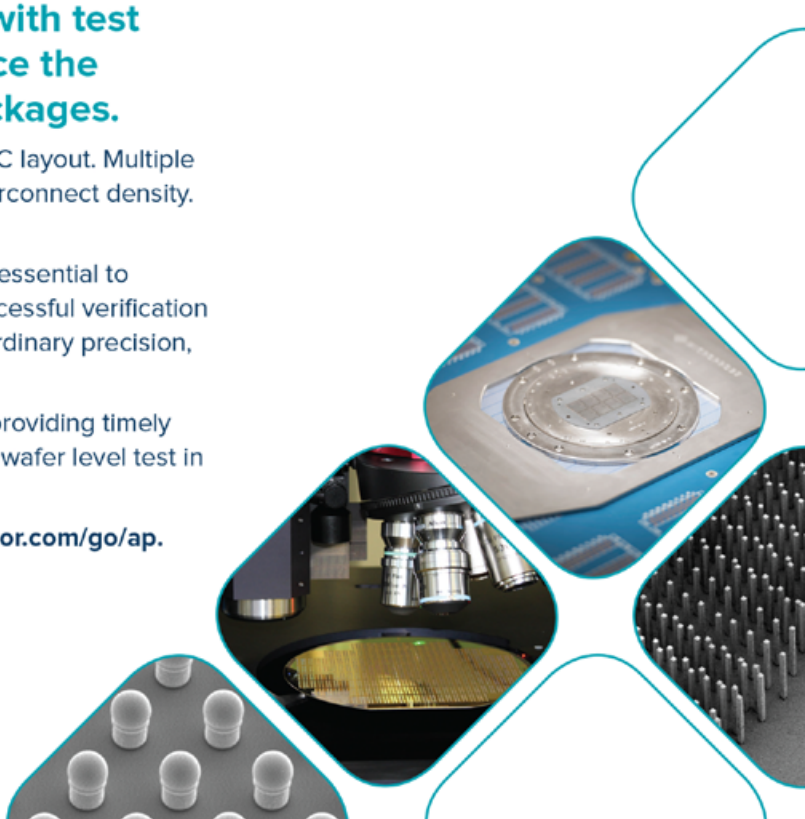

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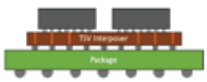
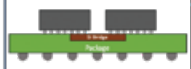
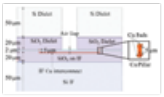
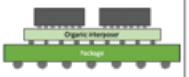
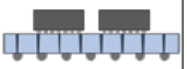
	2D/2.5D integration					
	Silicon			Organic		Glass Interposer [29]
	TSV Interposer [30]	Si Bridge (EMIB) [8,9]	Silicon IF [31]	Organic Interposer [32]	Chip-last Fanout [33]	
						
Status	Commercial	Commercial	Research	Commercial	Development	Research
Dielectric constant	3.9	3.9*	3.9	3.0*	3.2	2.5-3.0
IO pitch	50 µm	45 µm	10 µm	55 µm	40	55 µm
Interconnect length	5 mm	5 mm	0.5 mm	6 mm	1 mm	2.5 mm
Interconnect density	250 IO/mm/layer	300 IO/mm/layer	n/a	25 IO/mm/layer	500 IO/mm/layer	250 IO/mm/layer
V_{swing}	1.2 V	1 V	1 V	0.15 V	1 V	1 V
$R_{on}/C_{Tx}/C_{Rx}$ (Ω/F/F)	39/0.4p/0.4p	50/0.5p/0.5p	30/50f/50f	n/a	50/0.4pF/0.4pF	30/0.3pF/0.3pF
Data rate/IO	2 Gbps	5 Gbps	4.21 Gbps	20 Gbps	9.5 Gbps	9.2 Gbps
Bandwidth density	500 Gbps/mm	1500 Gbps/mm	1300 Gbps/mm	500 Gbps/mm*	4750 Gbps/mm	2300 Gbps/mm
Energy-per-bit	1.025 pJ/bit*	1.2* pJ/bit	0.4 pJ/bit	0.58 pJ/bit	0.78 pJ/bit*	0.36 pJ/bit

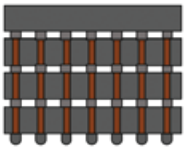
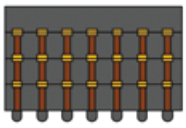
** Derived metric*

Table 2: Comparison of 2D approaches.

heights while also exposing the TSVs. Finally, the dies are stacked on top of one another through bonding techniques such as micro-bump (**Figure 6g**) and hybrid bonding (**Figure 6h**).

Micro-bumps typically consist of a copper pillar with a solder cap, which is reflowed during thermocompression bonding (TCB) to form the joints. TCB uses both high-temperature and high-pressure for allowing finer connection pitches as compared to conventional mass reflow techniques, but with a lower throughput. Examples of micro-bump 3D include Intel's Foveros and high-bandwidth memory (HBM) from SKHynix, Samsung, and Micron [34]. Bump pitches are ~40µm in production today and <20µm in research [35]. The assembly can be done either using die-to-die (D2D), die-to-wafer (D2W) or wafer-to-wafer (W2W), with each having its pros and cons relating to die size, yield, throughput, handling, and cost [36].

In hybrid bonding, as in TSMC's System on Integrated Circuit (TSMC-SoIC™) [37], the dies are bonded together using a two-step process, namely: 1) a dielectric-to-dielectric oxide bond followed by, 2) a metal-to-metal Cu-Cu bond. Hybrid bonding can be used for both D2W and W2W. The main advantage of such a technology is that it allows assembly pitch scaling beyond solder and overcomes several of the assembly limitations. Because of the close proximity of the transistors in adjacent dies, it allows the dimensions of pads and bumps to be reduced, thereby dramatically decreasing the electrical parasitics of the interconnections. At 2GHz, hybrid bonds can support a

	TSV-based		Non-TSV
	3D IC /w TSV [40]	Hybrid Bonding [37]	3D Glass Embedding [39]
			
Status	Commercial	Commercial	Research
Dielectric Constant	3.9*	3.9*	2.5-3
IO pitch	40 µm	10 µm	20 µm
Interconnect length	75 µm*	50 µm*	35-50 µm
Interconnect density (IO/mm^2)	625	10000	2500
V_{swing}	0.7 V*	1 V*	1 V
$R_{on}/C_{Tx}/C_{Rx}$ (Ω/F/F)	n/a	n/a	50/50f/50f
Data rate/IO	1.69 Gbps	n/a	1.86 Gbps
Bandwidth density	1.76 $Tbps/mm^2$*	n/a	4.65 $Tbps/mm^2$
Energy-per-bit	76.2 fJ/bit	7 fJ/bit*	11.2 fJ/bit

** Derived metric*

Table 3: Comparison of 3D approaches.

150x lower RC and a 12.5x lower IR drop when compared to micro-bumps [35]. However, hybrid bonding requires stringent surface planarity and usage of advanced cleanrooms, thereby limiting the potential use of this technology in a package foundry. The bump pitches today are <10µm, and with improved tools and alignment techniques, the pitch can be further scaled down to 1µm and below [38]. Hybrid bonding not only eliminates the need for bumps, but also reduces the pad sizes, thereby significantly improving energy-efficiency (as shown in **Table 3**).

Non-TSV based 3D

Figure 6f shows a non-TSV 3D architecture [39] using packaging technologies as opposed to foundry-only methods for creating 3D stacks. This architecture allows dies from multiple foundries to be connected, thereby enabling true heterogeneity. Such an architecture does not need TSVs in the logic die to establish short interconnect lengths and therefore can improve signal integrity, reduce real estate in expensive dies, and decreases overall system cost. As shown in **Figure 6f**, the solution consists of multiple embedded dies and assembled dies connected using RDL. There is no assembly required for the embedded dies. In research, the IO pitch today for such a package is at 20µm with 2/2µm for L/S and three metal layers. Unlike 2D approaches, because 3D solutions have area connections between two dies, we compare the three 3D approaches in **Table 3** separately, based on the metrics described earlier [40,37,39].

Future needs

As applications emerge in AI, there is a need for continuous interaction and learning from the environment. This requires neuro-evolution in hardware, where inferences need to be supported in the absence of pre-trained deep neural networks (DNNs) and labeled data sets, where energy and latency are of paramount importance. For such emerging applications a requirement is to evolve the DNN topology continuously in response to rewards using evolutionary algorithms. For such architectures, data movement with low energy per bit (EPB) and high-bandwidth density become even more critical. As shown in **Figure 7**, data movement can be separated into two major parts, namely: 1) over longer distances where interaction and data collection from the environment is necessary; and 2) over shorter distances for energy-efficient computing. The best mode for interaction with the environment is through wireless using emerging technologies such as 5G (24GHz–100GHz) and beyond (6G over 100GHz) to support the bandwidths required. Using these technologies requires integration of RF dies (GaAs, InP, power amplifiers, and Si beam formers) along with front-end circuity such as antenna arrays, passive elements such as matching networks, power dividers, diplexers and others, along with embedded and assembled dies in the interposer, as shown in Figure 2d (in Part 1). The heat flux for these dies varies between 0.2W/mm^2 for 5G to 2W/mm^2 for 6G, making the thermal management solutions quite challenging especially when the heat needs to be removed from the back side of the die through the package substrate. Such heat removal capabilities require new thermal interface materials with high thermal conductivity, and low CTE for reducing stresses.

The interposer described in Figure 2d (in part 1) consists of HBM, CPU, GPU, HMC and PIM accelerators. The CPU and GPU communicating with the 3D stack (HBM and HMC) support near-memory processing, while the processor in memory accelerators is added to further improve efficiency. Because the energy per bit is directly proportional to capacitance, achieving high energy efficiency requires the use of ultra-low dielectric constant materials in the interposer. As described in [27], a reduction in dielectric constant (D_k) from 3.9 to 2.4, can reduce the EPB by 40% for the silicon interposer with an interconnect length of 5mm. Along with low D_k, the ideal dielectric material to maximize reliability should support a thickness ≤5µm, with moisture absorption<0.1%, tensile modulus <2GPa, tensile strength >100MPa, residual stress <10MPa, elongation >30%, CTE<50ppm/°C, and contain no fillers. Such materials are unavailable today, and therefore, materials that meet most of these properties are required. It is important to note that a low D_k combined with a thicker dielectric helps improve the efficiency of integrated antennas provided the dissipation factor can be kept low (D_f<0.01@ sub-THz).

To scale the interconnect density beyond 500 IO/mm/layer, it is important to achieve a reduction in the L/S value so that it is less than 1µm along with reducing the microvia and pad diameters. From [1] in part 1, lowering pad diameter D increases the IO count and routing on a single layer. Lowering the number of layers is critical to reducing package thickness, improving overall yield, and lowering warpage.

The other key parameter is assembly pitch. Solder-based assembly is now reaching fundamental limits in pitch scaling as dimensions reduce below 30µm. With emerging applications requiring current handling capability exceeding 10^4A/cm^2, operating temperatures above 85°C, and thermomechanical reliability at small stand-off heights, new technologies are required. One approach is hybrid bonding for scaling IO pitch to <1µm. However, this process is foundry-limited and current options for high-throughput <20µm-pitches compatible with advanced packaging hasn't progressed much. Cu-to-Cu assembly using thermocompression bonding in a package foundry is a key enabler that can replace solder, provided reliability through improved compliance and higher-throughput can be achieved [41].

The EPB in interposers can be further reduced by decreasing interconnect length using a combination of fine-pitch assembly and reduced L/S. For example, an assembly pitch of 10µm with L/S of 1/1µm can reduce length by 75% and improve interconnect density by 120% as compared to a 55µm pitch and L/S of 2/2µm. Because wire lengths are reduced, such scaling can significantly decrease latency, increase bandwidth density, and improve signal integrity—all important metrics that are desired for emerging AI solutions.

The platform voltage (VR) on the PWB supports voltage conversion ratios of 48/12 and 12/1 for data center applications. The large currents from the VR powering the CPUs create routing losses, and because of their square law dependence on current, they reduce the overall system efficiency. To achieve power efficiencies of 90% and above, integrated voltage regulators (IVRs) are required. The IVR needs to reside on the interposer near other dies, as shown in Figure 2d (in part 1). Because the interposer needs to support dies from multiple process nodes with different voltages, several power domains are required. Power management for AI, therefore, requires integration of several IVRs on the interposer in the form of buck regulator dies using advanced GaN devices [42]. In addition, low dropout (LDO) regulators integrated into the CPU are required for providing fine-grained power management. Because buck regulators require storage devices, inductors and

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capacitors are necessary. Unlike capacitors, inductors require a larger footprint and therefore, their integration in the interposer becomes necessary using magnetic materials [43]. Along with magnetic material selection and process development, the design and integration of these inductors pose unique challenges that require significant co-design effort between the die and interposer.

As multiple dies are assembled and connected, the size of the interposer is bound to increase. The current trend in advanced packaging is towards supporting high interconnection density using fine-L/S (<1µm) and increasing pin count to support power delivery requirements. However, the maximum interposer size is restricted to 3000mm^2—either limited by reticle size for silicon, or warpage and nonplanarity-related issues for organics. We believe that future interposers would require larger sizes of 10000mm^2 that can support fine-L/S of 1µm or less. As package sizes increase, the dimensional stability of the substrate and CTE of the substrate need to be carefully chosen to manage wafer/panel warpage during processing. Panel-scale processing (on glass or organics) is seen as a path forward for cost-efficient scaling of the interposer size. Such processes today are limited to display technologies (glass) and low-IO count analog device manufacturing (laminates and panel fan out). Large-area lithography, precision deposition and etching tooling are needed to take this to high-volume manufacturing.

As neural networks (NNs) become more complex, increasing bandwidth density and reducing latency require connectivity between interposers through the package substrate. In such scenarios, optical IOs in the interposer and optical waveguides in the package substrate become necessary for communication over longer distances through serialization of data. SerDes is an option for supporting such functionality. However, SerDes-based approaches are not energy efficient because the EPB is around 23pJ/bit for transmission distances of ~1cm with data rates of 40Gb/s/lane (a bit error rate [BER] of 10^{-9}). An energy-efficient solution is the use of optical waveguides integrated into the package substrate coupled to

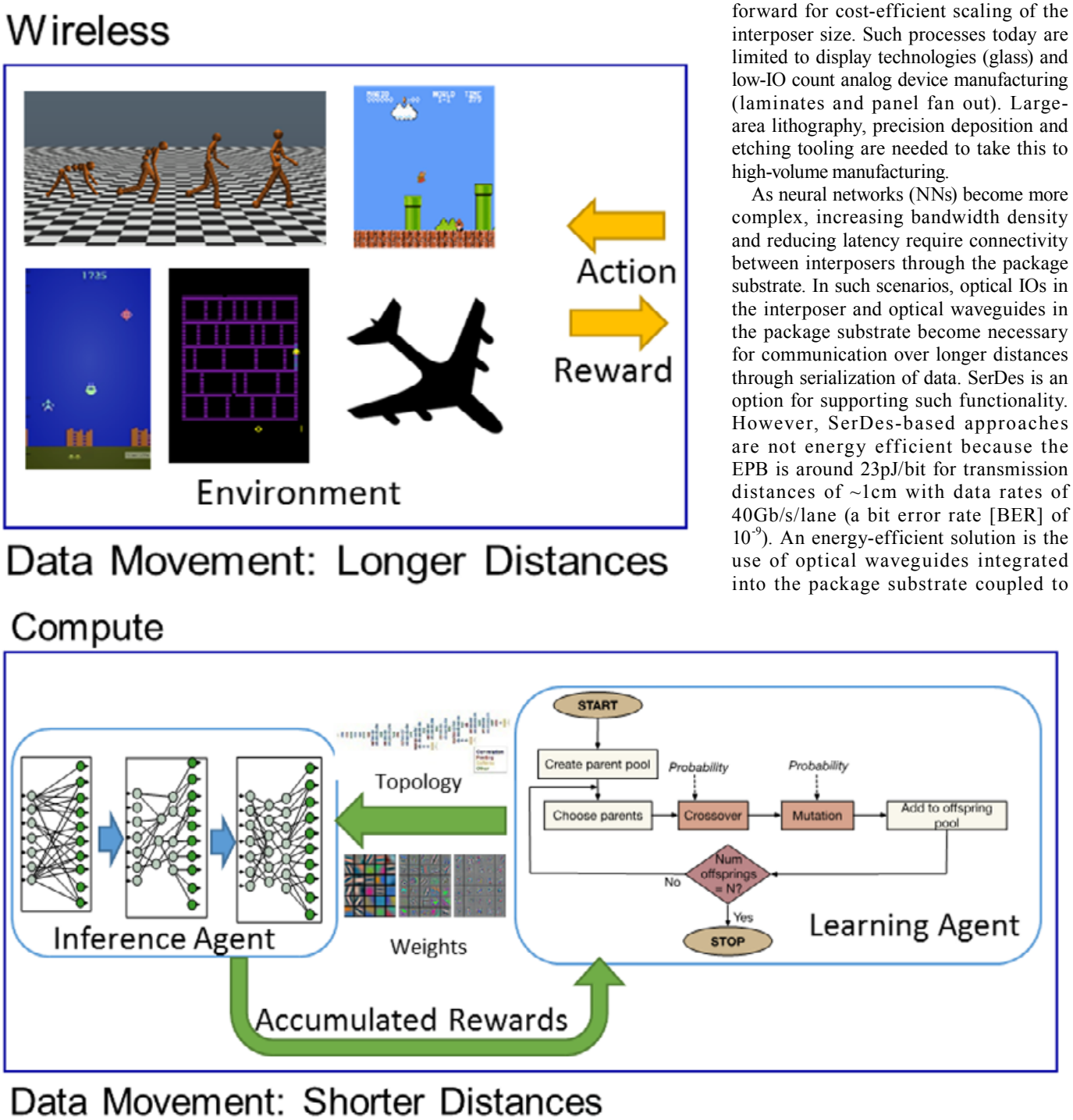

Figure 7: Continuous learning for AI using neuro-evolution in hardware. (Courtesy T. Krishna, Georgia Tech)

the optical IOs in the interposer where EPB≤1.2pJ/bit can be achieved with a 10^{-12} BER while supporting a data rate of 896Gb/s/lane over distances of 5cm or more. Another option is the use of optical fibers providing direct connectivity between interposers. The network integrated circuit (NIC) and photonic integrated circuit (PIC) dies shown in Figure 2d (in part 1), therefore, represent essential dies that need to be integrated in the interposer for serialization/deserialization of data and transmission. Optical coupling efficiency, waveguide loss and fiber alignment continue to be major challenges for achieving integrated photonic solutions.

Summary

For 3D stacking, power delivery and thermal management continue to be major problems. Emerging nonvolatile memory (NVM) devices such as resistive random access memory (ReRAM) and ferroelectric field-effect transistor (FeFET) integrated into 3D processing-in-memory (PIM) architectures suffer from stochastic variations in device properties and are very sensitive to temperature. As an example, the inference accuracy of ReRAM can be retained over long periods only if the junction temperature can be maintained below 85°C. Thermal management of NVM devices integrated into 3D stacks, therefore, represents a major challenge without which PIM- or HMC-based architectures may not be viable. Embedded fluidic channels in the stack for cooling these devices are therefore critical, which is an ongoing research area in academia.

To summarize, a combination of 2D packaging and 3D stacking are required for supporting current and emerging AI applications. With Moore's Law slowing down, advanced packaging is the path forward for continuing it at least for the next decade. The capability of interposers has advanced significantly in the last few years and this trend needs to continue. Advanced interposers of tomorrow will need to support digital, RF and optical functionality combined with high energy efficiency, low latency, and high bandwidth density—three metrics that will drive the next-generation of packaging technologies. Though HBM has become prevalent, 3D stacking of logic and memory continue to pose problems because of thermal management, and unless embedded cooling methods are developed inside the 3D stack, they will continue to pose problems.

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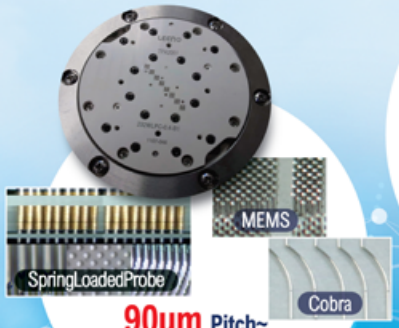
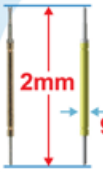


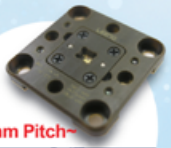
90um Pitch~ Probe Head



Specification

Pitch : Min.120um
Spring Force : 8.0g@ 250um
Current Rating : 1.0A
Inductance : 0.38nH

RF Probe for Fine Pitch Probe Head

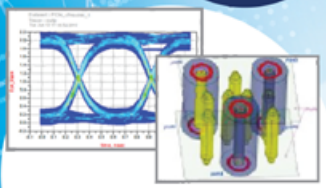

0.18mm Pitch~ RF Coaxial Spring Probe & Impedance Controlled


Logic Test Socket

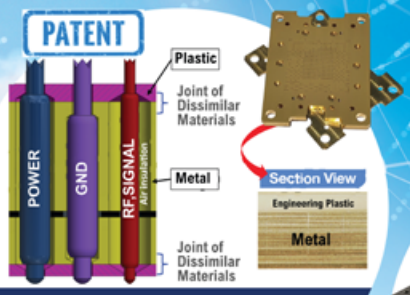

High Speed

Frequency : >20GHz
VSWR : < 1.2

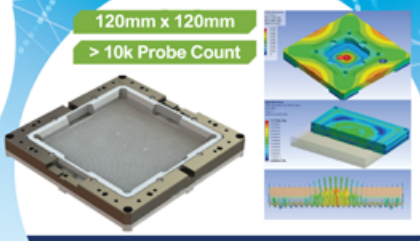
Automatic Coaxial Probe


Electrical Analysis

CCC Test, HFSS, TDR
Eye Diagram
4 Port VNA Test



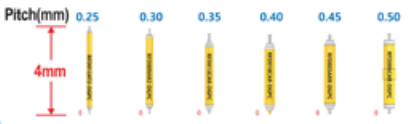
MP Socket



Large Device Socket

Specification

Frequency : 80GHz(BGA),
100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%



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Wafer-level polymer/metal hybrid bonding using a photosensitive permanent bonding material

By Baron Huang, Mei Dong, Shelly Fowler, Andrea Chacko, Rama Puligadda [Brewer Science, Inc.]

Downscaling is a never-ending task for the semiconductor industry to meet the ever-increasing electronic system demands for higher performance and functionality, smaller system form factor, and lower power consumption and cost. Moore's Law drove the industry for decades to double the number of transistors on a chip with node scaling for 2D device fabrication. However, the development of next-generation silicon node manufacturing becomes more and more challenging and costly because of lithography limitations.

System scaling for 3D device fabrication is an emerging concept for integrating more functional materials along with various semiconductor technologies in a chip, or more chip carrier packages stacked through advanced packaging and manufacturing process technologies [1-2]. Devices with higher bandwidth and with better power and signal integrity can then be achieved in a more economical way through finer-pitch die-to-die interconnection.

Bonding technology offers a z-axis direction of integration playing an important role in realizing 3D device fabrication. Chips or wafers with different functional or process technology can be fabricated separately and then stacked and integrated together by vertical bonding integration. The hybrid bonding technology, based on metal-to-metal and dielectric-to-dielectric bonding simultaneously with the die-to-die interconnection pitch shrinking down to sub-10µm has proven to be an effective way to enhance performance and density of die-to-die interconnects and can be used extensively in many computing and memory applications in the future [3].

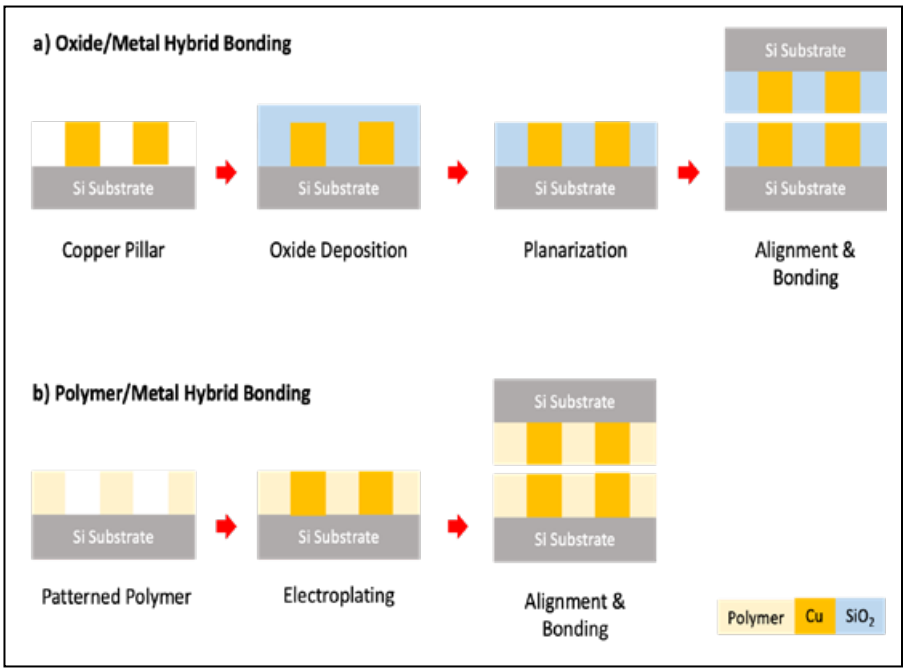

Figure 1: Process flow for wafer-level hybrid bonding using a) oxide, and b) polymer as a dielectric.

Dielectric/metal hybrid bonding

Conventional hybrid bonding uses silicon dioxide as a dielectric to fill up the interspace between micro-interconnections to enhance bond strength and reliability. Also, it can prevent metal oxidation during the bonding process. **Figure 1a** illustrates the process flow for the use of inorganic oxide as a dielectric for the oxide/metal hybrid bonding. However, there are some issues using silicon oxide for hybrid bonding. First, silicon oxide has poor stress absorption because of its high modulus and the hardness of silicon oxide makes it difficult to flow or deform in the bonding interface. As a result of these challenges, using silicon oxide requires an extra chemical mechanical polishing (CMP) process before bonding to ensure the bond interface is extremely flat (~1nm) to achieve a successful bonding.

Polymeric bonding material has a lower modulus than inorganic silicon oxide, and has been widely used in many fields of wafer-level bonding. Polymeric bonding materials exhibit good bond-line quality and excellent tolerance to surface topography [4]. The use of a polymeric bonding material as a dielectric layer provides several advantages including: 1) the polymer can flow better compared to oxide to fill air gaps between metal wires or pads during the bonding process and results in improvements to the quality and reliability of the bonded stack. Additionally, 2) the CMP process for the surface planarization prior to bonding could possibly be skipped with a better bonding capability and bonding strength from the polymeric bonding material. **Figure 1b** shows the process flow for using polymer as a dielectric for the polymer/metal hybrid bonding. However, the concern for using polymeric bonding material is that most of the polymer dielectric materials require 300°C or higher temperature for curing, which will limit the type of metals that can

be used and the thermal budget for the overall processes.

In this paper, a wafer-level polymer/metal hybrid bonding is demonstrated by using a developmental low-curing-temperature photosensitive permanent bonding material as the dielectric. Therefore, the thermal budget of the integration process can be controlled at 250°C. In addition, the merits of the photosensitive permanent bonding material including low dielectric constant and dissipation factor, superior thermal stability, low processing and curing temperatures, and excellent bonding strength, make it an attractive candidate for the future development of polymer/metal hybrid bonding to replace the current oxide/metal hybrid bonding.

Mechanical Properties

Cure Temp (°C)	Tensile Strength (MPa)	Elongation (%)	Modulus (MPa)	CTE (ppm/°C)	T_g (°C)	T_d (°C)	Moisture Uptake (%)	Thermal Conductivity (W/mK)
180	12.4	112	171	157	85	373	0.02	0.25

Electrical Properties

Dielectric Constant (10 GHz)	Dissipation Factor (10 GHz)	Breakdown Voltage (V/µm)	Volume Resistivity (Ω-cm)
2.6	0.0016	TBD	6.99×10^{16}

Reliability Test

THST (85°C/85% 96 hr)	TCT	b-HAST
Pass	TBD	TBD

Table 1: Material properties of photosensitive permanent bonding material (PS PBM).

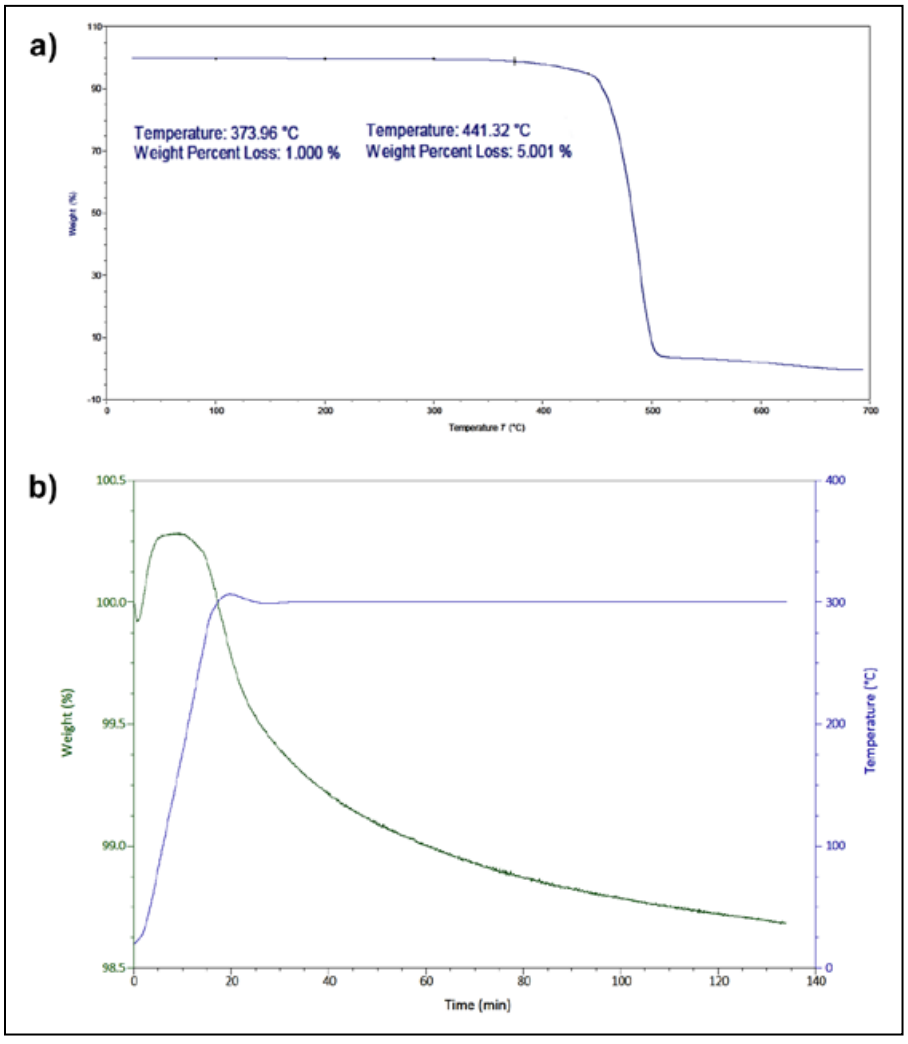

Figure 2: a) Ramp and b) isothermal TGA scan images for PS PBM under nitrogen (with a ramp of 10°C/min).

Photosensitive permanent bonding material (PS PBM)

A developmental photosensitive permanent bonding material (PS PBM) is proposed by Brewer Science, Inc. for the polymer/metal hybrid bonding application. The PS PBM can be coated at various film thicknesses, ranging from 3µm to 20µm in a single coat, which is good to cover most bumps or other surface topographies without causing much stress on the wafer stack.

Compared to most polymeric bonding materials, which require 300°C or higher for curing, the cure temperature for the PS PBM is only 180°C, allowing the thermal budget of the integration process to be greatly reduced. As a dielectric, the PS PBM possesses a low dielectric constant of 2.5 and a dissipation factor of 0.0016 at a frequency of 10GHz. The low Young's modulus and high elongation ensure it has the ability to absorb thermally-induced stress created during thermal processes, resulting in minimal bowing of the bonded substrates. The general mechanical, electrical, and reliability properties of the PS PBM are summarized in Table 1. The points outlined above are discussed in the sections below.

Thermal stability. The thermal stability of the PS PBM is evaluated using ramp and isothermal thermogravimetric analysis (TGA) (see Figure 2). The result shows the PS PBM has a good thermal stability with 1% weight loss at 373°C and a 5% weight loss up to 441°C in a nitrogen atmosphere. The isothermal TGA for the PS PBM heated at 300°C for 2 hours in nitrogen shows there is only about a 1% weight loss during thermal processing. The excellent thermal stability of the PS PBM ensures it has a good thermal budget, which is required for metal annealing and other thermal processes used for hybrid bonding.

Patterning performance. The PS PBM is designed as negative tone and sensitive to i-line (365nm) light sources. To demonstrate the patterning capability,

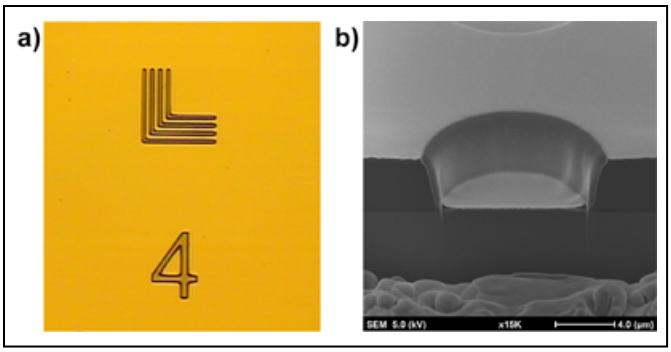

Figure 3: Patterning capability of PS PBM: with a) a microscope; and b) cross-section SEM inspections.

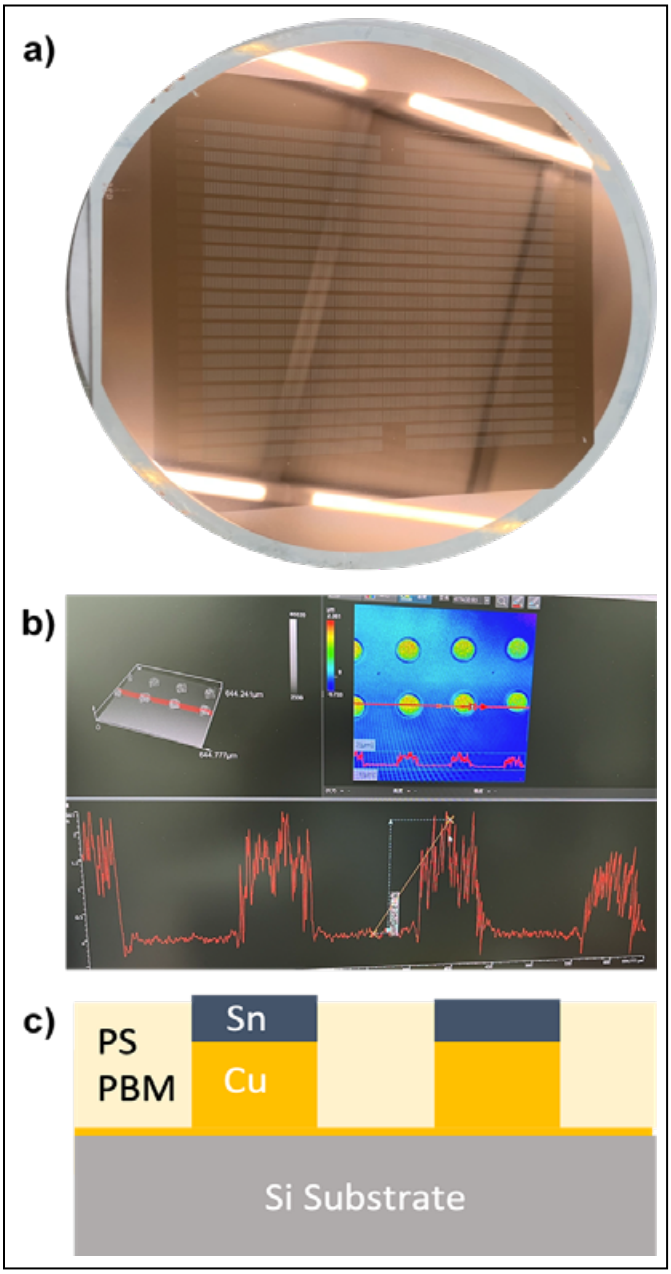

Figure 4: a) A patterned PS PBM wafer with electroplated Cu-Sn; b) a microscope image of a Cu-Sn bump; and c) a schematic of the structure.

a 5µm-thick film of the PS PBM was spin-coated onto a 100mm wafer. The wafers were contact-baked on hot plates at 60°C for 5 minutes and 120°C for an additional 10 minutes for soft bake. Exposure was conducted by an i-line mask aligner at an exposure energy of 100mJ/cm^2. The wafer was then developed using a puddle develop process with cyclopentanone as the developer. Figure 3 shows the fine-pitch patterning capability of the PS PBM for a 4µm line/space feature with a 5µm thickness PS PBM film (based on microscope inspection) and a steep sidewall angle (~90°) based on a cross-section measured using a scanning electron microscope (SEM) on a 10µm via pattern.

Cu-Sn electroplating. A silicon wafer with a patterned PS PBM was fully cured at 200°C for 1 hour for the metallization with electroplating. A Cu-Sn metal stack was selected for bonding because of the low metal annealing temperature at 250°C. A critical condition for the experiment is the metal height design and control because there is no surface planarization applied before the wafer-level bonding. In this study, we used Cu-Sn bumps with 2µm-thick Sn and 4µm-thick Cu electroplated on the patterned wafer with the thickness of the PS PBM film being 5µm. The Cu-Sn electroplated PS PBM wafer, its microscope image, and the schematic structure are shown in Figure 4.

PS PBM/Cu-Sn hybrid bonding. Finally, two PS PBM patterned silicon wafers with Cu-Sn plated metals were bonded together without CMP for surface planarization. The wafer-level hybrid bonding was conducted at 250°C for 60min with a bonding pressure of 20kN to form an interconnection between the layers. The bonded wafer pair was further analyzed by

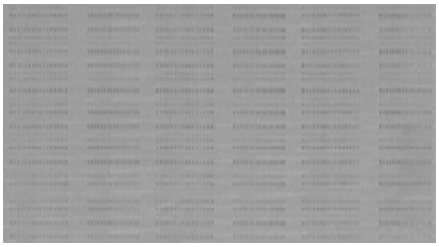

Figure 5: An SAT image of the metal interconnects area for a PS PBM/Cu-Sn bonded stack.

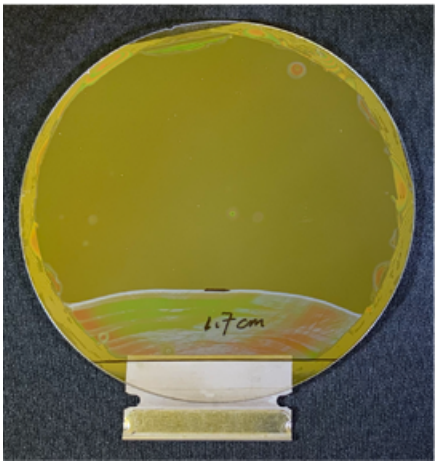

Figure 6: Wafer-level Maszara bond strength test.

scanning acoustic tomography (SAT) to inspect the bonding quality. **Figure 5** shows a magnified view of the SAT image focused on the metal interconnects area, which demonstrates a good bond line quality with no voids on both the PS PBM interfaces (light gray area) and the metal-to-metal contacts (dark gray area).

Bond strength. Silicon wafers coated with the PS PBM were bonded together to evaluate the bond strength of the polymeric bonding material. The bonding was carried out at 150°C, 8kN, for 15min. The temperature used for bonding the PS PBM itself is much lower than the temperature for PS PBM/Cu-Sn hybrid bonding because there is no metal annealing required. Actually, the PS PBM can be bonded at <100°C, or even room temperature. A detailed study will be published in a separate paper at the Electronic Components and Technology Conference (ECTC) later this year.

The bond strength was evaluated with a Maszara razor blade test at wafer-level [5-6] with the PS PBM in a fully-cured state before bonding. The test is performed by inserting a razor blade between the bonded PS PBM wafer pairs, and then measuring the resulting crack length via visual or infrared inspection. **Figure 6**

shows the razor blade test on a silicon-to-glass configuration with a measured crack length of 17mm. The corresponding bond strength was determined using the Maszara model to be >2.5J/m^2, which is greater than the bulk fracture strength of silicon. These results indicate the PS PBM has the strong bond strength required for hybrid bonding and is better than bonding with inorganic silicon oxide or silicon carbon nitride as the dielectric (0.9-1.8Jm^2) [7].

Summary

This paper introduces a developmental photosensitive permanent bonding material with features of a low dielectric constant and dissipation factor, superior thermal stability, and low processing and curing temperatures.

The fine-pitch patterning capability of the PS PBM is also shown, supporting its use for dense die-to-die interconnection. With proper design and control in metal height, the PS PBM/Cu-Sn structure has demonstrated a good wafer-level hybrid bonding quality between metal-to-metal and between polymer-to-polymer interfaces without CMP processing for surface planarization. The bond strength for the PS PBM was then evaluated to be stronger than using silicon oxide as the dielectric. More evaluations such as grinding, reliability, and electrical performance for the hybrid bonded stack with PS PBM will be conducted and shared in the future.

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Biographies

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Enabling low-profile LSCs for automotive flip-chip packaging

By Jaimal Williamson, David Chin [Texas Instruments]

Land-side capacitors (LSCs) are vital semiconductor packaging components implemented in package designs. LSCs enable a more constant voltage across different frequencies, with a primary goal of reducing device parasitics like crosstalk and impedance. One of its main advantages over other capacitor types, like die-side or top-side capacitors, is its inherent closer proximity to the silicon chip. Depending on design, LSCs can be placed less than 1.0mm from the silicon chip. As a comparison, die-side capacitors (DSCs) can be placed upwards to 4x farther from the silicon chip, as assembly keep out zone and design rules for manufacturing limit its proximity to the silicon chip. For example, in the flip-chip ball grid array (FCBGA) assembly process, underfill backflow and any resin bleed generated after the underfill dispense process can directly factor into the DSC placement and distance from the silicon chip. In the case of DSCs, the farther the distance away from the chip, the greater the deleterious implications on electrical performance, however, it is necessary to avoid assembly yield and reliability issues.

On the other hand, LSCs do not exhibit similar design rule constraints as their placement is directly underneath the die area within the ball grid array of a FCBGA package or substrate. Because LSCs are closer in distance to the silicon chip, LSCs outperform DSCs electrically. This is because LSCs minimize any positive or negative excursions around the DC voltage (noise), which can cause timing failures in digital circuits or functional failures in analog circuits. Therefore, use of LSCs lower peak-to-peak (pk2pk) noise as measured by the difference between minimum and maximum voltages as compared to DSCs (i.e., based on the aforementioned keep out zone constraints). Figure 1 showcases an illustration of both LSCs and DSCs on a FCBGA package.

One limitation of LSCs is the availability of low-profile automotive qualified capacitors per the AEC-Q200 specification at BGA pitches less than or equal to 0.8mm. Low-profile height LSCs are needed to maintain clearance between the LSC and printed circuit board (PCB) to ensure satisfactory surface mount technology (SMT) assembly. As such, to better understand assembly yield margin corresponding with the zero-defect automotive requirement, this review highlights the impact of LSC clearance height between the FCBGA package and PCB as a function of commonly employed SMT placement parameters. The purpose is to validate the efficacy of a robust SMT continuity yield with respect to non-wets and shorting as a function of clearance between the LSC and PCB. In addition, a multi-lot inspection of gap height measurements between the collapsed BGA solder ball and LSC (on package) is carried out to understand the process margin associated with chip-to-package effects (i.e., substrate size, die-to-package ratio) post-FCBGA assembly. The combination of both component- and board-level measurements between the LSC and the collapsed BGA solder ball and the LSC and PCB, facilitates a detailed understanding of SMT assembly margin for the safe launch of automotive flip-chip devices.

Background on the pick and place process

There are various types of SMT placement machines and software for handling different classes of packages. Component placement typically has two methods for accuracy that depend on machine type and placement software. Placement accuracy can be honed by understanding the balance between programming component thickness and placement speed. In essence, there are two types of SMT placement machines. The first type is based on programming in the package thickness, where the nozzle holding the part will travel that distance to release the part. Users choose the first type of programming component thickness for specific packages that require an accurate placement in terms of how deep the package is to be submerged into the solder paste (in this case in the range of 0.05mm–0.075mm). Example packages are quad flat no-lead (QFN) and small outline no-lead (SON). The

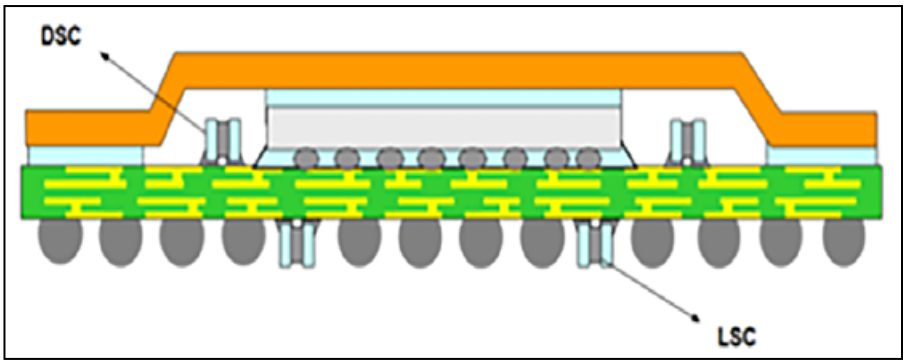


Figure 1: FCBGA package illustrating LSCs and DSCs.

disadvantages of this approach are the slower speed of placement, and an additional step to measure the package thickness during programming.

The second type of placement machine is based on using force to release the device onto the PCB. The nozzle holding the device carries the component until it touches the PCB surface with a reaction force. With respect to SMT assembly, placement force is associated with placement speed. The aforementioned method of using force (placement speed) is more common because users simply need to pick the placement speed option based on package type. For example, minimum or slow speed means a force of 2-3N, medium speed means a force of 4-5N, and maximum or fast speed means a force of 6-9N. It is customary that users choose maximum speed for packages as it offers a lower possibility of device damage during pick and place operation. Examples of devices are capacitors, resistors, and packages with leads like small outline (SO), thin shrink small outline package (TSSOP), quad flat pack (QFP), etc. As a comparison, slower speeds are usually chosen for packages such as QFN and ball grid arrays (BGAs).

SMT evaluation study

To comprehend any propensity for SMT yield loss with respect to LSC clearance issues to the PCB, five different SMT process parameters were evaluated across various conditions as defined in Table 1. As previously mentioned, SMT conditions were based on the most commonly employed methods of using package thickness and placement speed (or force) during pick and place. Referencing Figure 1, the test vehicle was a 24mm x 24mm lidded FCBGA at 0.8mm BGA pitch.

The objective of the SMT study is to evaluate if a minimum gap height of 100µm can be achieved between the LSC and PCB surface after mounting. As a rule of thumb, a gap height clearance of 100µm between LSC and PCB is used as a reference in the event underfilling the second level interconnect is required. From all SMT parameters investigated in Table 1, there were not any assembly yield

SMT parameter	SMT placement method	Output
Minimum (or slow) speed	Force	Cross-section analysis to monitor and measure the following: 1) Impact of solder bridging 2) LSC height measurement 3) Solder thickness between FCBGA BGA pad and LSC measurements 4) Gap height between LSC and PCB measurement 5) BGA solder ball stand-off height
Medium placement speed	Force	
Maximum (fast) placement speed	Force	
Release parts upon contact with PCB surface	Package thickness	
Release parts <0.1mm above PCB surface	Package thickness is programmed with an additional 0.05mm	

Table 1: Commonly used SMT placement conditions.

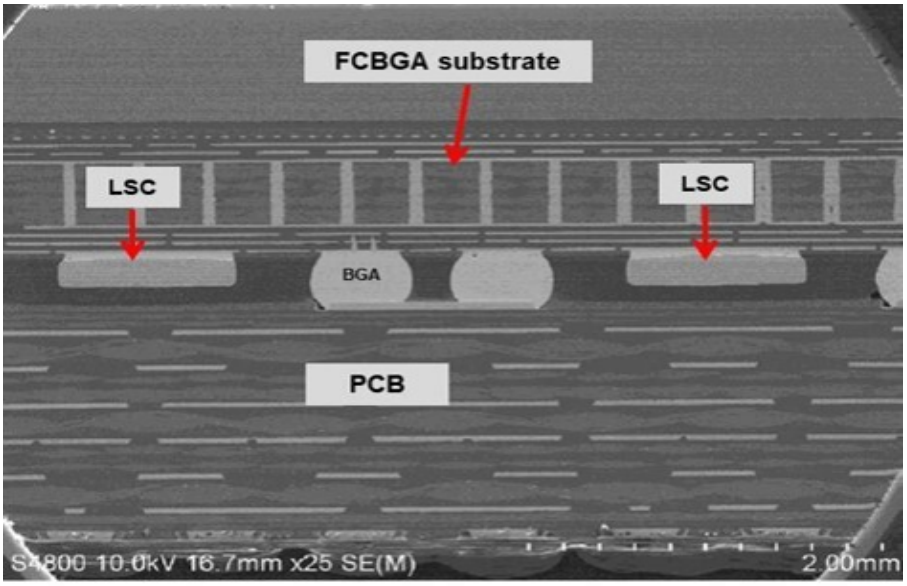


Figure 2: Image showing the FCBGA substrate mounted to a PCB.

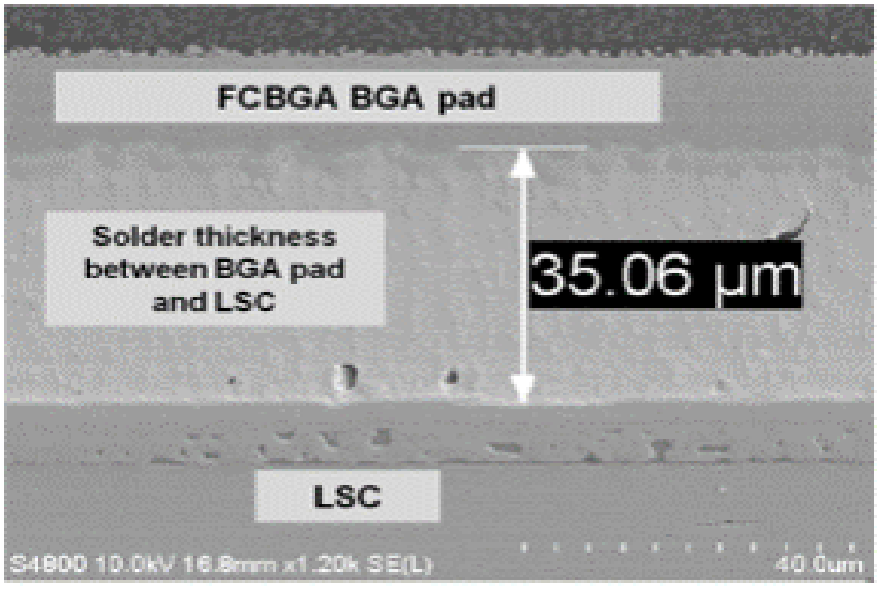


Figure 3: Solder thickness between the FCBGA pad and a LSC.

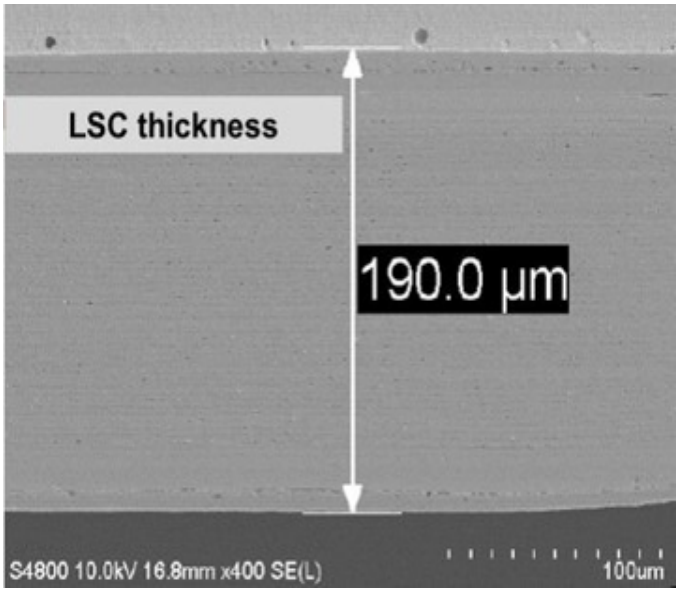


Figure 4: Thickness of a LSC.

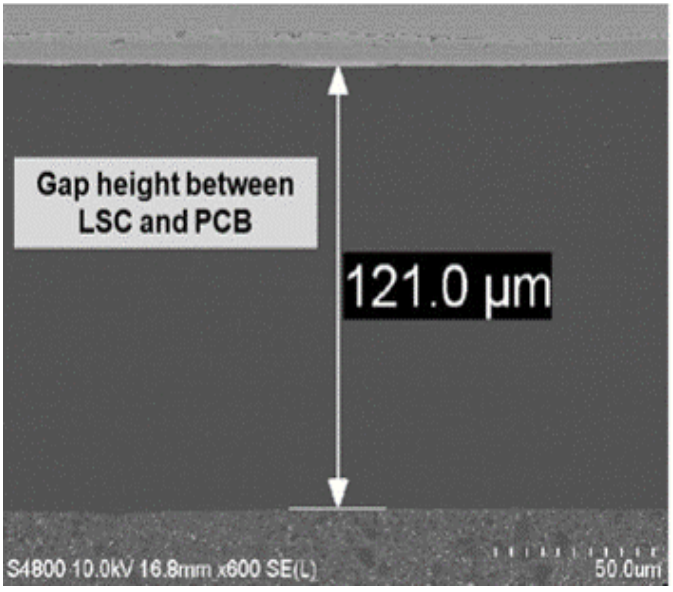


Figure 5: Gap height between a LSC and a PCB.

issues like solder bridging and non-wets among all splits. Based on cross-sectional analysis, all commonly used SMT placement conditions met the clearance target of 100µm. Figure 2-4 provide a pictorial of the outputs (i.e., as referenced in Table 1) being measured via cross-sectional analysis of FCBGA parts assembled to the PCB. Figure 2 illustrates the FCBGA package mounted to the PCB, where the FCBGA substrate, LSC, and PCB are annotated.

Figures 3 and 4 show measurements of solder thickness between the flip-chip substrate BGA pad and the LSC and the LSC thickness, respectively, which contributes to the gap height between the LSC and the PCB. Figure 5 shows the gap height or distance between the LSC and PCB.

Figure 6 shows a scatterplot comparing the relationship between the BGA standoff and gap between the LSC and PCB, where Figure 7 illustrates a moderate positive correlation is observed based on the same relationship between BGA standoff and gap between the LSC and PCB. Based on this relationship, further assembly optimization and LSC thickness control can be tuned to drive at stronger positive correlation.

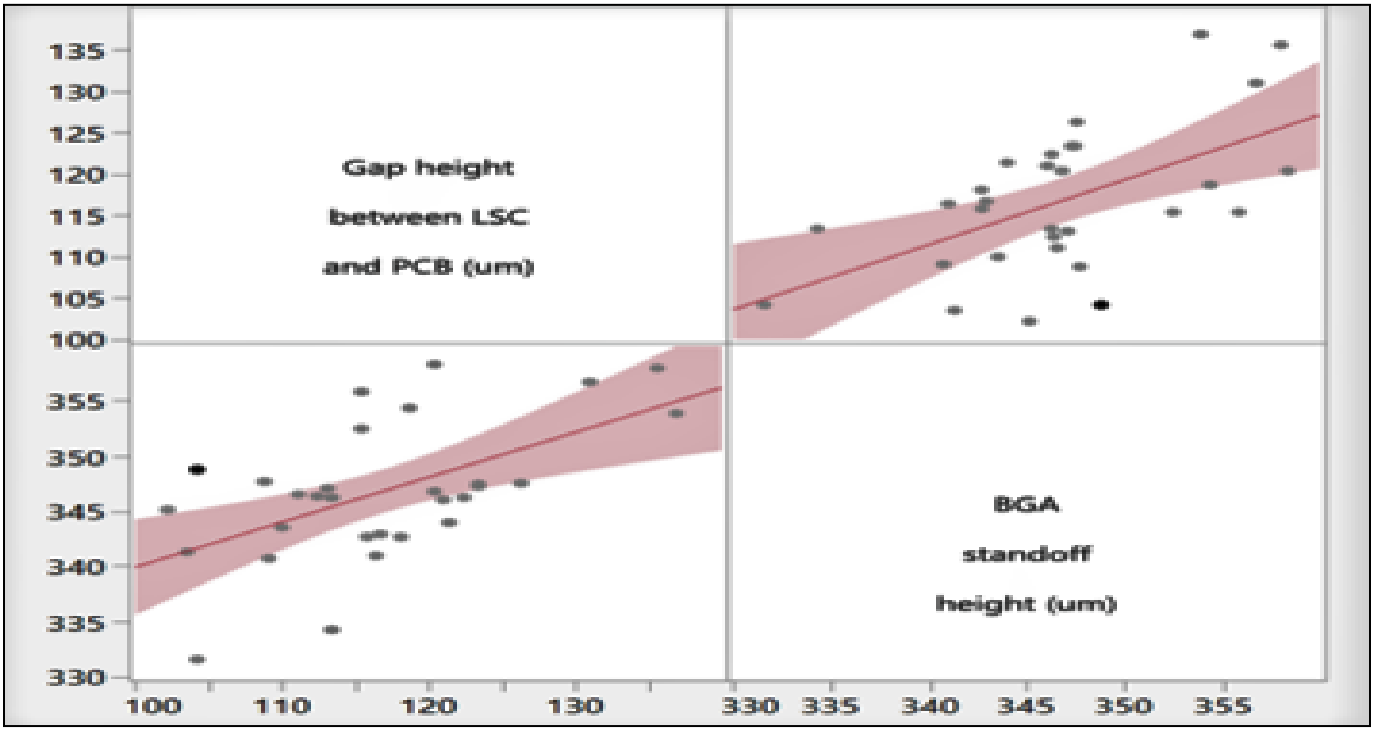


Figure 6: Moderate positive correlation between the gap height that is between an LSC and a PCB, and between the BGA standoff height.

Component-level gap height between LSC and collapsed BGA solder ball

As a continuation to the aforementioned SMT process corner investigation, quantifying the LSC process capability to the collapsed BGA solder ball gap height after the FCBGA assembly process was studied. High LSC process control to the collapsed BGA solder ball clearance is a prerequisite to a robust SMT assembly process to ensure no defects manifest associated with LSC clearance with the PCB after mounting (to the PCB). As such, gap height measurements between the LSC and BGA solder ball were evaluated across multiple assembly lots to determine if Cpk values meet automotive requirements, i.e., ≥1.67.

Figure 8 is a simplified illustration of the gap height measurement between the LSC and the collapsed BGA solder ball being investigated on the flip-chip substrate after the FCBGA assembly process. The target minimum gap height is greater or equal to 130µm. To prove a high assembly process margin, gap height measurements between the LSC and the BGA solder ball were performed on 100% of the units across three assembly lots using standard ball

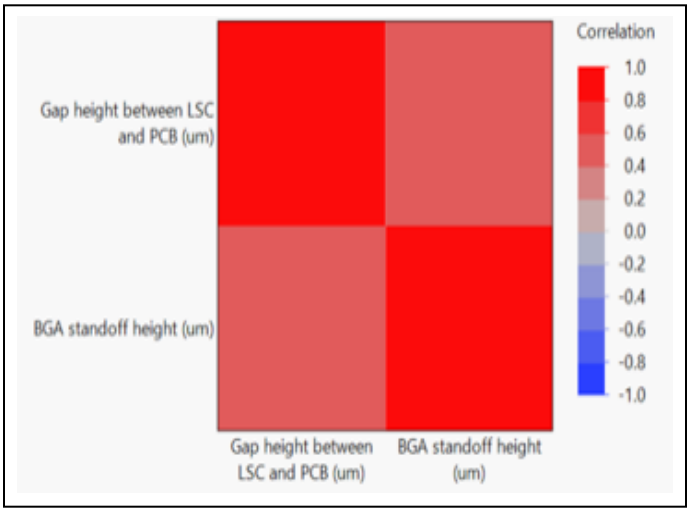


Figure 7: Color map showing a moderate positive correlation between the gap height between a LSC and a PCB and between the BGA standoff height.

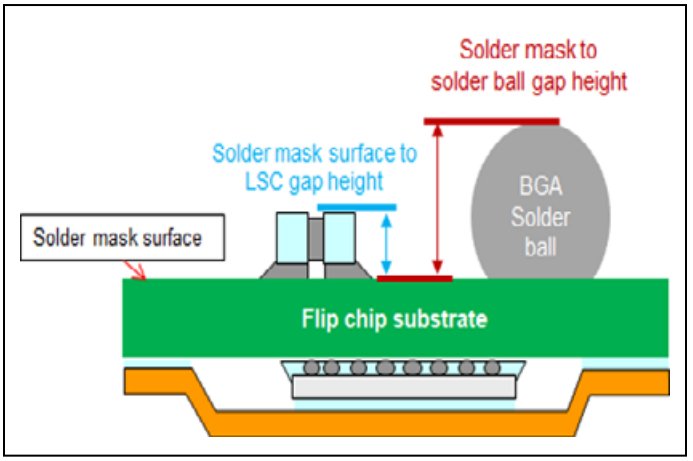
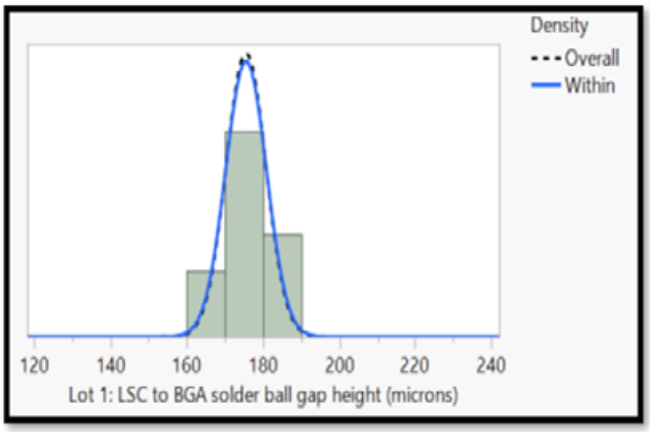
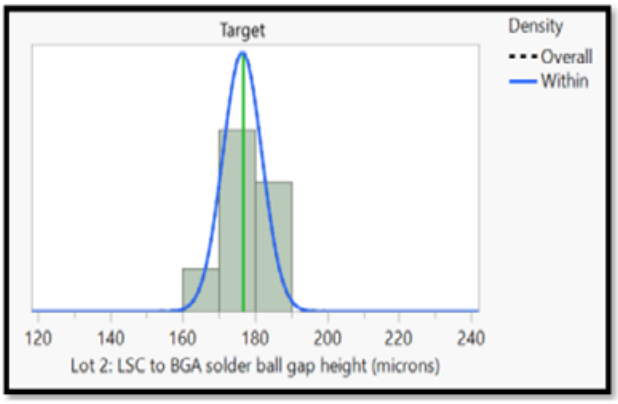


Figure 8: Dead-bug illustration of a LSC to a collapsed BGA solder ball gap height measurement.



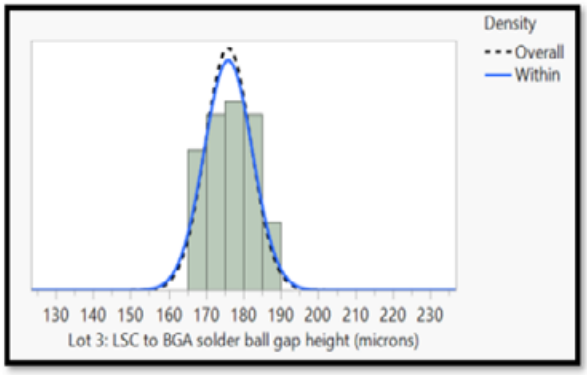
Within Sigma capability			
Index	Estimate	Lower 95%	Upper 95%
Cpk	2.846	2.547	3.145

Figure 9: LSC to BGA solder ball gap height from assembly lot 1.



Within Sigma capability			
Index	Estimate	Lower 95%	Upper 95%
Cpk	2.87	2.49	3.251

Figure 10: LSC to BGA solder ball gap height from assembly lot 2.



Within Sigma capability			
Index	Estimate	Lower 95%	Upper 95%
Cpk	2.388	2.224	2.552

Figure 11: LSC to BGA solder ball gap height from assembly lot 3.

inspection equipment. As evidenced by Figures 9-11, Cpk values across the three assembly lots all exceed the automotive target of ≥1.67. This high-margin process capability paves a pathway for a robust and defect-free SMT assembly that aligns with an automotive mindset as required from automotive Tier 1 suppliers.

Summary

LSCs are critical passive components utilized to reduce package impedance as their inherent closer proximity to the chip increases capacitance, thereby enabling crosstalk mitigation. The combination of low-profile LSCs and being automotive-qualified based on AEC-Q200 specifications, are not widespread within flip-chip packaging, which limits their use to BGA pitches less than or equal to 0.8mm because of clearance issues with the PCB.

A SMT design of experiment (DoE) was carried out based on five different component placement options to determine if a minimum gap height between the LSC and the PCB surface of 100µm can be achieved. This comprehensive study was done in order to understand the impact of clearance height between the LSC and PCB as a function of commonly-used SMT component placement conditions. SMT conditions were based on the most frequently used methods for pick and place, which involve using placement speed and package thickness to release the component to the PCB. The SMT DoE evaluation was performed on the following five different component placement options:

- Slow speed means minimum force in the 2-3N apply on the package;
- Medium speed means a force in the 4-5N range;
- Fast speed means a force in the 6-9N range;
- Component released after touching the PCB surface (program in package total thickness); and
- Component released after submerged 0.05-0.075mm into the solder paste (i.e., program in actual package thickness with additional 0.05mm).

Multiple cross-sectional analyses performed and verified that a

minimum gap height of 100µm can be achieved between the LSC and PCB ensuring a robust process free of continuity issues.

In addition, prior to the SMT process of FCBGA to PCB, a multiple assembly lot investigation of the gap height between the LSC and the collapsed BGA solder ball was conducted after the FCBGA assembly process. With the target criteria of minimum gap height greater or equal to 130µm, all parts demonstrated a high process margin with Cpk values >1.67 in alignment with automotive physical dimension requirements.

Ultimately, adhering to a zero defect mindset for automotive devices requires a fundamental understanding of assembly process variation and conditions, component tolerances, materials, and chip-to-package interaction, to name a few. Meticulous inspection using in-line optical inspection tools coupled with destructive package construction analysis are key benchmarks to understand process margin. Outputs like solder thickness between the flip-chip substrate and LSC, LSC thickness, and gap height between LSC and collapsed BGA ball, are prerequisites to establish robust clearance between low-profile LSCs and the PCB for automotive applications post-SMT. Taking a holistic approach in studying both package- and board-level effects in tandem provides high confidence for qualification, high-volume manufacturing (HVM), and reliability in the field.

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Biographies

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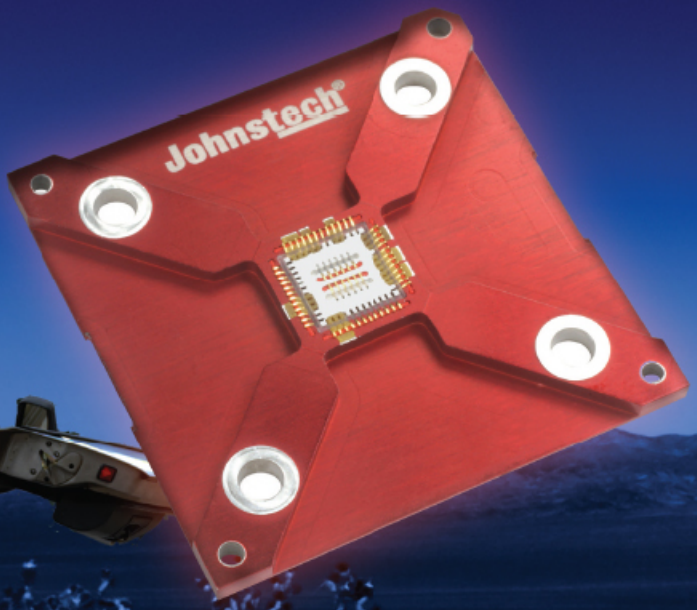

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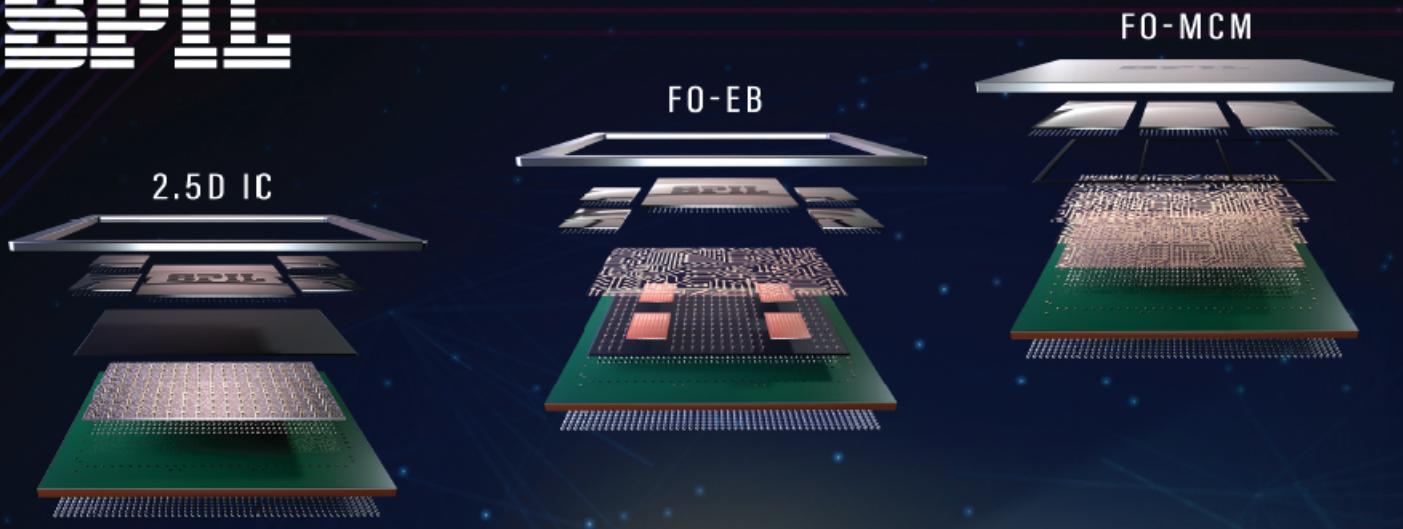

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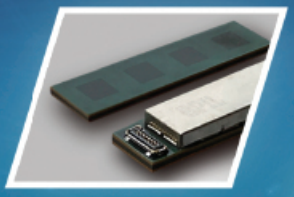
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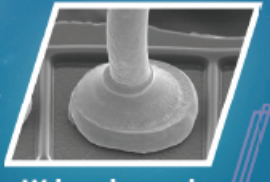
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