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Volume 25, Number 6

November • December 2021

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- Advanced WLP offers a sustainable path to HPC
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- Microelectronics packaging technologies and their performance
- Large-field, fine-resolution lithography enables next-generation PLP

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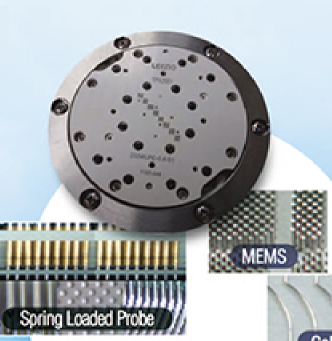

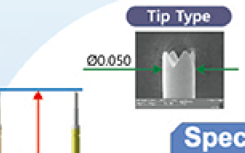

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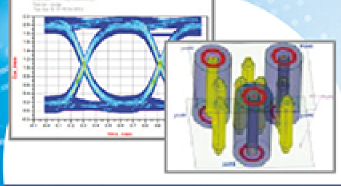

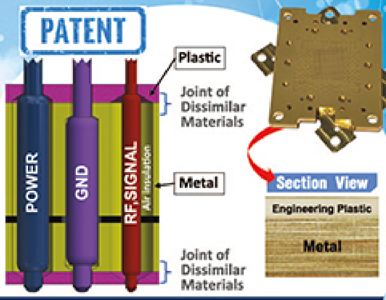

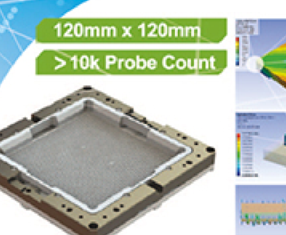

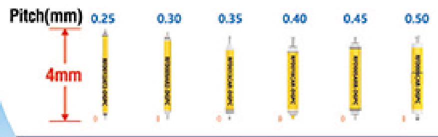

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There are a plethora of devices and architectures that hold the promise of taking scaling beyond traditional Moore's Law approaches. Research is being pursued in such technologies as qubits, spintronics, ultra-low power quantum devices, etc. But there is still much to be done with advancing transistor technologies, as well as the evolution of back-end-of-line technology. The cover article describes how graphene is being used to establish a new BEOL platform.

Cover image courtesy of Shutterstock

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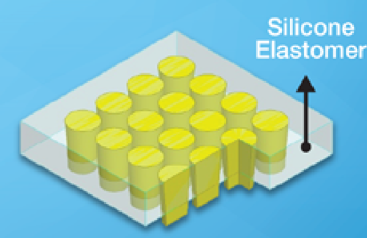

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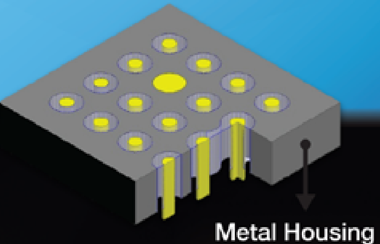

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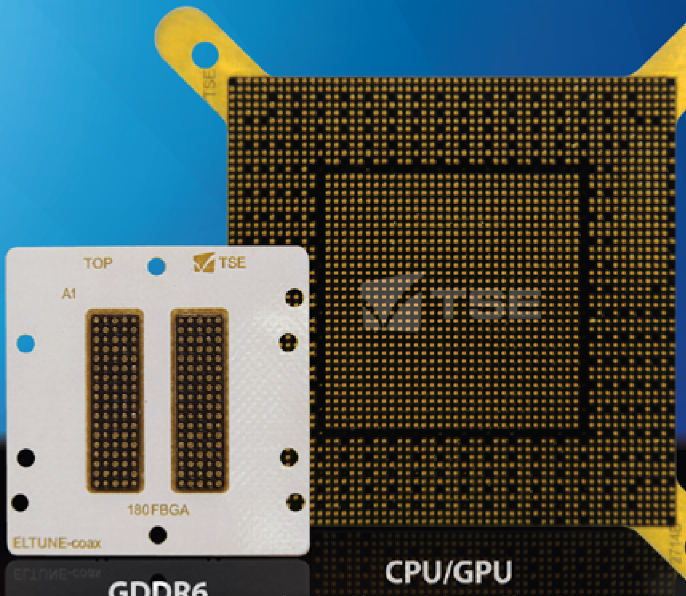

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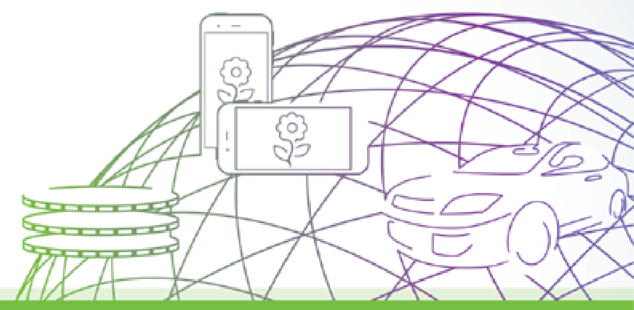

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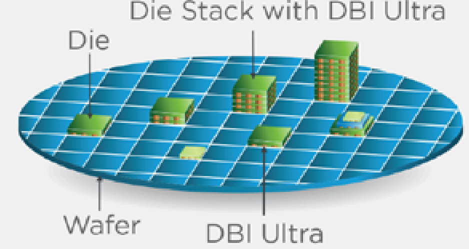

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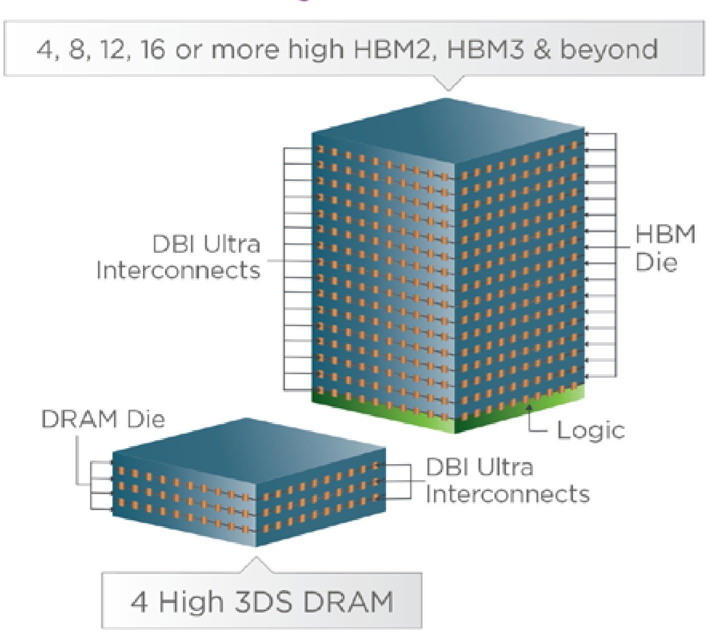

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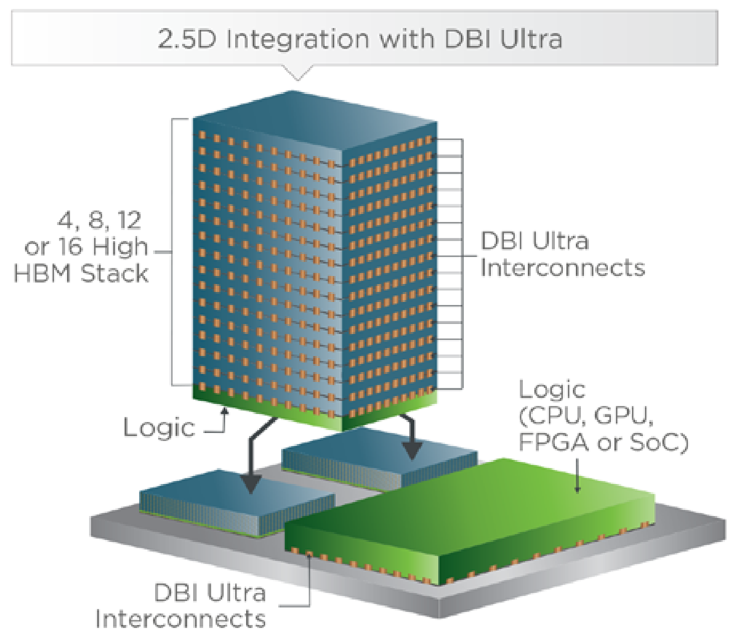

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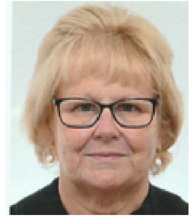

Advanced wafer-level packaging offers a sustainable path to high-performance computing

By Sally-Ann Henry, Jim Straus [ACM Research]

Heterogenous integration (HI), a key trend in semiconductor manufacturing, is becoming the path to extending Moore's Law in terms of power, performance, area and cost (PPAC). Advanced wafer-level packaging (WLP) architectures—including fan-in and fan-out WLP (FOWLP), 2.5D and 3D WLPs—are key enablers of HI. They make it possible to pack 5G, artificial intelligence (AI), memory, power, sensors, and more into the electronic devices the world relies on every day in more applications than ever.

Additionally, the power efficiency of 3D WLP helps to reduce carbon emissions, providing a sustainable pathway to high-performance computing (HPC). How those 3D WLPs are built in high volumes also contributes to achieving semiconductor manufacturers' goals of zero waste to landfills. In this article, we explore manufacturing processes and tools used to build WLPs, and what can be done to make them more sustainable.

WLP trends: what is driving growth?

Not only do WLPs provide the requisite design flexibility and thin form factor needed to increase the performance of today's data-driven devices and servers, they also deliver the reduced power consumption and extended battery life that sustainability-conscious consumers expect from their electronics. While WLP got its start in mobile devices, advanced FOWLP, 2.5D and 3D WLP using through-silicon via (TSV) interconnects are being used in HPC applications like data centers, gaming, 5G network infrastructures, AI, and more.

According to market analysts, the global WLP market size is expected to flourish at a compound annual growth rate of 21% between 2021 and 2028, as WLP continues to establish technical superiority over traditional packaging techniques [1]. According to Yole Développement, the total WLP market will reach $5.5 billion by 2025 [2]. This includes fan-in, FOWLP, 2.5D and 3D WLPs. It is the latter three that are impacting the shift in manufacturing process and tools.

While there was a brief pause in market growth, caused by uncertainty when COVID-19 began, the market quickly recovered and shifted into overdrive to meet the demands of the digital transformation. As a result, we are in the midst of a global chip shortage. The outsourced semiconductor assembly and test suppliers (OSATS) have indicated that they are at capacity for not only WLP, but all types of semiconductor packages, and the only thing that will slow the pace of growth are shortages in the supply chain.

WLP manufacturing trends

While traditional packaging architectures—such as lead frame, quad flat no lead (QFN), wire bond and even flip chip—begin with die that are diced and ready for assembly, WLP is so called because final assembly, packaging and test take place while the die are still in wafer form. FOWLP deviates slightly from this, as known-good dies (KGD) are assembled to create a reconstituted wafer that implements a redistribution layer (RDL) to fan out the interconnects from the die to the package, thereby increasing the interconnect density.

Achieving a high-density interconnect is the driving force in optimizing all types of WLP. To increase inputs/outputs (I/Os), RDL layers are added, bump sizes are reduced, and TSVs must have higher aspect ratios. For example, low density FOWLP—such as embedded wafer-level ball grid array (eWLB)—have fewer than 500 I/Os, no more than two RDL layers, and line/space widths of <8µm. Conversely, today's high-density FOWLPs have more than 500 I/Os, three to five RDL layers, and a line/space metric of less than 8µm, with many now down to 5µm in production and 2µm in development [3].

At around 65nm, copper (Cu) pillars replaced traditional wafer bumps to enable higher density interconnect between die, or between die and the packaging substrate. They are used mainly in 2.5D and 3D packaging where TSVs are used and are more complex to fabricate than bumps. Cu pillar diameters range from 20µm down to 5µm. At 5µm diameter and 50µm depth, TSVs are a challenge to plate and fill.

Many of the processes being used for advanced WLP are adaptations of those originally developed for front-end wafer processing. One example is using high-density RDL to maximize FOWLP performance. Processes used to create RDL patterns include advanced lithography, deposition, etch, and chemical mechanical planarization (CMP). TSVs require etch and deposition processes. Wafer bumping and wafer bonding also require CMP process steps.

Tools of the trade

In the early days of WLP, as it was beginning to take hold, the industry saw the proliferation of new tool suppliers who carved a niche for themselves by developing WLP process tools targeted specifically to the OSATS.

These tools included those used for:

- Electrochemical plating (ECP) for Cu bump RDL, as well as TSV metallization such as barrier, seed and fill;
- CMP for wafer bumping, RDL and hybrid bonding surface preparation; and
- Wet processing tools used for deposition processes such as coating, developing and plating, as well as stripping and etching.

Now that HI and "More than Moore" solutions are seen as the path to PPAC, leading foundries and integrated device manufacturers (IDMs) have shifted R&D focus from traditional scaling to develop leading-edge chiplet HI architectures using all the tools in the WLP toolbox. They are leveraging not only process know-how, but legacy systems to compete with OSAT providers for WLP business.

This worked well for early iterations of WLPs built using legacy node chips that did not quite need the level of precision and cleanliness required for today's advanced WLP technologies. Additionally, as OSATS couldn't easily absorb the cost of front-end tools, systems stripped of all the front-end bells and whistles made it economically feasible for OSATS to add capacity for WLP.

However, as technology nodes continue to shrink, the argument for front-end-level tool capability grows. From high-aspect ratio TSVs and finer-bump pitches to tighter RDL line/space widths and precision flatness for hybrid bonding, tools designed for early generations of WLP are not meeting today's needs for higher levels of precision, uniformity and contamination control. Wafer-level processes have become much less forgiving, and call for tools with front-end processing capabilities. But these tools must still be affordable to keep OSATS in the game. Additionally, as WLP products gain market share, all these processes must be adapted for high-volume manufacturing environments.

For example, there's a need for plating metal films in deep vias or troughs with depths more than 200µm at high plating rates. The process needs to address the mass transfer challenge while achieving a better pillar-top profile and delivering improved height uniformity, and better uniformity at a higher throughput.

The fine features of RDL line and space, Cu pillar bumps and TSV fabrication rely on advanced wet wafer processes for cleaning, coating, developing, photoresist stripping and etching. Hybrid bonding processes such as direct bond interconnect (DBI) calls for removing excess copper and the top barrier layer without inducing mechanical stress. It also requires wafers that are particle free, with extremely smooth surfaces.

The importance of sustainable manufacturing

While semiconductors are at the heart of all the smart technologies that promise to create a more sustainable world, the way we manufacture them is part of the global problem known as climate change. For example, fabricating a small 2g microchip requires 32kg of water, 1.6kg of petroleum, and 72g of chemicals [4]. Multiply this by vast volumes of chips we produce each year to support the global data explosion generated by these innovations, and we are at risk of causing as much harm as good [5].

As the semiconductor industry endeavors to support technologies that will make the world a better, safer, cleaner place, we need to increase efforts for sustainability in semiconductor manufacturing. If we focus on reducing our environmental footprint, we can make sure we're not simultaneously destroying the world we are trying to save [6].

So in addition to optimizing all these processes for WLP applications, today's tools must also be designed to help foundries, IDMs and OSATS reach their zero-waste-to-landfill goals with tools designed to reduce, reuse and recycle the chemistries used in wet wafer processing.

Summary

At ACM Research, we've leveraged our knowledge and expertise in front-end process solutions and adapted them to address today's high-volume WLP challenges. In addition to addressing ECP challenges, we have developed a process for removing excess copper and the top barrier layer from TSVs and Cu pillars without inducing mechanical stress. We are committed to supporting sustainable manufacturing efforts. To this end, we've developed closed-loop systems that require lower chemistry volumes and recycle and reuse chemistries in real time to make the processes eco-friendly.

References

1. "Global wafer-level packaging market is expected to grow at a rate of 21.0% during the anticipated period of 2021 to 2028," Data Bridge Market Research https://www.databridgemarketresearch.com/news/global-wafer-level-packaging-market
2. M. LaPedus, "Shortages, challenges engulf packaging supply chain," Semiconductor Engineering, Feb, 18, 2021 https://semiengineering.com/shortages-challenges-engulf-packaging-supply-chain/
3. M. LaPedus, "Electroplating IC challenges," Semiconductor Eng., April 10, 2017, https://semiengineering.com/electroplating-ic-packages/
4. "How can the semiconductor industry achieve sustainability?" Semiconductor Review, Oct. 12, 2020, https://www.semiconductorreview.com/news/how-can-the-semiconductor-industry-achieve-sustainability--nwid-135.html
5. J. Straus, "What you need to know about sustainability in semiconductors," May 12, 2021, https://www.3dincites.com/2021/05/what-you-need-to-know-about-sustainability-in-semiconductors/
6. Ibid.

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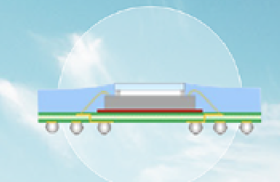
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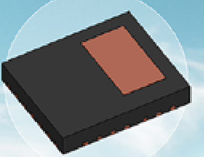
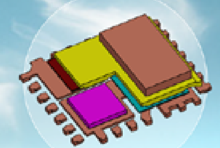
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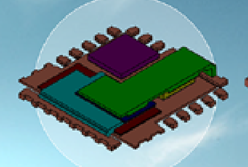
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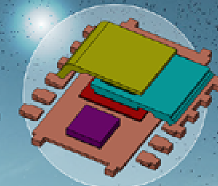
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Advanced microelectronics packaging technologies and their performance

By Ray Fillion [Fillion Consulting]

New packaging technologies are developed for one of two reasons: either to address advances in semiconductor device technology, such as higher I/O counts, faster clock rates, higher power dissipation and lower operating voltages; or to meet the requirements of new application areas, such as smartphones or implantable medical devices. Any new packaging development must meet the basic packaging functions for semiconductor devices.

Basic packaging functions

Packaging a semiconductor device involves a number of key functions with diverse requirements. First, the package must protect the chip from the following: 1) physical damage from handling or assembly; 2) excessive moisture from the environment; 3) caustic fluids and gases; and 4) electromagnetic interference. These functions are generally provided by the package enclosure such as a plastic molded package for commercial use, or a ceramic carrier for harsh environments. The package must be able to provide power and ground rails without excessive voltage drops, ripple or noise. It must provide input/output (I/O) connections that meet the switching frequencies and the operating voltage margins of the chip. I/O signal and power/ground connections must be sufficiently robust to meet the operating temperature and thermal cycling requirements of the end-use environment. The package must provide a thermal cooling path that can handle the chip power dissipation without creating an excessive chip thermal rise. The package must provide sufficient I/O capacity to meet the I/O count and power/ground requirements of the chip. Finally, the package must have physical dimensions that meet the footprint and thickness requirements of the intended application area.

Semiconductor advancements

Semiconductor wafer fabrication capabilities as measured in minimum gate width or minimum line width, have been the main driving force for semiconductor device advancements for the past five decades. These advancements were due to improved photolithography, more precise equipment, cleaner fab spaces, innovative materials, and new device structures. **Figure 1** depicts a plot of semiconductor minimum feature sizes (typically gate lengths) for each semiconductor node from the 1970s to the present, going from 10µm in 1972, to 10nm in 2019 [1]. It shows a 1000-fold reduction in feature size, which corresponds to a 10^6 increase in the number of gates per mm^2. With each node shrink, semiconductor devices achieved higher speeds, higher I/O counts, lower operating voltages, higher current levels and higher power dissipation. In response to these semiconductor advances, packaging and interconnection technologies have evolved with their own feature size shrinks, such as finer line printed circuit boards (PCBs) and substrates, finer wire bond pitch, and tighter pitch solder joints. In other cases, the state-of-the-art packaging technologies needed to be replaced with totally new approaches such as the transitions from wire bonds to solder bumps, from perimeter leads to ball grid array (BGA), from 2D assemblies to 3D assemblies, and from single-chip packaging to multi-chip modules (MCMs). The following paragraphs will look at the latest advanced packaging technologies.

Embedded chip packaging

Embedded chip packaging (ECP) was developed as a high-performance MCM with greatly reduced interconnect parasitics. ECPs embed bare chips under a high-density organic interconnect layer. Electrical connections from chip-to-chip or chip-to-I/O pad are made with a photo-patterned, redistribution layer (RDL) on the dielectric and through microvias directly to the chip I/O pads. This structure eliminates traditional package wire bond and solder bump connections and their interconnect parasitics. **Figure 2** depicts a perspective view and a cross-sectional view of a typical ECP with perimeter I/O pads formed on the top RDL layer for lead frame attach. Alternatively, BGA pads can be formed over the whole top surface of the module. ECPs have an order of magnitude lower interconnect inductance and resistance than flip-chip MCMs and two orders of magnitude lower interconnect inductance and resistance than wire bond MCMs [2].

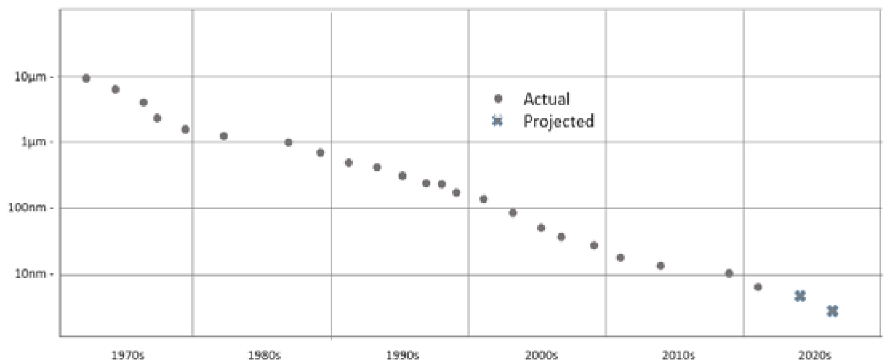

Figure 1: Plot of basic semiconductor node minimum feature size, 1972 to 2019, for Intel memories and microprocessors [2].

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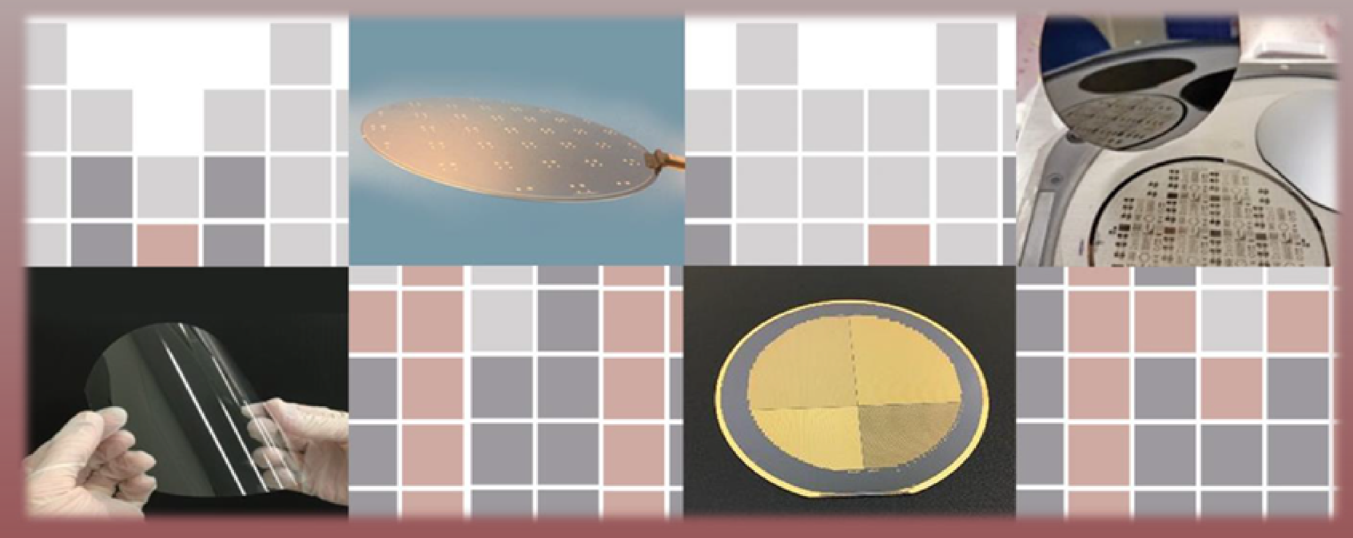


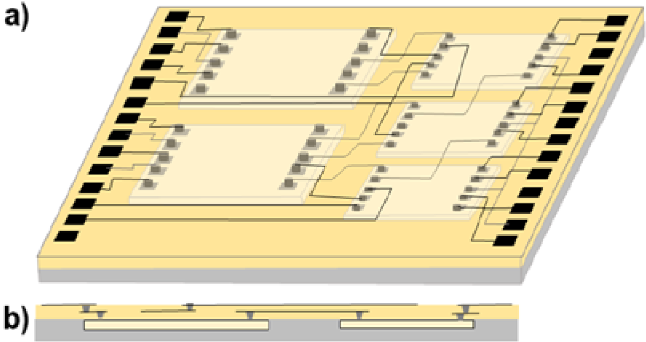


Figure 2: Multi-chip embedded chip package: a) (top) Five-chip ECP, perspective view; and b) (bottom) cross-sectional view.

The downside of having a smaller footprint is a higher power density that needs to be considered. ECPs also have the issue of the bare chips not being fully tested prior to embedding, potentially causing lower assembly yields.

Fan-in wafer-level packages (FIWLPs)

Fan-in wafer-level packages (FIWLPs) are chip-scale packages (CSPs) that are fabricated at wafer level as an extension of semiconductor fabrication back-end-of-line (BEOL) processing. The purpose of forming a FIWLP is to convert a chip with perimeter wire bond pads (about 90 to 95% of all chips) into a flip-chip like device with an array of solder bump pads. **Figure 3** depicts a typical FIWLP in perspective view and cross-sectional view. The perimeter I/O pads are rerouted onto the center area of the die. A thin (5–10µm) organic

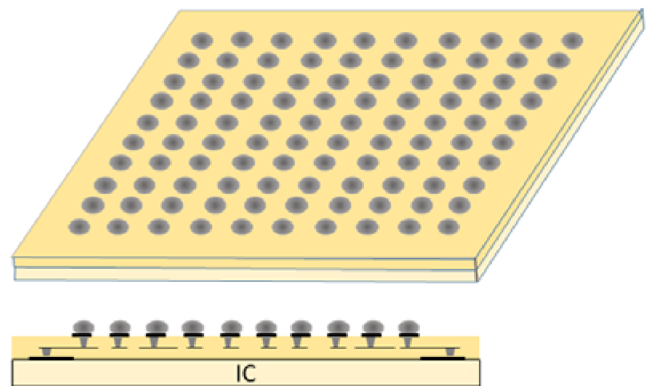


Figure 3: FIWLP or chip-scale package (CSP) with area array solder bumps.

dielectric layer covers the die surface. An RDL metallization connects to the chip perimeter I/O pads through microvias. After wafer dicing, the FIWLP is then flip attached using solder bump technology. The interconnect resistance, inductance and capacitance are reduced by an order of magnitude over the wire bonded device. As with the ECP devices above, the bare chip going into the FIWLPs are not fully tested and generally have a lower assembly yield. Like the earlier flip-chip devices, FIWLPs have a smaller footprint and have a higher power density. A FIWLP has some surface protection with its organic dielectric layer protecting the chip's active surface, although it provides no protection to the chip sides and back surface making it somewhat less protective than standard packages.

Fan-out wafer-level packages (FOWLPs)

As the I/O count of high-end devices continued to increase, particularly processor chips, there were too many I/Os to reliably fan in to the center of the chip. Embedded chip packaging technology (detailed above) was utilized to create fan-out wafer-level packages (FOWLPs) that increased the area available for I/O pads. Bare chips are embedded in molding material forming a carrier. The same RDL interconnect structure is used as on the FIWLP technology above. The chips are spaced apart sufficiently to form the required device footprint. The chip pads are routed both over the chip center area and over the molding material. Flip-chip technology is used to form area array solder bumps. Complex devices with very high I/O counts often require the application of one or more additional RDL layers. **Figure 4** depicts a typical fan-out device with I/O pads formed over the chip center area and over the molding material. Early fan-out fabricators utilized the same 300mm wafer carrier format, equipment and processes as used on FIWLP devices, while also adding a molding step. FOWLPs like the FIWLPs above had lower interconnect parasitics, and a significantly reduced footprint versus standard chip packages (about 4:1 less area). Like the FIWLPs above, FOWLPs' smaller footprint would result in a higher power density. Because the chips were fully encapsulated, with molding material on the chip sides and back surface and an organic dielectric layer on the active surface, FOWLPs offered some additional chip protection.

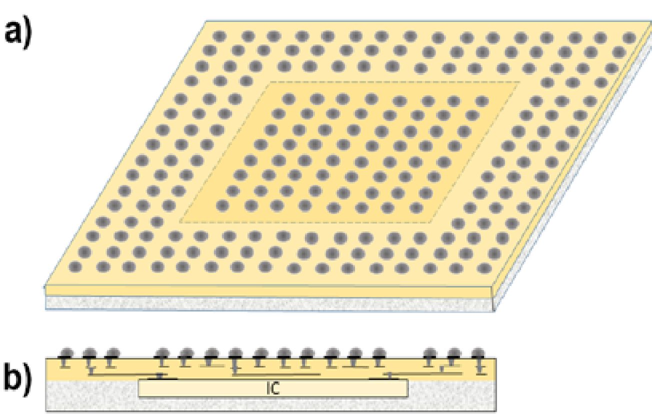


Figure 4: FOWLP or PLP with the chip perimeter I/O pads routed both over the molding material and over the chip center area. a) (top) Perspective view with embedded chip position shown with dashed lines; and b) (bottom) Cross-section view showing embedded chip with two RDL layers.

Fan-out panel-level packages (FOPLPs)

As the photolithography capabilities of high-end organic substrate facilities improved with finer feature capabilities, organic substrate fabricators developed fan-out processes on organic fabrication equipment in larger format panels forming fan-out panel-level packages (FOPLPs). Structurally, FOWLPs and FOPLPs are identical with similar materials, feature sizes, performance and footprints. Multiple companies have introduced, or are in the process of introducing, FOPLPs fabricated on larger PCB format panels such as 450mm by 550mm or larger panels. These include Amkor, Deca, SPTS, STATS ChipPAC, and others [3]. Panel-

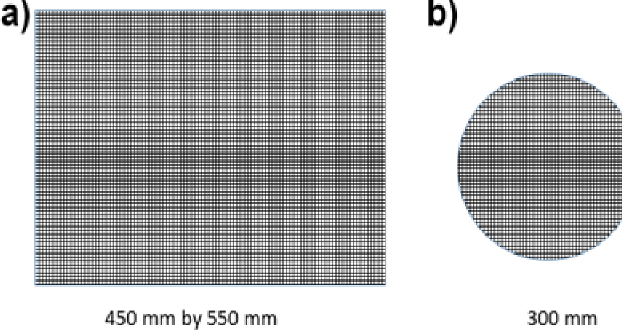


Figure 5: FOPLP versus fan-out FOWLP: a) (left) 450mm x 550mm panel format; and b) (right) 300mm diameter wafer format.

level processing of fan-out devices with their larger format panels will yield significant cost reductions over wafer-level processing because of the larger panel area and the lower equipment costs [4]. A wafer-level process on a 300mm line has about 70Kmm^2 of processing area while a 450mm by 550mm panel has about 240Kmm^2 of processing area—a 3.5 to 1 increase in processing area as depicted in **Figure 5**. FOPLPs are electrically, thermally and physically identical to FOWLPs.

3D-chip stacking

In order to increase the memory capacity per unit area and to minimize the physical distance from the memory chips to the processor chip, semiconductor companies and assemblers developed a number of chip stacking technologies. In the early chip stacking approaches, multiple bare memory chips with perimeter wire bond pads were stacked one on top of another forming a stack of two, four, or more chips. In one approach, chips were designed with all I/Os on one chip edge. Chips were then mounted with every other chip offset on one side and then the other with all I/O pads exposed. Low-profile wire bonds connected each chip pad either to a lower chip's pad or to the package substrate. For higher I/O count chips, a spacer would be mounted between each chip allowing wire bonding on all four sides. 3D stacking with through-silicon vias (TSVs) was developed to handle high-bandwidth memory (HBM) devices that have multiple 128-bit data channels—far too many for perimeter wire bond pads. HBM chips are stacked with each chip mounted directly over a lower chip. **Figure 6** depicts a four-memory chip, staggered-chip stack with the chips wire bonded to an organic substrate (top) and a four-memory chip stack on a processor or interface chip with TSVs in the lower chips and micro-solder bumps interconnecting the chips. 3D chip stacking can increase circuit density by a factor of 2X to 10X, depending on how many chips are stacked. It also lowers the interconnect parasitics from the memory chips to the processor chip by more than an order of magnitude. 3D chip stacking is generally limited to memory chips where only one chip in the stack is active at a time. 3D chip stacking can have a higher yield loss as the chips have only been wafer tested. This is similar to the yield issues in ECPs noted above.

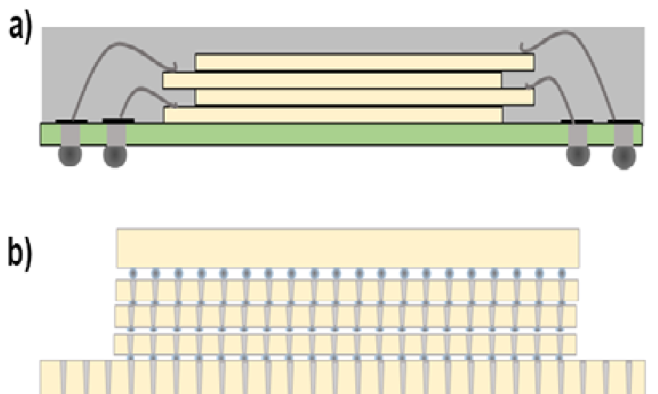
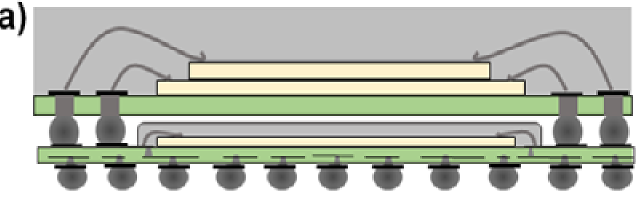


Figure 6: 3D chip stacking: a) (top) three staggered, wire bonded memory chips on an organic BGA substrate; and b) (bottom) four stacked memory chips on a processor or interface chip with TSVs in the lower four chips and micro-solder bumps connecting the chips.

Package-on-package (PoP) stacking

For non-memory 3D applications such as mixed memory and processor applications, package-on-package (PoP) technologies were developed. In this approach, single chips and chip stacks can be packaged in a stackable chip carrier and two packages can be directly stacked on each other using BGA solder attach. Two typical PoPs are depicted in **Figure 7**. A lower performance PoP configuration is depicted on the top with its lower package having a wire bonded application-specific integrated circuit (ASIC) and its upper package containing a two-chip, wire-bonded memory stack. A higher performance PoP is depicted on the bottom with its lower package a FOPLP package and with its upper package containing a four-chip, wire-bonded memory chip stack. The PoPs have a 2:1 footprint reduction and the memory-to-processor interconnection parasitics are reduced by more than 2:1. Because a PoP has a power density that is 2X that of single-chip packages, the thermal cooling of the assembly may be an issue.



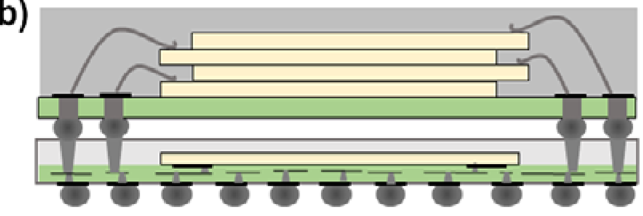
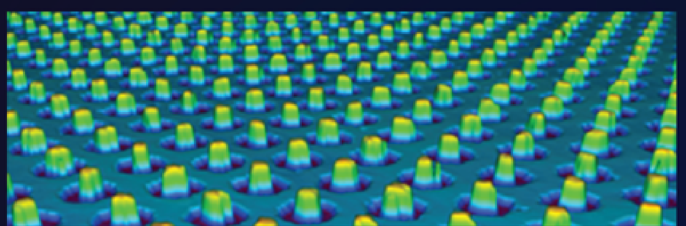
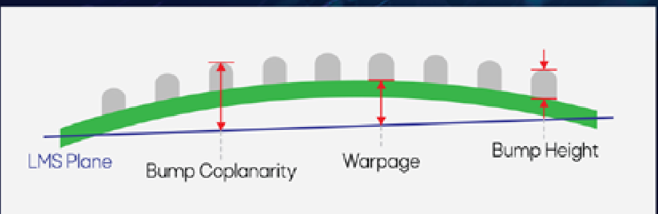


Figure 7: Typical PoP modules: a) (top) lower performance PoP with wire bonded ASIC in the lower package and a wire bonded, two-chip memory stack on the upper package; and b) (bottom) high-performance PoP with a processor chip in the lower FOPLP package and a four-chip, wire bonded memory stack in the upper package.

3D Solution for FC-BGA Bump Inspection





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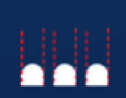

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System-in-package (SiP)

One of the latest packaging development areas is the system-in-package (SiP). SiP is a combination of multiple active electronic components of different functionality, assembled in a single unit that provides multiple functions associated with a system or sub-system (JEDEC). A SiP generally contains processor chip, memory chips, assorted logic chips, and can contain discrete or integrated passive devices (IPDs), microelectromechanical systems (MEMS), optical components and other packaged or unpackaged devices. The core of a SiP is an interposer or high-density substrate on which the components are mounted with multiple routing layers interconnecting between devices and vias to the bottom side I/O connections. High-end SiPs with fine-pitch components use a Si interposer for several reasons: 1) its coefficient of thermal expansion (CTE) match to Si chips; 2) its fine-line interconnect capability; 3) its ability to incorporate active elements; 4) its high thermal conductivity; 5) its ability to utilize ultra-high-density micro-bumps for chip-to-interposer connections; 6) and for the high vertical I/O density that can be achieved with TSVs. **Figure 8** depicts a SiP with a Si interposer mounted on an organic substrate with an IPD embedded in the substrate. An integrated power electronic component (IPEC), a three-chip HBM stack, a processor chip, and an interface (I/F) chip are attached on top of the Si interposer with micro-solder bumps and connected to the substrate with TSVs in the Si interposer and solder bumps to the substrate.

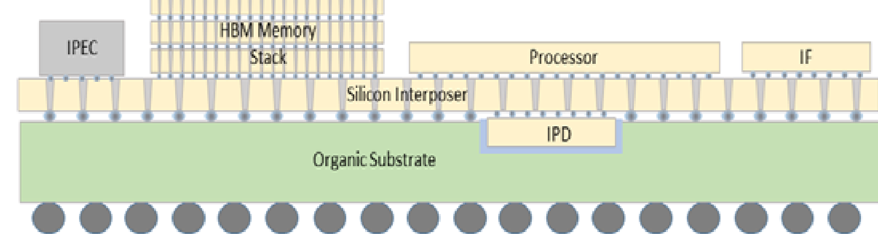

Figure 8: Cross-section of a SiP with a silicon interposer. A HBM stack with TSVs, an IPEC, a processor chip and an IF chip are solder bump attached to the Si interposer that has TSVs to an organic substrate containing an embedded IPD.

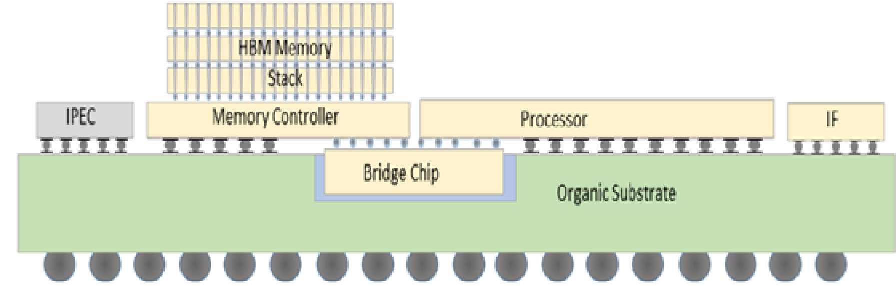

Figure 9: Cross section of a SiP with an organic interposer. A HBM stack and memory controller with TSVs, an IPEC, a processor chip and an IF chip are solder bump attached on the organic interposer. A high-density interconnect Si bridge chip is embedded in the interposer, connecting the processor to the HBM 3D stack.

Depending on the density of I/Os on the chips, efforts are underway to utilize a fine-line organic substrate as the interposer in the SiP, eliminating the costly large-area silicon structure. The organic substrate would potentially be a lower cost solution than the Si interposer, but it cannot directly support high-density micro-bump contacts because of its high CTE and photo-patterning limitations. One solution is to incorporate Si bridge chips to form high-bandwidth communication between the HBM chips or stacks and the processor. The bridge chip is an inactive Si chiplet with fine-line capability that directly connects a processor chip and a memory chip at very high density and with very low parasitics. The rest of the SiP chip-to-chip and chip-to-PCB connections are done using the fine-line organic interposer. Intel has demonstrated this concept with its embedded multi-die interconnect bridge (EMIB) [5]. **Figure 9** depicts a cross-sectional view of a SiP with an organic interposer and a high-interconnect density bridge chip, as well as the IPEC, the HBM stack, the processor chip, and the interface chip.

Heterogeneous integrated SiPs

A new push is underway to expand the capabilities of SiPs by implementing heterogeneous integration within the SiP. An IEEE-led task force is underway to develop a Heterogeneous Integration Roadmap, describing the applications, the technology and the research needed to provide "More Than Moore" capability over the next 15 years with a vision out to 25 years [6]. It is a growing belief that the five-decade long semiconductor feature size shrink characterized by Moore's Law that has driven the gate count increase per high-end chip for each new semiconductor node is slowing down for two main reasons: 1) because of the physical limits of minimum gate features, and 2) that the next few generations of high-end devices will not be monolithic dies, but rather integrated assemblies of heterogeneous chips from multiple suppliers on a high-performance interposer. Heterogeneous integration refers to the integration of separately manufactured components from multiple sources into a higher-level assembly. Under this concept, microprocessors will be de-integrated from one complex chip, with 50 or more cores, each with separately controlled power rails, into 6 to 10 chiplets, each with multiple cores all mounted on a silicon interposer.

Packaging technologies vs. packaging performance

Table 1 compares how the various packaging technologies, detailed above, address the main packaging and interconnect requirements of semiconductor devices. Packaging technologies such as 3D chip stacks and SiPs require an enclosure structure to provide normal device protection. Although **Table 1** lists the 3D chip stack and the SiP as having low mechanical and environmental protection, they would generally be mounted into a package that would provide the required protection.

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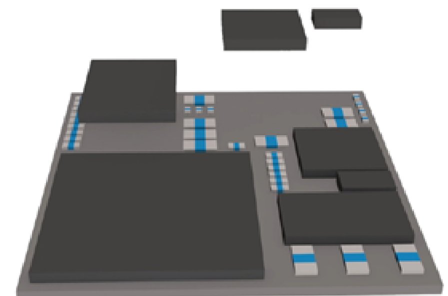

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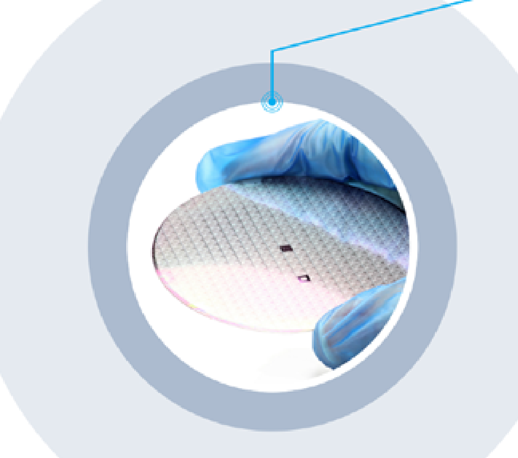

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Packaging Technology / Packaging Functions	Multichip Package Wire Bonds (MCP)	Embedded Chip Package (ECP)	Fan-In Wafer Level Package (FIWLP)	Fan-Out Wafer Level Package (FOWLP)	Fan-Out Panel Level Package (FOPLP)	3D Chip Stacking Wire Bonds (3DWB)	3D Chip Stacking TSVs (3DTSV)	Package-on-Package WB (PoP)	Package-on-Package ECP (PoP)	System-in-Package (SiP)
Wire Bonds	Yes	No	No	No	No	Yes	No	Yes	Yes/No	No
Protection										
- Mechanical	excellent	excellent	good	excellent	excellent	requires package	requires package	excellent	excellent	excellent
- Moisture	good	good	fair	good	good	requires package	requires package	good	good	requires package
- Chemicals	good	good	fair	good	good	requires package	requires package	good	good	requires package
- EMI/EMS	fair	excellent	excellent	excellent	excellent	fair	excellent	fair	good	excellent
Clean Power & Ground Rails	fair	excellent	good	good	good	poor	excellent	fair	good	excellent
Low I/O Parasitics	fair	excellent	good	good	good	poor	excellent	fair	good	excellent
Thermal Performance	poor	variable	good	good	good	poor	poor	poor	poor	good
Robust Assembly	variable	variable	excellent	excellent	excellent	poor	excellent	good	good	variable
I/O Count Capacity	good	excellent	good	excellent	excellent	good	excellent	good	good	excellent
Functional Density	good	excellent	excellent	good	good	excellent	excellent	good	good	excellent
Thin Package	low	excellent	excellent	excellent	excellent	low	good	low	low	good

Table 1: Packaging function comparisons of advanced packaging technologies.

Summary

Semiconductor advances have delivered exponential increases in gate counts and I/O counts, faster clock rates, and lower operating voltages over the past five decades that also came with higher power dissipation and higher supply currents. At the same time, new applications, such as smartphones arose, which also put new restrictions on the size and thermal performance of the devices. When these semiconductor advances and the new application requirements reached a point where standard packaging approaches could no longer be extended to meet the device needs, new advanced packaging technologies were developed and scaled-up into high-volume production. These new technologies included various forms of 2D-integration (ECPs, SiPs), 3D-integration (chip stacks, PoPs), and shrinking packages (FIWLPs, FOWLPs, FOPLPs). The next, though not likely the last semiconductor packaging development, is the heterogeneous integrated SiP that can incorporate many of these current advanced packaging technologies along with advanced interposers and de-integration of complex processors into multiple chiplets. All of these packaging approaches are in, or are moving toward, high-volume production and all meet the key packaging functions the latest semiconductor devices need and the unique requirements of today's high-volume applications.

References

1. "Process Technology History – Intel," https://en.wikichip.org/wiki/intel/process
2. R. Fillion, et al., "Embedded chip build-up using fine-line interconnect," ECTC (2007).
3. "Global fan-out panel-level packaging market 2021 to record an exponential CAGR by 2026," Midwest Expositor, Market Research Reports, 9/15/2021.
4. B. Meihach, "Advanced packaging inspection solutions for fan-out panel-level processing," et al., Proc. of the International Wafer-Level Packaging Conf. (2017).
5. "Embedded multi-die interconnect bridge," https://www.intel.com/content/www/us/en/silicon-innovations/6-pillars/emib.html?wapkw=embedded%20multi-die%20bridge
6. Ch. 1, 'HIR Overview and Executive Summary,' in *Heterogeneous Integration Roadmap*, http://eps.ieee.org/hir

Biography

Ray Fillion is Managing Director at Fillion Consulting, Schenectady, NY. He retired after 40 years from the GE Global Research Center where he worked in various engineering, management, business development and licensing positions in embedded chip, MCMs, 3D modules and power electronics. He has over 100 publications, has 45 issued U.S. patents and was the lead inventor on the GE Embedded Chip Build-Up and the GE Power Overlay technologies. Email fillion.consulting@gmail.com

A new, higher density QFP

By Chu-Chung (Stephen) Lee, Yao Jinzhong, Glenn G. Daves [NXP Semiconductors N.V.]

This technical article (part 2) is a continuation of the Emerging Technologies column entitled, "A new, higher density QFP" in the September • October 2021 issue of Chip Scale Review.

MaxQFP (**Figure 1**) is a new high-density quad flat pack (QFP) that combines both gull-wing and J-leads in an over-molded package body. The outer row of leads are gull-wing (GW) leads, with the J-leads located inward towards the center of the package and interstitially between two GW leads. The external lead pitch between adjacent leads of the same type (e.g., J-leads) is 0.65mm and that between adjacent leads of different types (i.e., between the J- and GW-leads) is 0.325mm. As an example, on the 100-lead MaxQFP (10x10mm body size), each side of the package has 13 GW-leads and 12 J-leads resulting in a total of 25 leads per side and 100 leads for the package. One notable feature of MaxQFP is that these two rows of leads are not located on the same plane during molding—i.e., there is no dam bar on the lead frame strip. This design allows the leads to be vertically displaced from each other even at the position of the molded body. The resulting separation reduces the chances of shorting between leads and effectively enables almost the entire perimeter of the package to be used for I/O.

Two MaxQFP body sizes have been developed to date: a 172-lead (16x16mm body size) version and a 100-lead version. Together, these are able to replace five JEDEC-compliant QFPs with lead counts of: 64, 80, 100, 144 and 176 as illustrated in **Figure 2**.

For high-power applications, MaxQFP_EP (exposed pad) has also been developed as shown in **Figure 3**. It is similar to the QFP_EP, where a portion of the die flag is exposed, enabling it to be soldered to a printed circuit board (PCB) resulting in short thermal connection between the PCB, package, and die. Its thermal performance is significantly better than can be achieved by a similar

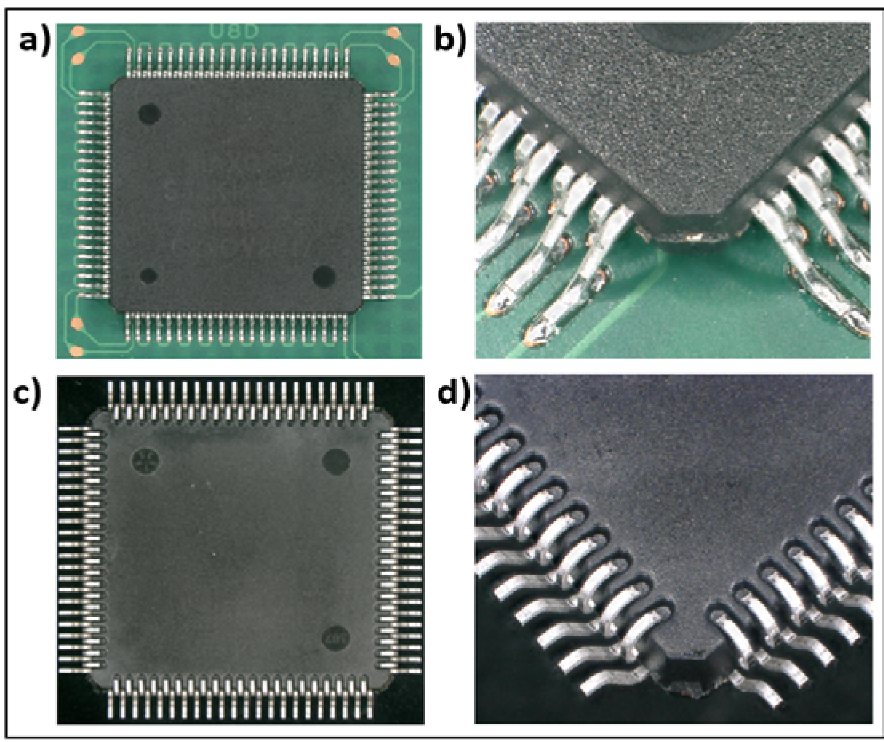

Figure 1: a): (left) MaxQFP packages combine both QFP gull-wing and PLCC J-leads; b) (right) A top view of the 172-lead MaxQFP package is pictured, showing outer gull-wing and inner J-leads, positioned interstitially; c) (left) Bottom view of the 172-lead MaxQFP package; and d) (right) Close-up view of the same package.

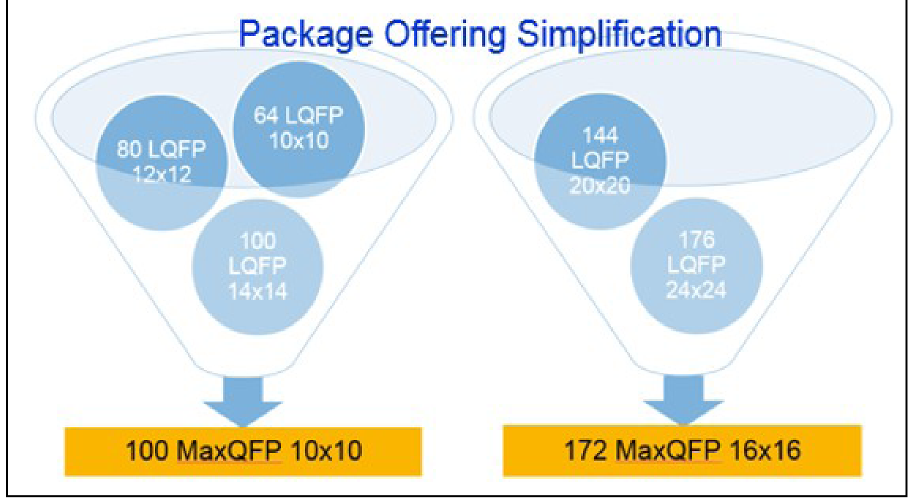

Figure 2: MaxQFP simplifies package portfolios. The 100-lead MaxQFP (10x10mm) replaces the 64-, 80-, and 100-lead QFPs, while the 172-lead MaxQFP (16x16mm) can replace both the 144- and 176-lead QFP.

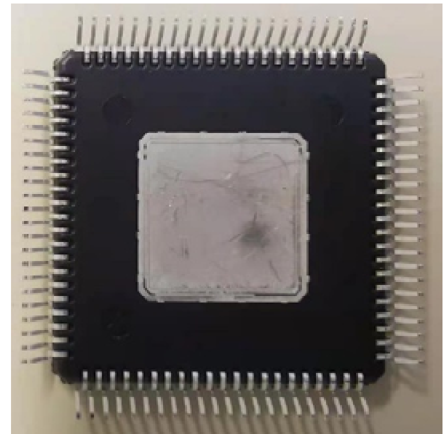

Figure 3: MaxQFP_EP with exposed pad to improve thermal performance.

leaded package without an exposed pad. The thermal performance (e.g., thermal resistance) of both the MaxQFP and MaxQFP_EP packages will be detailed later.

Compared to JEDEC-compliant QFP packages, MaxQFP offers higher pin counts at similar body sizes, thereby enabling reduced consumption of PCB area. This is a space savings and, ultimately, cost-saving advantage to users. For example, the 172-lead MaxQFP

Figure 4: A visual comparison between the 172-lead MaxQFP (16x16mm) and the 176-lead QFP (24x24mm) showing the body size reduction of 55%.

is in a 16x16mm body size, while the 176-lead QFP is in a 24x24mm body size. This represents a comparative 55% reduction in area, as shown in **Figure 4**.

Because of the intended use of MaxQFP in industrial and automotive applications, both the inspectability of each lead after PCB mount is important, as is the overall reliability of the package. Extensive data have been collected, which are detailed below, but are summarized here. First, automated optical inspection (AOI) has been investigated on several commercial systems with positive results. In addition, board-level solder joint reliability (SJR) data meet or exceed AEC Grade 1 standards. Also, component-level reliability stresses defined by the AEC Q100 standard, including temperature cycling (TC), high-temperature storage life (HTSL), and un-biased humidity accelerated stress test (uHAST) were conducted—also with positive results. For these tests, two different functional die were used, one from the 7 metal layer C40 nm silicon technology node and one from the 4 metal layer C90 nm node. Data in support of the AEC Q006 standard for copper wire devices were also collected, and also had positive results.

Technical data summary

As summarized above, the MaxQFP package was extensively evaluated by reliability testing, construction analysis, inspectability evaluation, and mechanical, thermal, and electrical simulation. Details of these evaluations follow.

Package reliability. AEC Grade 1 reliability data were collected using a C90 nm test vehicle die (with full functionality) in a 172-lead MaxQFP and are summarized in **Table 1**. This test vehicle passes all requirements to 2X at a minimum. In an attempt to capture some of the possible manufacturing process variations, four separate assembly lots were used for each stress test. Of particular note is the temperature cycling results, where the 3,000 cycles passed represent twice the requirement of the AEC Grade 0 standard. This standard is intended for the highest reliability and most extreme automotive

Stress test	Test condition	Sample size	Pass read points
TC	-55 to 150 C	4 x 90	**1000**/2000/3000 cycles
uHAST	110 C/ 85%	4 x 90	**264**/528 hours
THB	85C/ 85%	4 x 90	**1008**/2016 hours
HTSL	150 C	4 x 90	**1008**/2016 hours

Table 1: Reliability results for C90 nm test vehicle in a 172-lead MaxQFP (the bold text denotes the requirement of the AEC Grade 1 standard) (all tests passed).

Stress tests	Test condition	Sample size	Pass read points
TC	-55 to 150 C	3x 109	**1000**/2000 cycles
uHAST	110 C/ 85%	3x 80	**264**/528 hours
HTSL	150 C	3x 85	**1008**/ 2016 hours

Table 2: Reliability tests for C40 nm test vehicle in a 172-lead MaxQFP (the bold text denotes the requirement of the AEC Grade 1 standard) (all tests passed).

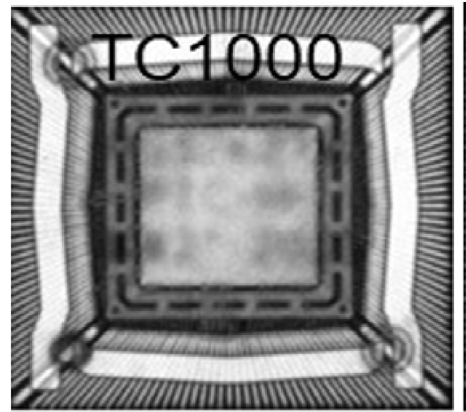

Figure 5: Both TC 1000 and 2000 cycle SAM images show no delamination that would violate AEC requirements.

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environments, typically experienced for electronics in close proximity to the engine, transmission, or braking systems.

Similar reliability data were also collected for the C40 nm test vehicle, again leveraging the 172-lead MaxQFP. These data are detailed in **Table 2**. This test vehicle also passed 2X AEC Grade 1 requirements. As before, multiple assembly lots were used for each stress test.

In addition to the raw results noted above, post-stress scanning acoustic microscopy (SAM) images were taken to look for any package delamination. Examples of SAM images of post-TC 1,000- and 2,000-cycle data are shown in **Figure 5**. In all cases, no delamination violating AEC requirements was observed on the test vehicles. Also, post-stress decapsulation wire pull and ball shear tests were performed. All passed AEC Q006 requirements. Cross-section scanning electron microscope (SEM) images were also taken to assure that the ball bonds have no Cu-Al intermetallic degradation (**Figure 6**) [1,2] and no Cu void formation [3,4].

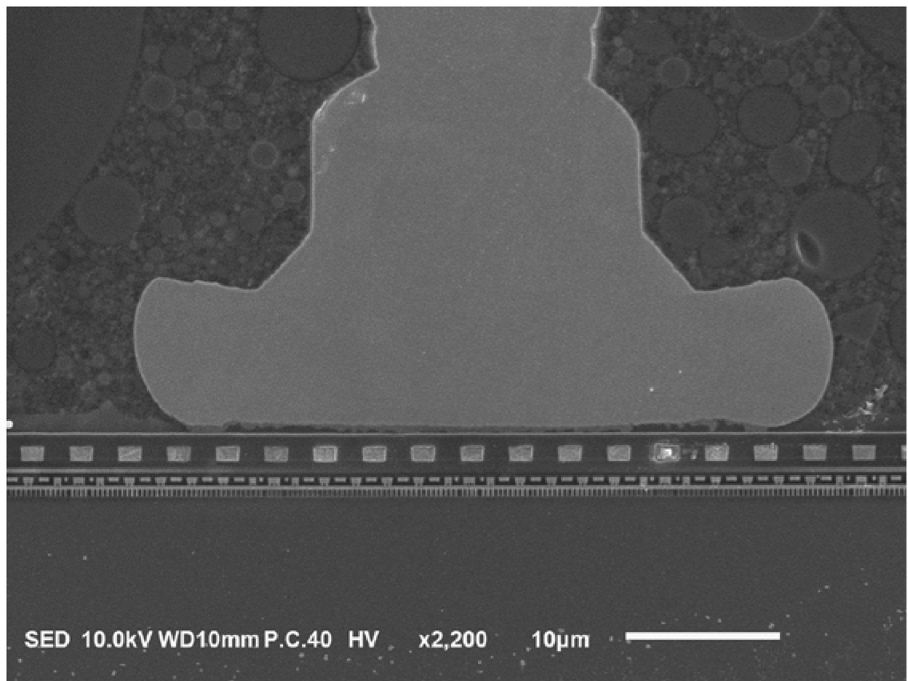


Figure 6: Cross section/SEM image of Cu ball bonds of post-HTSL 2016 hrs showing no sign of Cu-Al IMC degradation and no Cu void formation.

Board-level solder joint reliability. MaxQFP uses the same PCB design rules as a standard 0.5mm pitch QFP—namely 0.1/0.1mm line/space [5]. Therefore, even though the interstitial pitch of the leads is smaller, no finer-pitch (higher cost) PCB manufacturing is required to design with MaxQFP. Board-level SJR data were collected using a daisy chain die in a 172-lead MaxQFP under the temperature cycling stress condition of -40 to 125ºC. Cycling was continued until at least 50% of the parts failed, thereby enabling a statistical view of reliability performance. For this study, four separate PCB board footprints were designed (**Table 3**). The general automotive board-level SJR requirement is to pass 2,000 cycles before the first fail is detected.

Design A is the baseline design, which is identical to the existing PCB footprint for both QFP gull-wing leads and plastic-leaded chip carrier (PLCC) J-leads. Design B shares the same lead length of design A with an increased pad width. Design C is an aggressive, shorter, footprint length, but has been eliminated because it cannot be detected by AOI systems. Design D is a modified version of design C, which is inspectable by AOI systems. The board-level SJR results are plotted in **Figure 7**. All three footprints (A, B, and D) exceeded the general automotive SJR requirement. Design D performs the best—not showing a failure on the J-leads until 9,791 cycles. It is the recommended PCB footprint design for MaxQFP.

Automated optical inspection system study. Because the solder joints of J-leads after PCB mounting reside under the package body, they are not inspectable with legacy AOI systems that only offer a top view. Therefore, for solder joint inspection of MaxQFP (or a PLCC, for

Footprint design	Gull-wing lead pad length (mm)	J-lead pad length (mm)	Pad width (mm)
A	1.45	1.00	0.28
B	1.45	1.00	0.30
C	1.12	1.12	0.28
D	1.40	1.40	0.28

Table 3: Four PCB footprints explored for MaxQFP.

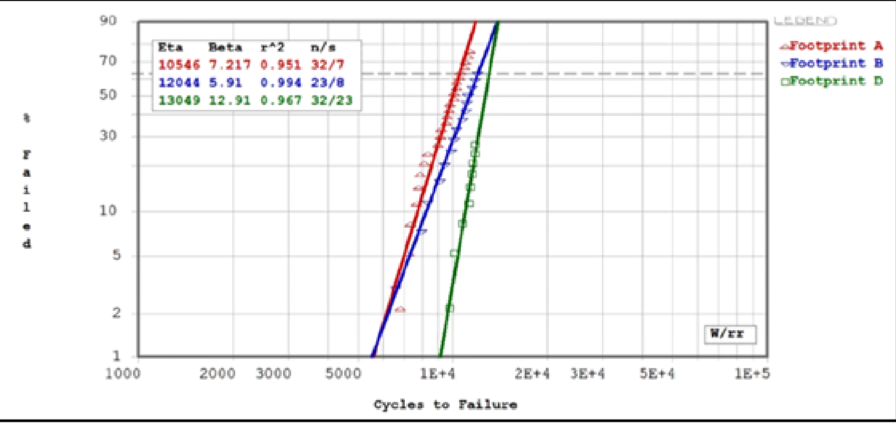


Figure 7: Board-level TC stresses (-40 to +125ºC) results for designs A, B, and D using daisy chain samples. The first failure on design D is 9,791 cycles on the J-lead.

that matter), systems equipped with side-view cameras are required. An example of such AOI images are shown in Figure 8. The side camera of this AOI system is able to capture the light reflection of J-lead solder joints, where a top-view camera is not able to do so.

Thermal performance study. As with any semiconductor package, thermal performance is a critical characteristic. For MaxQFP, this is particularly so because it effectively shrinks the body size compared to QFPs. This smaller body size results in less area from which to conduct or convect heat. The thermal resistance from junction to ambient air (θ_{JA}) is commonly used to determine thermal performance of each package type and can be calculated by a thermal simulation model. The procedure is defined in the JEDEC JESD51-2A specification [10] for a natural convection environment. Following this method, the θ_{JA} values of a 172-lead MaxQFP, a 172-lead MaxQFP_EP, a 176-lead QFP, and a 176-lead QFP_EP are calculated and compared in Table 4. These packages are all modeled assuming a two layers of signal and two layers of power (2s2p) thermal test board consistent with that described in the relevant JEDEC specification (JESD51-7) [11]. These θ_{JA} values are not meant to predict the performance of a package in an application environment on a product PCB.

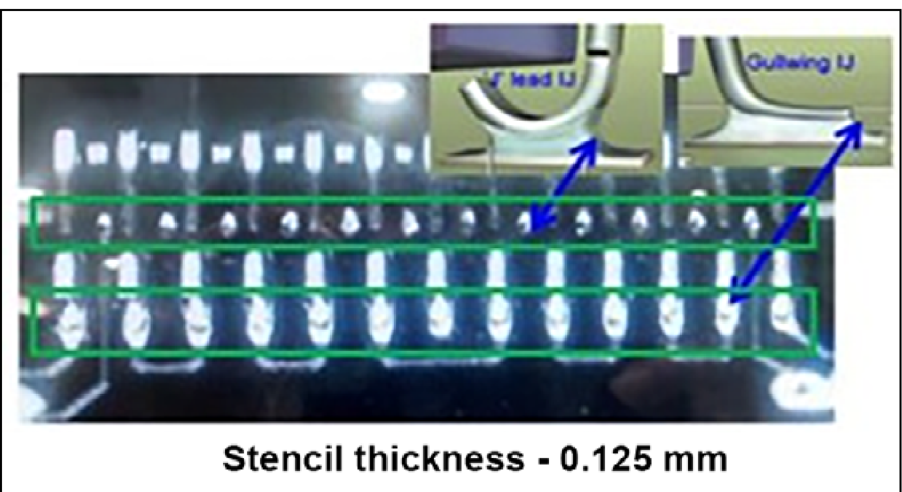


Figure 8: An AOI image of a good solder joint where both J- and gull-wing lead joints are visible. This PCB used a 0.125mm solder paste stencil thickness. This image required a side camera to capture the light reflection.

	θ_{JA} (C/W)		
Die size (mm^2)	45	50	55
172 lead MaxQFP (16x16)	27.14	26.54	25.94
176 lead LQFP (24x24)	32.67	31.00	29.33
172 lead MaxQFP_EP (16x16)	20.40	20.00	19.60
176 lead LQFP_EP (24x24)	22.67	22.33	22.00

Table 4: Thermal resistance value (θ_{JA}) comparison between MaxQFP and QFP at similar pin counts.

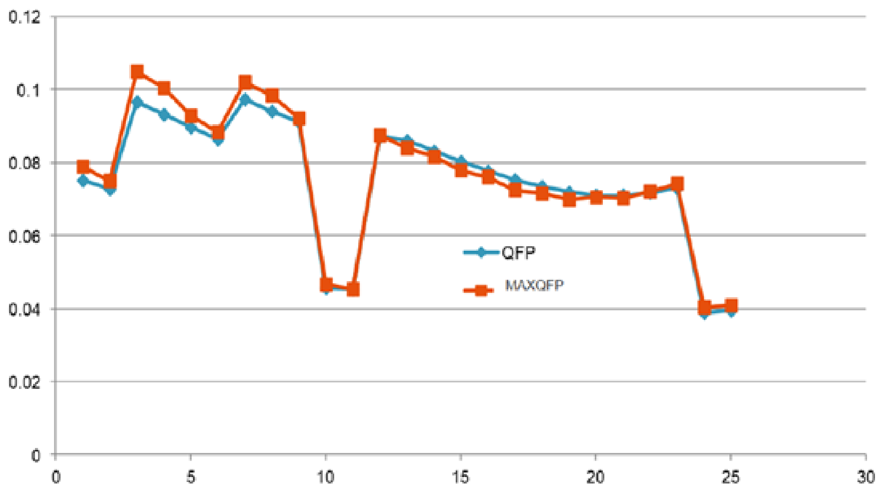
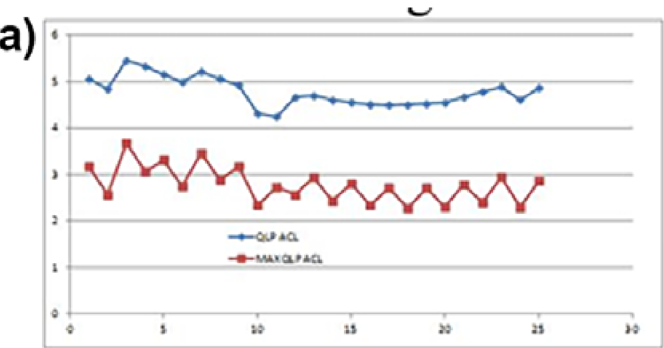


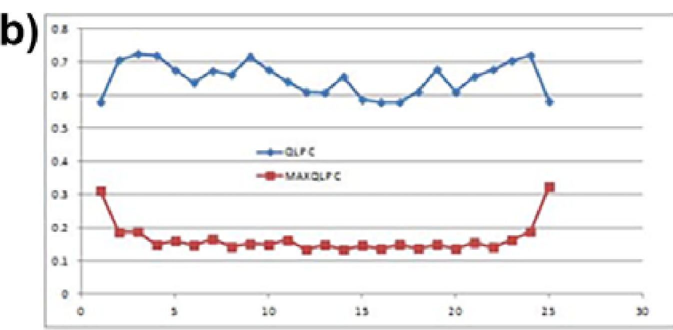
Figure 9: DC resistance comparison between a 100-lead MaxQFP and a 100-lead QFP.

Three die sizes (45, 50 and 55mm^2) were modeled for all four package types to calculate the θ_{JA} values. As expected, a larger die size can result in a relatively smaller θ_{JA} value at the same body size. Also expected, a package with an exposed pad has much better thermal performance than one without, because the additional heat transfer area is considerable. The surprising result here is that the 55% smaller MaxQFP package performs better thermally than the larger QFP package at similar pin counts. Comparing same die sizes, the improvement is about 16% for MaxQFP and about 10% for MaxQFP_EP. The reason for this performance improvement is likely the high lead count density (i.e., leads per area) of MaxQFP compared to QFP. Again, this was a nonintuitive and surprising result, especially for the exposed pad package. But, these results clearly indicate that MaxQFP can fully replace QFP from a thermal perspective and even offer an advantage.

Electrical performance study. The 100-lead MaxQFP package (body size 10x10mm) was chosen for an electrical performance study and its characteristic results were compared with those of a 100-lead QFP (body size 14x14mm). Like the thermal performance study discussed above, this electrical performance study was also conducted by simulation. The die size used in the simulation was 4.25 x 3.91mm. The wire lengths ranged from 1.71 to 2.36mm for the 100-lead MaxQFP part, and from 1.84 to 2.35mm for the 100-lead QFP part. The direct current (DC)



MaxQFP has lower signal net self inductance(@ 100 MHz)



MAXQLP has lower signal net self capacitance(@ 100 MHz)

Figure 10: a) (left) Self-inductance values at 100MHz for both 100-lead MaXQFP and 100-lead QFP; and b) (right) Self-capacitance values at 100MHz for both 100-lead MaXQFP and 100-lead QFP.

resistance is almost identical between these two parts as shown in Figure 9. However, because of a smaller body size, the 100-lead MaxQFP shows lower signal net self-inductance and capacitance values at 100MHz than those of the 100-lead QFP (Figure 10). As a result of lower self-inductance and capacitance, the 100-lead MaxQFP package is expected to have less return loss for signal nets than the 100-lead QFP, as indicated in Figure 11. Overall, the 100-lead MaXQFP package has improved electrical performance as compared to an equivalent lead count QFP, driven both by the smaller body size, and the addition of the short-electrical-path J-leads.

Summary

The semiconductor industry is in a constant drive for miniaturization, reduced cost, increased performance, and improved quality and reliability. This drive persists even in spaces where more mature packaging technologies reign. MaxQFP is a new package aimed precisely towards these objectives.

Often, the goal of package miniaturization can only be accomplished by increasing the fragility of the package and by driving ever-finer dimensions on the PCB. Notably, MaxQFP performs even in extreme environmental use cases as encompassed by the AEC Grade 1 and Grade 0 standards and can be used even with standard PCB design rules.

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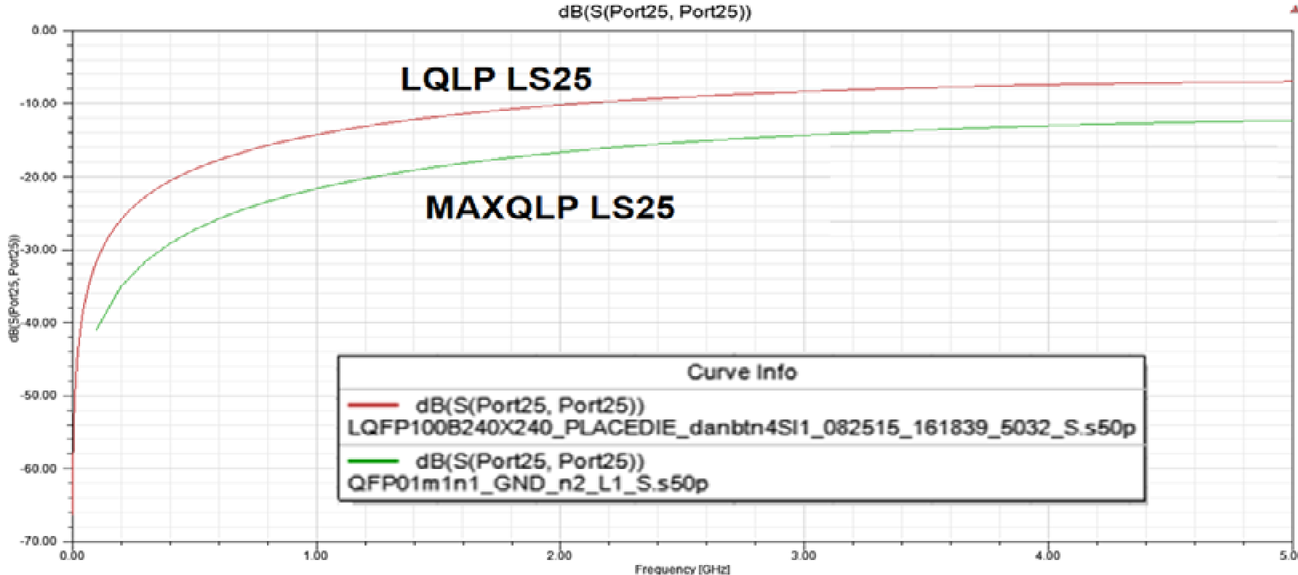

Figure 11: Return loss of signal nets for both 100-lead MaxQFP and 100-lead QFP.

Most of the reliability results presented here focus on the MaxQFP package without an exposed pad. Mechanical simulations indicate that the MaxQFP_EP package will have similar reliability performance. As a future effort, empirical data will be collected on 172-lead MaxQFP_EP packages to verify this prediction.

References

1. C. C. Lee, et al., "Challenges of Cu wire bonding on low-k/Cu wafers with BOA structures," Proc. 60th Elec. Comp. & Tech. Conf. 2010, pp. 342 – 349.
2. T. A. Tran, et al., "Copper wire bonding on low-k/copper wafers with bond over active structures for automotive customers," Proc. ECTC 2011, pp.1508-1515.
3. C. C. Lee, et al., "Copper versus palladium coated copper wire process and reliability difference," Proc. 63rd ECTC 2014, pp.1539 – 1548.
4. C. C. Lee, et al., "Copper ball voids for Pd-Cu wires: affecting factors and methods of controlling, Proc. 66th ECTC 2016, pp. 606 – 613.
5. https://www.nxp.com/products/processors-and-microcontrollers/arm-microcontrollers/s32k-automotive-mcus/s32k3-microcontrollers-for-general-purpose:S32K3
6. P. Su, et al., "Effect of the microstructure and whisker growth propensity of Sn finish," Proc. 55th ECTC 2005, pp. 434 – 440.
7. JESD201, "Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes" (available at http://www.jedec.org).
8. http://thor.inemi.org/webdownload/newsroom/Presentations/ECE/Tin%20Whisker%20Workshop%20May%202005/Statistical%20Study.pdf
9. P. Su, J. Howell, S. Chopin, "A statistical study of Sn whisker population and growth during elevated temperature and humidity storage tests," IEEE Trans. Elec. Packaging Mfg., 55th ECTC Workshop 29 (2006) 246.
10. https://www.jedec.org/document_search?search_api_views_fulltext=jesd51
11. https://www.jedec.org/standards-documents/docs/jesd-51-7

Biographies

Chu-Chung (Stephen) Lee is the Development Leader for MaxQFP at NXP Semiconductors in Austin, TX. He has 24 years of experience in the semiconductor industry, specializing in wire bonding and packaging. He holds 28 U.S. patents and has published 38 technical papers in the fields of semiconductors and electrochemistry. He earned his doctorate in Materials Science from the U. of Southern California. Email: stephen.lee@nxp.com

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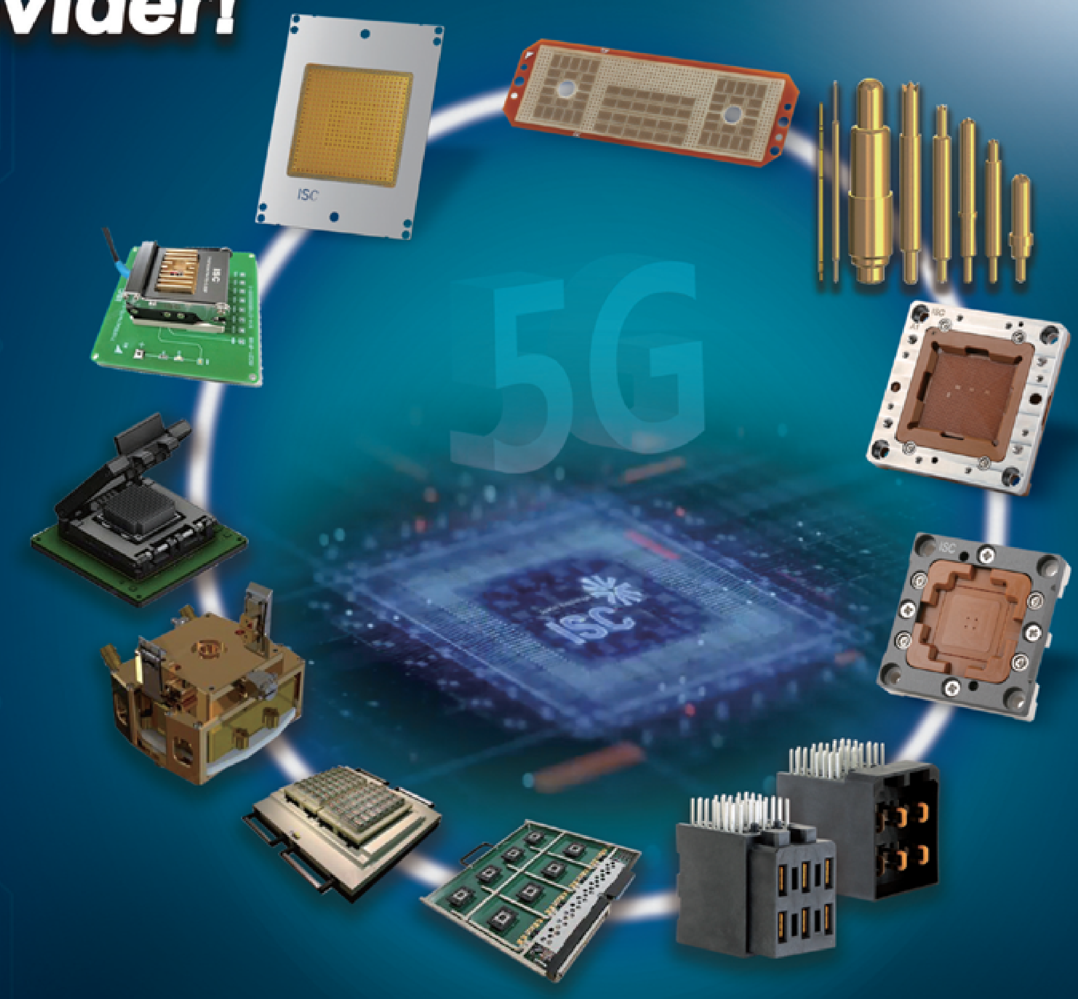

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Sustaining Moore's Law with graphene

By Kunjesh Agashiwala, Junkai Jiang, Ankit Kumar, Chao-Hui Yeh, Kaustav Banerjee [University of California, Santa Barbara]

Since the invention of metal-oxide-semiconductor (MOS) integrated circuits in the early 1960s, the speed, capacity, and complexity of the chips have increased dramatically, roughly following Moore's Law, owing to various technological and process breakthroughs that doubled the transistor count per chip area every two to three years. Along with the advancement in transistor technology, the wires (or interconnects) that connect these billions of transistors have also evolved tremendously. **Figure 1** provides a snapshot of the evolution of the interconnect and intra/inter-layer dielectric (ILD) technology, also known as back-end-of-line (BEOL) technology. The aluminum (Al) wires used initially during 1960-1980 were replaced by better performing aluminum-copper (Al-Cu) wires, which were followed up in 1997 by the currently employed dual-damascene (DD) wiring scheme utilizing electroplated Cu, resulting in denser, faster, and more reliable wiring solutions.

Scaling limitations of conventional interconnect materials

Even though cobalt (Co) has recently been introduced as a possible substitute for the narrowest Cu lines to keep Moore's Law alive, these technologies will eventually run out of steam when wiring dimensions approach sub-20nm. At these critical dimensions, conventional technologies such as Cu, Co, and noble metals such as ruthenium (Ru) suffer from significant size effects, mainly due to a nonlinear increase in resistivity, and resulting wire and via resistances, which increases RC-delay and self-heating, degrades electromigration reliability, and thereby limits their current-carrying capacity and performance (**Figure 2a-c**) [1,2]. Additionally, void formation during metal fills in highly scaled (and high aspect ratio [AR]) trenches and via holes during the DD process exacerbates the reliability and variability problems, thereby making further increase in the aspect ratio difficult. Traditional solutions will fail to meet the performance-based current density requirements set forth by the International Roadmap for Devices and Systems (IRDS) beyond 15nm wiring dimensions, as shown in **Figure 2d**, necessitating an urgent need to identify alternative metallization strategies to keep Moore's Law alive.

What is so exciting about graphene interconnects?

Since its discovery in 2004 [4], graphene has been proposed as a potential material for future electronics because of its unique electrical, optical, and mechanical properties. Initially derived from its 3D layered allotrope-graphite (**Figure 3a**), graphene is a single atomic-layer-thick sheet of carbon atoms (**Figure 3b**). A hexagonal honeycomb crystal structure of graphene (**Figure 3c**) is formed by the sp^2 hybridized in-plane bonding arising from the electron sharing of each carbon atom with three nearest carbon atoms (**Figure 3d**) with exceptionally high mechanical strength. This results in a unique electronic band-structure shown in **Figure 3e** where the conduction and valence bands precisely

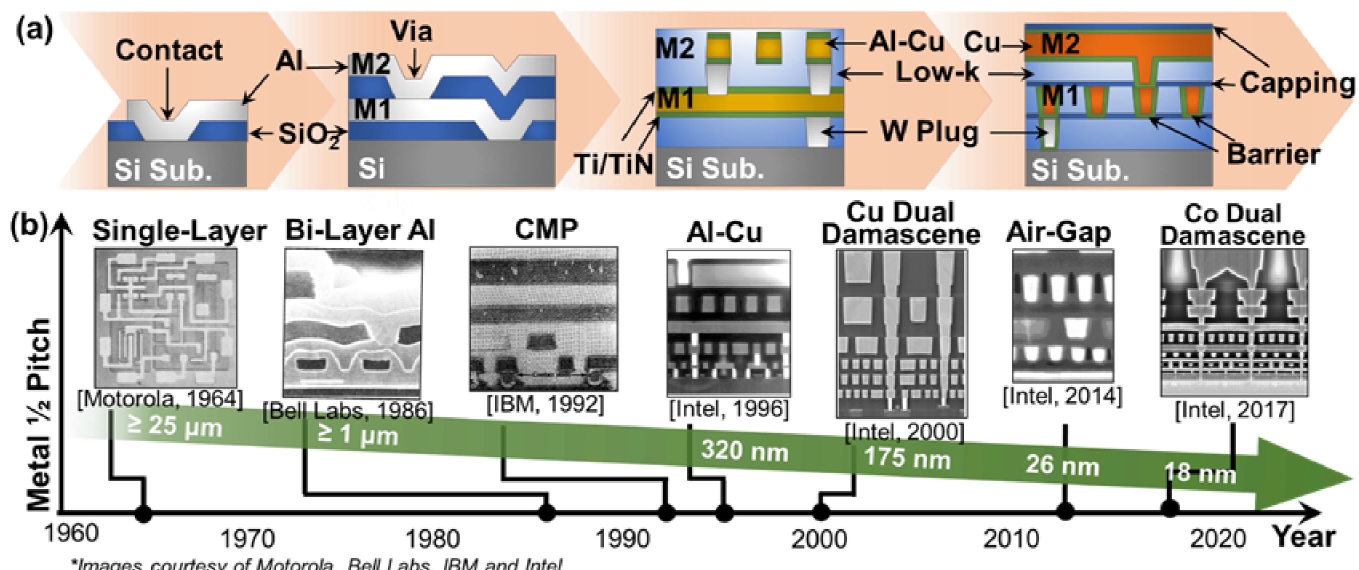


Figure 1: Evolution and scaling of BEOL technology—from the use of Al wires and SiO_2 dielectric to the current state-of-the-art dual-damascene technology based on Cu and low-k dielectrics: a) A cross-sectional view of the various metallization technologies adopted by the semiconductor industry. b) Scaling of the metal-1 ½ pitch along with the cross-sectional scanning electron microscope (SEM) images corresponding to each new technological evolution.

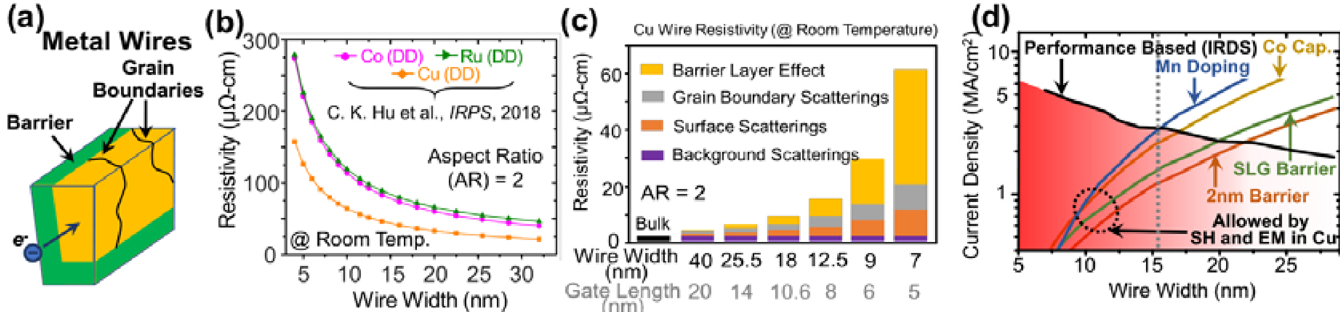


Figure 2: Challenges of the current BEOL technology: a) Schematic of the typical interconnect structure used in current CMOS technology with the barrier layer (in green) and the metal (in yellow). b) Resistivity vs. wire width for conventional metal interconnects as a function of wire width. The significant resistivity/resistance increase for sub-20nm critical dimensions is primarily due to the inability of the barrier layer to be scaled down at the same rate as the actual metal itself, which is shown in (c) to contribute more than 50% of the total wire resistivity at sub-10nm wire widths. d) Circuit-performance required current density for integrated circuit interconnects and the maximum allowed current density for Cu interconnects with TaN and single-layer graphene (SLG) barrier, Co capping, and Mn doping (from electromigration (EM) reliability and self-heating). While Mn doping and Co capping help in increasing the current-carrying capacity by restricting the diffusion (and hence, EM) of Cu atoms, it severely increases the wire resistance. The maximum current density allowed by self-heating and EM for Mn doping and Co capping are estimated from Black's equation by using the experimentally obtained activation energy and the time to fail data. More information is available in [3].

cross at Dirac points, thereby making graphene a zero-bandgap semimetal. Moreover, the linear energy dispersion (E-k relation) of electrons around Dirac points (**Figure 3e**) makes graphene different from other materials like silicon with parabolic electron dispersion. By patterning graphene into nanoribbons (**Figure 3f**), a bandgap can be opened (**Figure 3g**) because of the confinement of carriers in such materials; the magnitude of this bandgap is a critical function of the graphene nanoribbon (GNR) width and thickness [5] (**Figure 3f**). Furthermore, this bandgap is an indication of the highly nonlinear effects that occur at sub-50nm wire dimensions in these materials [6]. These nonlinearities can be alleviated by introducing foreign atoms/molecules between the layers of graphene, also called intercalation doping, offering high flexibility in designing systems using graphene [7-9].

Multiple layers of graphene (also called multilayer graphene (MLG)) are preferred for designing interconnects and systems as compared to monolayer graphene. This is primarily because of its lower contact resistance and higher density of states compared to monolayer graphene. Unlike monolayer graphene, MLG has a parabolic band structure, which, after intercalation, significantly shifts the Fermi level and restores the linear band structure of monolayer graphene, offering a dual benefit of not only tackling the nonlinearities, but also significantly modulating its conductivity [9]. Moreover, the strong sp^2 hybridized bonds in graphene/MLG offer a substantially higher melting point than conventional metals (**Figure 4a**), and significantly higher mechanical strength (stronger than steel) and in-plane thermal conductivity. On the other hand, graphene's extraordinary electrical conductivity is due to the π band (**Figure 3d**, **e**). These unique traits, in conjunction with low $\rho_0\lambda$ product (**Figure 4a**) (which signifies lesser electron scatterings at the surfaces and grain boundaries at ultra-scaled dimensions, and hence reduced resistivity size effect, **Figure 4b**), high carrier mobility, and high carbon abundance (inset of **Figure 4a**) make graphene (or more specifically, doped multi-layer graphene (DMLG)) an ideal candidate for next-generation on-chip interconnects [7,8]. Apart from Cu, Co, and the noble metal Ru, several other noble metals (Pt, Ag, Au) and layered materials (MoS_2, WTe_2) have been considered as potential interconnect candidates, however, they either cannot match the performance-based current density requirements, or suffer from poor carrier concentration, thereby restricting their use in upcoming BEOL technology nodes [7].

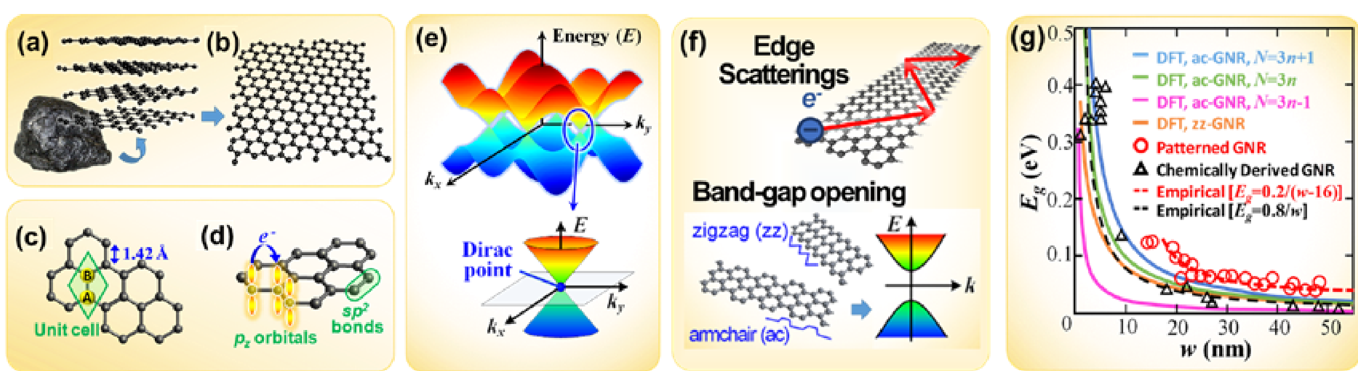
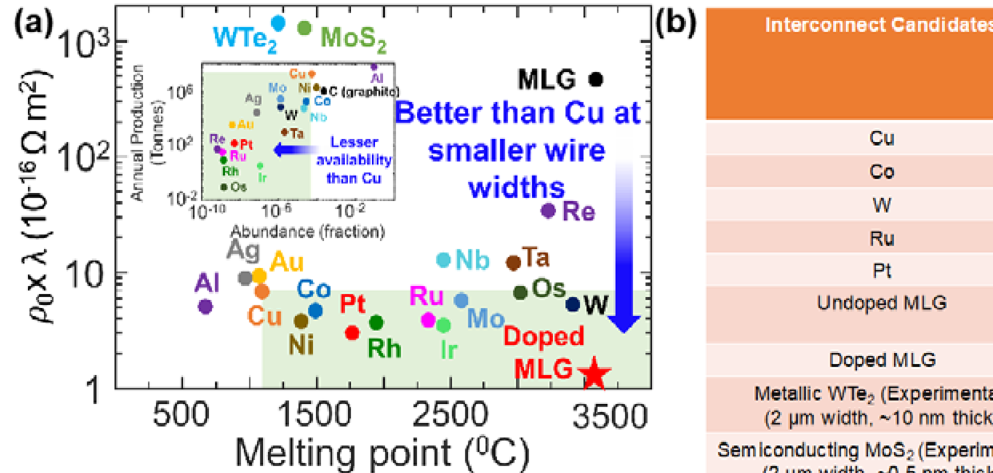


Figure 3: Fundamentals of graphene and GNR. a-b) Graphite to graphene transition; c) Crystal structure of graphene showing the unit cell. d) sp^2 bonding of graphene forming in-plane σ band, and origin of the π bands (from the out-of-plane p_z orbitals) that are responsible for its amazing electrical conductivity. e) Electronic band-structure of the π band of graphene displaying linear E-k dispersion of electrons and zero bandgap with the conduction and valence band edges meeting at the Dirac point. f) Various nonlinear effects (edge scatterings and bandgap opening) in graphene as its width is scaled down to sub-50nm critical dimensions. g) Bandgap (E_g) tunability of GNR, where N is the number of carbon atoms along the width (w) of GNR and n is a natural number [5].



Interconnect Candidates	Resistivity (µΩ-cm) @ 20 nm wire width		
	AR = 2	AR = 1	AR = 0.5
Cu	32.91	45.8	62.03
Co	59.88	82	113.27
W	34.04	36.864	42.517
Ru	66.033	88	119.06
Pt	30.93	34.69	42.23
Undoped MLG	543.37	543.37	543.37
Doped MLG	15.17	15.17	15.17
Metallic WTe_2 (Experimental) (2 µm width, ~10 nm thick)	~8x10³		
Semiconducting MoS_2 (Experimental) (2 µm width, ~0.5 nm thick)	~5x10³		

Figure 4: Advantages of graphene as a prospective interconnect technology can be seen in the following: a) Product of bulk resistivity (ρ_0) and mean free path (λ) vs. the melting point of various conventional interconnect candidates in comparison to that of MLG, used for identifying the best interconnect candidate for advanced technology nodes. The conductivity of bulk MLG can be significantly modulated by doping to bring it inside the desired green corner, making it the best interconnect candidate for replacing Cu. The inset figure shows the annual production of various metals used in (or considered for) the BEOL technology. b) Table showing the resistivity of various metal candidates and two-dimensional (2D) van der Waals materials in comparison with doped ($E_F = \pm 0.6$eV) and undoped MLG at a wire width of 20nm and aspect ratios of 0.5, 1, and 2, indicative of the resistivity size effect for the conventional metals as compared to graphene.

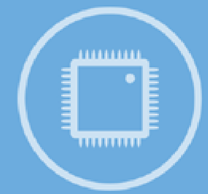
Integrating graphene interconnects in CMOS

Micromechanical (or liquid) exfoliation of graphene from bulk graphite yields relatively small (micron sized) flakes that are not suitable for a complementary metal-oxide semiconductor (CMOS) process. The most common approach for growing relatively large-area graphene is to use chemical vapor deposition (CVD), which is based on the thermal decomposition of its gas-based precursors on a metal catalyst substrate such as Cu or Ni. While this approach yields high-quality graphene/MLG, it not only requires temperatures that are far higher than the BEOL thermal budget (<450ºC), but also requires a transfer from the metallic growth substrate to the desired substrate, making it unsuitable for direct application in the BEOL CMOS process. Other techniques to grow graphene, such as epitaxial growth, or solid-phase growth, also require much higher temperatures than the allowed thermal budget and the resulting MLG quality is not sufficient for interconnect application (see **Table 1** for a summary of various growth methods). Recently, the Nanoelectronics Research Lab (NRL) at UC Santa Barbara devised a new approach for growing high-quality multi-layer graphene at significantly lower temperatures (~300ºC), by a pressure-assisted solid-phase diffusion of carbon atoms through the bulk and grain-boundaries of a sacrificial catalyst metal (Ni) [8]. Approximately 20nm-thick MLG can be grown using ~65-80psi of mechanical pressure and ~30-60min of growth time.

Figure 5a shows the cross-sectional schematic of the wafer/chip during the growth process. This technique is highly versatile and possesses the capability to be engineered to directly grow high-quality low-temperature graphene/MLG with varying thicknesses on arbitrary substrates [10]. The quality of graphene/MLG developed using this technique is equivalent to that produced using traditional methods (**Figure 5b**), making

Graphene Synthesis Technique	Pros	Cons	CMOS-Compatible?
Mechanical Exfoliation	• Excellent quality (high crystallinity) • Room temperature process	• Requires transfer • Difficult to control the number of layers • Small area flakes	No
Liquid Exfoliation	• Good growth quality • Room temperature process • Large-area flakes (~50-100 µm)	• Non-uniform area coverage • Difficult to precisely control thickness • Low-crystallinity • Requires transfer	No
Chemical Vapor Deposition (CVD)	• Excellent growth quality • N/P doping possible	• High growth temperature (~1000 °C) • Requires transfer • Difficult to control the number of layers and area coverage	No
Plasma Enhanced CVD (PECVD)	• Excellent growth quality • Direct growth on dielectric substrates • N/P doping possible	• High growth temperature (~600 °C) • Non-uniform area coverage • Non-uniform doping	No
Epitaxial Growth on SiC/Ru	• Direct growth on SiC/Ru • Excellent growth quality • Wafer-scale area coverage	• Very high growth temperature (~1100 °C) • Thickness restricted to 1-2 layers • Need UHV environment	No
Solid-Phase Epitaxy (using amorphous carbon)	• Good growth quality • Direct growth below catalyst metal (no transfer)	• High growth temperature (~900 °C) • Non-uniform growth quality	No
Solid-phase Segregation and Precipitation	• Good growth quality • Wafer-scale coverage	• High growth temperature (~1000 °C) • Difficult to control the number of layers • Graphene growth on catalyst metal	No
Catalyst Metal Agglomeration	• Good growth quality • Direct growth on multiple substrates • Controllable thickness	• High growth temperature (~800 °C) • Non-uniform growth • Small area coverage	No
Pressure and Temperature Assisted Solid-Phase Growth (NRL-UCSB)	• Low-temperature (~300-350 °C) • High quality growth • Direct growth (no transfer) • Wafer-scale coverage • Controllable thickness • N/P doping possible	• Needs specialized tool – commercially unavailable • Graphite powder may require specialized processing/handling	Yes

Table 1: Summary of various graphene/MLG growth techniques reported in the literature. The growth method developed in NRL-UCSB is the only method capable of satisfying the crucial CMOS-compatibility criterion.



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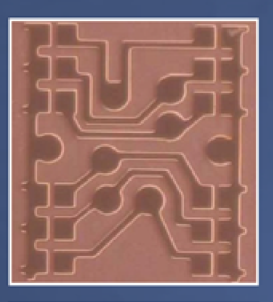
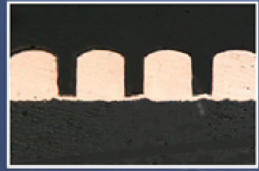
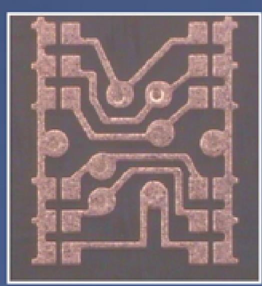
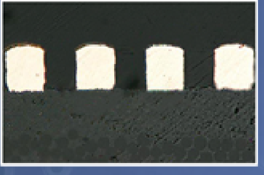



Before Final Etch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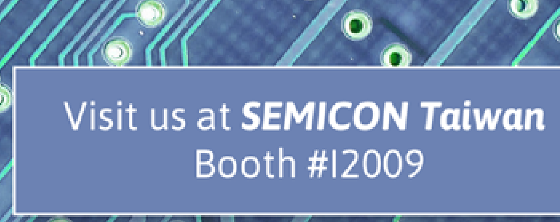

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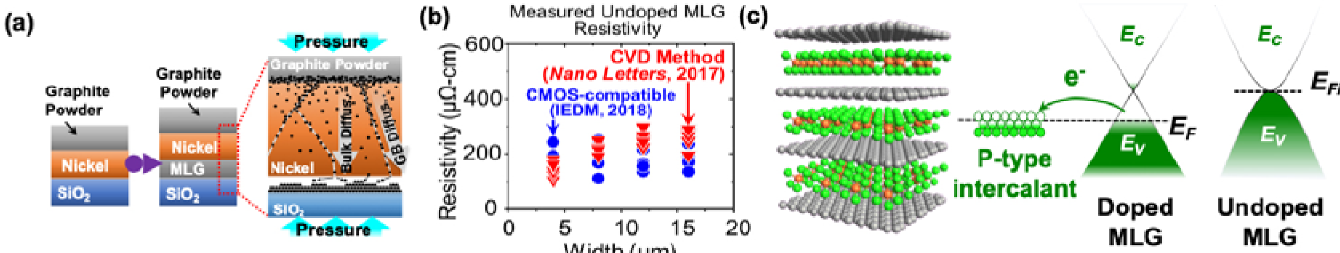

Figure 5: CMOS-compatible multilayer graphene (MLG) growth. a) Cross-sectional view of the wafer during the pressure-assisted CMOS-compatible solid-phase graphene growth technique. The growth occurs through the diffusion of carbon atoms through the grains (bulk) and grain boundaries of the sacrificial catalyst metal, Ni. b) Resistivity vs. wire width of undoped MLG using the CMOS-compatible growth technique in comparison with the conventional CVD method [7]. c) Schematic of $FeCl_3$ intercalation-doped MLG structure, and the corresponding band-diagram of MLG before (undoped) and after (doped) intercalation.

it a viable option for BEOL integration [8,11]. Additionally, the introduction of suitable intercalants/dopants between the layers of MLG (**Figure 5c**) can lead up to ~5x improvement in resistivity, ~4x improvement in RC-delay, and ~80%/72% benefit in switching energy at the local/global level wires as compared to conventional interconnect materials (**Figure 6a-d**) [7], respectively. Furthermore, DMLG interconnects provide 100-fold higher current-carrying capacity with respect to conventional metals, making them an ideal material for next-generation interconnect technology. While the above-mentioned demonstration has opened a clear pathway for the integration of graphene/MLG in CMOS technologies, it is worth noting that the idea of DMLG was first proposed by NRL [13], followed by various other important technological innovations relevant to graphene/MLG interconnects. **Figure 7** provides a snapshot of the evolution of the key achievements in graphene/MLG interconnect technology at NRL including its robustness under high-current/electrostatic discharge (ESD), which is a major reliability issue [14].

While the reliability and performance of single-level MLG wires have been studied in detail, a key remaining requirement in the application of MLG as interconnects in today's semiconductor technologies is the demonstration of a multi-tier MLG wire/via system incorporating low-resistance contacts. This is crucial for demonstrating the benefit of MLG wires in contacting the transistors at the local level. The primary step for achieving this is to first grow high-quality MLG reliably on multiple levels. **Figure 8a-b** shows the demonstration of large-area multi-level graphene (separated by a 200nm ILD) using the CMOS-compatible growth technique. Almost identical characteristics as compared to the bottom MLG are also observed for the top MLG, as evidenced by the various structural and optical characterizations for both top and bottom levels (**Figure 8a-b**). The layered structures at both the top and bottom levels confirm the versatility of the growth technique for arbitrary surface topologies. Because of the difficulty of graphene/MLG to be grown vertically in trenches, we employed the age-old subtractive etching (SE) technique, which was initially used for Al interconnects, to join multi-level MLG interconnects with metal vias in an edge-configuration [10], which is the preferred method of contacting MLG while simultaneously minimizing the additional contact resistance. Rigorous scaling analyses indicate that the increase in the total via resistance in the case of the MLG/metal-via multi-level structure is more than compensated by the reduced MLG wire resistance (for a fixed AR = 2), resulting in ~2-fold improvement in the overall circuit performance at sub-10nm critical dimensions.

It is worth observing that the CMOS-compatible growth process can be extended to grow MLG on arbitrary substrates if the growth conditions do not result in the thermal degradation of the substrate [10]. Because of the inability of the conventional barrier/capping layer materials (TaN/Si_3N_4) to be scaled down below ~0.5nm (as it could otherwise lead to the diffusion of Cu into the surrounding dielectric), graphene-based capping to conventional metal

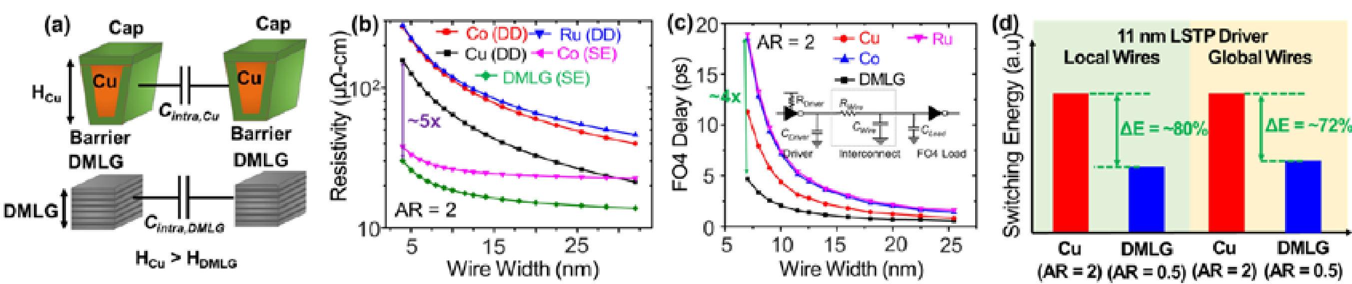

Figure 6: Performance analyses of CMOS-compatible single-level MLG interconnects: a) Schematic of two parallel copper wires of thickness H_{Cu} with barrier layer, in comparison with two adjacent doped-MLG wires, with a height of H_{DMLG}; significant reduction in intra-layer parasitic capacitance can be obtained for DMLG wires, as compared to copper ($C_{intra,Cu}$>>$C_{intra,DMLG}$). b) Resistivity vs. wire width for conventional metal interconnects in comparison with DMLG. c) Delay for a unit-sized inverter driving a FO4 load via 100x minimum gate pitch local interconnects, as a function of wire width. d) Switching energy comparison between Cu and DMLG interconnects connecting 11nm multi-gate LSTP driver, showing ~80%/72% benefits in energy savings for local/global wires, respectively, assuming the same delay penalty of ~5% for both local/global wires. A power-optimal repeater insertion methodology [12] has been assumed for global wire simulations.

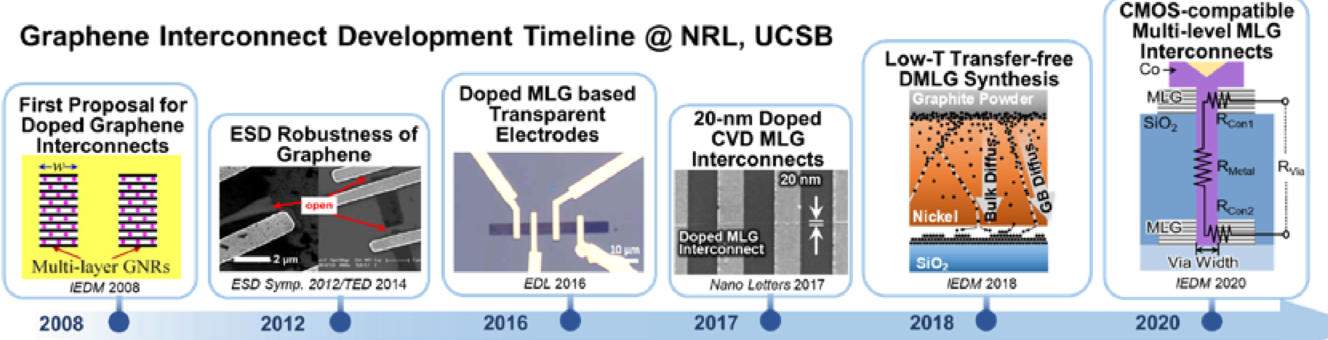

Figure 7: Graphene interconnect technology development timeline at NRL, UCSB: Evolution of graphene as an interconnect technology from the first proposal of doped graphene interconnects in 2008 to the demonstration of CMOS-compatible multi-level graphene interconnects in 2020.

interconnects is being actively evaluated, and has been demonstrated to reduce overall resistance by 15% [15]. With that in mind, NRL recently demonstrated BEOL-compatible growth of high-quality MLG directly on Cu by inserting ~2nm amorphous carbon layer between Ni and Cu [10]. In principle, with a smart choice of the overall growth conditions, and a thorough knowledge of the relative diffusion coefficients of carbon in the growth catalyst and growth substrate, this technique can be engineered to grow MLG on various metallic (Co, Ru, W, Pt, etc.) and dielectric surface topologies. Moreover, the current wafer coverage of ~10mm^2 can be expanded to directly grow high-quality MLG on 300mm industry standard wafers, making this technique extremely versatile and industry friendly.

Intercalated MLG inductors overcome a 200-year-old limit

On-chip inductors are essential components in almost all modern electronic gadgets such as smartphones and computers and can occupy up to 50% of the total chip area. However, unlike all other IC components that shrink with each technology node, inductors are hard to scale down as they solely rely on their magnetic inductance (**Figure 9a**). Therefore, the design of inductors has remained basically unchanged since their invention almost two centuries ago. NRL at UCSB overcame this fundamental scaling challenge by evoking sizable "kinetic inductance (KI)" (**Figure 9b**) in intercalation-doped MLG inductors at room temperature, leading to materials with the highest inductance densities ever created [9]. In contrast to conventional magnetic inductance, kinetic inductance arises from the intrinsic inertia of the charge carriers and appears in series with magnetic inductance, hence increasing the overall inductance for a given inductor footprint (**Figure 9b**). Intercalation

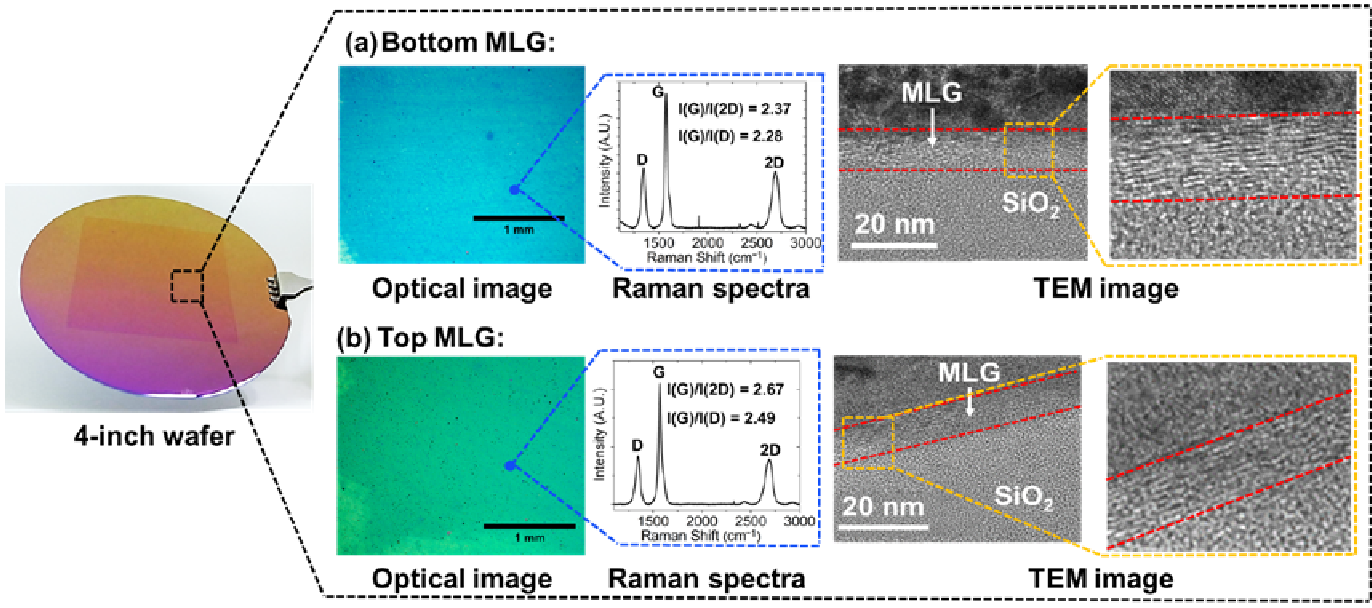

Figure 8: CMOS-compatible multi-level MLG interconnects (separated by 200nm ILD) grown on a 4-inch silicon wafer. a) Optical image of a large-area MLG (bottom level) grown using the solid-phase growth technique. The sharp G and 2D peaks in the single-point Raman spectrum confirm the uniform high-quality growth. Cross-sectional transmission electron microscope (TEM) images clearly show the layered structure of graphene, once again confirming the high growth quality. b) Similar to the bottom-level, the top MLG (optical image) is fabricated under the same conditions and exhibits almost comparable quality and thickness, as evidenced from the large area optical image, single-point Raman spectra and cross-sectional TEM image. The electrical properties of the bottom MLG before and after the fabrication of the top MLG (and Co-via) yielded nearly identical resistances.

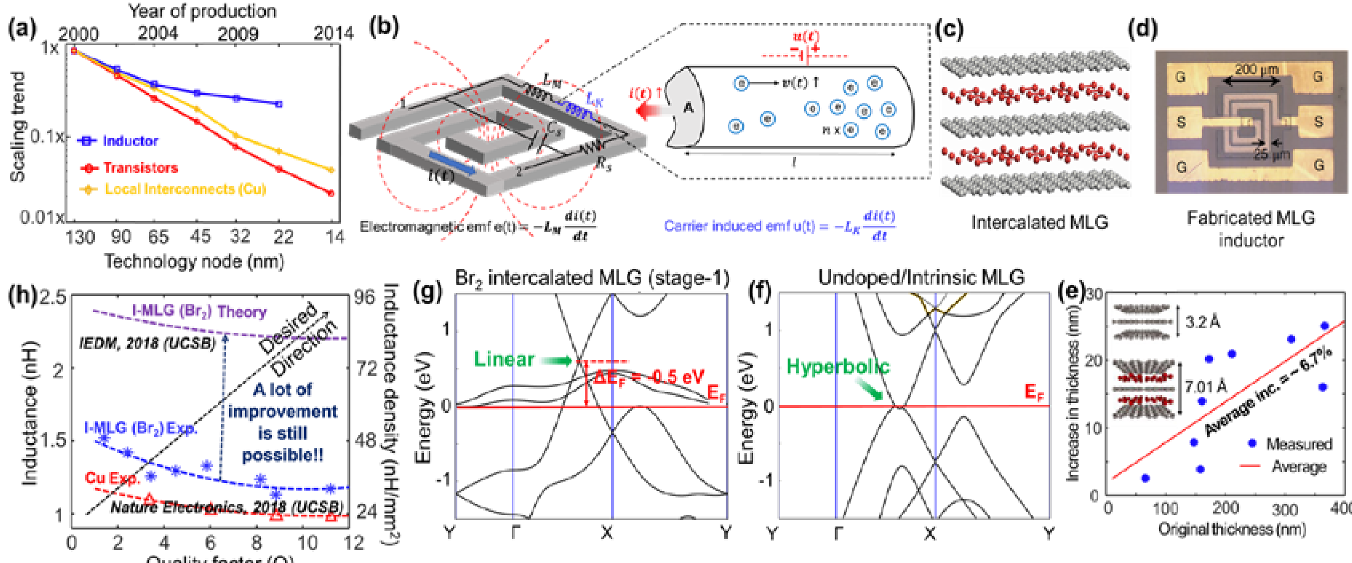

Figure 9: High-performance intercalation-doped MLG inductors exhibiting kinetic inductance: a) Comparison of scaling trends: required area of a typical on-chip inductor vs. area of a single logic transistor (= gate pitch × metal pitch) and width of M1 interconnect. All the data were normalized with respect to the 130nm node. b) Schematic showing the difference between the conventional magnetic and kinetic inductance. c) Schematic of an intercalation-doped MLG. Intercalation doping introduces foreign atoms (Br_2) between the layers of MLG. d) Optical image of a Br_2 intercalation-doped MLG inductor. e) Thickness increment after doping for MLG ribbons with various initial thicknesses. f) Hyperbolic band structure of intrinsic/undoped MLG. g) Linear band structure of intercalation-doped MLG showing the doping effect, as evident from the shift in the fermi level. h) Inductance and corresponding inductance density versus quality factor for the spiral square inductor fabricated in (d).

doping provides high Q-factors of up to 12, while the KI increases the total inductance-density by ~1.5-fold and thereby allows inductor scaling for the very first time. This development is crucial for the Internet of Things (IoT) industry and has been justifiably touted as a "trillion-dollar breakthrough" by Forbes magazine [16] (**Figure 9b-g**). Intercalation doping essentially increases layer separation in MLG that leads to recovery of the linear band structure of monolayer graphene, which possesses the highest KI (**Figure 9e-g**). Further process and doping optimization can provide up to 10-fold higher inductance densities [17] and pave the way for next-generation IoT and wireless applications (**Figure 9h**).

Wafer-scale integration and manufacturing challenges for graphene

One of the main challenges for the large-scale integration of MLG/DMLG into CMOS processes is the absence of a wafer-scale MLG growth tool satisfying the BEOL thermal budget and process requirements. The graphene synthesis technology pioneered by NRL presents a comprehensive solution to the various challenges of integrating MLG into large-scale manufacturing of not only interconnects and inductors, but also graphene-based transparent electrodes [14,18], RFIDs and solar cells (**Figure 10a**), and therefore, warrants the need for more sophisticated temperature and pressure controllers to precisely deposit a desired thickness of graphene/MLG on a given substrate over a large area.

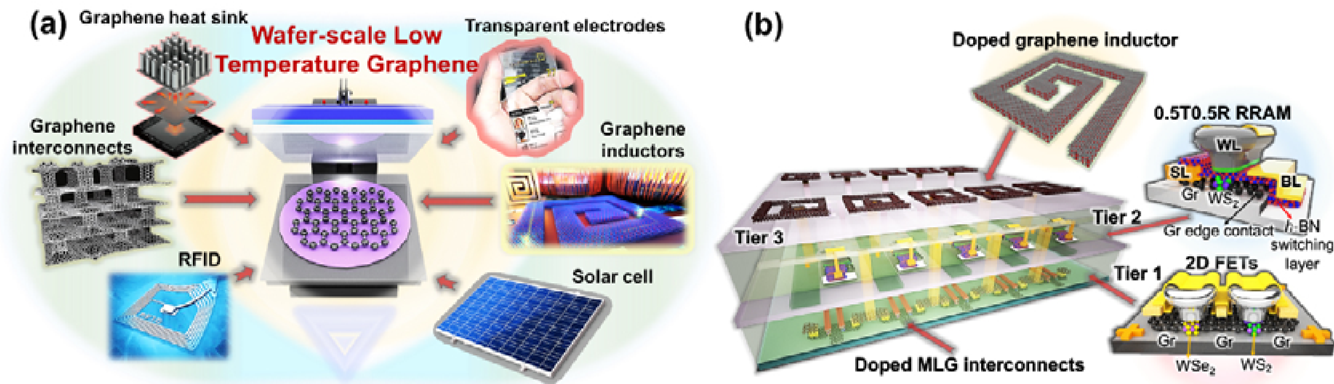

Figure 10: Applications of MLG in electronics: a) Schematic illustrating the various applications where the wafer-scale low-temperature graphene growth developed by UCSB NRL can be utilized. b) Schematic showing the prospects of monolithic 3D integration using 2D materials, where each tier consists of an active layer, a BEOL layer and an ILD. At the first level, 2D field-effect transistors (FETs) are connected via graphene (Gr) and DMLG interconnects and inter-tier metal vias are used for establishing connection between the two tiers. The second tier consists of the recently demonstrated 0.5T-0.5R RRAM cells, which are connected by DMLG interconnects. The top tier consists of doped MLG inductors, which are connected to both the bottom tiers 1 and 2 using monolithic inter-tier vias.

Apart from conventional transistor and interconnect scaling, the massive computing requirements for future generations necessitate the need for alternative architectures. One such approach is 3D integration, or the sequential stacking of chips—including front-end-of-line (FEOL) and BEOL materials, devices, and interconnects in the vertical direction, which can not only reduce the interconnect delay, but also improve the bandwidth and energy-efficiency of the entire chip. Various approaches such as through-silicon via (TSV), flip-chip or wire bonding, have been used for interconnecting multiple levels in a 3D-IC for a long time. However, their large parasitic capacitances and severe electrical, thermal, mechanical reliability, and adhesion challenges, as well as increasing costs and complexity with each generation, severely restrict their use for future technology nodes. Monolithic-3D (M3D) integration is another type of 3D integration scheme, where multiple stacked tiers are fabricated sequentially on the same wafer via deposition/recrystallization of the upper tiers (**Figure 10b**).

Theoretical studies have demonstrated that graphene-based interconnects, inductors, and shielding layers in conjunction with 2D semiconductor material-based transistors can improve the integration density by more than 10-fold when compared to TSV-based 3D integration density, and by more than 1.5-fold when compared to conventional monolithic 3D integration [19]. Additionally, the integration of logic and memory levels (**Figure 10b**) using M3D integration can alleviate the memory wall problem for today's computing architecture, paving the way for high-speed data transfer and computation. Consider, for example, the recently demonstrated 0.5T0.5R ultra-compact hybrid memory cell that reduces the device count by half for the very first time in resistive random-access memory (RRAM) technology history. It also simultaneously allows for higher lateral and vertical (3D) integration density with respect to the conventional 1T1R architecture, and can be monolithically 3D-stacked to build the ultimate high-density nonvolatile memory arrays and neuromorphic/in-memory computing systems, with significantly higher vertical density than the conventional 1T1R architecture (with RRAM on top of the transistor). These attributes enable unprecedented performance and energy-efficiency to emulate the workings of the human brain in the near future [20]. Therefore, effective methods for the seamless integration of graphene/MLG, and/or other 2D materials with mainstream CMOS could lead to revolutionary new devices, circuits, and beyond-Moore architectures to fuel next-generation electronics.

Summary

BEOL passive devices including metal interconnects and inductors are facing fundamental scaling limitations that threaten to derail Moore's Law. Pioneering inventions led by Professor Kaustav Banerjee at UC Santa Barbara have revealed that judiciously engineered

graphene, and synthesized in a CMOS-compatible manner, can not only help overcome such major bottlenecks in CMOS technologies, but also bring unprecedented energy-efficiency and performance gain in next-generation IC products. Thereby, these inventions have established a revolutionary new BEOL technology platform for future ICs and paved the way for graphene's entry into mainstream electronics.

Acknowledgement

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References

1. K. Banerjee, A. Mehrotra, "Global (interconnect) warming," IEEE Circuits and Devices Magazine, vol. 17, no. 5, pp. 16-32, 2001.
2. C.-K. Hu, J. Kelly, H. Huang, K. Motoyama, H. Shobha, Y. Ostrovski, et al., "Future on-chip interconnect metallization and electromigration," IEEE Inter. Reliability Physics Symp., pp. 4F.1.1-4F.1.4, 2018.
3. C. K. Hu, E. G. Liniger, L. M. Gignac, G. Bonilla, D. Edelstein, "Materials and scaling effects on on-chip interconnect reliability," MRS Online Proc. Lib., vol. 1559, 2013.
4. K. S. Novoselov, A. K. Geim, S. V. Morozov, D. A. Jiang, Y. Zhang, S. V. Dubonos, et al., "Electric field effect in atomically thin carbon films," Science, vol. 306, no. 5696, pp. 78-83, 2004.
5. M. Y. Han, B. Ozyilmaz, Y. Zhang, P. Kim, "Energy band-gap engineering of graphene nanoribbons," Physical Review Letters, vol. 98, no. 20, pp. 206805, 2007.
6. C. Xu, H. Li, K. Banerjee, "Modeling, analysis, and design of graphene nano-ribbon interconnects," IEEE Trans. on Electron Devices, vol. 56, no. 8, pp. 1567-1578, 2009.
7. J. Jiang, J. Kang, W. Cao, X. Xie, H. Zhang, J. H. Chu, et al., "Intercalation doped multilayer-graphene-nanoribbons for next-generation interconnects," Nano Letters, vol. 17, no. 3, pp. 1482-1488, 2017.
8. J. Jiang, J. H. Chu, K. Banerjee, "CMOS-compatible doped-multilayer-graphene interconnects for next-generation VLSI," IEEE Inter. Electron Devices Meeting, pp. 34.5.1-34.5.4, 2018.
9. J. Kang, Y. Matsumoto, X. Li, J. Jiang, X. Xie, K. Kawamoto, et al., "On-chip intercalated-graphene inductors for next-generation radio frequency electronics," Nature Electronics, vol. 1, no. 1, pp. 46, 2018.
10. K. Agashiwala, J. Jiang, K. Parto. D. Zhang, C. H. Yeh, K. Banerjee, "Demonstration of CMOS-compatible multi-level graphene interconnects with metal vias," IEEE Trans. on Electron Devices, vol. 68, no. 4, pp. 2083-2091, 2021.
11. S. Thomas, "CMOS-compatible graphene," Nature Electronics, vol. 1, no. 12, pp. 612, 2018.
12. K. Banerjee, A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," IEEE Trans. on Electron Devices, vol. 49, no. 11, pp. 2001-2007, 2002.
13. C. Xu, H. Li, K. Banerjee, "Graphene nano-ribbon (GNR) interconnects: A genuine contender or a delusive dream?," IEEE Inter. Electron Devices Meeting, pp. 8.5.1-8.5.4, 2008.
14. H. Li, C. Russ, W. Liu, D. Johnsson, H. Gossner, K. Banerjee, "On the electrostatic-discharge robustness of graphene," IEEE Trans. on Electron Devices, vol. 61, no. 6, pp. 1920-1928, 2014.
15. R. Chau, "Process and packaging innovations for Moore's law continuation and beyond," IEEE Inter. Electron Devices Meeting, pp. 1.1.1-1.1.6, 2019.
16. E. Siegel, "The last barrier to ultra-miniaturized electronics is broken, thanks to a new type of inductor," 2018. [Online]. Available: https://www.forbes.com/sites/startswithabang/2018/03/08/breakthrough-in-miniaturized-inductors-to-revolutionize-electronics/?sh=84ecbd4779ec
17. K. Agashiwala, A. Pal, W. Cao, J. Jiang, K. Banerjee, "Can kinetic inductance in low-dimensional materials enable a new generation of RF electronics?," IEEE Inter. Electron Devices Meeting, pp. 24.4.1-24.4.4, San Francisco, 2018.
18. W. Liu, J. Kang, K. Banerjee, "Characterization of $FeCl_3$ intercalation doped CVD few-layer graphene," IEEE Electron Device Letters, vol. 37, no. 9, pp. 1246-1249, 2016.
19. J. Jiang, K. Parto, W. Cao, K. Banerjee, "Ultimate monolithic-3D integration with 2D materials: Rationale, prospects, and challenges," IEEE Jour. of Electron Devices Soc., vol. 7, pp. 878-887, 2019.
20. D. Zhang, C. H. Yeh, W. Cao, K. Banerjee, "0.5T0.5R- An ultracompact RRAM cell uniquely enabled by van der Waals heterostructures," IEEE Trans. on Electron Devices, vol. 68, no. 4, pp. 2033-2040, 2021.

Biographies

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LEENO

Coaxial Probe for 100GHz

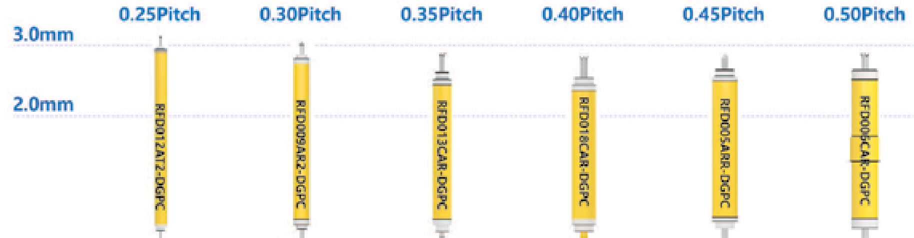
Specification

Frequency : 80GHz(BGA),
100GHz(QFN, LGA)

Pitch : 0.25mm ~

Crosstalk : -60dB

Impedance : 50Ω±10%



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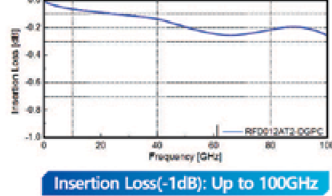
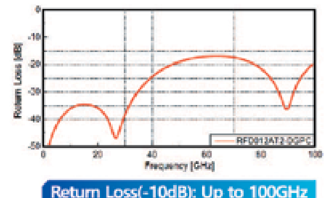
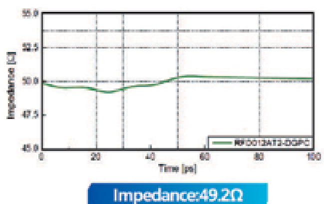


Insertion Loss(-1dB): Up to 100GHz

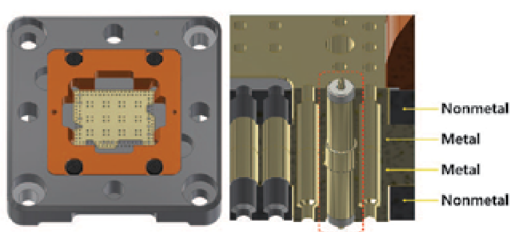


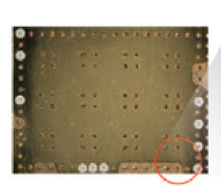
Return Loss(-10dB): Up to 100GHz

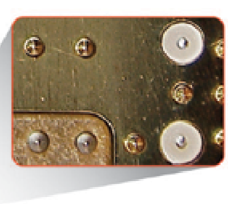


Impedance:49.2Ω

Coaxial Probe Socket Structure







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Introducing hybrid graphene/metal structures in the BEOL technology roadmap

By Swati Achra, Inge Asselberghs, Zsolt Tokei [imec]

Advanced scaling in the front-end-of-line (FEOL) needs to go hand in hand with innovations in the back-end-of-line (BEOL)—the network of interconnects that connects seamlessly to the underlying device structures. This BEOL is organized in different metal layers (local, intermediate, semi-global and global) that are vertically-interconnected by means of via structures – filled with metals. Today, Cu-based dual-damascene is the workhorse process flow for making the interconnects. But with each new technology generation, routing congestion and a dramatic signal delay (resulting from an increased resistance-capacitance (RC) product) become more and more problematic, forcing chipmakers to consider new integration schemes and materials for fabricating the interconnects. Imec, for example, foresees the introduction of alternative integration schemes such as hybrid via metallization, a semi-damascene process and hybrid height with zero vias for the nodes to come. These innovations promise to address the challenges that come along with metal pitches moving towards 21nm and beyond.

In parallel, alternative conductors with better figures of merit are being investigated to be used in combination with these advanced process schemes. The figure of merit is defined as the product of the bulk resistivity and the mean free path of the carriers in the metal. Of interest are cobalt (Co), ruthenium (Ru), tungsten (W) and ordered binary intermetallic compounds such as AlNi or RuV_3 (**Figure 1**) [1]. Researchers also look intensely at graphene, which, thanks to its remarkable properties, is making its way into many interesting fields of application such as (bio)sensing, energy storage, photovoltaics, optoelectronics and complementary metal-oxide semiconductor (CMOS) scaling.

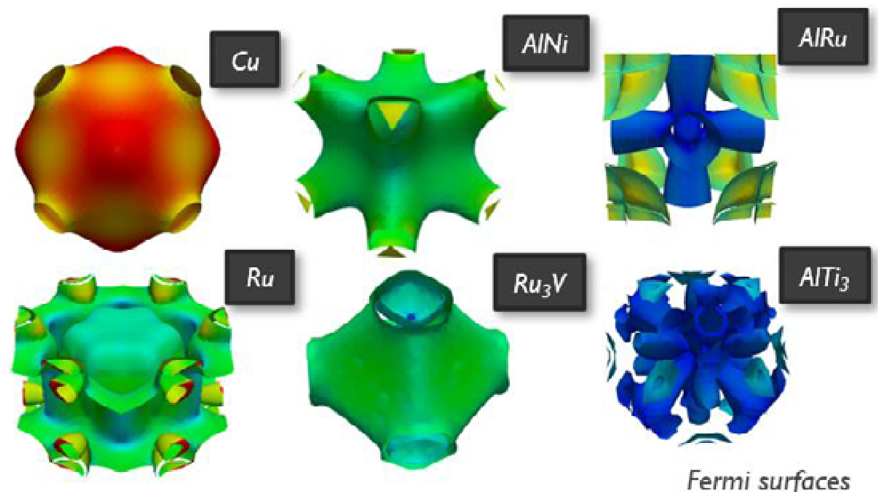

Figure 1: A grasp of new alloys screened for future interconnects [1].

The promise of graphene for interconnect applications

Interest in graphene for interconnect applications comes as no surprise. Graphene exhibits a high intrinsic carrier mobility (up to 200,000$cm^2V^{-1}s^{-1}$) and a large current-carrying capacity (up to 108A/cm^2) (**Figure 2**). In addition, graphene has a high thermal conductivity and competitive robustness against electromigration. It can also be made atomically thin, which helps alleviate the thickness contribution to the RC delay. Because of these exceptional properties,

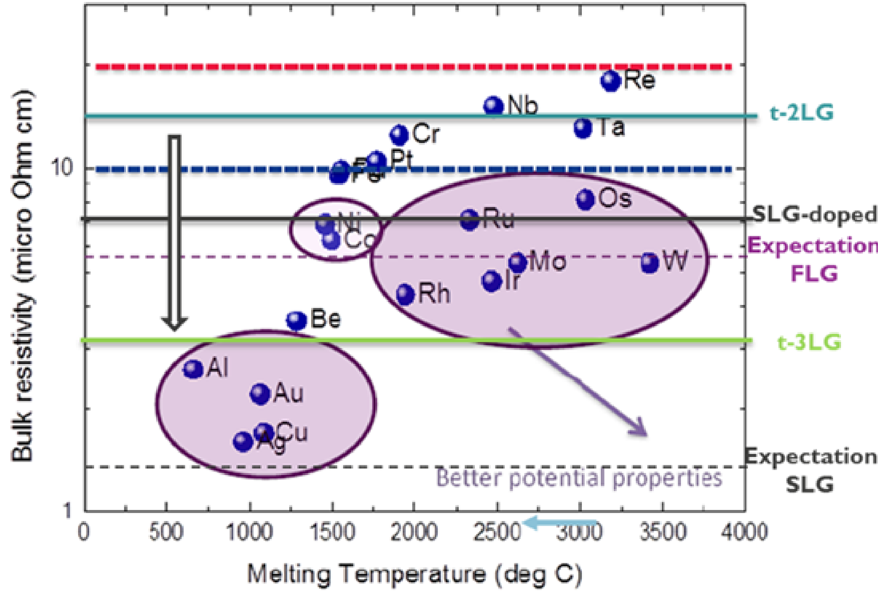

Figure 2: Comparing properties of graphene (single-layer and few-layer) with other interconnect materials of interest.

it has potential to fulfill diverse roles in interconnect applications. The material has, for example, been considered as an oxidation barrier and as an ultrathin diffusion barrier for metals. Researchers have also investigated the feasibility of using multilayer graphene wires or nanoribbons as an alternative conductor.

Graphene, however, comes with one major drawback: intrinsically, it does not hold enough charge carriers to be useful as a local interconnect. The lack of charge carriers severely reduces its electrical conductivity—a key metric for interconnect performance that is proportional to both the mobility and the carrier concentration. For this reason, several layers of graphene will be needed to cross-over Cu for example, for (local) interconnect applications – as confirmed by modeling. The number of layers will be a trade-off between the material's overall contribution to resistance and capacitance.

Fortunately, there are ways to further modulate graphene's conductivity. This has driven the research of so-called graphene nanoribbons – graphene layers patterned into narrow strips. The specific angular orientation of the graphene layers with respect to their underlying layer provides another knob for improvement.

Finally, the conductivity of graphene can be boosted by doping, thereby providing graphene with extra electrons or holes to carry the current. Doping can be performed in several ways, for example by metal-induced doping—enabled by bringing graphene in direct contact with metals like Cu or Ru. These hybrid metal/graphene schemes bring together the best of both worlds: the high carrier concentration of the metal and the high mobility of graphene.

Exploring hybrid graphene/metal interconnects

Below, we discuss the feasibility of using hybrid metal/graphene structures for sub-2nm interconnect applications. Two different structures are being examined: graphene-capped metal and metal-capped graphene devices.

Graphene-capped ruthenium. Of interest for interconnect applications is the metal-induced doping of graphene that is expected to happen at the interface with Ru. To understand and be able to control the doping, the charge transfer at the Ru/graphene interface was systematically investigated. Interfaces were formed after transferring a multilayer graphene film (grown by chemical vapor deposition (CVD)) onto a thin Ru film (typically 5nm-thick) that was grown by physical vapor deposition (PVD) (Figure 3). After transfer, graphene was found to adhere well to the large area PVD Ru film.

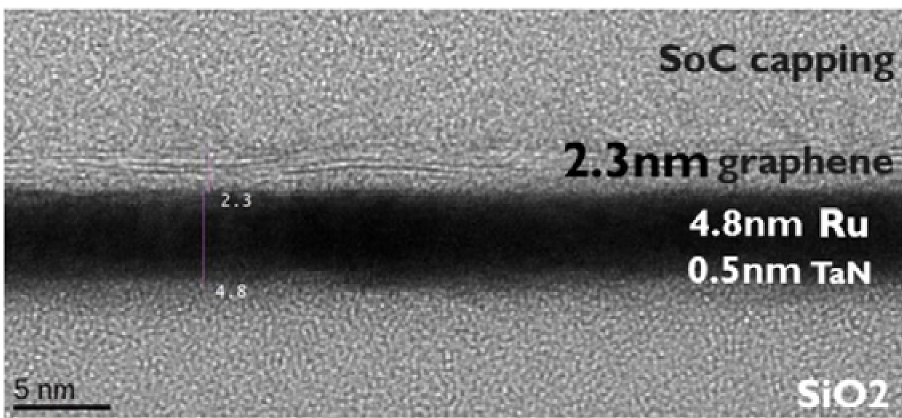

Figure 3: Transmission electron microscope (TEM) image of a graphene-capped Ru structure.

The two main observations can be summarized as follows. First, the researchers found that the average resistivity of Ru dropped by more than 15% after encapsulation with graphene, accompanied by a significant decrease in contact resistance (Figure 4). Second, internal photoemission spectroscopy experiments indicate a downward shift of graphene's Fermi level into the valence band by ~0.5eV compared to intrinsic graphene, corresponding to a hole concentration of 1.9E13cm^{-2}. This observation is an indication of metal-induced doping that happens at the interface, causing graphene to become p-doped when added as a capping layer on Ru [2-4].

Furthermore, the Ru lines were observed to be less sensitive to temperature fluctuations when encapsulated with graphene. This could be due to the high thermal conductivity of graphene, providing an alternative/additional path for efficient heat

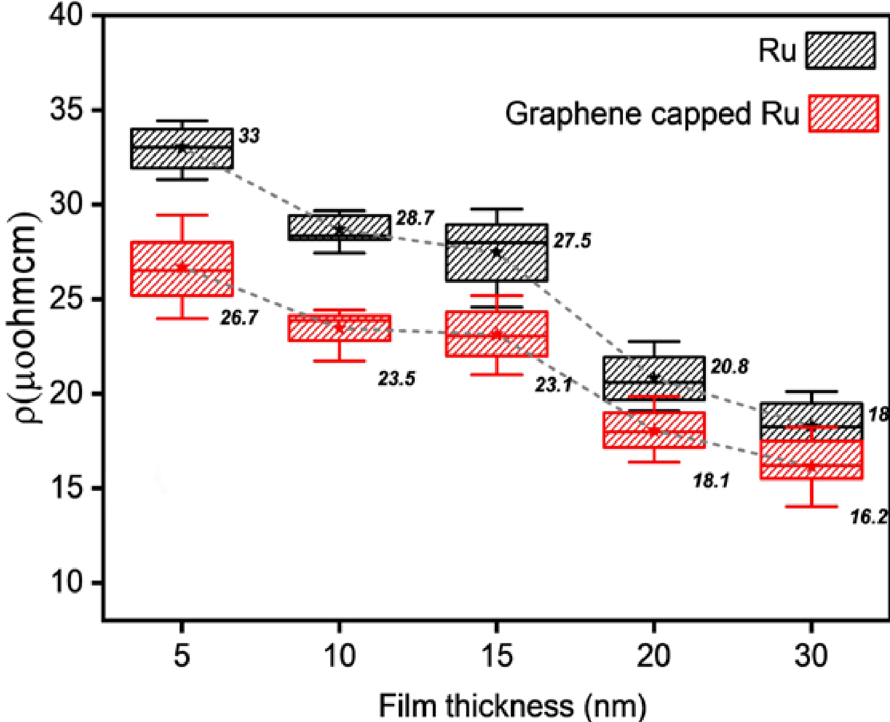

Figure 4: Experimentally measured hybrid film resistivity of bare Ru (black) and graphene-capped Ru (red) devices for different thicknesses of Ru thin-film [4].`

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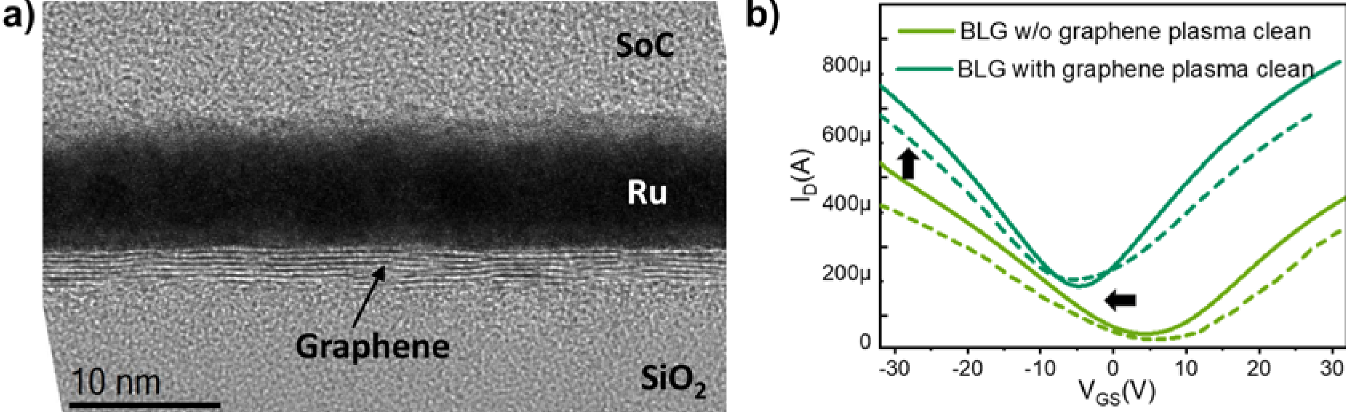

Figure 5: a) (left) TEM image of Ru-capped plasma-cleaned few-layer graphene; b) (right) Transfer characteristics curves of bilayer (BLG) devices showing the change in the on-current and shift in charge-neutrality point (CNP) for as-transferred and plasma-treated graphene after the "graphene plasma clean" step. The solid and dashed lines represent the upper and lower bounds of the transfer curves, respectively, obtained from 63 devices.

dissipation. This observation is of interest for future interconnect applications, as the self-heating in highly-scaled IC wires and an insufficient heat dissipation to the surrounding dielectric can degrade the interconnect's thermal reliability.

Overall, the researchers conclude that these graphene-capped metal/hybrid structures provide an answer to the RC delay problem for future interconnects. Imec envisions their introduction in the BEOL technology roadmap for the 1nm node and beyond. Yet, more fundamental insights are needed to determine the exact conduction mechanism taking place within the capped structure. Either Ru remains the main conductor, with graphene helping to reduce its resistivity by suppressing scattering mechanism(s) in the metal. Or, the two conductors now act in parallel, with a higher conductivity for graphene (with respect to intrinsic graphene) because of the charge transfer. Modeling work is currently ongoing to get a better understanding.

Ruthenium-capped graphene. In the longer term, researchers at imec are looking into stacking alternating layers of graphene and metal to further boost the electrical conductivity. In such a metal/graphene/metal/etc. sandwich-like structure, a second and different interface will now play an equally important role: the interface that results from depositing a layer of metal on top of graphene. Just like in the above study, the nature of the graphene/metal interaction at the interface can modify the physical properties of graphene. And its electronic band structure can also be significantly altered by the charge distribution at the interface.

Engineering the graphene/metal interface is, however, one of the most challenging bottlenecks. The (as-transferred) graphene layer typically contains many randomly-oriented grains where the grain boundaries act as line defects and nucleation centers for metal deposition on top surface. This makes it challenging for depositing a metal uniformly covering the entire basal plane of graphene by means of traditional deposition method such as PVD or atomic layer deposition (ALD). Moreover, after transfer, the graphene surface suffers from contamination—calling for a suitable cleaning method that does not damage the graphene layer.

In a laboratory study, the imec researchers performed a hydrogen plasma cleaning of the graphene surface (by using an Ar/H_2 downstream plasma), and subsequently deposited the metal (i.e., Ru) by using electron beam evaporation (Figure 5a). It was then investigated how these processes affected the electrical conductivity of the graphene/Ru stack. They found that after exposure to hydrogen plasma, graphene experiences n-doping and a rise in charge carrier concentration. Unfortunately, single-layer graphene also suffers from plasma-induced defectivity. Thicker graphene films are observed to be less affected. Under these conditions, an overall improvement of 18% in electrical conductivity of Ru-capped (plasma treated) graphene devices could be observed (Figure 5b). These first results are encouraging, and further improvements can be expected by tuning the hydrogen plasma chemistry and conditions, and by increasing the number of alternating layers [5].

Towards industrial adoption

These results demonstrate the performance potential of hybrid metal/graphene schemes in advanced interconnects. Yet, several integration challenges remain to be solved before these interconnect schemes can be adopted in a 300mm fab. For example, while this study focuses on graphene transfer, a more elegant way of depositing graphene would be direct growth on the metal template of interest. Growing high-quality graphene requires, however, high-growth temperatures (900-1000°C) and, as such, cannot be applied on interconnect-type of metals. Deposition at lower temperatures has been demonstrated, but comes at the expense of defectivity and reduced quality of graphene.

An alternative route that was applied in this study includes the transfer of high-quality graphene that was previously grown on platinum foils by using CVD. This transfer route provides an interesting approach when the thermal budget is restricted. At imec, delamination and subsequent transfer of high-quality graphene on 300mm wafers has been demonstrated, but might be challenged by the topography of the underlying metal layer. This process also comes with a significant addition of process steps and calls for improved uniformity and process control. In addition, further research will be needed to optimally control the defectivity and specific orientation of the graphene layers. Studies at imec are ongoing to solve these integration issues and to turn the hybrid graphene/metal schemes into true industry-grade options.

Summary

The feasibility of using hybrid metal/graphene structures for sub-2nm interconnect applications was discussed. Two different structures were examined: graphene-capped metal and metal-capped graphene devices. In both cases, the interfaces between graphene and metal play a crucial role in the overall electrical behavior of the hybrid interconnect. While graphene-capped metal interconnects are the most mature, stacks of alternating layers may come into play in the longer term. It should finally be noted that the above study focused on Ru as a metal of interest, a material that has recently emerged as a potential alternative for Cu metallization. But the concepts presented here are expected to be expandable towards other "interconnect" metals.

References

1. C. Adelmann, et al., "Alternative metals: from ab initio screening to calibrated narrow line models," Proc. IEEE IITC 2018, pp.: 154-156
2. S. Achra, et al., "Graphene-ruthenium hybrid interconnects," Proc. IEEE IITC 2019; To be published.
3. S. Achra, et al., "Characterization of interface interactions between graphene and ruthenium," Proc. IEEE IITC 2020, pp.: 133-135
4. S. Achra, et al., "Metal induced charge transfer doping in graphene-ruthenium hybrid interconnects," Carbon 183 (2021) 999-1011.
5. S. Achra, et al, "Enhancing interface doping in graphene-metal hybrid devices using H2 plasma clean," Applied Surface Science 538 (2021) 148046.

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Large-field, fine-resolution lithography enables next-generation panel-level packaging

By John Chang [Onto Innovation]

Rapidly growing demand for new types of functionality across an expanding range of applications, including 5G communication, smartphones, data centers, servers, high-performance computing (HPC), artificial intelligence (AI) and the Internet of Things (IoT), is driving a fundamental shift in the way electronic devices are designed and manufactured. Gone are the days when advances were defined by an increasing number of shrinking transistors with ever-faster switching times and lower power consumption, all fabricated as a single, monolithic integrated circuit (IC). Many of today's most advanced systems integrate multiple die, each optimized for a specific capability and fabricated with a process designed specifically for that type of circuit. These disparate chips are then connected using advanced packaging (AP) technologies, a process known as heterogeneous integration (HI) (**Figure 1**).

One example of HI uses advanced IC substrates (AICS) in a process known as ultra-high density (UHD) panel fan-out. This fan-out panel-level process (FOPLP) is a redistribution lines (RDL)-first approach, where many layers of patterned conductive and insulating material are processed on both sides of a large panel to route electrical signals between the integrated chips, which are added last. Once the RDL layers are complete, solder bumps are added to form connection points that will mate with matching connection pads on the component ICs. Package substrate sizes are expected to reach 150mm x 150mm in the next few years. Panels, which may be 500mm x 500mm or larger, can accommodate many more packages per panel than the substrates used in wafer-level processes, which are restricted to round, wafer-like substrates of 300mm or less in diameter (**Figure 2**).

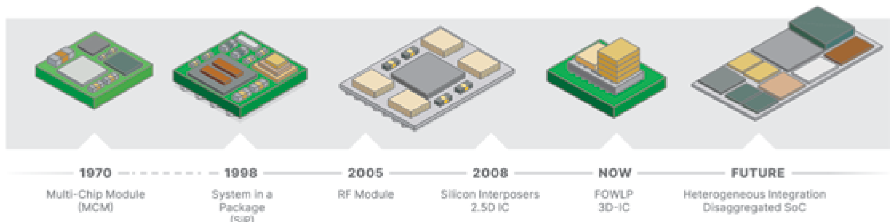

Figure 1: Heterogeneous integration enables next-generation device performance gains by combining multiple silicon nodes and designs inside one package. The package size is expected to grow significantly. SOURCE: Cadence

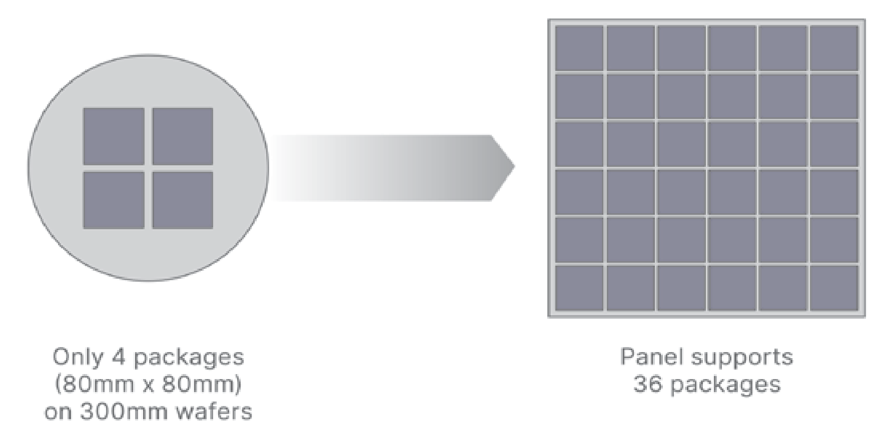

Figure 2: The number of 80mm x 80mm packages that fit on a 300mm wafer compared with the number of 80mm x 80mm packages that fit on a 515mm x 510mm panel.

The lithography challenge for large heterogeneous integration is the limited size of the exposure field (typically 60mm x 60mm or less) for most currently available lithography systems. Smaller-field systems can be used to pattern large substrates by stitching together multiple exposures, but this affects both productivity and yield because of the need for multiple exposures of multiple reticles and the risk of errors at the stitching boundaries. A large exposure field would eliminate these impediments. However, there are also challenges associated with a large exposure field. These include panel warpage and distortion, which can impact critical dimensions, uniformity and overlay.

We describe here the use of our large-field lithography system (JetStep® X500) to expose 250mm x 250mm substrates in a single shot on 515mm x 510mm panels. Our evaluation included: 1) critical dimension (CD) control for 3µm, 5µm and 6µm lines/spaces, and 15µm and 20µm vias; 2) CD uniformity across the exposure field; and 3) overlay accuracy. We used copper clad laminate (CCL) and Anjinomoto build-up film (ABF) panels for resolution, and glass panels with liquid resist for overlay and uniformity. The large field eliminates stitching, allows the exposure of more large package substrates in a single shot and requires fewer shots to complete a panel. **Figure 3** compares the exposure layout for a large field (250mm x 250mm)

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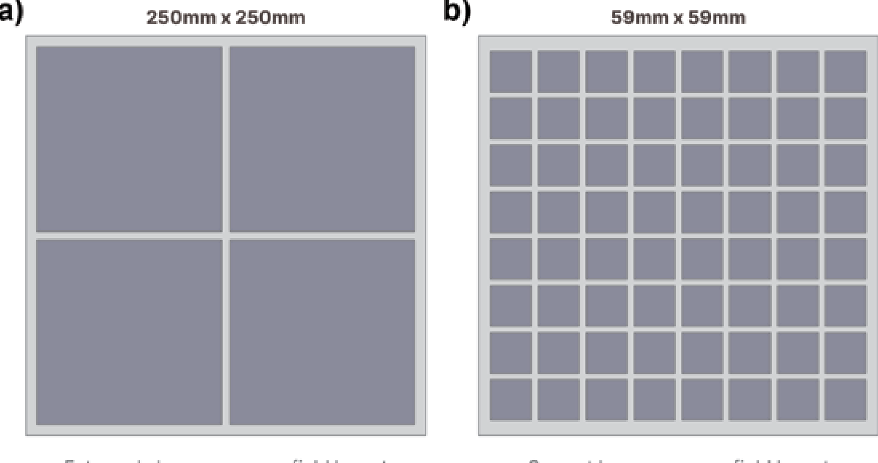


Figure 3: a) (left) The exposure layout for a 515mm x 510mm panel using a large exposure field (250mm x 250mm) compared with b) (right) the exposure layout of a smaller field (59mm x 59mm).

and a smaller field (59mm x 59mm) on a 510mm x 515mm panel. With the large exposure field, the panel can be completely exposed with just four shots, while the smaller field requires 64 shots.

Lithography system

The increased topological variation expected for larger panels, physical distortion during the RDL build-up process and the greater feature heights typical of RDL all contribute to the requirement for more depth of focus (DOF) in the pattern projecting optics. In any optical system, DOF and resolution are inversely related, i.e., gains in resolution require sacrifices in DOF and vice versa. Resolution and DOF are related through the system's numerical aperture, as shown in **Equation 1** and **Equation 2**. With feature sizes in the micrometer range, the resolution requirements for advanced packaging and advanced IC substrates are less demanding than requirements for front-end lithography, where feature sizes are 1,000 times smaller. At the same time, the use of thicker resist films and larger variations in substrate topography require greater DOF. The projection optics of the lithography system used in this demonstration were designed with a lower numerical aperture to meet both the resolution and DOF requirements of the application.

$$R = k1\lambda / N.A. \quad \textbf{Eq. 1}$$

$$DOF = k2\lambda / N.A.^2 \quad \textbf{Eq. 2}$$

Where k1 and k2 are process factors, and λ is wavelength.

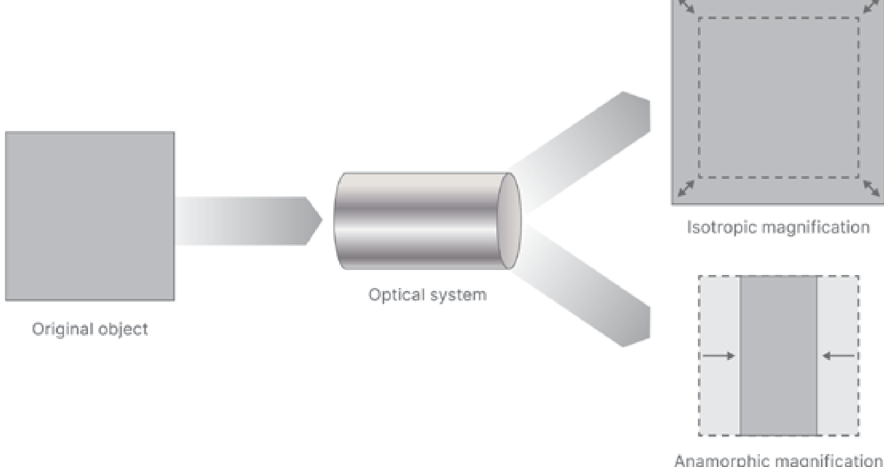


Figure 4: Isotropic magnification and anamorphic magnification compensation.

The system's 2.2x magnification projection lens enables up to a 250mm x 250mm exposure field size, with 3µm line/space resolution, ±400ppm magnification compensation and ±100ppm anamorphic magnification compensation, with overlay accuracy better than 1µm.

Low lens distortion and accurate step and settle movement are also key to meeting the overlay and uniformity requirements. Distortion in this system is less than 1µm across the 250mm exposure field. The system's stage is driven by 8 motors to ensure accurate step and settle behavior, even when loaded with the weight of the large panel.

During the FOPLP substrate build process, many layers of RDL and ABF are added to the panel. These films distort the panel in the X axis, Y axis and Z axis during thermal cycling. Magnification compensation allows the system to accommodate these changes in the substrate. Two kinds of compensation are needed. Isotropic magnification shrinks or enlarges the pattern equally in all directions. Anamorphic magnification enlarges or shrinks the patterns anisotropically to correct for distorted panel registration errors. Both adjustments are necessary to achieve good overlay and maintain high package yields. **Figure 4** shows the difference between isotropic magnification and anamorphic magnification.

Resolution

The large-field lithography system was evaluated for CD control of lines/spaces and vias, CD uniformity, and overlay.

3µm lines. Figure 5 shows the results of the 3µm line/space resolution evaluation. A CCL/ABF substrate with a 10µm-thick dry film resist was selected for this demonstration, resulting in lines with just over a 1:3 aspect ratio. Best dose and best focus were determined using a focus exposure matrix (FEM). Best dose was used for the resolution demonstration. The figure indicates that CDs showed less than 10% deviation from -10µm to -70µm, at a DOF of 60µm. The data from the FEM were used to generate a Bossung plot (**Figure 5a**) in which the X-axis is focus (µm) and the Y-axis is CD (µm). The plot shows the 60µm DOF. **Figure 5b** also includes a lower magnification

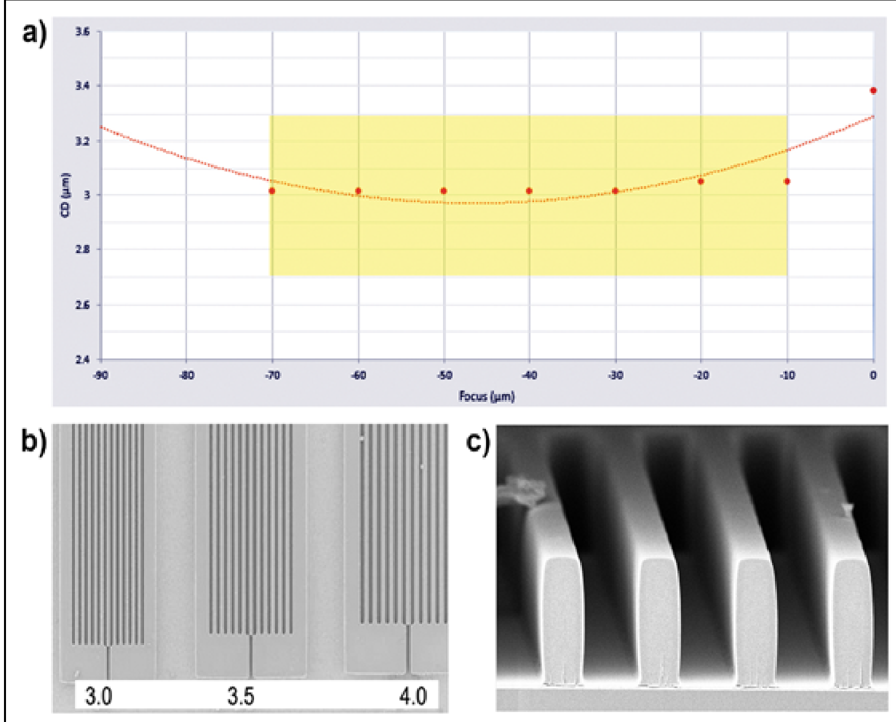


Figure 5: a) Bossung plot generated from FEM data showing less than 10% deviation over 60µm DOF; b) Lower resolution image of 3µm, 3.5µm and 4µm isolated and dense area line/space arrays; c) Cross-section image of 3µm lines in 10µm thick dry film resist on copper substrate; the line critical dimension is 3.181µm, and the resist height is 9.873µm in the cross-sectional image.

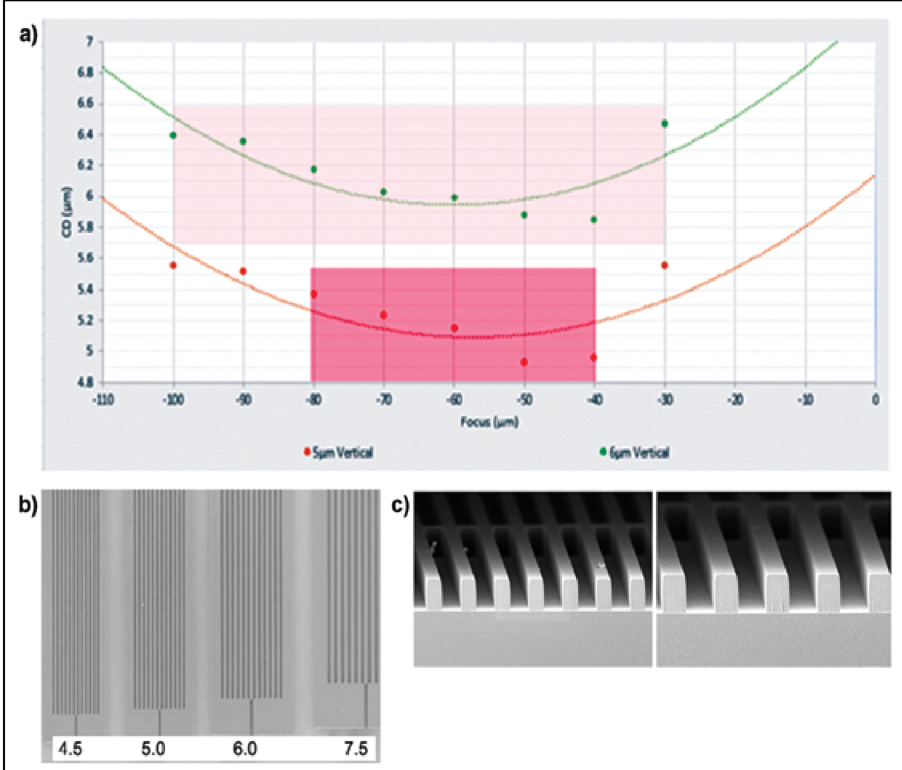


Figure 6: a) Bossung plot generated from FEM data showing less than 10% deviation over 40µm DOF for 5µm lines and 70µm DOF for 6µm lines. b) Lower resolution image of 4.5µm, 5µm, 6µm and 7.5µm isolated and dense area line/space arrays. c) Higher resolution cross-sectional images of 5µm and 6µm lines in a 10µm-thick dry resist on copper substrate.

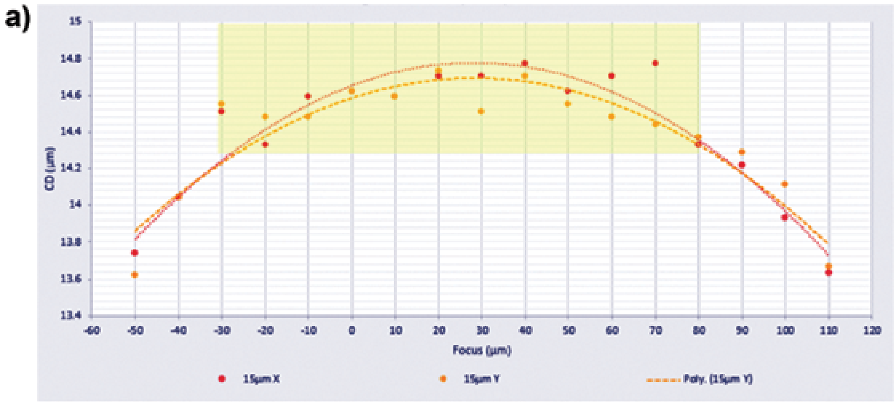
image of 3µm, 3.5µm and 4µm isolated and dense line/space arrays. A higher resolution cross-sectional image of 3µm lines (Figure 5c) shows dimensions for the middle line: 3.181µm line width and 9.873µm line height (resist thickness).

5µm and 6µm lines. Larger feature sizes were also investigated. A CCL/ABF substrate with a 25µm-thick dry film resist was selected for this demonstration, resulting in lines with an aspect ratio of about 1:5. Best dose and best focus were determined using FEM. Best dose was used for the resolution demonstration. The 5µm line CDs showed less than 10% deviation from -40µm to -80µm, and a DOF of 40µm. The 6µm line CDs showed less than 10% deviation from -30µm to -100µm, and a DOF of 70m. The data from the FEMs were used to generate Bossung plots (Figure 6a). The plots show a 40µm DOF for 5µm lines and a 70µm DOF for 6µm lines. Figure 6b also includes a lower magnification image of 4.5µm, 5µm, 6µm and 7.5µm isolated and dense line/space arrays and higher resolution cross-sectional images of 5µm and 6µm lines in a 10µm-thick resist (Figure 6c).

15µm and 20µm square vias. Via resolution was also investigated (Figure 7). Best dose and best focus were determined using a FEM and a CCL/ABF substrate with 40µm-thick dry film resist; best dose was selected for this demonstration. Bossung plots were generated for both via sizes. The 15µm vias showed less than 10% deviation from -30µm to 80µm, and a DOF of 110µm. The 20µm vias showed less than 10% deviation from -40µm to 110µm, and a DOF of 150µm.

Uniformity. We used a 1.4µm-thick liquid resist film on a 510mm x 515mm glass panel and 3µm lines to test uniformity across the panel. The uniformity data in Figure 8 show a maximum CD of 3.258µm, a minimum CD of 2.988µm and an average CD of 3.099µm. Deviation ranges from -0.20% to 4.12% for an overall uniformity of 4.32%. The deviation chart shows no peaking or trending and indicates a stable exposure field.

Overlay. Overlay accuracy is essential. We used a 510mm x 515mm glass panel with a 1.4µm-thick liquid resist as the overlay test vehicle. The exposure field was 250µm x 250µm. Four shots covered the entire panel. The test procedure comprised the deposition and patterning of an initial layer, followed by deposition and patterning of a second, overlying layer. Patterning



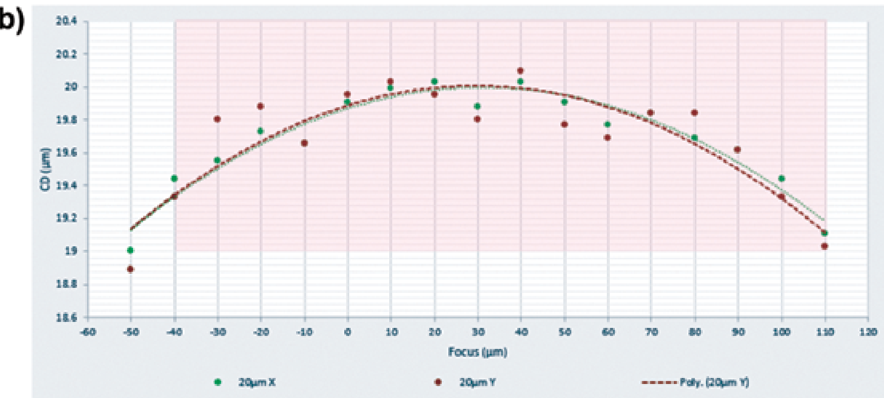


Figure 7: a) Bossung plot for 15µm vias showing 110µm DOF. b) Bossung plot for 20µm vias showing 110µm DOF.

of the second layer included site-by-site correction for each exposure field. Overlay error was checked by reading overlapped verniers (Figure 9) included at certain locations in the patterns. Each exposure field contains 3 x 3 measurement points; and 2 x 2 shots per panel were measured to determine the overlay performance. The mean +3 sigma in X was 0.91µm, and the mean +3 sigma in Y was 0.91µm. The table in Figure 9 summarizes the results of the overlay error measurements.

Summary

In this study, an extremely large exposure field size (250mm x 250mm) successfully resolved 3µm line/space features with a depth of focus >60µm on a 510mm x 515mm CCL/ABF stack with a 10µm-thick dry film resist. This study also demonstrated successful 5µm and 6µm line/space features with a 25µm-thick dry film resist and 15µm and 20µm vias with a 40µm-thick dry film resist. Fine resolution and a large field size provide the user with the opportunity to increase the package size beyond 150mm x 150mm and maintain high throughput. This new capability has the potential to pave the way

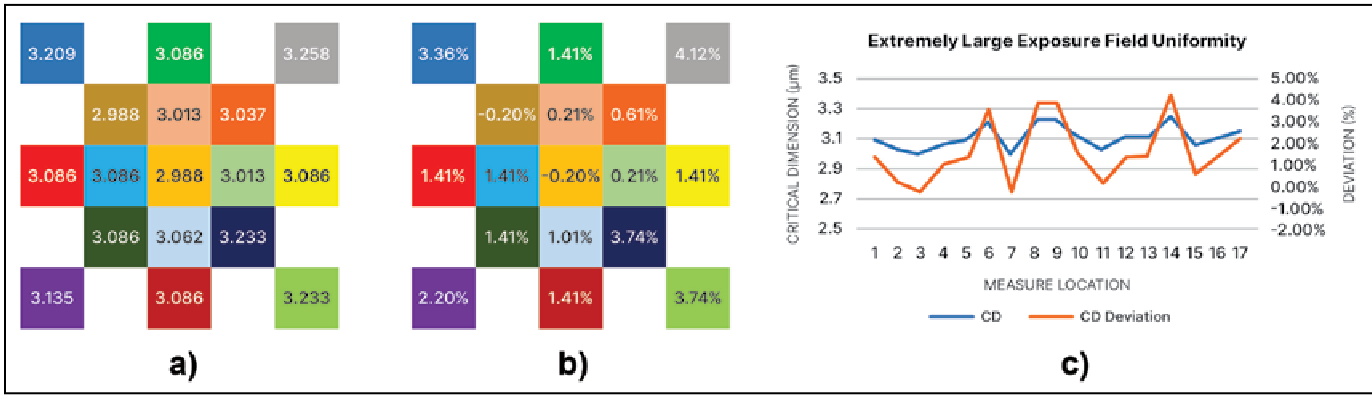
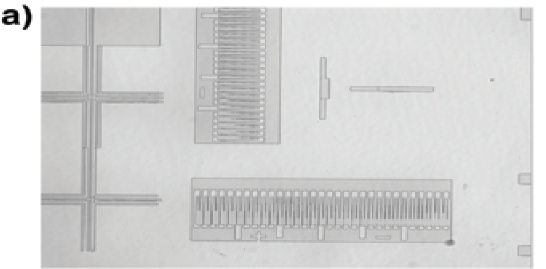


Figure 8: a) 3µm CD plot in 250mm x 250mm exposure field: The maximum CD is 3.258µm, and the minimum CD is 2.988µm; the average CD is 3.099µm, and the uniformity is 4.32%. b) 3µm CD deviation contribution map in 250mm x 250mm exposure field: The center location has a minimum deviation of -0.20% and the deviation trend up to 2.2% to 4.12% at corner locations, the maximum deviation is 4.12%, which is at the top-right corner. Overall, the deviation meets our expectation. c) 3µm CD and CD deviation chart: No trending or peak is observed. This chart indicates the CD performance with a 250mm x 250mm exposure field is stable.

a)



b)

	Dx	Dx
Max	0.52	0.39
Min	-0.32	-0.39
Mean	0.2	0.2
Std	0.24	0.24
Mean + 3σ	0.91	0.91

Figure 9: A summary of the results of overlay measurements: a) Overlapped verniers included in the pattern were used to measure overlay errors. b) The table summarizes the measured errors.

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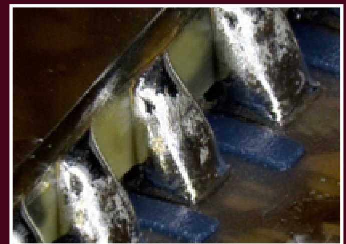
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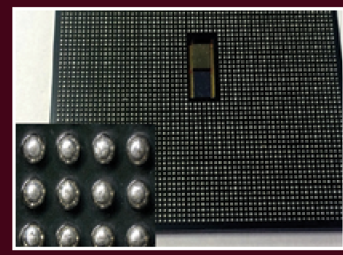
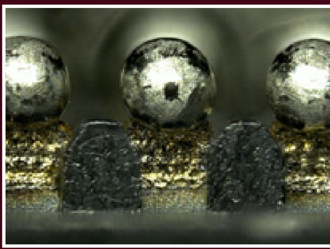

BGA Soldering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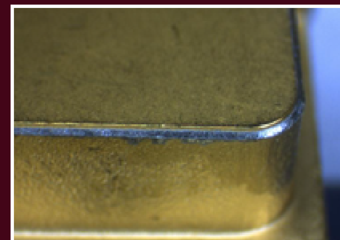
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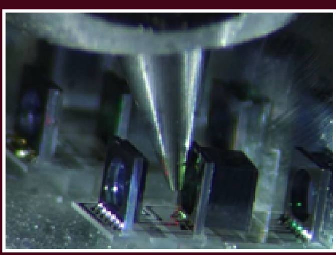
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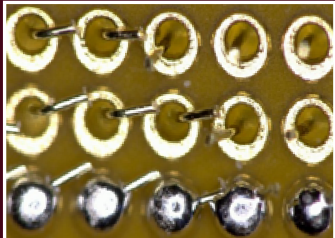
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for the next generation of heterogeneous integration packages and future imaging and process studies.

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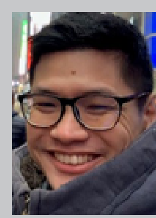
References

1. J. Chang, K. Best, J. Lu, B. Ali, M. Marshall, "Adaptive shot technology to address severe lithography challenges for advanced FOPLP," pp.: 918-923, ECTC, 2020.
2. K. Best, J. Chang, M. Marshall, J. Lu, "FOPLP lithography solutions to overcome die placement error, predict yield, increase throughput and reduce cost," International Wafer-Level Packaging Conf. (IWLPC), 2019.
3. K. Best, M. Marshall, "Advanced packaging metrology and lithography that overcomes FOWLP/FOPLP die placement error," IWLPC, 2018.
4. K. Ruhmer, "Lithography challenges for 2.5D interposer manufacturing," pp.: 523-527, ECTC 2014.
5. R. McCleary, "Panel-Level advanced packaging," ECTC 2016.
6. K. Ruhmer, P. Cochet, R. McCleary, "Panel-based fan-out packaging to reduce costs," SMTA/*Chip Scale Review* IWLPC, Nov. 11-13, 2014.
7. K. Ruhmer, P. Cochet, R. McCleary, N. Chen, "High-resolution patterning technology to enable panel-based advanced packaging," pp.: 129-136, IMAPS 2014, Oct. 13-16, 2014.



Biography

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A coaxial elastomer socket for system-level test

By Dave Oh, BH Kim [TSE]

As the technologies of full-scale 5G, artificial intelligence (AI), self-driving automobiles, augmented reality (AR) and virtual reality (VR) are used in daily life, the required conditions and environments for use are more diverse and accordingly, the components of semiconductors continue to become more complex. As these components become more complex, however, the number of test items also increase. At the same time, product launch periods are getting shorter and shorter, and, it is more important to check the interaction between software and hardware in the actual use environment in order to minimize errors as operational defects occur in new products. Therefore, operation inspection of semiconductors in the ultimate use environment (i.e., at system level) has become an essential process for quality assurance [1]. As a result, the socket used in system-level test (SLT) requires and becomes important with respect to loss-free signal transmission at high frequencies in accordance with the complex components of semiconductors and the fast interaction between software and hardware.

In securing such signal transmission characteristics, crosstalk between the signal and the adjacent signal becomes a problem as the operating frequency increases and the ball pitch gradually decreases.

Crosstalk occurrence increases as the frequency increases and becomes a factor that interferes with the transmission of high-quality signals [2]. One proposal for addressing crosstalk is to use a coaxial spring socket that shields the signal with metal to solve the crosstalk problem. However, a coaxial spring socket has the disadvantages of high transmission loss

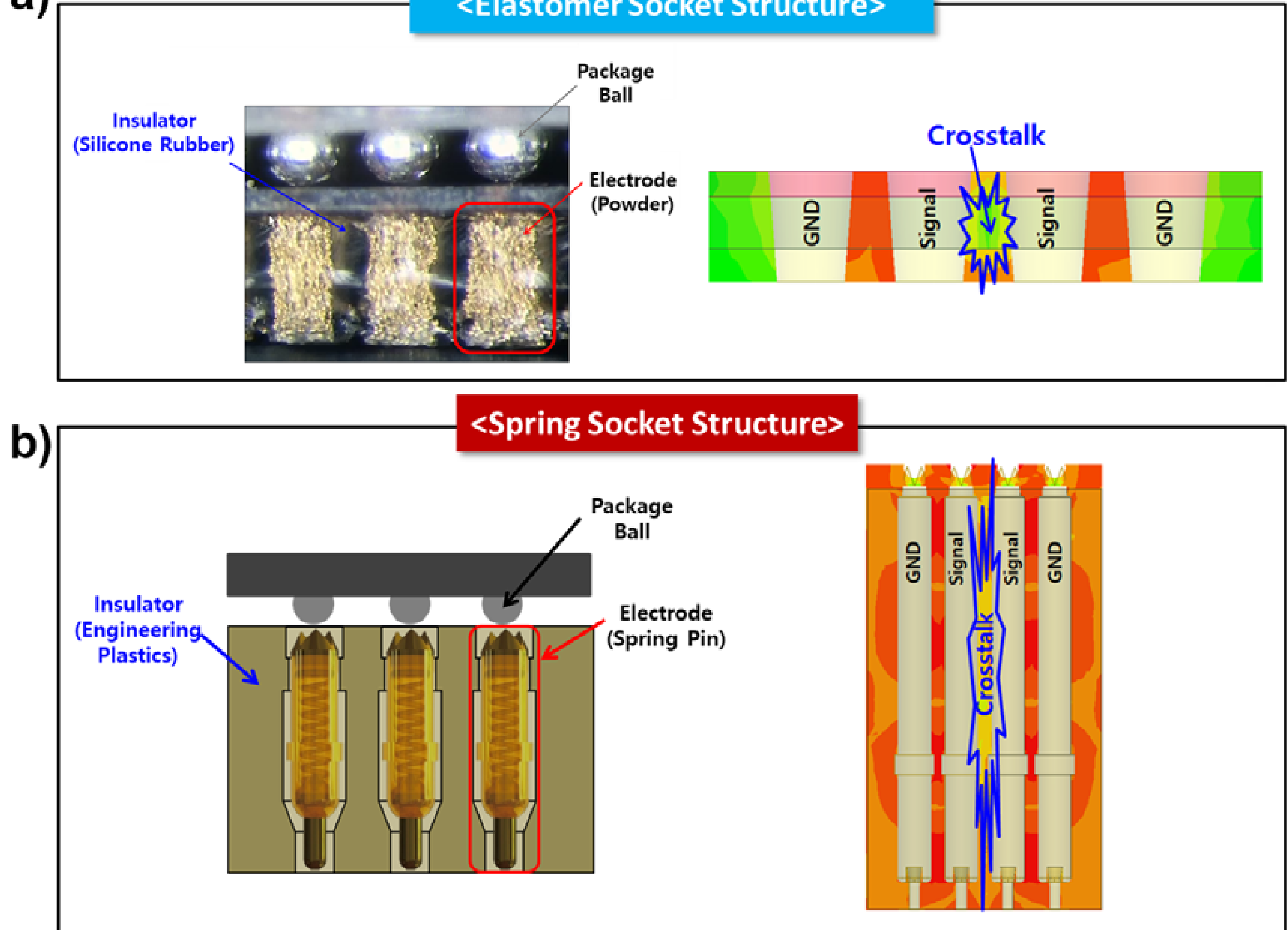

Figure 1: Crosstalk: a) (top) in a silicone rubber test socket; and b) (bottom) in a spring socket structure.

because of its long signal length and its high manufacturing cost [3]. To address these disadvantage, a coaxial elastomer socket based on the elastomer socket is proposed. Such a coaxial elastomer socket solves the crosstalk problem, and has the advantages of a shorter length, lower transmission loss, and a lower manufacturing cost than the spring socket.

Crosstalk in an elastomer socket and a spring socket

When the test socket is used at high frequency, an electromagnetic wave is generated from the signal—this wave affects the adjacent signal line through the insulating part. This effect is called crosstalk, and the smaller the interval between signals and the higher the frequency, the greater the crosstalk effect. In the same position as the package ball, the test socket has a conductive path made of powder with gold plating applied to nickel material. Crosstalk also occurs in silicone rubber (Figure 1a), which is an insulator in the elastomer socket. Crosstalk occurs in an insulator housing made of ULTEM™ and PEEK material comprising the spring socket (Figure 1b). It has a conductive path composed of BeCu or Pd alloy material with a gold-plated barrel and a spring that acts as an elastic body.

Spring socket with metal housing to prevent crosstalk

In the case of the spring socket, a coaxial spring socket with an insulating housing applied to a metal housing is proposed as a way to prevent crosstalk. The coaxial spring socket with an insulating housing applied to a metal housing prevents signal interference of the electromagnetic wave generated from the signal to the adjacent signal as the metal housing acts as an electromagnetic shielding. If, however, the housing is made of metal but does not have an insulating housing, a short circuit occurs. As shown in Figure 2, when the outside of the signal is composed of an insulator, a short circuit is prevented.

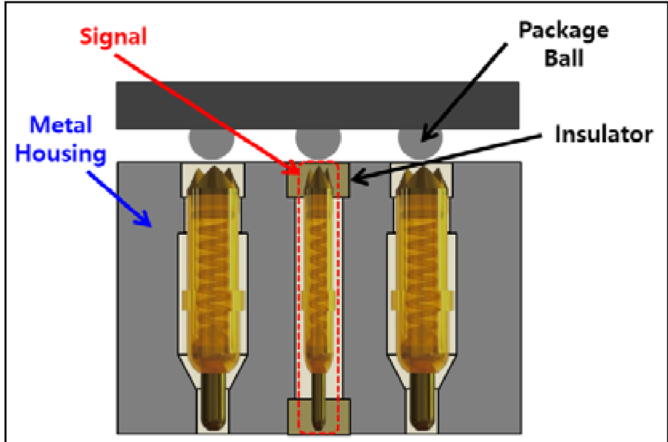

Figure 2: Structure of a coaxial spring socket.

Through the structure shown in Figure 2, the coaxial spring socket has the advantage of improving the signal transmission characteristics by shielding the electromagnetic wave of the signal at high frequency, but it has the disadvantage that the signal length is long. If the signal length is long, the inductance value increases, and that leads to a degradation of signal transmission characteristics. In order to optimize the reflection characteristics of the signal, the characteristic impedance should be matched. For this, the signal diameter of the coaxial spring socket should be smaller than the ball pitch. For this reason, when the diameter of the signal becomes very small, the manufacturing cost of the coaxial spring socket increases as the mechanical components, such as the spring and barrel that make up the spring socket, must be made smaller. Therefore, the demand for a high-frequency test socket with a short conductive path and low manufacturing cost is growing.

Elastomer socket with metal housing to prevent crosstalk

In this article, we propose the use of a coaxial elastomer socket with a metal frame instead of the typical elastomer socket configuration that uses a silicone rubber for the insulating part. The ground is configured to form a ground connection notch inside the housing hole so that the conductive path and the metal housing are short circuited, so that the reference to which the return path of the signal is realized becomes the metal housing. Figure 3 shows the structure of the coaxial elastomer socket.

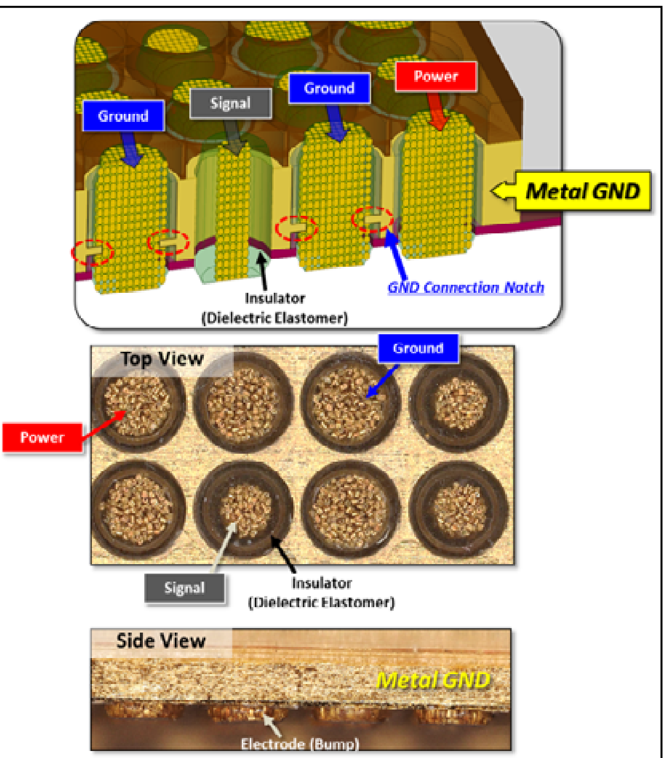

Figure 3: Structure of a coaxial elastomer socket.

The coaxial elastomer socket also needs to implement a small signal diameter for impedance matching, but there is no significant increase in manufacturing cost to do so. This is because of the implementation of powder gathering by magnetic force rather than because of the miniaturization of various parts made by machining compared to a spring socket. Because the length of the conductive path in a coaxial elastomer socket is much shorter than that of the spring socket, the inductance value is low and the signal transmission characteristics are excellent. Moreover, it has a crosstalk shielding effect because it is completely wrapped around the signal with a metal frame. It has the same shielding

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effect as the coaxial spring socket, as well as superior transmission characteristics and low manufacturing cost.

High-frequency electrical simulation analysis and verification

In order to check the crosstalk according to the structure, high-frequency analysis of the spring, elastomer, coaxial spring, and coaxial elastomer sockets was performed in the frequency and time domains. Insertion loss, return loss, and crosstalk were analyzed in the frequency domain, and an eye diagram was used for the time domain analysis [4].

Crosstalk is divided into near-end and far-end crosstalk. In general, near-end crosstalk has a greater loss than far-end crosstalk. Therefore, the analysis was performed based on near-end crosstalk for purposes of this article. The ball pitch applied to the analysis is 0.80mm pitch, and the ball array is shown in Figure 4.

Frequency domain analysis. As for the analysis conditions in the frequency domain, the solution frequency was set to 20GHz and frequency sweep was set

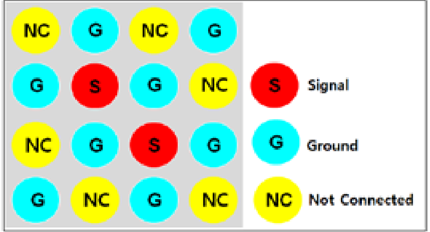
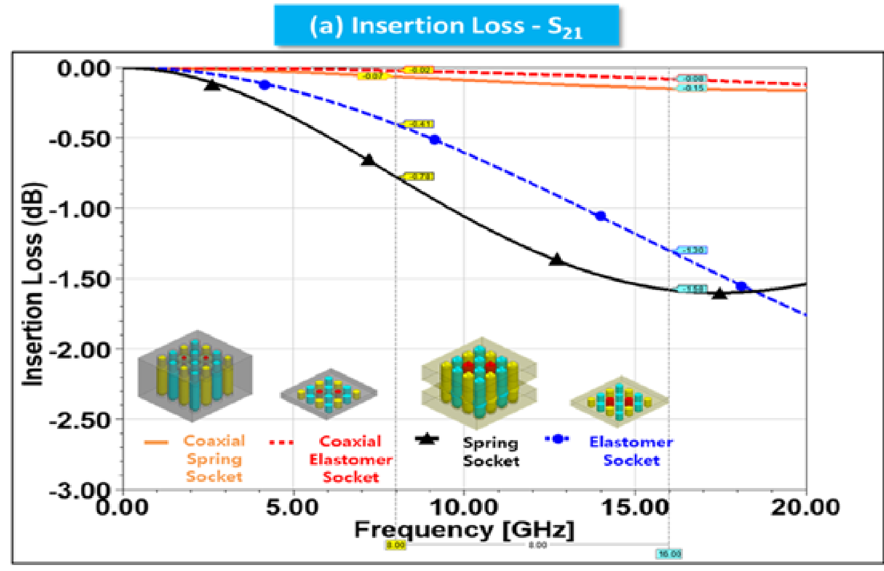
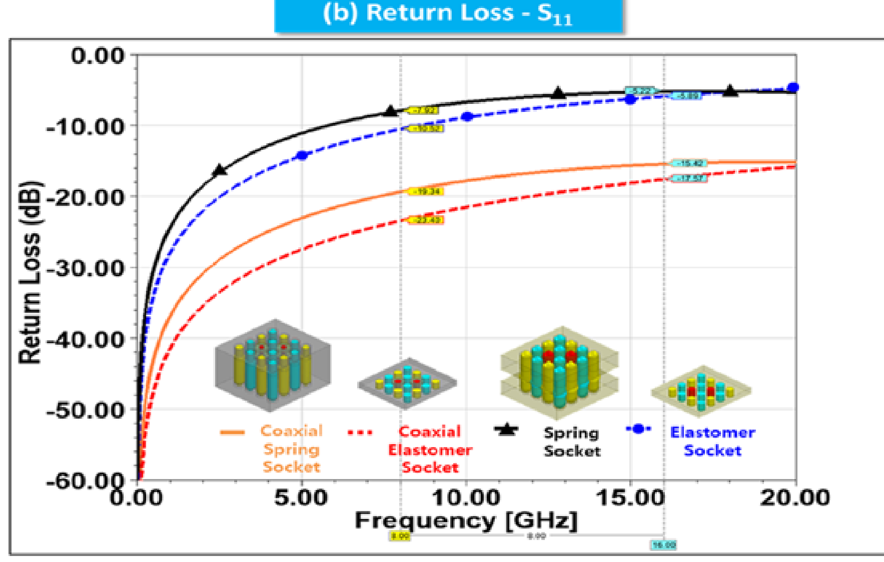


Figure 4: A ball array.

from 10MHz to 20GHz, and the analysis frequency point was set to 8GHz and 16GHz based on data rates of 16Gbps and 32Gbps. The results are shown in Table 1. The insertion loss characteristic of the elastomeric socket is 17% better than the spring socket, and the return loss characteristic is 13% better based on 16GHz. This means that the elastomer socket has a shorter signal length than the spring socket and the characteristic impedance is matched to nearly 50 ohms.

Crosstalk, however, which is a factor that interferes with the transmission of high-quality signals, is occurring at 16GHz and -34.79dB for the spring socket, and at -41.40dB for the elastomer socket as shown in Figure 5. To prevent such crosstalk, we have proposed a coaxial spring socket with metal housing, which improves crosstalk to -44.66dB (about





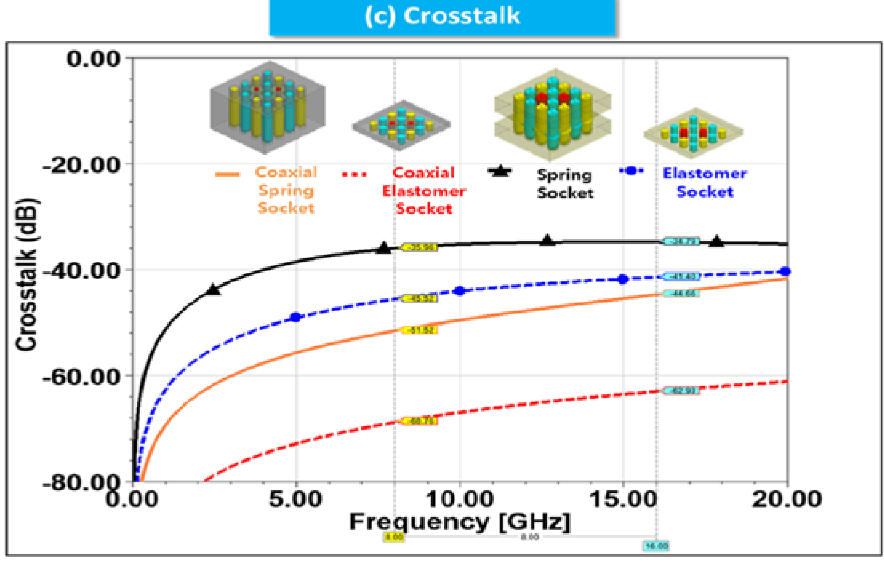


Figure 5: Graphs showing: a) insertion loss, b) return loss, and c) crosstalk of spring and rubber socket materials.

Single-Ended (Unit : dB)	Insertion Loss		Return Loss		Crosstalk	
	8GHz	16GHz	8GHz	16GHz	8GHz	16GHz
Spring Socket	-0.78	-1.58	-7.92	-5.22	-35.96	-34.79
Elastomer Socket	-0.41	-1.30	-10.52	-5.89	-45.52	-41.40
Coaxial Spring Socket	-0.07	-0.15	-19.34	-15.42	-51.52	-44.66
Coaxial Elastomer Socket	-0.02	-0.08	-23.40	-17.57	-68.76	-62.93

Table 1: Frequency domain analysis comparison.

1.3X better) based on measurements at 16GHz. As a result, the insertion loss was improved by -0.15dB (about 10.5X) and the return loss was improved by -15.42dB (about 3X). This shows that insertion loss, return loss, and crosstalk are all improved compared to the elastomer socket. However, the coaxial spring socket has 53% insertion loss characteristics compared to the coaxial elastomer socket based on measurements at 16GHz. Return loss characteristics tend to drop by 14% and crosstalk by 30% because of the large number of components and the long signal length to secure the spring tension. This means that the coaxial elastomer socket is shorter than the coaxial spring socket and

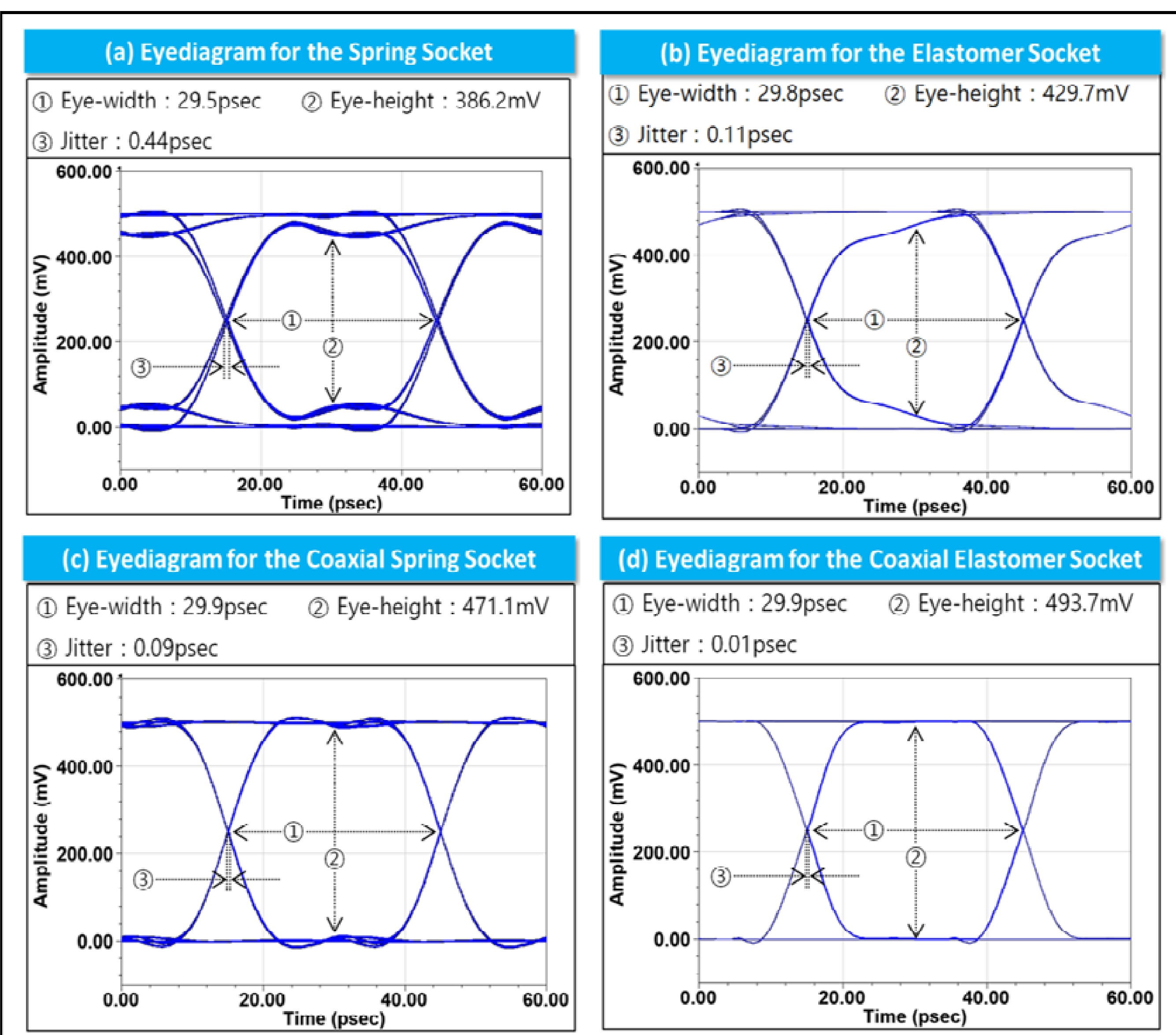


Figure 6: Eye diagrams of: a) a spring socket; b) elastomer socket; c) coaxial spring socket; and d) a coaxial elastomer socket.

Time-domain	Eye-width	Eye-height	Jitter
Spring Socket	29.5psec	386.2mV	0.44psec
Elastomer Socket	29.8psec	429.7mV	0.11psec
Coaxial spring Socket	29.9psec	471.1mV	0.09psec
Coaxial Elastomer Socket	29.9psec	493.7mV	0.01psec

Table 2: Time domain analysis comparison.

the characteristic impedance is matched to nearly 50 ohms.

Through analysis of the frequency domain, the signal integrity characteristics of the spring, elastomer, coaxial spring, and coaxial elastomer socket were revealed, and it was confirmed that the insertion loss, return loss, and crosstalk loss characteristics of the coaxial elastomer socket were the best. As a result, the coaxial elastomer socket has the advantage of being shorter than the coaxial spring socket, so it has excellent signal transmission characteristics and can achieve impedance matching. Therefore, it has excellent signal reflection characteristics, and has the advantage of improving crosstalk with the metal housing.

Time domain analysis

Analysis of signal characteristics in the time domain was conducted through use of an eye diagram, and the rise time of the signal based on a 16GHz operating frequency was applied as 10ps. The eye diagram is an indicator that can check signal characteristics in the time domain, and it is concluded that the larger the eye width and eye height, the smaller the jitter, and the better the signal characteristics. Figure 6 shows the eye diagram for the test socket and coaxial test socket.

As a result of analysis, as shown in Table 2, the eye width and eye height of the spring socket were the narrowest and the jitter value was large. Because the spring socket does not have impedance matching and the length of the signal is relatively long, the eye diagram characteristic is not the best. The elastomer socket also does not have impedance matching, but because it is shorter than the spring socket, the eye diagram characteristics are better than those for the spring socket. On the other hand, the coaxial spring socket and coaxial elastomer socket, which have impedance matching through the coaxial structure, have better eye diagram characteristics than the noncoaxial structures. In particular, it was confirmed that the eye diagram characteristics of the short coaxial elastomer socket secured the best signal characteristics.

Summary

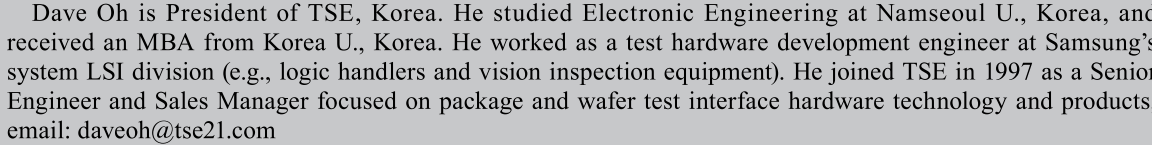
Currently, an optimal socket solution that could deliver high-quality signals by minimizing crosstalk between signals is needed because the sockets used in system-level tests require signal transmission characteristics without loss at high frequencies. Therefore, to find the optimal socket solution as discussed in this article, a high-frequency electrical simulation analysis of a spring, elastomer, coaxial spring, and coaxial elastomer socket was conducted in the frequency and time domains. It was concluded that the coaxial elastomer socket had the best signal characteristics in both the frequency and time domains.

In conclusion, the coaxial elastomer socket based on the elastomer socket has the advantages of a short signal transmission length and an excellent manufacturing cost, as well as the characteristics of electromagnetic wave shielding by a metal frame. Therefore, it was concluded that it could be another solution that could show the best performance in the SLT environment.

References

1. K. Ranganathan, A. Bhalla, "Key trends driving the need for more semiconductor system-level testing," https://www.evaluationengineering.com/instrumentation/article/13017769, Jun 22nd 2018.
2. E. Song, J. Cho, J. Kim, Y. Shim, G. Kim, J. Kim, "Modeling and design optimization of a wideband passive equalizer on PCB based on near-end crosstalk and reflections for high-speed serial data transmission," IEEE Trans. on Electromagnetic Compatibility, V. 52, No. 2, pp. 410~420, May 2010.
3. J. Kim, S. Shin, D. Shin, N. Jeong, "Coaxial probe for RF solution," TestConX Session 6A Presentation 2, pp. 623~640, Mar. 2019.
4. G. Kim, D. G. Kam, S. J. Lee, J. Kim, M. Ha, K. Koo, J. S. Pak, J. Kim, "Modeling of eye-diagram distortion and data-dependent jitter in meander delay lines on high-speed printed circuit boards (PCBs) based on a time-domain even-mode and odd-mode analysis," IEEE Trans. on Microwave Theory and Techniques, V. 56, No. 8, pp. 1962~1972, Aug. 2008.

Biographies



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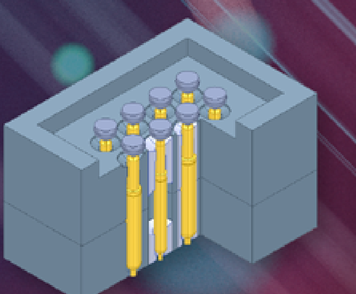

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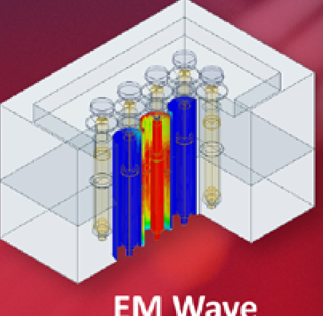

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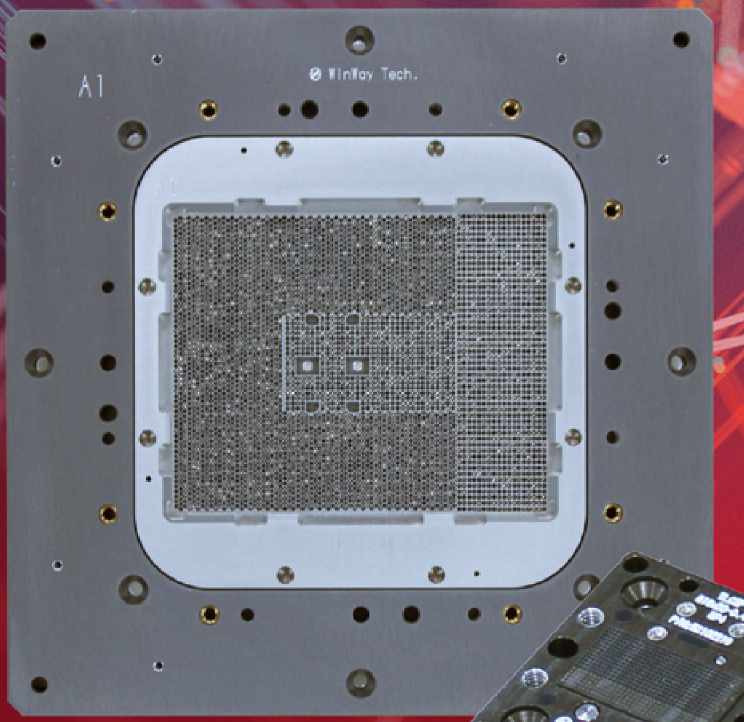

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Age of convergence and exascale computing drive ATE requirements

By Matthias Stahl [Advantest Corp.]

The technology world is currently in the midst of the age of convergence—that is, the convergence of data from a diverse range of applications and data sources. These sources include anything that creates data—ranging from humans, who create data using voice, to automotive, mobile, and wireless/Internet of Things (IoT) devices. Data sources also include edge-computing devices and the servers that store the massive amounts of data needed for high-performance computing (HPC), artificial intelligence (AI), machine learning (ML), and many other applications.

This age of convergence represents the latest wave in a series of semiconductor buying waves extending back 60 years. In the 1960s, the military industrial complex drove worldwide annual semiconductor sales beyond $1.4 billion. The age of business computing coupled with the emergence of the first personal computers and networks saw annual semiconductor sales exceed $5.9 billion in the mid- to late-1970s. The age of the internet and the initial age of mobility drove semiconductor sales to $50.5 billion in 1990. And the addition of mobile computing saw sales exceed $166 billion in the early 2000s. Finally, the age of convergence saw annual semiconductor sales rise from $335 billion in 2015 to reach $527.2 billion this year (a 19.7% increase from the 2020 sales total of $440.4 billion), according to data from the World Semiconductor Trade Statistics (WSTS) organization [1]. (Figure 1 tracks the buying waves over 60 years. The chart was created three years ago, but its estimates still track well with recent WSTS updates.)

The age of convergence is bringing about the increasing use of natural user interfaces, in which we interact with devices and systems using natural speech, gestures, hearing, and vision.

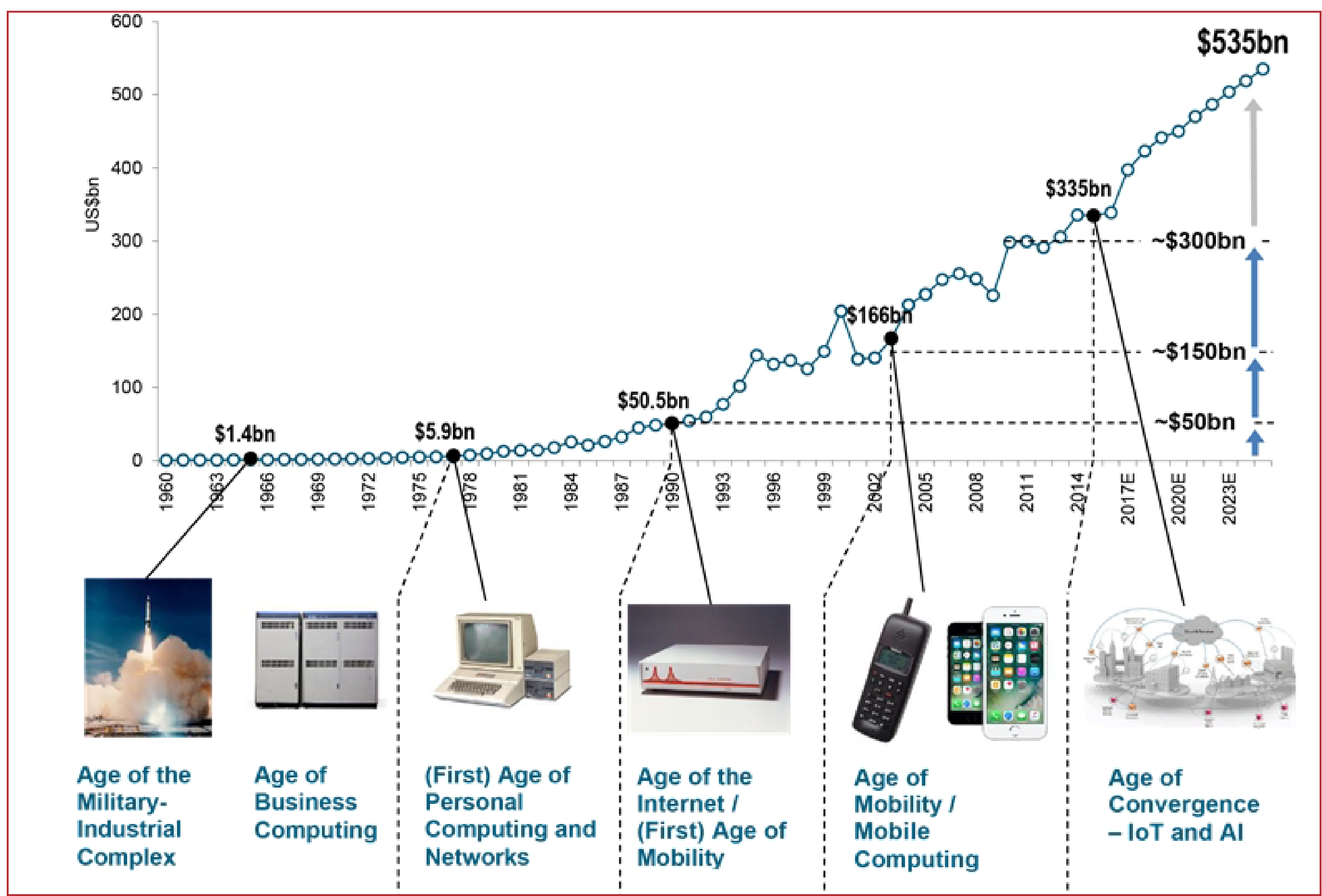

Figure 1: Innovation has driven waves of semiconductor purchasing over the last 60 years. SOURCE: WSTS data, Macquarie Research estimates, October 2017.

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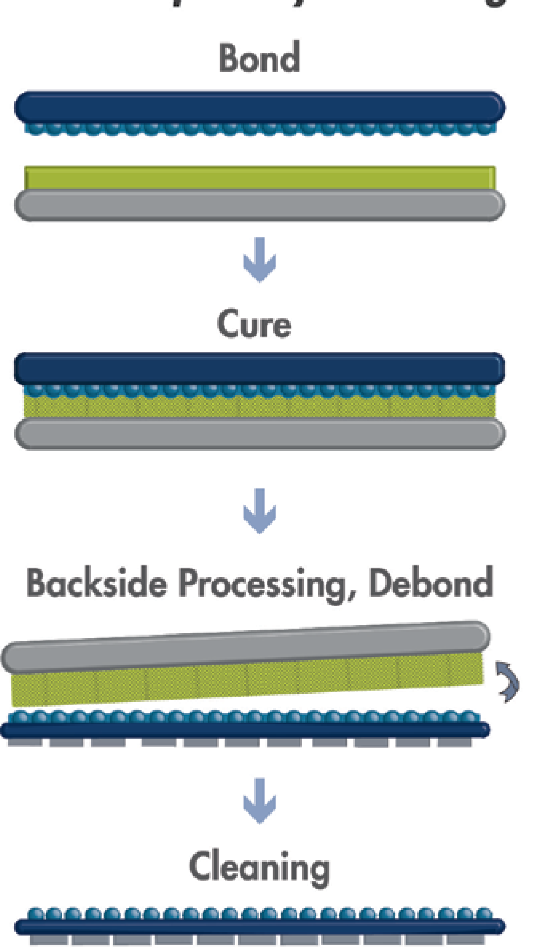

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It also is bringing about the increasing use of local and mobile artificial intelligence, implemented on your phone or in your car; wireless networking, including 5G, Wi-Fi, and IoT devices; edge artificial intelligence (AI), implemented on edge-computing devices; and a fiber backbone that connects to a server that performs HPC to implement high-end ML and AI. The key takeaway is that there is no single application driving today's wave of semiconductor purchases—rather, the combination and convergence of all applications is driving the wave.

Driving the need for exascale computing

The massive amounts of data that the converged technology ecosystem generates must be processed, thereby driving the advent of exascale computing. The term exascale refers to a supercomputer capable of calculating at least one exaflop, or 10^{18} floating-point operations per second—a thousand-fold increase in compute power vs. the first petascale computer, which began operating in 2008, according to the Los Alamos National Laboratory [2]. Currently, no single exascale computer exists, although the first, called Frontier, may debut at Oak Ridge National Laboratory (ORNL) later this year [3]. Nevertheless, the combined compute power currently available certainly exceeds the exaflop number. Aggregate exascale compute power resides on everything from a high-end server to a handheld smartphone—whose capability exceeds that of a high-end PC of just a few years ago.

The industry is looking at new approaches to getting even more compute power and overcoming the challenges that the new approaches entail. For example, the mobile computing industry is moving to new processing nodes and will have to address the tradeoffs between power and performance while accommodating new failure models. Companies serving high-performance compute and graphics applications will deploy chiplet technology—a building-block approach that will allow them to precisely match their speed requirements to their intended applications and to improve yield. These companies will also rely on advanced packaging techniques while contending with power and thermal challenges. Furthermore, in their drive toward exascale computing, makers of datacenter infrastructure will deploy millions of heterogeneous cores to achieve scalability and parallelism they need while maintaining resilience to failures and finding innovative ways to manage power.

Implications for test

Convergence and exascale computing combine to present unique testing requirements as chipmakers move toward more advanced process nodes. Because transistor density increases at smaller nodes, scan-test data volume is exploding, creating the need for more memory, faster scan techniques, and new methodologies. Advantest estimates that scan data volume has increased 250% since 2018 and will reach 450% of 2018's level by 2023.

Handling this increasing scan data volume will require automatic test equipment (ATE) with deeper vector memory and, to keep test times under control, faster scan-test methodologies such as scan over high-speed input/output (HSIO), which can employ a SERDES interface or the IEEE 1149.10 high-speed test access port and on-chip distribution architecture. We estimate that in 2020 the classic scan-test technique provided scan access to 90% of all digital devices, with muxed scan taking up the remainder. By 2025, classic scan's share could drop to 40%, with muxed, SERDES, and 1149.10 scan

implementations each providing scan access to about 20% of all digital devices. By 2030, SERDES and 1149.10 could combine to provide scan access to about 60% of all digital devices, with classic scan finding use in only about 20% of devices.

At the same time, as device nodes continue to shrink, power-supply requirements continue to escalate. ATE makers are seeing a demand for more power in general as well as a need to support more power domains and test integrated power-management ICs (PMICs), requiring high-performance and flexible device-power-supply (DPS) test resources.

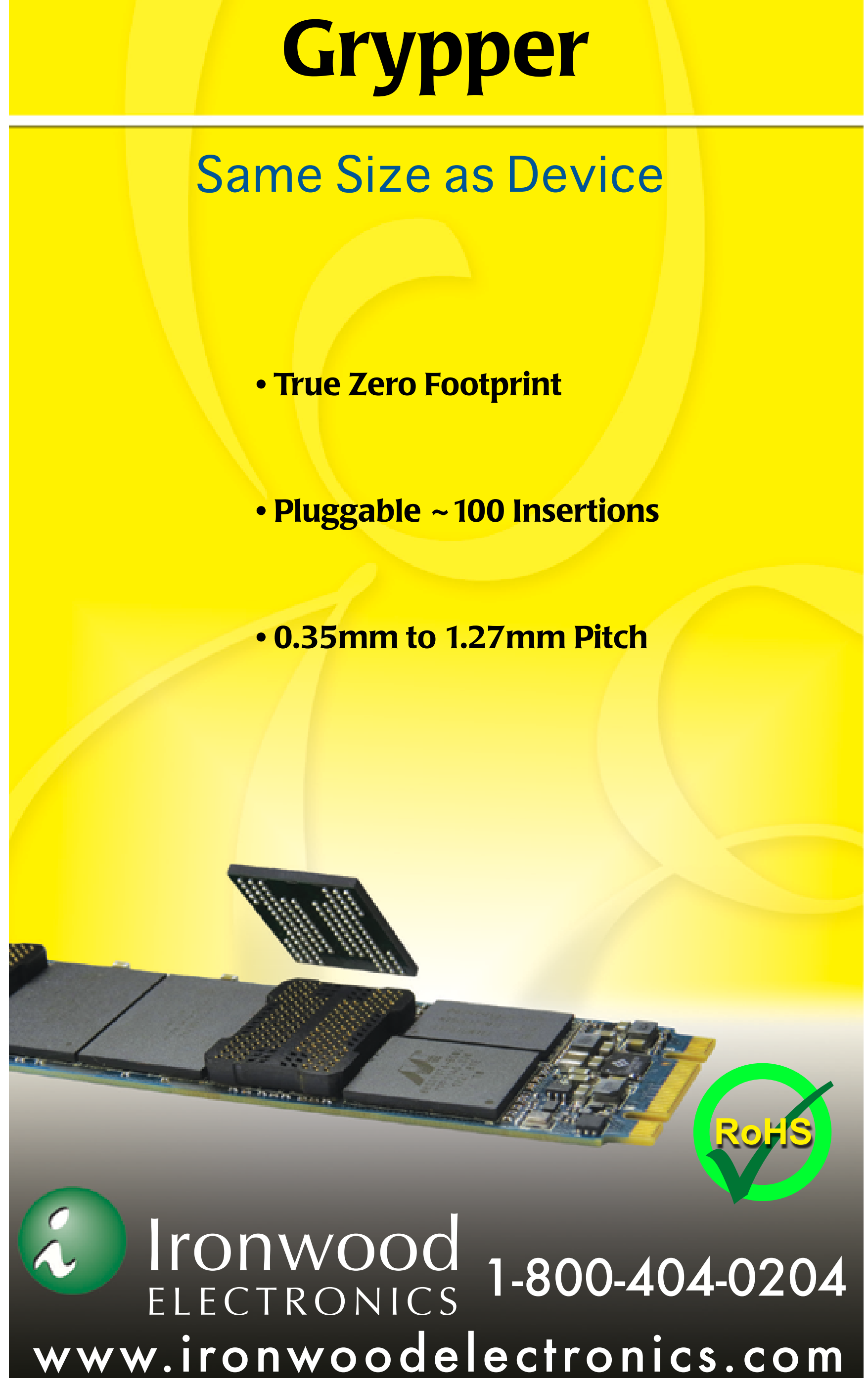
In addition, as voltage levels go down, device power supply (DPS) instruments must offer better accuracy and better dynamic performance. For example, devices require power supplies that can accommodate fast switching with no glitches, providing stable and consistent performance. Today, PMICs already reside close to the central processing unit (CPU), and the trend will continue. The age of convergence will also see new requirements for high-voltage test. While 48V levels have been found primarily in PMIC chips targeting datacenter equipment, the higher voltages are beginning to appear on system on chips' (SoC) designs as well. In addition, multisite testing demands will increase, with the industry looking to keep test costs in line and to shrink time to market.

In the age of convergence and exascale computing, test data collection is becoming critical—the ATE must collect massive amounts of test data quickly by employing advanced error-capture modes, and it must subsequently feed that data back into electronic design automation (EDA) tools to help isolate yield-limiting issues and accelerate yield learning. Yet another trend involves the increasing levels of radio frequency (RF) integration into digital chips, driving requirements for ATE signal processing units that can perform the number crunching required for the post-processing of mixed and RF signal data.

Fortunately, the ATE industry can leverage the same convergence and exascale technology trends and technologies that chip manufacturers are exploiting to meet emerging test challenges. For example, a test company can leverage new technology waves to build high-performance test processors that can operate at 5Gbps transmit and receive rates while supporting advanced flexible error-capture modes at the same speeds.

Similarly, convergence technology can be leveraged to implement a dual sequencer that can speed up test tasks involving matched loops and jumps while minimizing test-time overhead, and it can enable fast and simple timing measurements. An ATE system can also incorporate edge computing in the form of a commercially-available processor core that can handle calibration, data embedding, compensation, and related tasks without burdening a dedicated test processor.

In addition, an ATE system used to test convergence and exascale devices can be seen as a distributed system with massive compute power, posing data aggregation and distribution challenges involving the ATE's system level, card-cage level,



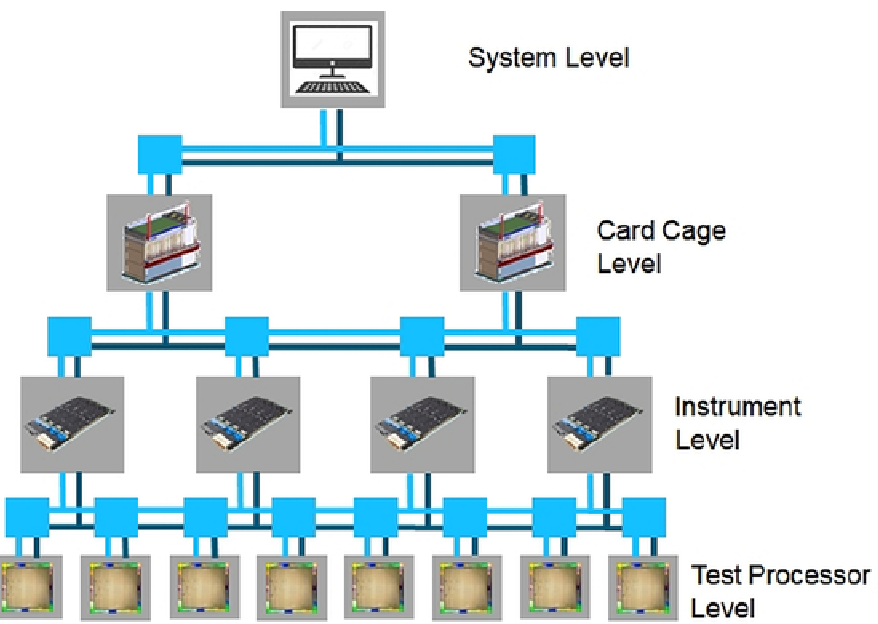


Figure 2: ATE designed to test high-performance devices for the age of convergence and exascale computing can benefit from a computing network that interconnects the system, card-cage, instrument, and test-processor levels.

instrument level, and test-processor level (**Figure 2**). A dedicated communications bus that is embedded in the test system and that exhibits very low latency can support concurrent communications at the system, card-cage, instrument, and test-processor levels, facilitating pin-to-pin communications for protocols, synchronization, and power ganging while enhancing throughput and multisite efficiency (MSE).

Advanced packaging technologies also have a role to play. They can allow the tester maker to use 2.5D integration to combine a test system and memory in a single package. For instruments such as DPS boards that do not require a lot of vector memory, such integration can eliminate the need for an additional memory chip, resulting in more fully-independent pins in a small form factor.

There are several other factors to consider when choosing ATE for semiconductor devices targeting convergence and exascale computing applications. Choose a platform that can be configured to scale from an engineering station to a full high-volume multisite production system that can cover all application segments. Choose a system that is compatible with your existing device under test (DUT) interface boards while offering a seamless upgrade path to larger load boards. Water-cooled instruments can achieve the highest levels of accuracy and repeatability. Still other factors to consider include instrument and software compatibility.

ATE for the exascale age

An example of an ATE system designed to address the age of convergence and exascale computing is the Advantest V93000 EXA Scale. The system incorporates the company's Xtreme Link, a specialized ATE network with edge-computing capabilities. Xtreme Link makes use of an optimized protocol focused on test needs and requirements—such as high throughput and MSE as well as large test-data handling capabilities—that would not be available with an off-the-shelf communications technology like Gigabit Ethernet.

Instruments for the EXA Scale system include the DC Scale XPS256 DPS card, which offers 256 pins at 1A and which limits droop to less than 40mV after any load step to ensure a stable supply voltage for high-performance DUTs designed for mobile, HPC, AI, and other convergence applications. The water-cooled instrument offers full four-quadrant voltage-current capabilities and an accuracy of ±150µV, a level that can help tester customers achieve higher yields for devices such as AI processors or top-of-the-line GPU or CPU.

Another instrument for the EXA Scale system is the Pin Scale 5000 digital card, which offers 256 pins running up to 5000Mbps maximum speed with less than 1.5ps of RMS jitter to enable accurate reference clocks. It supports scan-test result capture at up to 5000Mbps and is designed to enable all scan

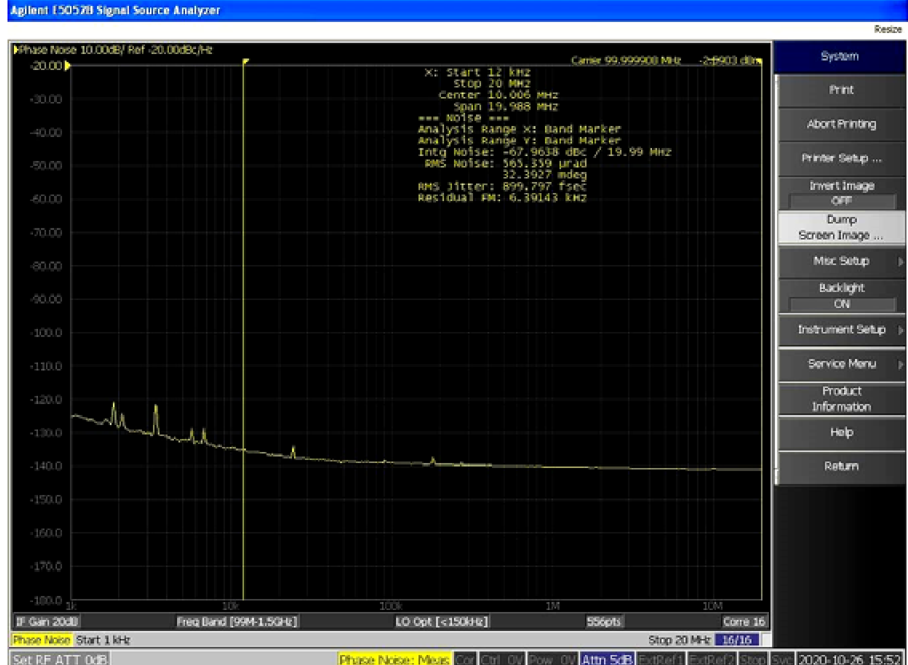


Figure 3: This Pin Scale 5000 phase-noise measurement example shows that the RMS jitter is just 0.9ps—well below the specified 1.5ps.

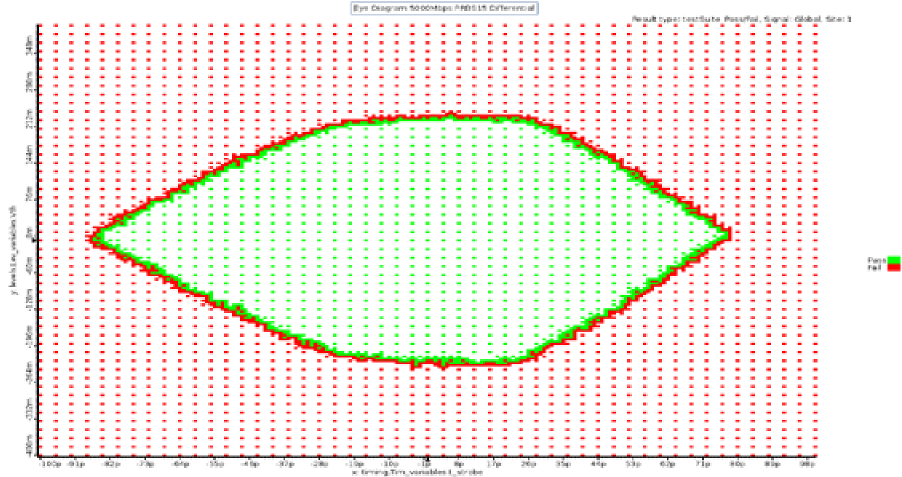


Figure 4: This eye diagram representing a 5Gbps differential signal shows a 55% height and 75% width.

implementations, including parallel, multiplexed, and HSIO scan. In addition, its configuration flexibility supports high site count, allowing users to speed their overall test time by performing parallel core test. The Pin Scale 5000 offers 3.5-gigavector (GVec) scan memory per pin or 28GVec scan memory per eight pins using pooling and fan-out technology. **Figures 3** and **4** show Pin Scale 5000 measurement examples. The **Figure 3** phase-noise measurement example shows that the RMS jitter is just 0.9ps, below the specified 1.5ps. The **Figure 4** eye diagram representing a 5Gbps differential signal shows a 55% height and 75% width. Finally, EXA Scale offers three new extended test heads that scale from engineering configurations to high-count multisite systems and all feature a zero-footprint design—all electronics are integrated into the test head, eliminating the need for a separate rack.

Summary

In summary, the age of convergence has arrived, and we are crossing into the exascale computing frontier, even if the exascale computer named Frontier has yet to execute any calculations at an exaflop rate. Convergence and exascale computing have combined to place stringent new demands on semiconductor ATE, including requirements for more vector memory, for scan over HSIO interfaces, for more bulk power and power domains, for better DPS performance, and for higher multisite test counts. In addition, ATE must implement more and faster data collection operations to accelerate yield learning, and it must have the ability to handle integrated PMICs and the increasing levels of RF integration into big digital chips. Advances arising throughout the industry in pursuit of convergence and exascale computing can be integrated into ATE to meet the emerging new requirements.

Acknowledgment

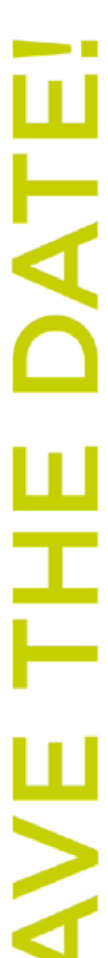
This article is based on the article "ATE in the Age of Convergence and Exascale Computing," by Matthias Stahl, Business Development Manager, Advantest Corp., in *GO SEMI & BEYOND*, Feb. 25, 2021.

References

1. "Global Semiconductor Sales Increase 1.9% Month-to-Month in April; Annual Sales Projected to Increase 19.7% in 2021, 8.8% in 2022," Semiconductor Industry Association, June 9, 2021.
2. https://www.lanl.gov/projects/exascale-computing-projects
3. T. Trader, "Frontier to Meet 20MW Exascale Power Target Set by DARPA in 2008," HPCwire, July 14, 2021.

Biography

Matthias Stahl is Business Development Manager at Advantest Corp., Boeblingen, Germany. He is responsible for the V93000 product line. Throughout his 30-year career in ATE he has also held positions in technical marketing and application engineering. He holds a Dipl.-Ing. in Electrical Engineering and Electronics from the U. of Braunschweig, Germany. Email: Matthias.stahl@advantest.com



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As systems grow, so must FOWLP flow

By Keith Felton, John Ferguson [Siemens EDA, a part of Siemens Digital Industries Software]

As package-level integration and complexity grow, so do the required design iterations, costs, and manpower. Methods that worked in the past are not scaling and are therefore resulting in adoption challenges. Monolithic advanced-node single-chip packaging is no longer the solution for emerging market demands and trends. Fortunately, multi-chip heterogeneous packaging provides a platform for delivering integrated multi-function capabilities, flexibility, better performance, and lower cost. For these reasons, according to a study conducted by Prismark Partners [1], the highest growing substrate market in 2020 was for integrated circuit (IC) packaging with 19% growth, compared with printed circuit boards (PCBs) at only 0.3%.

To address the challenges listed above, one option is to integrate many heterogeneous or homogeneous, high-yield ICs in a single, high-density advanced package (HDAP). HDAP ICs (also known as chiplets) are smaller functional components that can be combined to provide the same capabilities as a monolithic system on chip (SoC). Many leading foundries and outsourced semiconductor assembly and test suppliers (OSATS) now offer HDAP services to their customers.

HDAPs represent technologies that are disruptive to traditional tools and methodologies and generally need a new approach to the planning, design, verification and sign off methodologies. As Raja Koduri, Chief Architect at Intel, was quoted in the *Business Telegraph*, "No single transistor is optimal across all design points. The transistor we need for a performance desktop CPU, to hit super-high frequencies, is very different from the transistor we need for high-performance integrated GPUs" [2].

Multi-die fan-out wafer-level packaging (FOWLP) is probably the most well-known of the HDAP technologies, thanks to Apple and TSMC. TSMC created its integrated fan-out (InFO) process, which was adopted by Apple for its iPhone A10 processor in 2016 and has been Apple's iPhone processor package platform ever since.

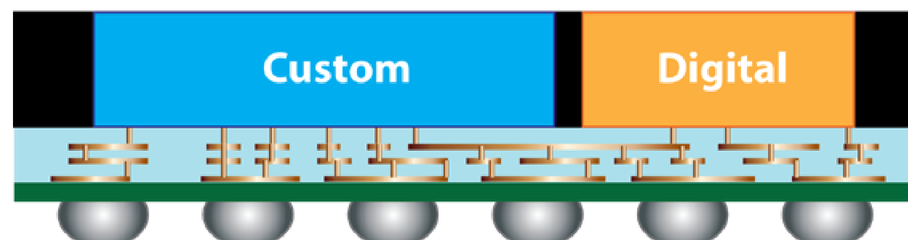

Figure 1: FOWLP multi-die package.

FOWLP design uses materials and processes that are often more similar to silicon wafer fabrication processes than to traditional organic package substrate processes (Figure 1). However, FOWLPs bring design challenges with which traditional organic laminate processes and design tools struggle and often fail to overcome. This article describes in some detail how a 3D digital model (digital twin) of the complete package device assembly can be used to drive detailed substrate layout and verification.

Co-optimization and the digital twin

The scale and complexity of FOWLP designs requires a process transformation to enable designers to address design and verification issues accurately and efficiently. For instance, if a company wants to optimize its package design for size and/or performance, then the design team must optimize the entire system, not just the individual elements. An IC designer can design a really small IC, but it will probably be much more difficult to connect that die into the package, expanding the package footprint. Similarly, a package designer may design a clean and tight package in which it is impossible for the IC designers to get their die I/Os to match specific locations.

To optimize the entire package design, IC designers must know more about the intended package, and package designers must know more about the ICs included in the package. One promising approach is the adoption of co-optimization design, where multiple designers simultaneously

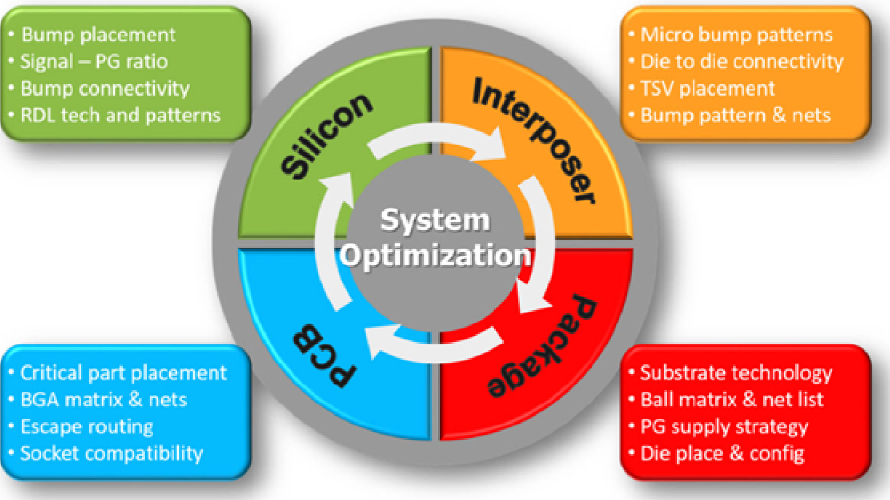

Figure 2: Co-design optimization across all connected substrates.

work on the same design across local or global networks yet retain the ability to visualize all design activity. Obviously, to make co-optimization practical and profitable, designers must be able to collaborate without onerous set up or process management.

A 3D digital model (i.e., the digital twin) of the FOWLP assembly provides a comprehensive representation of the full system comprising multiple devices and substrates. With a digital twin, each team can design and verify their piece in the context of the entire system, even if other teams' design work is not yet complete. This co-optimization approach ensures overall system success when all components are completed and integrated together (Figure 2).

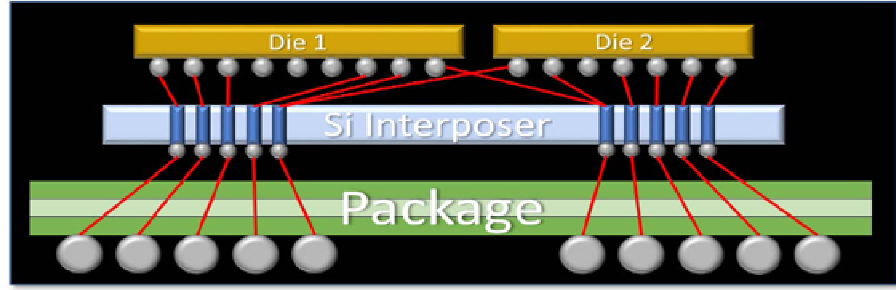

Figure 3: Three substrate levels from different design teams.

Once the digital twin is complete, extensive validation and verification of the design before it moves to fabrication and assembly means problems and issues can be found and resolved without disrupting the current design process or methodology. Teams can also review the architecting and planning process and use it as a left-shift strategy to drive a validated, optimized concept that can greatly reduce implementation and final validation/sign off issues.

Constructing a digital twin for a FOWLP enables designers to work through a series of critical "what if" questions and resolve numerous challenges before any physical construction begins. Using the digital twin also enables teams to design and verify their portion within the system independently, without regard to the completion status of other teams' components. This independence ensures overall system success when all components are completed and integrated together.

The digital twin provides a model of the entire package assembly—a "blueprint"—that drives all levels of implementation, verification, analysis, and manufacturing. The digital twin eliminates the use of multiple static spreadsheets to represent pin and connectivity information by replacing them with a full, system-level netlist in Verilog format. This netlist drives complete physical and electrical verification at every level of the design hierarchy (dies, interposers, embedded bridges, and package substrates).

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Digital twin construction requires tools that can aggregate data from different sources and in different formats into a cohesive system representation suitable to drive verification and analysis, ideally using industry-standard formats. The tools should be able to automatically recognize device and substrate interfaces without having to instantiate pseudo-components. This enables multi-designer asynchronous design, allowing co-development by different teams on different timelines in different locations.

Designers must account for the manufacturing layer sets, position within the package, and scale factor of each component and die. At the same time, they must manage and optimize the connectivity throughout the hierarchical multi-die, multi-substrate system. This process includes defining and optimizing the pin-outs required for package substrates, silicon interposers, and new ICs. Signal to pin assignments, as well as power/ground patterns, must be defined.

Once all the components are accurately captured, the next step is the construction and definition of the reference top-level netlist of the complete, integrated FOWLP. It is critical to build this netlist correctly, as it will be used to drive the verification of the final assembled device at multiple levels. The preservation and reuse of original data, such as a device's Verilog description, is essential. The greatest risk exists during translation or conversion, such as with a schematic or spreadsheet. If this step is done incorrectly, the "digital thread" breaks and the threat of connectivity errors rises steeply.

Let's get physical…and electrical

Because FOWLP manufacturing technologies differ substantially from traditional organic laminate substrate packages, the verification process is also substantially different. One major difference is the use of GDSII instead of Gerber as the manufacturing interface format, and the challenges that brings to the design process. With such a very different fabrication process comes a very different verification process that introduces unfamiliar verification rules, technologies, and associated methodologies.

FOWLP packages typically contain multiple devices and multiple substrates that are often stacked (Figure 3). These components are typically designed by separate designers and teams who may or may not communicate and collaborate efficiently and consistently with each other. When these designs are integrated, a number of system-level verification and validation procedures are required to ensure that they are connected correctly, both logically and physically. Ideally, the solution should be minimally disruptive to the overall design process while providing comprehensive design rule checking (DRC), layout vs. schematic (LVS), and layout vs. layout (LVL) verification of both the individual components and the final, assembled package.

Verification procedures must also be capable of managing the complexity and scale of such a fully-integrated 2.5D/3D assembly, where die pins can equal/exceed 40,000 and total interposer pins can easily

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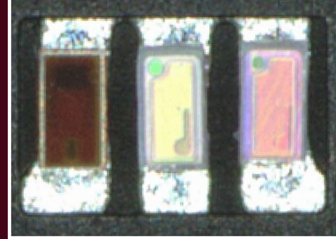
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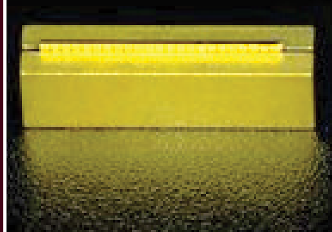
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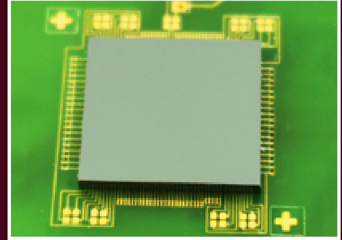
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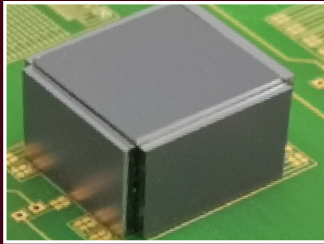
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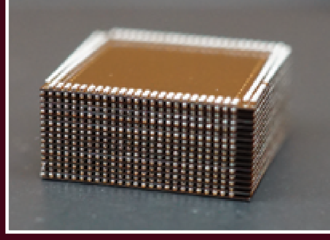
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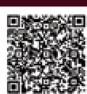


exceed 250,000. Such levels of validation and verification are commonplace in chip design but are a new phenomenon for package designers.

Although the technology needed to perform the critical checks noted above exists today, it has to be integrated into the package design flow and process. Ideally, it also must be capable of providing results that can be displayed with packaging design tools. Typically, the required checks fall into two categories: physical (geometric) and electrical connectivity.

Physical verification of FOWLP designs must address the unique physical characteristics of these packages, including the presence of multiple components, non-Manhattan shapes, and disparate file standards. Fortunately, FOWLP designers do not need to check every geometry in every die. Each individual die in a FOWLP package is already taped out for its target foundry with respect to DRC and LVS comparisons. FOWLP verification does require designers to check the interactions between the dies, which may require extracting several layers within each die to see what their impacts are on each other and on the full package.

Regardless of the configuration, the verification tool must understand the layering per die and per placement, including the ability to distinguish between two die with the same layer name. The key inputs for this sign-off verification are the definition of the assembly stack-up of the components and the reference LVS source-system netlist.

As shown in **Figure 4**, the typical FOWLP physical verification process is to validate individual components (die, interposer, package) separately using their process-specific requirements, and then define and check the 3D assembly of the interfaces between the components, preferably using a single rule deck or assembly design kit (ADK). For LVL verification, the focus is on analyzing and verifying alignment, scaling, and overlaps between devices and substrates, as shown in **Figure 5**.

The next step is validation of the electrical connectivity across the assembly. LVS connectivity verification between all the components and substrates verifies the electrical connectivity between connected shapes, mismatched connections, and the locations of electrical pins, as shown in **Figure 6**.

LVS checking in an IC compares the physical netlist, derived from the physical layout data, against the schematic netlist to verify connectivity. Connectivity checking is performed at each substrate level and across substrates. An automated package LVS flow in its simplest form must ensure that the interposer and package GDSII correctly connect die to die (for multi-

Figure 4: Two-step FOWLP physical verification process.

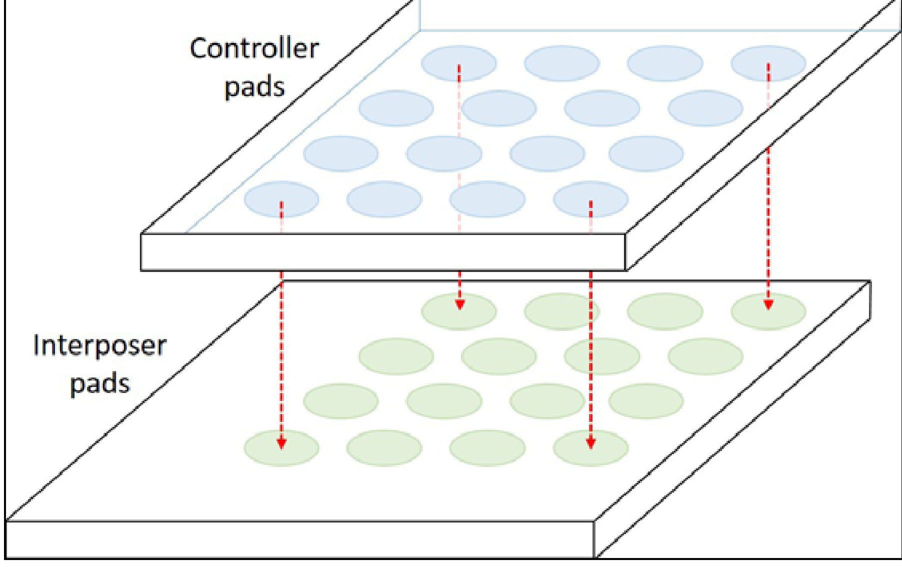


Figure 5: LVL checking of die to interposer.

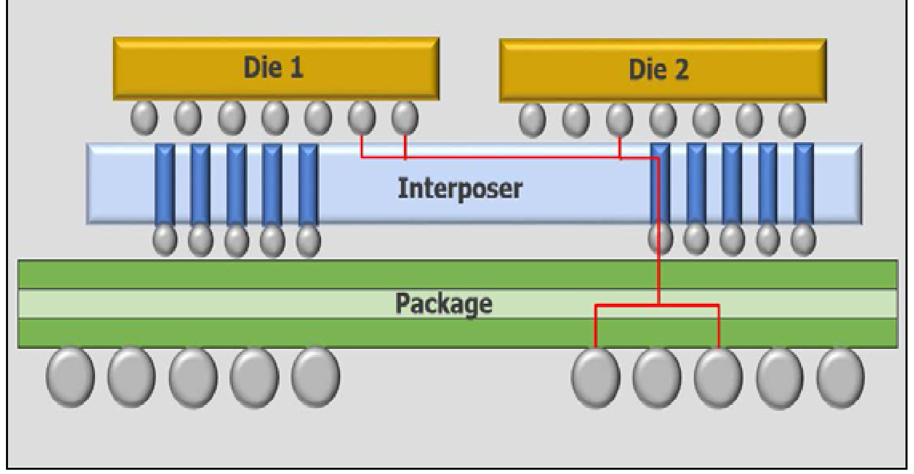


Figure 6: LVS verification across the package system.

die systems) and die to controlled collapse chip connection or ball grid array (C4 or BGA) bumps (for both single-die and multi-die systems) as intended by the designer.

Regardless of the configuration, it all starts with the ability to generate and manage a system netlist. The system netlist is compiled from the digital twin of the overall assembly, as discussed earlier. This system, or reference netlist, is then compared against the physical design connectivity derived from the manufacturing data, such as GDS. Warnings or violations can be highlighted in the digital twin model to trace and debug errors.

FOWLP connectivity verification begins by separating process and assembly integration rule requirements from the design assembly definition. The package house or OSAT company is responsible for creating, validating, qualifying, and delivering the package and interface rules. The package designer is responsible for describing how the assembly is put together, so the tool can understand how to differentiate the layers per die. This step can be automated by extracting the assembly design information from the design tools used to build the flow.

Syntax in the verification tool can combine the two types of rules and provide rule checking capabilities. With this information, the designers can compare the physical package assembly against a source netlist. Errors can be highlighted in the package design as well as in an extracted netlist representing the assembly in order to cross-probe connectivity results.

The essential kit

Another difference between traditional printed circuit boards (PCBs) and FOWLPs is the greater level of guidance FOWLP designers require from the manufacturer/fabricator. This need has driven an entirely new approach for sign-off quality physical verification of packages: the ADK.

An ADK provides a standardized process both chip design companies and assembly houses can use to ensure the manufacturability and performance of FOWLP packages. Similar to an IC process design kit (PDK), an ADK includes the standardized rules, qualified tool flows, interface formats, and input/

output formats that designers need for successful design—all of which have been tested, qualified, and proven to produce working products. A complete ADK must work across both IC and packaging domains, implying that the flow must support multiple formats: IC layout design formats as well as package formats. By implementing a standardized, proven process, all participants can improve both their first-time success rate and overall product quality.

Creating an ADK is a non-trivial effort, requiring cooperation and collaboration between design houses, assembly houses, and electronic design automation (EDA) vendors. Yet using an ADK can reduce the risk of package failure while also reducing turnaround time for both the component providers and assembly houses. In short, an ADK is the key to achieving first-pass, high-yield success for packaging technologies such as FOWLP.

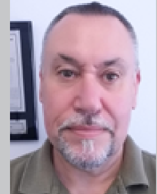
Summary

Next-generation packaging solutions like FOWLP require innovative design strategies coupled with standardized design requirements and a proven, automated sign off for physical, electrical, thermal, and manufacturing performance, all within a single environment that enables designers to manage all of these processes in an efficient, repeatable, and automated flow.

The digital twin methodology enables design companies to create and maintain a single, comprehensive, and standardized representation of the full system that facilitates the use of automated electronic design automation (EDA) tools and processes for analysis and verification of FOWLP assemblies. Combining the digital twin approach with industry standardization and EDA tool automation is an essential part of a unified approach to providing proven, qualified sign off flows for automated heterogeneous verification.

References

1. Prismark Partners LLC, "The Printed Circuit Report," Aug. 2020, www.prismark.com.
2. "Intel leans hard on advanced chip packaging technologies in battle for computing supremacy," *Business Telegraph*, Sept. 16, 2020, https://www.businesstelegraph.co.uk/intel-leans-hard-on-advanced-chip-packaging-technologies-in-battle-for-computing-supremacy/



Biography

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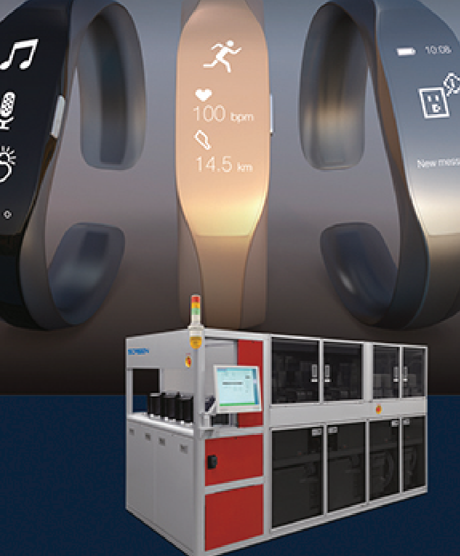

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