Chip Scale Review®

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The Future of Semiconductor Packaging

Volume 25, Number 5

September • October 2021

Laser-assisted rework of multi-die chip packages, 3D-stacks and µLEDs

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- The future is bright for semiconductor industry growth
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- Enabling the 5G RF front-end module evolution with the DSMBGA package
- From wafer to panel: the evolution of an electroplating tool for advanced packaging
- Silicones for chip packaging: stress management, reliability and assembly considerations

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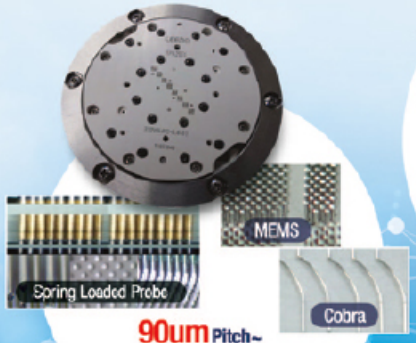
Spring Contact Probe

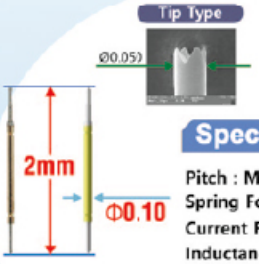
90um Pitch ~

Probe Head



90um Pitch~

RF Probe for Fine Pitch Probe Head



Specification

Pitch : Min.120um
Spring Force : 8.0g@250um
Current Rating : 1.3A
Inductance : 0.3nH

RF Coaxial Spring Probe & Impedance Controlled Socket

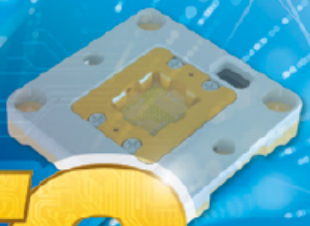
0.18mm Pitch~

Logic Test Socket

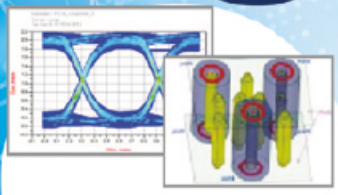
High Speed Automatic Coaxial Probe

Frequency : >20GHz
VSWR : < 1.2

5G

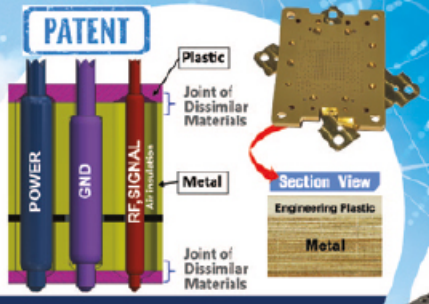


Electrical Analysis

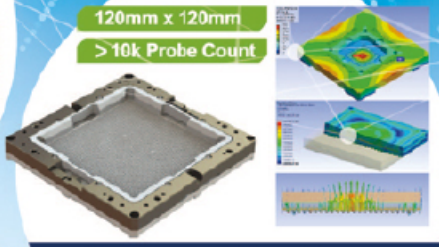


CCC Test, HFSS, TDR
Eye Diagram
4Port VNA Test

MP Socket



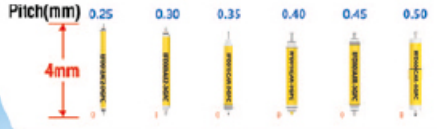
Large Device Socket



Coaxial Probe for 100GHz

Specification

Frequency : 80GHz(BGA),
100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%



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Volume 25, Number 5

The picture shows the result of a highly selective laser-assisted flip-chip removal from a randomly selected printed circuit board assembly. A ceramic tooling holds the chip after the separation step. A uniform and homogeneous solder depot matrix remains on the chip and board. The removed chip can be directly placed onto a new board to retain its functionality, or a new chip can be placed on the board.

Photo courtesy of PacTech – Packaging Technologies GmbH

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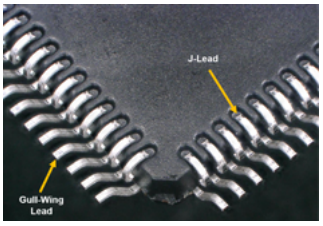
DEPARTMENTS



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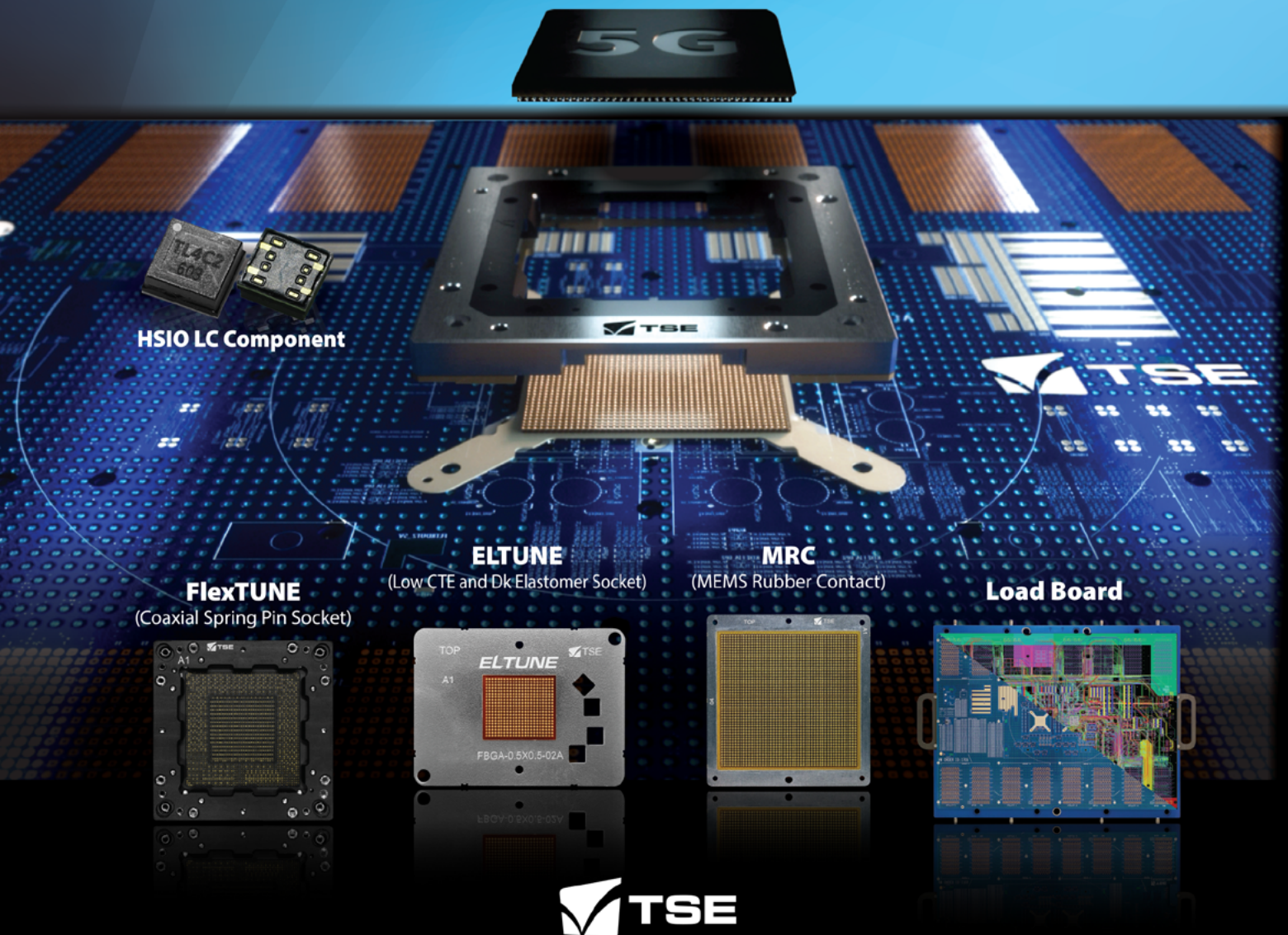
TSE

64Gbps ULTRA HIGH SPEED TEST SOLUTION



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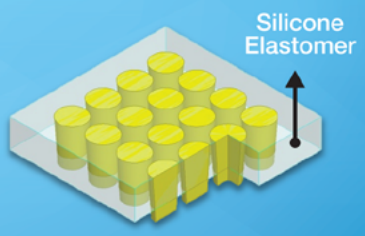
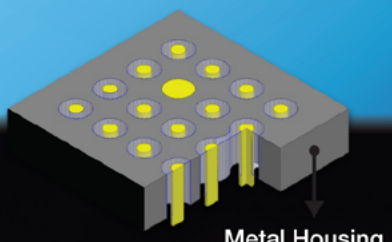
COAXIAL ELASTOMER SOCKET

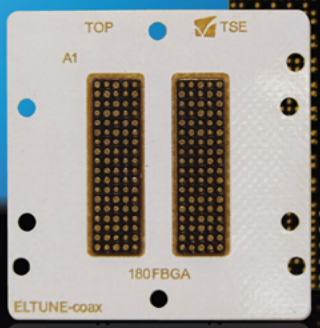
ELTUNE-coax™



Conventional Elastomer Socket



ELTUNE-coax



GDDR6
(18Gbps)

CPU/GPU
(32/64Gbps HSIO,112Gbps PAM4)

• Mechanical Specification

(unit: mm)

0.80mm pitch	Spring Pin	Elastomer	ELTUNE-coax
Over-drive	0.40	0.25	0.25
Test height	3.50	0.60	0.60

• Electrical Specification

(unit: GHz)

42.5Ω, 0.80mm pitch		Spring Pin	Elastomer	ELTUNE-coax
Insertion Loss S_{21} @-1dB	Single Ended (G-S-G)	13.93	27.81	>100
	Differential (G-S-S-G)	25.39	28.94	>100
Return Loss S_{11} @-10dB	Single Ended (G-S-G)	10.98	15.89	>100
	Differential (G-S-S-G)	20.77	25.20	48.21
Crosstalk S_{311} @-20dB	G-S-S-G	8.50	9.43	>100

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The future is bright for semiconductor industry growth

CSR asked Asif R. Chowdhury, SVP, UTAC Group, to share his insights on semiconductor industry growth trends and the current supply chain constraints.

CSR: You are rather bullish on the prospects for the semiconductor industry to see double-digit year-over-year (YoY) growth for the second half of this decade. Could you highlight those developments that you believe will lead to this growth projection?

(**Figure 1**). I predict that this growth will be driven by the convergence of certain fundamental technologies such as 5G mmWave communications, which will enable connectivity at about 100 times faster than what we have today. We are now beginning to experience a higher level of maturity of artificial intelligence (AI), virtual and augmented realities (AR/VR) and cloud computing. These technologies will get a significant boost from the faster, smoother, and ubiquitous connectivity of 5G mmWave—this is what I am calling

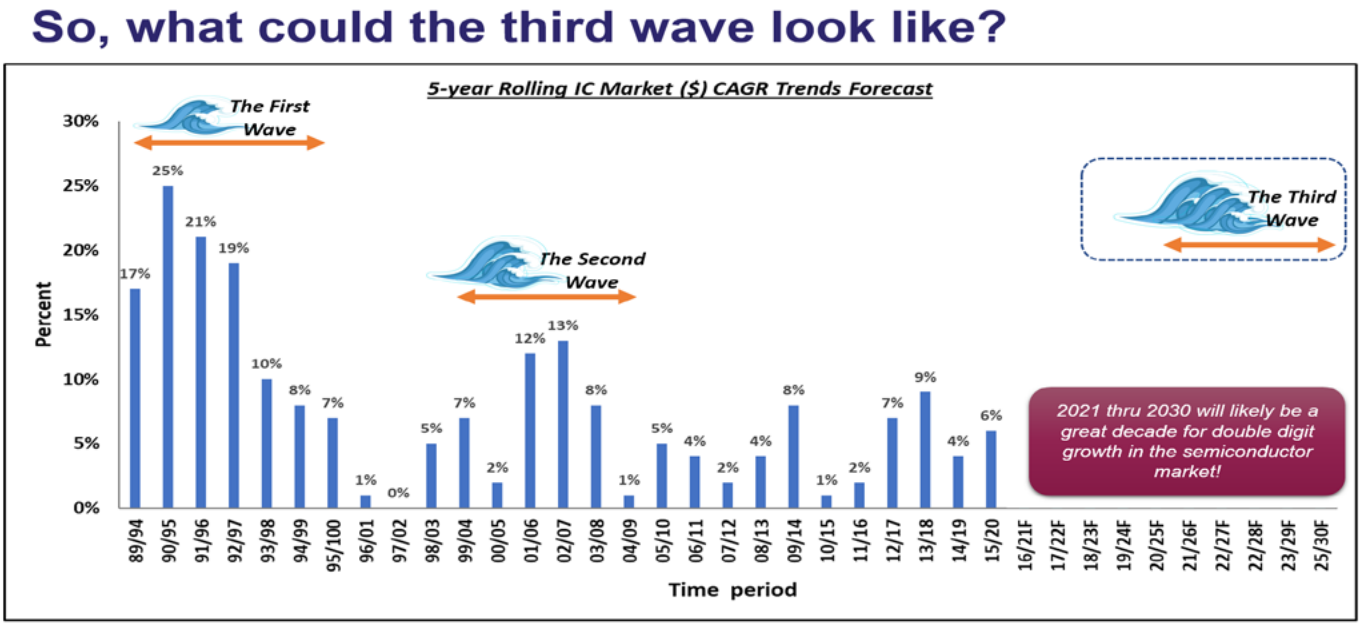

Figure 1: 5-year rolling IC market ($) CAGR trends forecast. SOURCE: Asif Chowdhury, UTAC

AC: While the semiconductor sector accounts for only 0.5% of global gross domestic product (GDP), I think people and governments all over the world are coming to the realization that a significant portion of the remaining 99.5% of the GDP is dependent on it. It is telling when one sees the U.S. president holding a wafer and talking about the importance of semiconductors-–frankly, this was the first time for me to witness such a thing in my thirty plus years in the industry. Indeed, I do believe that we have another golden era of the semiconductor industry upon us with significant growth potential this decade, especially in the second half

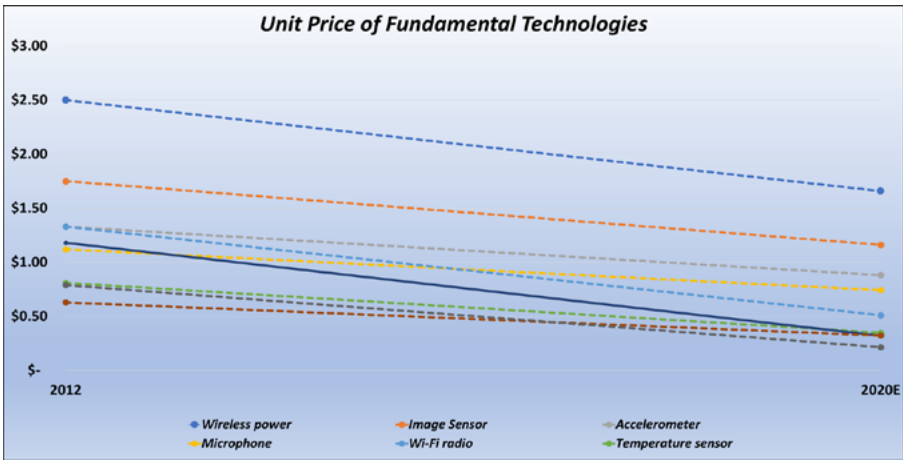

Figure 2: Unit price of fundamental technologies. SOURCE: Asif Chowdhury, UTAC

the technology convergence. In parallel, the price points of certain enabling semiconductor technology nodes such as microelectromechanical systems (MEMS) and other key sensors, converters, microcontrollers, image sensors, Bluetooth® and other wireless radios, have come down during the last decade (**Figure 2**). The technology convergence along with the affordability finally make the Internet of Everything (IoT) a reality. It will also enable the proliferation of full autonomous vehicles within this decade. Semiconductors are at the heart of all of these technologies and this convergence will drive what I call the third wave of semiconductor growth.

CSR: While you see a bright future for growth later this decade, please summarize how UTAC has been handling the current supply constraint challenges that have arisen during the global pandemic response.

AC: Perhaps this current imbalance of supply and demand of semiconductors is a glimpse into the future growth and demand for semiconductors through this decade. The entire semiconductor industry was caught off guard with the demand significantly outstripping the supply that started since last year, and all of us are still struggling with this issue. We are working very closely with all our partners and stakeholders, both on the supplier and customer sides.

We see the shortage and limitation on the supply side across the board starting from raw materials, to wafers, to substrates and to overall manufacturing capacity. Frankly speaking, there is not much anyone can do about these shortages in the short term. So, the key is to "manage" this predicament that no one, unfortunately, foresaw. The way we are handling this crisis (I think the word "crisis" is apt) is through open, honest and regular communications with both our suppliers and customers. We are working closely with our customers to understand the "true" demand. In some cases, we are asking them to prioritize the demand based on the supply shortage. While they are not happy, I must say that most customers are quite understanding and cooperative as long as the communication remains regular and open. Similarly, we are

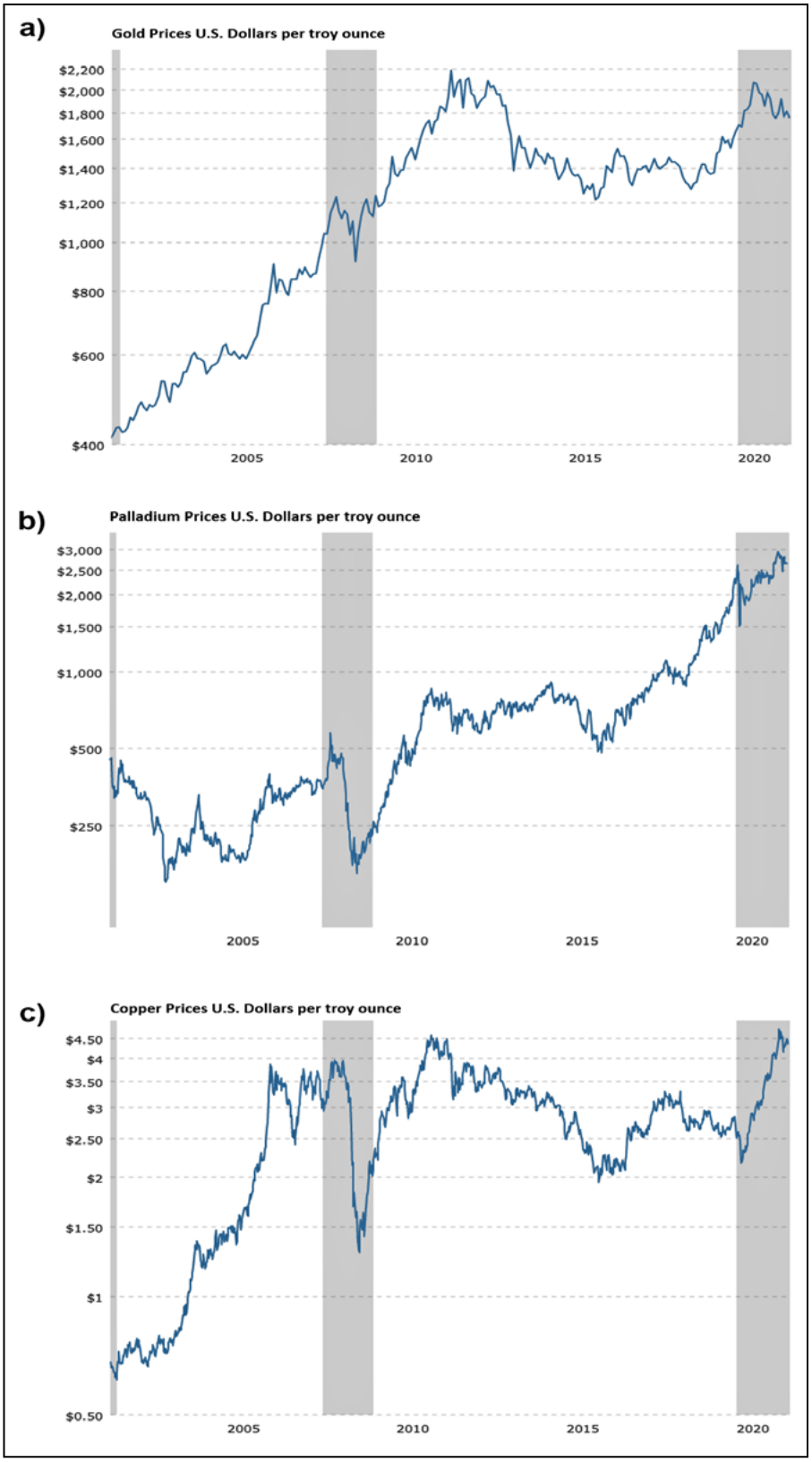

Figure 3: Historical prices of: a) gold; b) palladium; and c) copper. SOURCES: [1-3]

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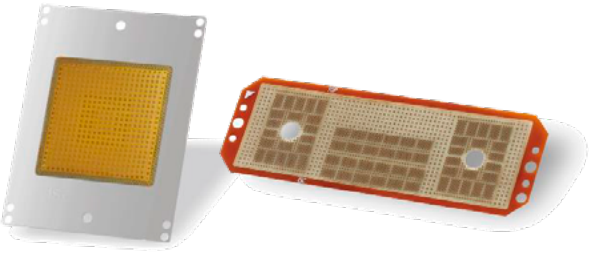
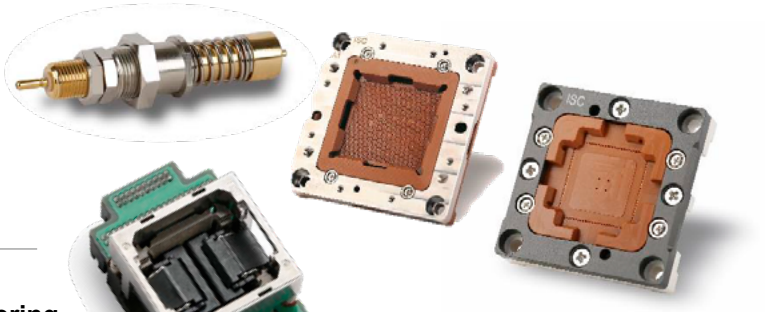


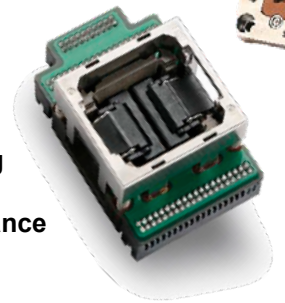
- High performance and competitive prices
- High speed & RF device capability
- No load board pad damage & no contact trace on the ball
- Customized design to meet challenging budget constraints
- Full thermal and electrical simulation

POGO SOCKET SOLUTIONS



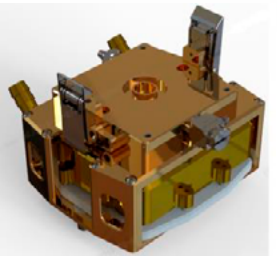
- Various design available
- Excellent gap control & long lifespan
- High bandwidth & low contact resistance

BURN-IN SOCKET SOLUTIONS



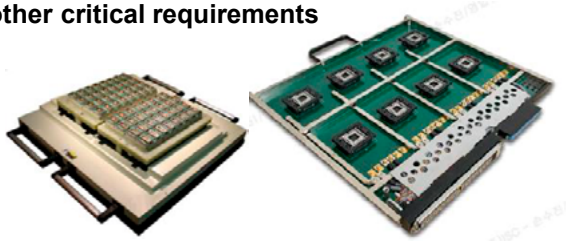
- No ball damage
- Direct inserting on Burn In Board without soldering
- No damage on Burn In Board land
- Simple structure without sub PCB & easy maintenance

THERMAL CONTROL UNIT



- Extreme active temperature control
- Customized design to meet challenging requirements
- Price competitiveness through self-designing and fabrication
- Safety auto shut-down temperature monitoring of the device & thermal control unit
- Full FEA analysis for strength, deflection, air flow and any other critical requirements

Hi-fix & Burn In Board



- High performance and competitive price
- Test fine pitch, high speed device at hot & cold temperature
- Customized design to meet individual requirements

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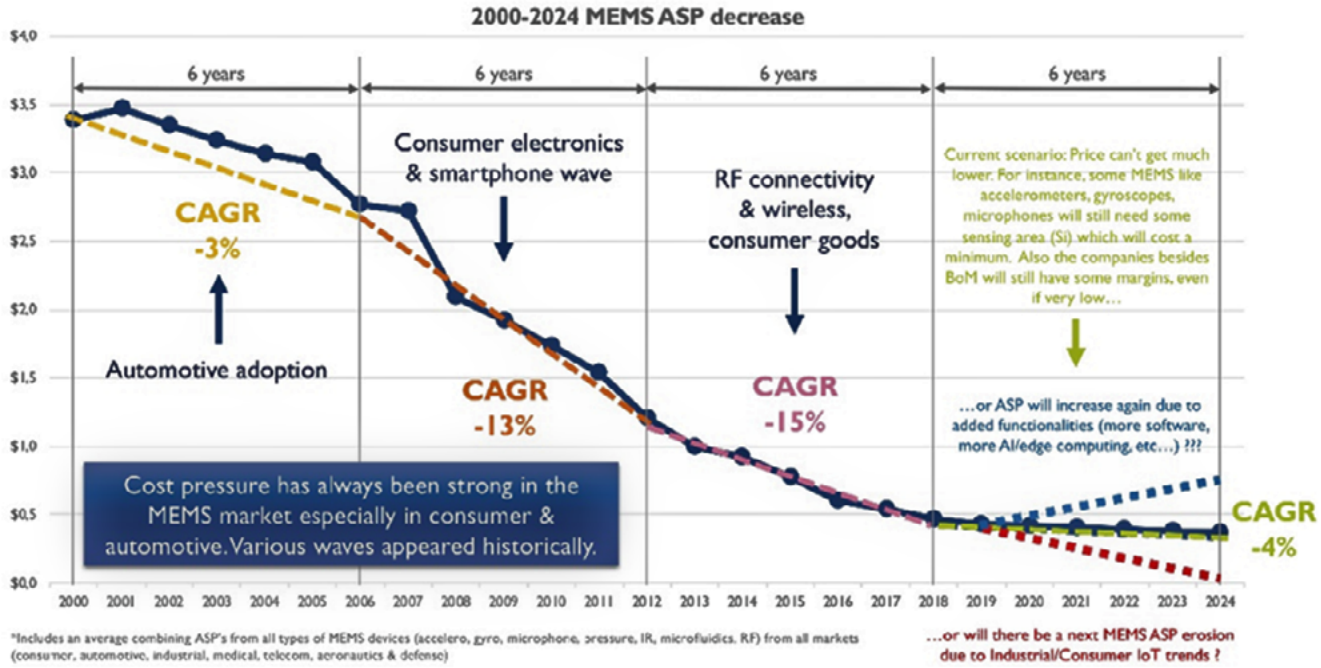

Figure 4: MEMS average selling prices (ASP) evolution. SOURCE: "Status of the MEMS Industry" report, Yole Développement, March 2020

communicating with our suppliers based on this "true" customer demand and ensuring that they keep us posted on their constraints on raw materials and capacity. We have customers signing long-term agreements that provide the ability to do long-term forecasting. These binding agreements reflect realistic forecasts and prevent the market from intentionally inflating future demands. It is not an easy problem to navigate, and our management team is being vigilant in addressing this crisis on a daily basis. Perhaps one silver lining of this predicament is that finally, we are seeing an appropriate upward adjustment of prices based on the market value across the supply chain (**Figure 3**). I think people are realizing that year after year of price reductions, especially against the headwind of increasing raw material prices, is simply not sustainable.

CSR: How will cost competitiveness drive the development of novel advanced packaging solutions?

AC: The cost competitiveness of semiconductors will continue to be a very important factor in the proliferation of these technologies, especially now with the increasing cost of certain raw materials, as well as increasing labor costs in certain markets. As most of your readers are aware, the hype of IoT never materialized during the last decade. In my opinion, it has a lot to do with relatively higher overall product costs. So, unless new semiconductor products and the packaging solutions are cost competitive, they will not likely be successfully adopted by the broader market.

From a product perspective, MEMS is a good example of how the industry has successfully driven the cost down over the last twenty years, most of which was driven by the cost reduction effort in packaging technology. **Figure 4** shows this historical cost reduction. MEMS are one of the most critical products that has not only taken automotive safety to a whole new level during the last two decades, but are critical for many IoT products because these sensors digitize our senses: what we see, feel and touch. The cost of MEMS has significantly been driven down both through device-level advancements and novel packaging solutions—moving away from expensive ceramic packaging to lower cost laminate cavity packaging, or even more mainstream over-molded packaging solutions in some cases. We will see similar trends across most key product segments.

We are already witnessing wider adoption of some of the new packaging and process platforms that are driving down costs. Multi-layer lead frame packages, such as molded interconnect system (MIS), have started to compete with costlier land grid array (LGA) and ball grid array (BGA) counterparts, at least in products with relatively lower I/O counts. We are also witnessing the growth of our own multi-row quad flat no-lead packages (QFNs), known as GQFNs, directly competing with laminate solutions both for cost and performance reasons. I believe that we will soon see large panel-level solutions for some of the lead frame-based packages; if this is successful, the cost will come down significantly. Obviously, there is quite a bit of work going on to improve the yield and cost of existing 600x600mm panel-based solutions for fan-out wafer-level chip-scale packaging (WLCSP) and for multi-die integration. We are also starting to

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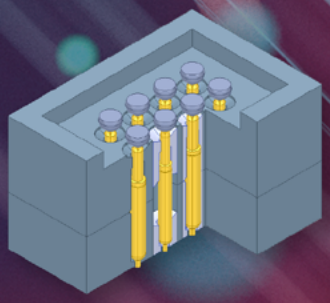
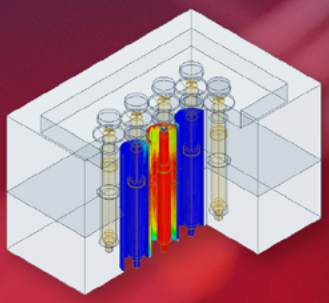
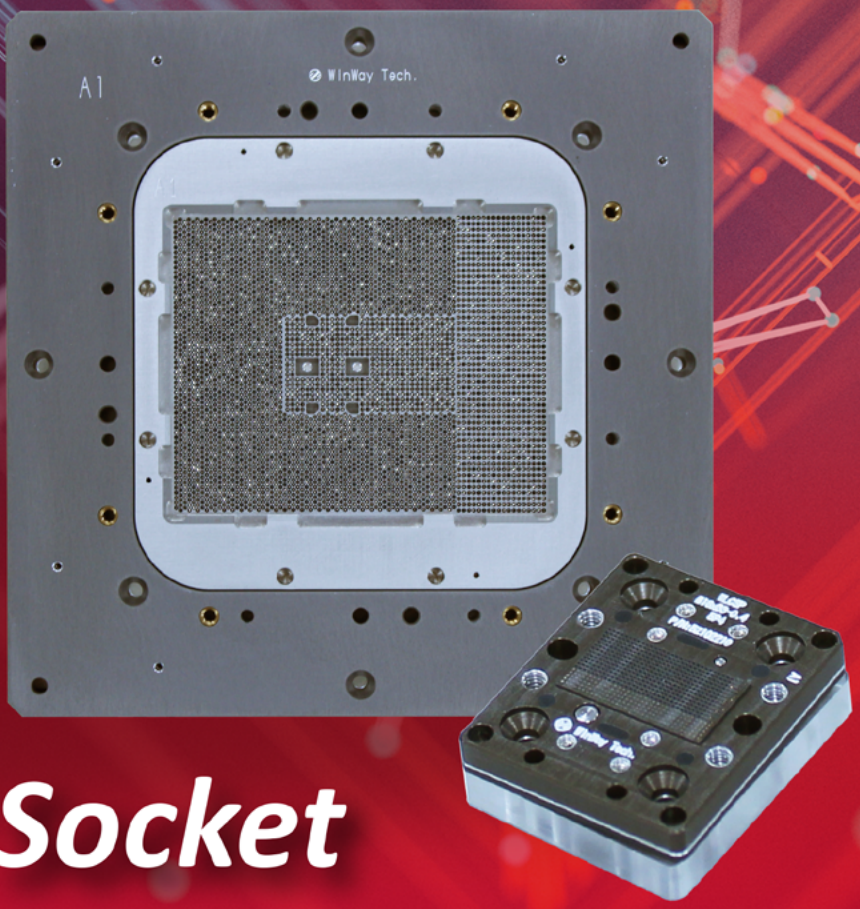


Co-grounding Design



EM Wave



Coaxial Socket

- Package Size > 100 X 100 mm^2
- Mass Production Pitch: 0.35mm (Evaluating 0.3mm)
- Excellent Impedance Control and Crosstalk Reduction

Solution	Bandwidth	Crosstalk	Impedance (50Ω)
Plastic Socket	<20 GHz	-10 ~ -25 dB	△>10 %
Coaxial Socket	>80 GHz	-50 ~ -70 dB	△3 ~ 5 %

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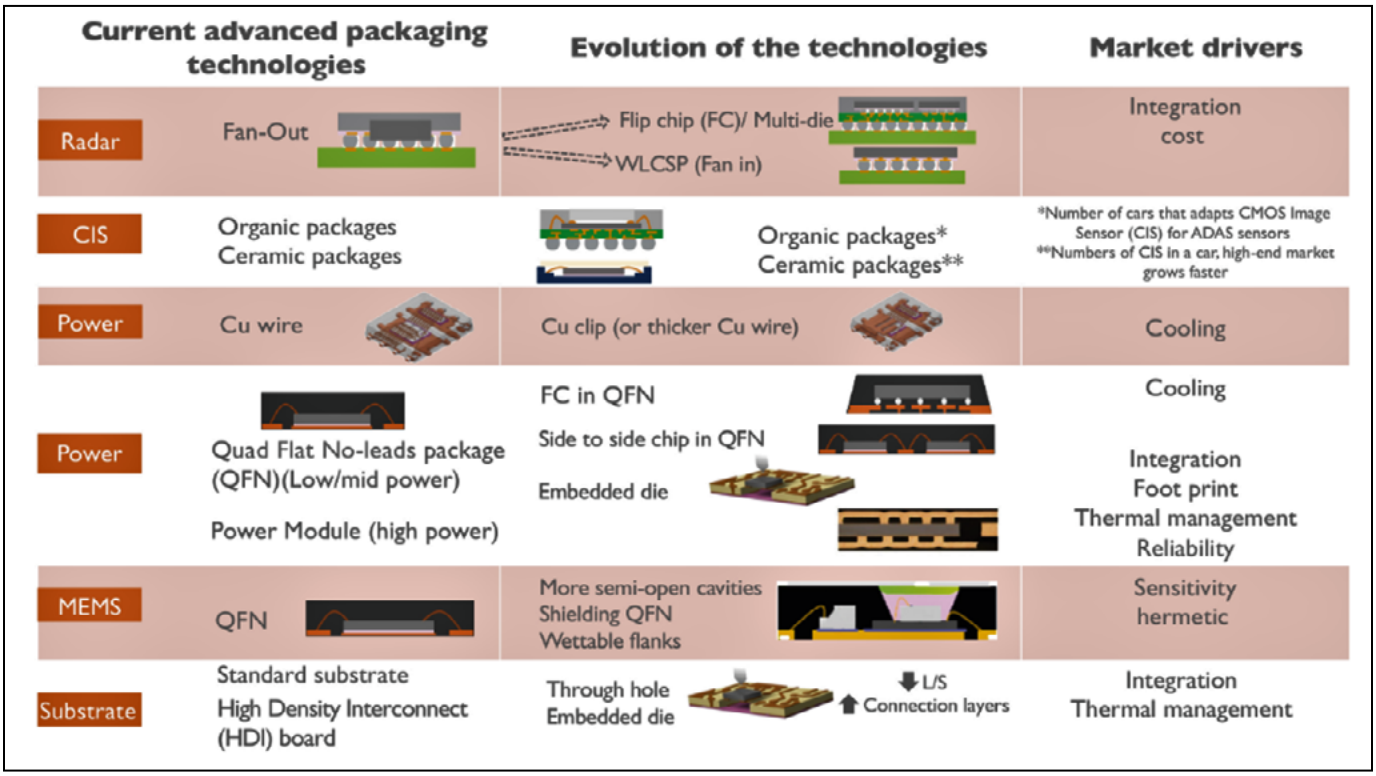

Figure 5: Automotive packaging roadmap. SOURCE: Yole Développement

see customers showing interest in our plasma dicing solution, which enables a very narrow scribe street, thereby allowing a dramatic increase in die per wafer, especially for smaller die sizes. For mature wire bond packages, there has been a steady migration from gold wire to copper wire during the past two decades, and we will continue to see this trend. So, cost will continue to be a key factor in developing new packaging solutions going forward.

CSR: How will the proliferation of multi-die package-level integration come to fruition?

AC: We will likely witness significant growth in system-in-package (SiP) solutions during this decade. It is not just SiP—there will be a proliferation of multi-die solutions in various package types. We are already seeing multi-die requirements from a broad customer base in standard QFN and system on integrated chips (SOIC)-type packages, as well as in more advanced laminate-based BGA solutions. Many of the multi-die solutions in standard mainstream packages will be driven by various products for wider IoT applications such as smart homes. Perhaps a good example of this can be seen in the automotive packaging roadmap by Yole Développement (**Figure 5**). The roadmap rightfully predicts multi-die package and SiP solutions across the product spectrum for the automotive market. Complex, but cost-effective SiP packaging solutions, are now being developed for radars, especially solid-state light detection and ranging (LIDAR) products—a key enabling technology for autonomous vehicles. For power products, we are now witnessing the slow yet steady proliferation of multi-die, multi-Cu clip types of QFNs. Even for standard packages such as quad flat pack (QFP) packages, workhorse of the automotive industry, we are seeing a demand for multiple die solutions. Similarly, driven by both cost and real estate, we will see multi-die and SiP solutions for other semiconductor products for various applications across market segments. I think the decade of SiP is here.

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2. https://www.macrotrends.net/2542/palladium-prices-historical-chart-data
3. https://www.macrotrends.net/1476/copper-prices-historical-chart-data

Biography

Asif R. Chowdhury is SVP at UTAC Group, Singapore. He has over 30 years of experience in the semiconductor industry. Before joining UTAC, he held senior positions at Amkor Technology, Chandler, AZ, and Analog Devices, Wilmington, MA. He holds a BS in Mechanical Engineering from U. of Texas at Arlington, an MS in Mechanical Engineering from Southern Methodist U., and an MS in Finance and an MBA from Northeastern U. Email asif_chowdhury@utacgroup.com

A new, higher density QFP

By Glenn G. Daves [NXP Semiconductors N.V.]

*The genesis of the MaxQFP package is told in the **prequel** sidebar. The engineering team's quest to find a better packaging solution that also accommodates the drive to zero defects for automotive applications was an exciting journey that calls to mind the "eureka" moment all innovators experience. I hope you find the narrative to be a fun read. The feature article below discusses more of the technical aspects of the package as well as the challenges tackled between concept and production.*

The "eureka" moment: innovation culture and a new idea

"What is it?" I asked. I was in our factory in Tianjin, China, and my team (**Figure S1**) there had just handed me a flat plexiglass object with some metal protrusions sticking out of it. The metal was obviously shim stock that had been cut with scissors (leaving a bit of a jagged edge) and bent with needle nose pliers. It was hardly a masterpiece.

Figure S1: The MaxQFP team in Tianjin.

"It's an idea—an idea for a new package," was the reply. I was intrigued—they had really gone out of their way to present the idea in a creative way—far above the usual PowerPoint cartoon engineering that we all typically rely on, but I wanted to know what it does. The answer: "It's a package that will allow us to significantly shrink the size of a quad flat package (QFP) while maintaining everything else we like about QFPs. And, it's fully inspectable!"

Green check mark! When it comes to automotive packaging, a QFP is in many ways ideal. It is ultra-reliable, surviving thousands of temperature cycles before first fail. Thermally, exposed pad QFPs are about as good as you can get in their class and, of course, they hit the mark on the three all-important metrics: cost, cost, and cost. In addition, the drive for zero defects in the automotive industry makes the inspectability of each soldered lead after it is mounted to a board an imperative. QFPs check this box also. The downside of a QFP is, of course, its size. Because it has all its I/Os arranged peripherally, gaining more I/Os requires significant area growth in the package. This is the motivation to move to area-array packages, like ball grid array (BGA), or array quad flat no-leads (QFN), or even other versions of a more dense QFP with QFN-like leads tucked underneath. They have a much higher I/O density than peripheral-lead packages. But, they also come at the expense of either significantly higher cost, the loss of inspectability, or both. The plexiglass mock-up (**Figure S2**) I held in my hand that day apparently delivered on the dream of higher I/O density, while maintaining cost and inspectability. A real win-win, if it delivered.

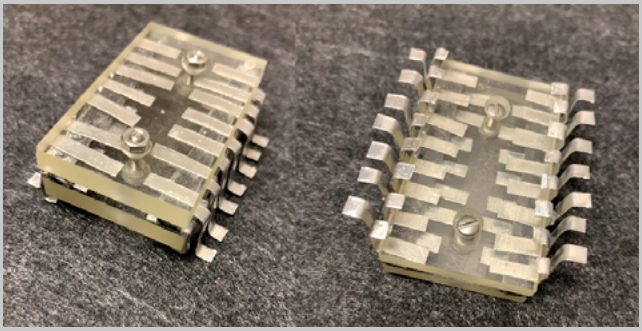

Figure S2: The original concept mocked-up in plexiglass and shim stock.

Fresh ideas don't come around often. We mostly work in a world of incremental improvement, with each successive generation stretching out from the previous one just a bit with a little more performance, or a little tighter spacing, or a little different material that provides that little bit more needed to solve the problem at hand. All of us in the research and development world stand on the shoulders of giants, adding our next little piece, adding a little bit more to the tower's height. But sometimes, an idea comes along that seems to change the scene—an idea that breathes life into a development team and gets them excited about what else might be possible. These are the ideas that bounce from person to person and take on a life of their own as everyone contributes and adds a little to it. And this is what had happened in Tianjin in the weeks and months before my visit.

We had been working as an organization to improve our innovation culture. We'd started by challenging ourselves to find more patentable ideas, and had made dramatic improvements, doubling, and then doubling again our output

from a base that was already respectable. But that effort didn't entirely scratch the itch. We still weren't dreaming about what could be. So, we started a new initiative, which I unimaginatively named "emerging technology." We set aside a modest budget (from money that I didn't have per se but thought I could squeeze in and still hit my targets) and told the worldwide team that we would fund interesting ideas to see where they led. The idea didn't have to be grandiose, nor did it have to succeed. The only requirement was that the idea could be tried out with relatively few dollars and relatively little time, and that it might be able to inspire a little excitement more broadly within the team.

I can't remember if it was the first year or the second of our "emerging technology" effort that this plexiglass super-QFP landed in my hands but, somewhere in the drive for innovation and creativity, the idea was born and generated an excitement we had not experienced for some time.

The basic idea was to combine the gull-wing leads of a QFP with the J-leads of a plastic leaded chip carrier (PLCC) in two interstitial tiers of leads extending from the package body. Such a configuration would provide a very dense array of leads—basically eliminating the spaces between the leads—and effectively gaining the full periphery of the package for use as I/O. Because both kinds of leads are inspectable, with the solder fillets of both exposed, it stood to reason that their combination would be inspectable as well. The challenge was that two tiers of leads in a QFP had never been done before, and it was not entirely clear how to create such a structure from a single lead frame, how to wire bond to it, or how to mold it. And, the lead frame's dam bar would have to be eliminated; therefore, there would likely be significant mold bleed that would inhibit wettability. Additionally, there didn't appear to be a way to form the leads in trim and form. Other than all those things, it seemed pretty straightforward.

The mere fact that they were able to enumerate all the challenges was a clear indication that the team had already given this thing considerable thought. My response: full speed ahead! Even if it didn't work, this was the kind of idea that could inspire many more.

As we set out on exploring this new idea, step one was to bring a few trusted tooling design partners on board. We quickly brought them under NDA and asked if they were up to a challenge. The immediate "yes" we received was testament to the power of a new idea. It generates energy and creativity on its own. But, in just about every case, after a few rounds of designs that didn't work, each partner reached the point of bewilderment as the scale of the challenge they had undertaken sank in. We knew that feeling well; it's a familiar place. Problems yield to effort, but the fount of effort comes from a deep confidence that the problem at hand can actually be solved. Over time, we became skilled in the art of coaching ourselves and our partners that approaching a challenge with confidence was a key element to overcoming it.

Step two was less crucial to engineering success, but still very important. Before we could really get out there and sell this new idea, it needed a name. There were many ideas, but none seemed to hit the mark. After a few trial balloons over several months, finally, the team on the ground made a sensible and descriptive proposal: dual-row QFP, or DuQFP for short. I had interjected myself into the naming process, and thoughtfully mulled over this new suggestion. But, no matter how hard I tried, I could not get myself past the idiomatic connection that DuQFP would somehow become "Duh!-QFP" in the minds of its hearers, and I vetoed the name. In frustration, the second-best name was then proposed, MaxQFP. It lacked specificity (other than maximizing the peripheral I/O on the package) but did convey the idea of newer and better. So, not having a better alternative, that became the name. It has grown on me over time. Recently, JEDEC has suggested the scintillating name of "H-PMFP-E" to the package. But, I still think MaxQFP has a nicer sound to it.

This article (including the **Sidebar/"Prequel"**) discusses the genesis of the MaxQFP package, which was intended to greatly increase I/O density while still meeting the demanding requirements for automotive applications. Once our team had developed the concept for the new package as described in the **Sidebar**, we generated some concept drawings and then set out to demonstrate feasibility of the idea (**Figure 1**). The immediate challenges tackled were molding and trim & form.

On the molding front, we had to carefully consider how to create the structure we had in mind. It required an interlocking "toothed" mold chase, with a self-alignment more accurate than any mold chase yet built. To minimize mold bleed around the leads, the tolerances of each "tooth" were critical, and the degree of interference fit between the lead and the chase needed to be carefully designed. After several design iterations, we had a design that worked pretty well in balancing the alignment and the fit of the leads into the mold chase, minimizing though not completely eliminating the dreaded mold bleed issue.

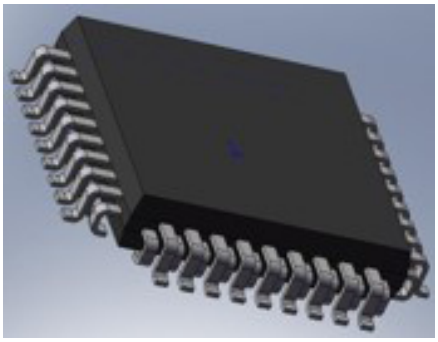

Figure 1: An early MaxQFP concept drawing.

For trim and form, we quickly came to the realization that there would be no way to accomplish the task in a standard three-stage forming process. It was simply too complex. Three stages had to become at least four, which meant customized equipment.

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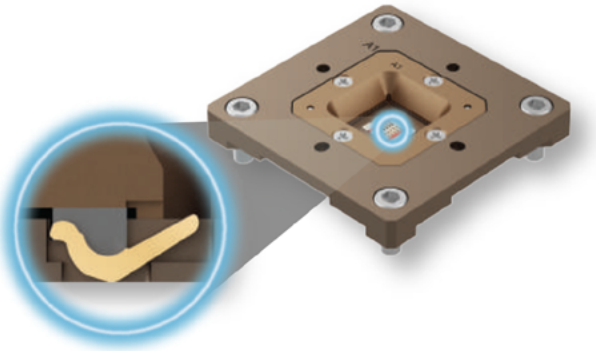

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Luckily, modern trim & form equipment is modular, and additional stages can be added readily, but already this new package was deviating a bit from our goal of complete re-use of standard QFP manufacturing equipment. Soon we had manual mold and trim & form tooling (**Figure 2**) and were able to build our first parts by hand.

Figure 2: The manual trim and form tool used to build the first MaxQFP samples by hand.

Securing internal support

The advantages of MaxQFP were clear. The technology saved significant board real estate (up to 55%), which meant a cost savings for users. For our businesses, it meant that we could deliver the same I/O in a smaller footprint, or more I/O in the same footprint than others, giving us an edge. For NXP manufacturing, it meant that five different QFP body sizes could be consolidated into two for MaxQFP—streamlining equipment change-overs and shipping container inventory. It also (mostly) re-used existing QFP equipment, so the benefits could be had for very little capital investment.

Even with such clear advantages, however, there was hesitancy to invest in the R&D required to make it happen. The first impediment was the risk. Could we really come up with cost-effective solutions to all the challenges? The second impediment was the eventual supply plan. Would we keep this as a proprietary, internally-manufactured package, or bring it to market in partnership with an outsourced semiconductor assembly and test (OSAT) supplier? These questions led to detailed development plans and presentations expanding in detail on the possible paths to solution for the various issues. These were intended to show that there were several possible ways to solve each of the key challenges and that the various options could be evaluated quickly and cheaply. The questions also led to research into the QFP and lead frame market in general. How fast was it growing? How large was the industry-wide volume? How much of that volume could be positively addressed by MaxQFP? How much did NXP stand to gain in licensing/royalties? The company fondly remembered the licensing and royalty revenue generated by Motorola's ball grid array (BGA) patents. Could this be repeated?

There was also another issue always lurking in the background: which business would fund the R&D? In NXP, packaging R&D is a central function that is funded by each of the businesses. This model ensures that the packaging products and technologies developed are those that are desired and will be used by the businesses. This is an effective way to ensure a high return on the dollars invested. But there is always a rubber-meets-the-road moment when everything hinges on one of the businesses agreeing to take the risk and fund the development effort. Once that first business makes the investment, then other businesses will typically jump in as fast followers, funding incremental expansions to address their own unique needs. So, for MaxQFP, we had reached the moment when the search began for the first business and first customer who could not live without this new package.

Securing a first product and customer

We knew that microcontrollers were a great fit for MaxQFP because they were on the lower-end of I/O counts, suitable for lead frame packages, but were increasingly hungry for more and more I/Os. We also knew that one of our key customers of these products was more receptive to new technology proposals than others. They were willing to take more risk if there was a technical or a business advantage. And so this customer and these products became our focus.

Step one was to think about MaxQFP from the perspective of that customer. What did they care about? Certainly, they would want to be assured that the package was reliable and capable—electrically, thermally, and mechanically. We gathered the data to demonstrate these. Next, as an automotive customer, certainly they would want to know that all the leads on the package were truly inspectable after soldering to the board. That problem the team in Tianjin had already solved. They had worked with a local board assembly line to try out MaxQFP's inspectability on their line. The result was positive. An added bonus: the board assembly line in question happened to be owned by our target customer!

The last issue that we thought would matter for our customer was that using MaxQFP should not require a more expensive board with finer line and space rules in order to route it. Even though the package was smaller with higher I/O density, it still had to be routable on the same board. Leveraging the expertise of our internal board design team in NXP, we unfortunately concluded that our original design for MaxQFP would not work. We had assumed that the outside dimensions of MaxQFP should exactly match those of a standard QFP of the same body size. But, when laid out on a board, it was not possible to get a trace between the board pads of the outer gull-wing leads and the inner J-leads without shrinking the trace widths and spacings. This meant that a higher cost board would be required. This was bad news and a big specification miss on our part. I was guilty of making dimensional equivalence to standard QFP a goal for MaxQFP. It seemed logical and intuitive to me. But now we were faced with the consequences of my intuitive decision-making. We would have to start over (i.e., re-working trim & form tooling) in order to make a package that could be routed on the same board as a standard QFP. The change required that the foot of the gull-wing lead be moved outward slightly and the J-lead moved inward slightly in order to accommodate routing (**Figure 3**). It was not a huge change, but was still a re-do that could have been avoided.

At last, with agreement from our business leads, we were ready to present MaxQFP to our target customer in one of our regular

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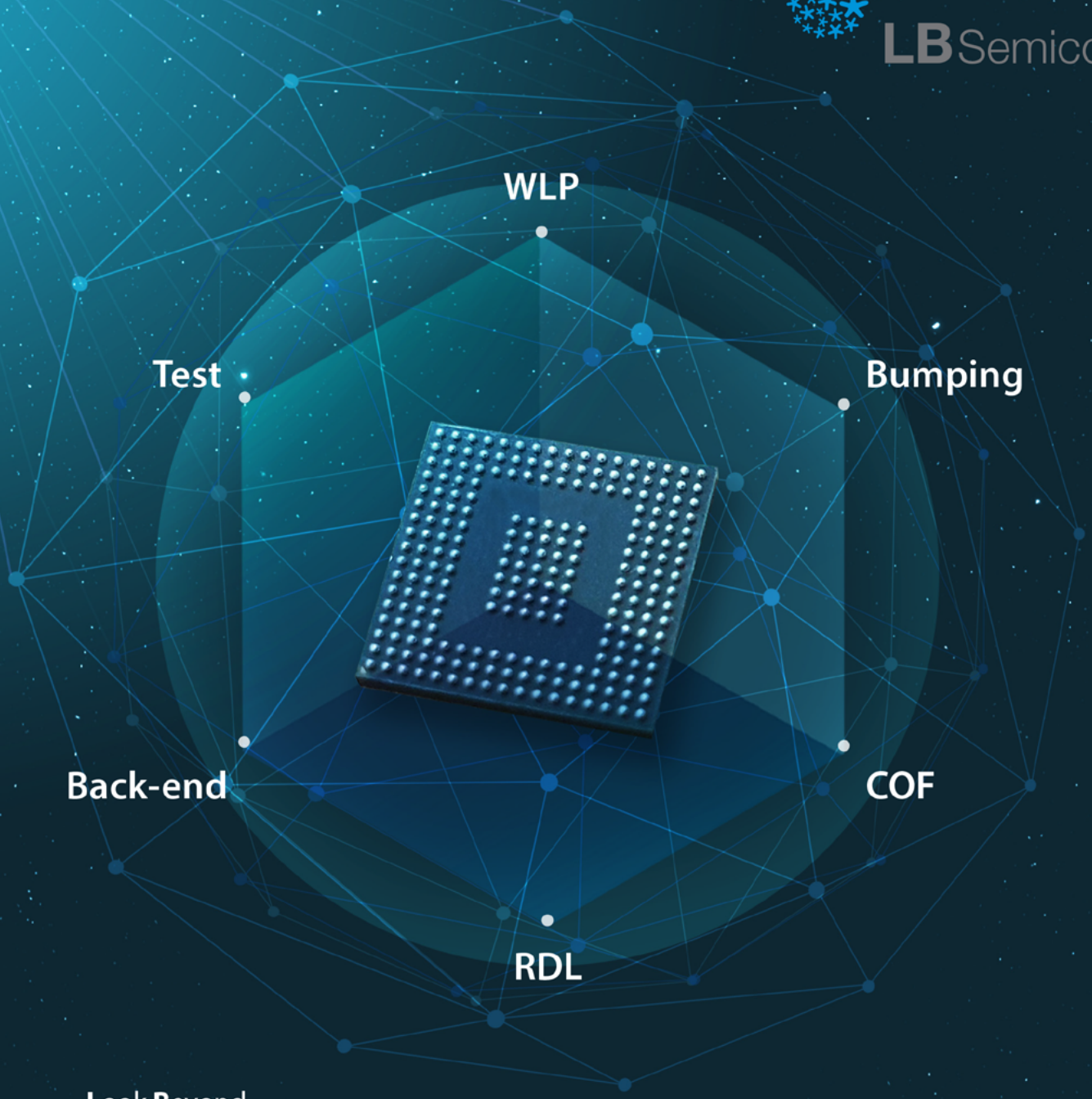

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technology engagements with them. The response was positive, and all the more satisfying when they learned that the positive inspection data was generated by their own factory! But they asked a pointed question as we described the routability of (the newly re-designed) MaxQFP: Had we done our routing analysis using their board rules? Unfortunately, the answer to that was no; we had used "industry low cost" board rules. For our customer, that was not good enough. They sent us their board rules and asked for a re-layout and re-assessment. We did it and the result was positive! With this, our target customer signaled support for taking on a new package, and our automotive microcontrollers business signaled support for investing in MaxQFP.

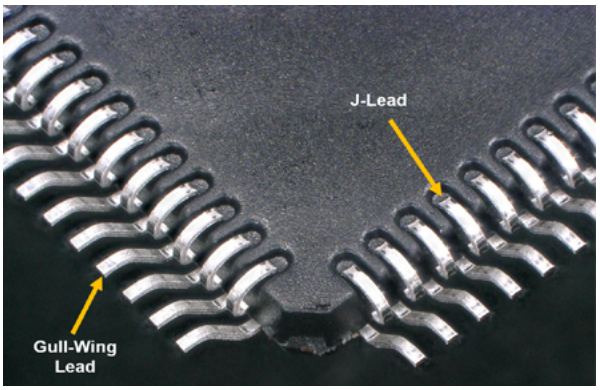

Figure 3: MaxQFP bottom view, showing the final spacing between J-lead and gull-wing leads.

More challenges

The mold bleed problem proved to be intractable. We were constrained on all sides. If we wanted the lead frame to easily align and seat into the toothed mold chase, then we needed a loose fit and got a lot of mold bleed. If we wanted to stop the mold bleed, then we needed an interference fit between the leads on the lead frame and teeth of the mold chase, and ended up with alignment issues and bent and stuck lead frames. Once we had that first design that mostly worked, we thought we were a few minor tweaks away from the full solution. But, there proved to be no happy medium between the extremes. Further, the QFP water jet deflashing process step was ineffective at removing the worst of the bleed. We were stuck.

We pulled a worldwide team together and started brainstorming. The best of the new ideas came out of Europe and the U.S., both from seasoned technical leaders who had seen more than their fair share of lead frame packaging issues. One idea amounted to a clever design change to the lead frame. The other involved new equipment. Of course, the design change was my preferred option because it would not add cost or require capital investment. But, in the end, the decision was that new equipment would be required to solve the problem. It worked, but it was another deviation from the goal of total re-use of standard QFP equipment and processes.

Another challenge arose: the latest quotes from the lead frame suppliers were too high. We brought in more suppliers in the hopes that more competition would result in lower quotations. But this did not work. It seemed like the lead frame suppliers were tired of all the nonstandard heavy design work required on seemingly one-off special lead frames that offered no clear return on their investment. Here we were able to re-use the QFP and lead frame market research and analysis we had already done. We flew to Japan along with our procurement team and walked the key suppliers through our analysis of the business opportunity. We showed them our productization plans and showed them the positive reactions from multiple customers. Suddenly the light bulb came on. A good idea can do that. Indeed, most of our suppliers commented at some point along the way that there had not been such a large change to the basic QFP in a long time. In the end, the quoted prices came down and the competition for the business fired up.

Around this time, we failed a routine check on wire bond reliability. Because of the unique way we were molding the package, the wire bonds actually displaced after the lead frame was loaded into the molding machine. This was the plan, and we thought the slight movement would pose no issues. We had even verified the reliability of our method in previous tests. But we were wrong, and the initial data were not predictive of future results. We carefully inspected the fails and thought through how they initiated and propagated. We held intensive brainstorming sessions and ultimately concluded that a clever redesign of the lead frame would eliminate the issue. At this point, we were years past the day of the plexiglass mock-up. Yet we were still making a fundamental change to the design to improve reliability performance.

Fine tuning

Some time after the lead frame redesign, I was again in Tianjin and again treated to an incredible presentation on MaxQFP. The problem was that, the more samples we built, the more we noticed that the tin-plated leads showed a bit of unexpected shininess on some parts. It was very subtle, and didn't appear on every unit, but once it was noticed, the team immediately began to investigate. The result of the investigation was the presentation, which included a full dynamic model (and resulting animation) of the entire trim & form process along with a transient mechanical analysis of the stresses on the tin plating. Sure enough, one die set in one stage of the forming was contacting the plating in an unexpected way and leaving a burnish mark. If small adjustments were made to the angle of the tooling die, the issue would be resolved. I looked at the affected parts in a microscope and could only just barely see the issue they were describing even when I knew what to look for. How did they even see the issue? How many hundreds of hours had they spent staring at every turn and bend of every lead on countless parts? And, once the issue was found, there had been months of daily meetings with the tooling designers, carefully discussing and modifying every micron of the key dimensions and tolerances.

Coplanarity and test socket design and shipping container design were similarly addressed and honed until we had robust solutions in place. This was despite initial reactions that what we were asking for couldn't be done. It turns out that careful engineering and design go a long way when coupled with some motivational coaching about having confidence.

Throughout the development process, we also gave significant attention to manufacturability, yield, and early engagement of the manufacturing assembly and test teams. Especially with

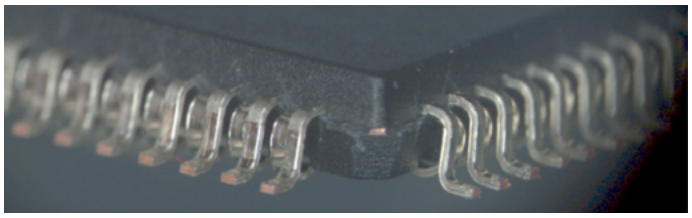

Figure 4: MaxQFP viewed from the corner edge.

a package aimed for automotive markets, the fine-tuning needs to be done ahead of time, not once production begins. Doing so requires focus and effort and attention to nuances, but makes a real difference in the end (**Figure 4**).

Summary

At long last an announcement was made: "EINDHOVEN, The Netherlands, Nov. 09, 2020 (GLOBE NEWSWIRE) -- NXP Semiconductors N.V. (NASDAQ: NXPI) today announced the S32K3 microcontroller (MCU) family, the newest addition to its S32K product line." In the announcement, we pointed out that NXP's S32K3 MCU contains a host of features, including advanced security and enablement for over-the-air updates of automotive software. But, tucked into the announcement was also the following sentence: "Plus, it is the first NXP MCU to offer the breakthrough MaxQFP package which reduces the footprint compared to a standard QFP by up to 55%."

That is the conclusion of this story: a single sentence within a larger product announcement. But it is a sentence that was enabled by years of engineering inspiration and perspiration. Indeed, from concept to announcement, MaxQFP proved to require a host of skills, from deep technical know-how, to market insight, to strong customer relationships, and even some political and negotiating savvy. The efforts spanned years and continents and required the expertise and engagement of many to make it a reality.

Volume manufacturing will begin in 2021.

Acknowledgements

The MaxQFP team in NXP spanned NXP's development, manufacturing, test, product, marketing, and sales teams (**Figure S1**). It is too large to fully list here. Much of the original inspiration came from Bai Zhigang and Yao Jinzhong in NXP's facility in Tianjin, China. They, along with Pang Xingshou, Xu Xuesong, Ma Chao, Li Jun, and Stephen Lee did much of the development heavy lifting. Productization was led by Katie Yu, Veer Dhandapani, Tu-Anh Tran, and Ed Sarrat.

Biography

Glenn G. Daves is VP, Package Innovation at NXP Semiconductors in Austin, TX. He is responsible for packaging R&D in support of NXP's full product portfolio. Prior to NXP, Glenn led packaging development at Freescale Semiconductor and IBM. He holds 27 U.S. patents and has degrees from Brown U., the U. of Illinois, and Alliance Theological Seminary. He serves on the board of trustees of Nyack College and on the National Leadership Council of World Vision U.S. Email: glenn.daves@nxp.com

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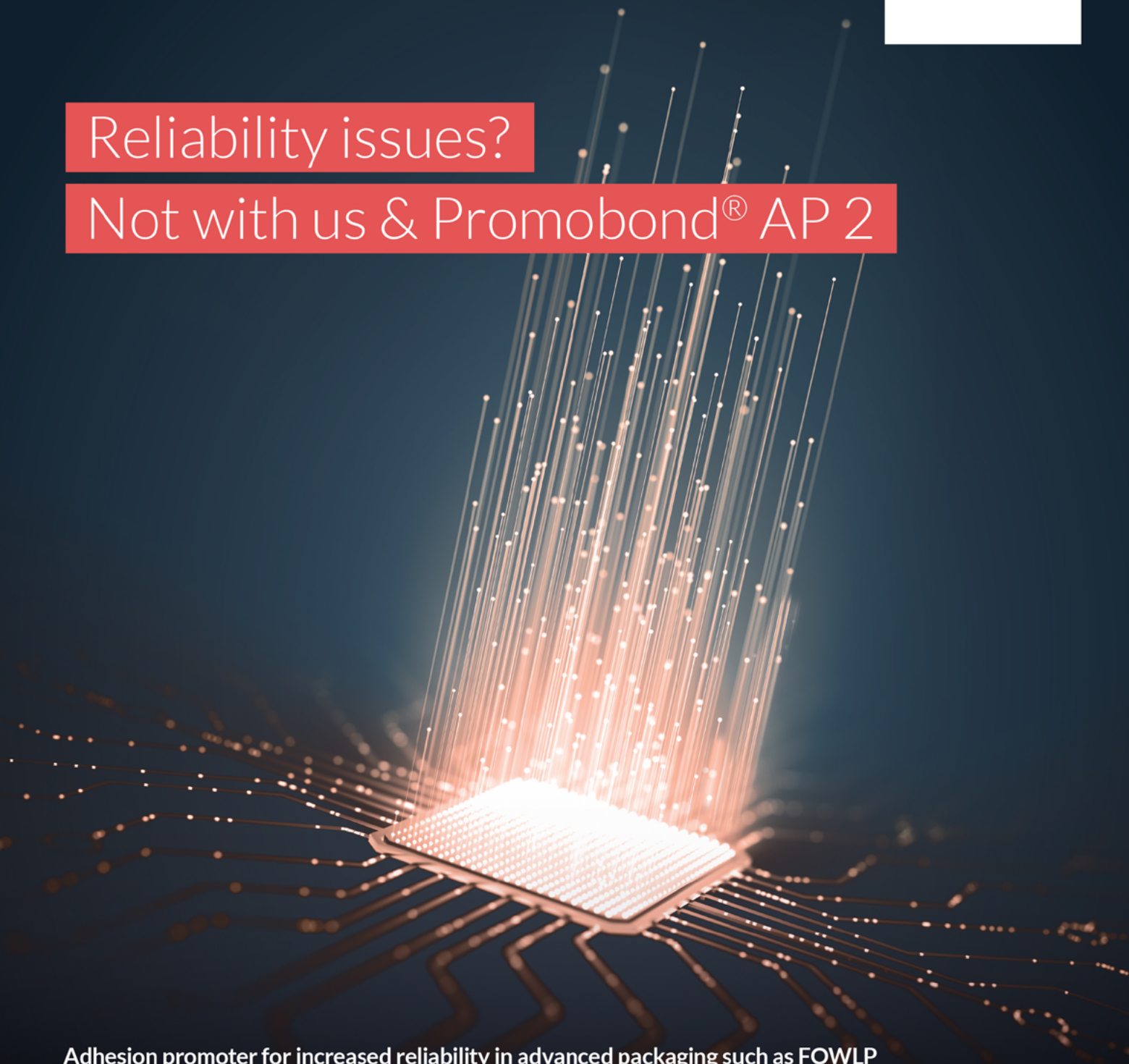

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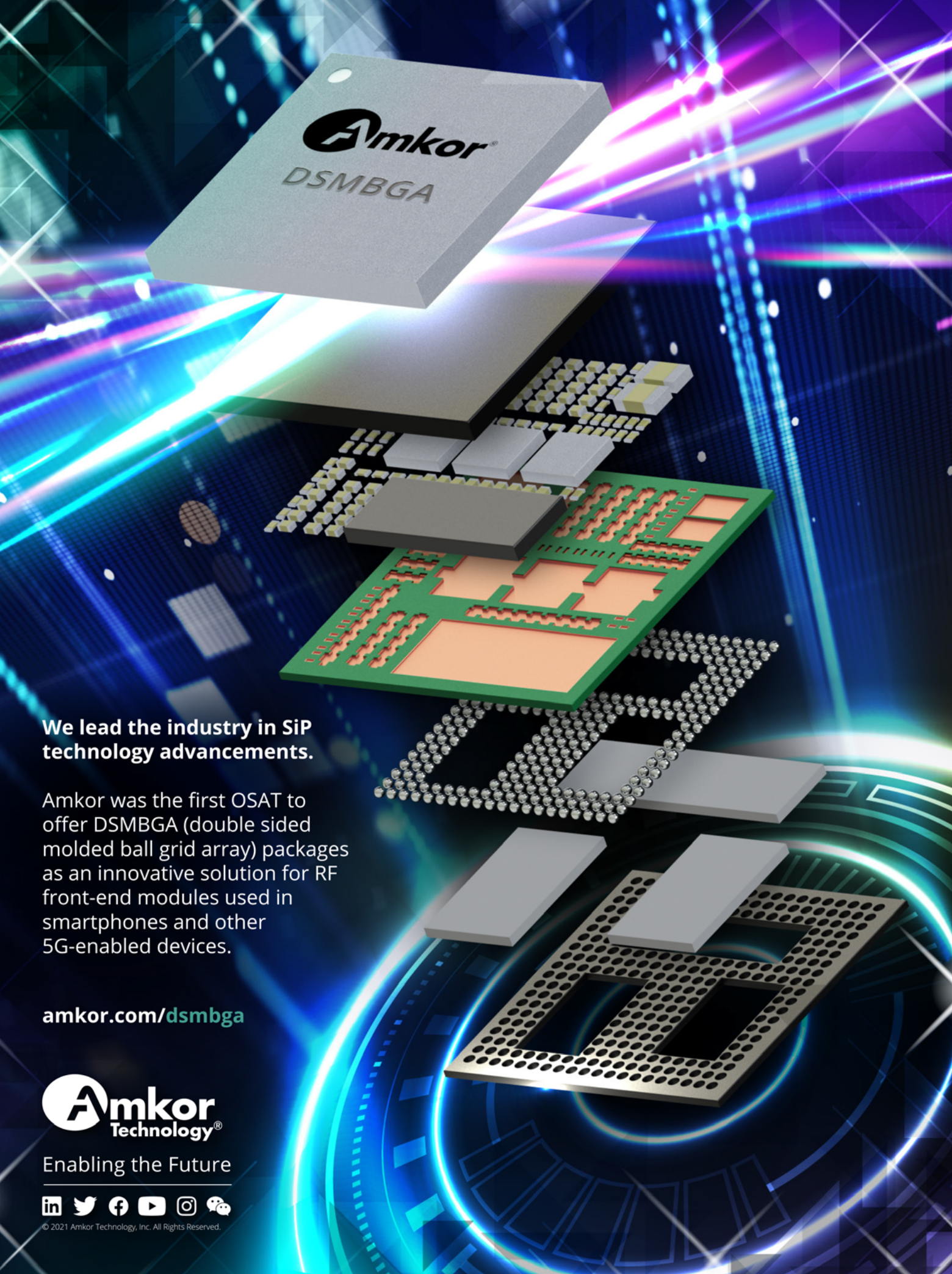

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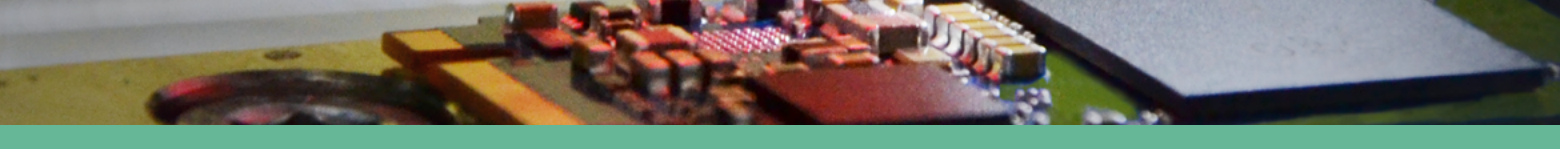


Laser-assisted rework of multi-die chip packages, 3D-stacks and µLEDs

By Matthias Fettke [PacTech – Packaging Technologies GmbH]

The demand for efficient repair processes and technologies for the recovery of semiconductor elements has never been higher than it is today. Even popular non-technical media such as *The Guardian, Fortune, Times*, etc., are reporting about the shortage of semiconductor components, which will last until 2023, and probably beyond. In particular, the automotive market has been affected. More and more small companies are being founded to deal with the increasing call for the recovery and rework of defective microchips and semiconductor packaging. Chip manufacturers focusing on the improvement of productivity and yield are also increasingly integrating entire repair production lines into their production process in order to achieve this.

In general, there is the necessity for repair technologies that enable cost-effective and sustainable reactivation of faulty semiconductor components. The primary goal is to avoid further damages to the device, and to reactivate the original functionality without any negative effects on quality and lifetime.

One of our areas of specialization is the development of new rework processes and machines for professional post-processing of defective semiconductor components, as well as complete assemblies. Since 1995, we have been developing laser-assisted assembly processes that meet the complex demands for minimally invasive mechanical and thermal interaction during desoldering, repairing and assembly. In [1] we reported about the laser-assisted repair opportunity for defective solder bumps at the wafer, chip and substrate levels, and explained the advantages of using a laser over other industry standard practices. In this article we are reporting about our laser-assisted debonding solution for removing, or separating flip chips, light emitting diodes (LEDs), and complete assemblies such as package on package (PoP), or system in package (SiP), from their carrier substrates.

The basic process sequence of our laser-assisted debonding solution is shown in **Figure 1**, and corresponds to an inverted flow of our laser-assisted bonding process described in [2]. The repair sequence can be split into three basic sections. In section one, the bond tool is positioned and placed onto the defective assembly under minimal vertical force. It is recommended to use flux in order to realize a homogeneous residual solder depot structure on the chip and the carrier substrate. Alternatively, a process gas chamber can also be used for substituting liquid flux materials—for example, formic or forming gas.

In a second process step, the laser is activated and melts the solder interface. In order to meet the requirements for a local limited interaction with minimal thermal load for the semiconductor device and the surrounding substrate, the laser wavelength and beam profile must match with the substrate material characteristics. For example, lasers in the near-infrared range (NIR) are particularly suitable for processing silicon chips because of their low absorption coefficients. The optical radiation is only partially absorbed and can penetrate directly into the interface of the bonding zone to interact thermally with the solder joints. In the third section, the thermomechanical separation step takes place by use of a highly dynamic vertical axis movement. Vacuum is used during this process to hold the chip properly to the bonding tool, the laser switches off within 1ms after the completion of the separation process, which can be detected by a rapid increase of the chip temperature. Depending on the application, either the defective chip is disposed of and a new chip is placed to repair the assembly, or the

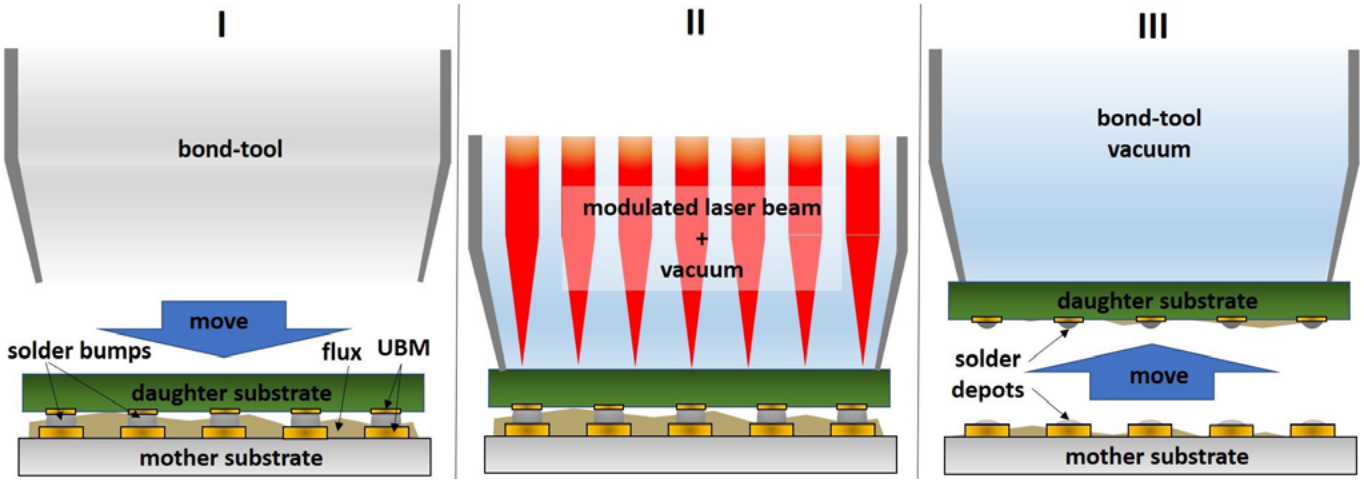
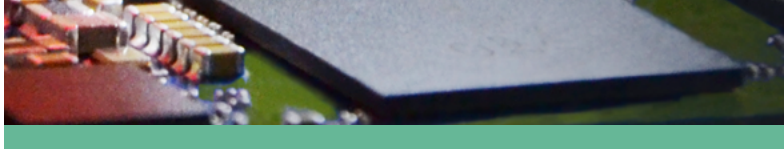


Figure 1: Schematic representation of PacTech's laser-assisted debonding process LAdB [1].



removed functional chip is populated with a new solder interface and integrated into a new package.

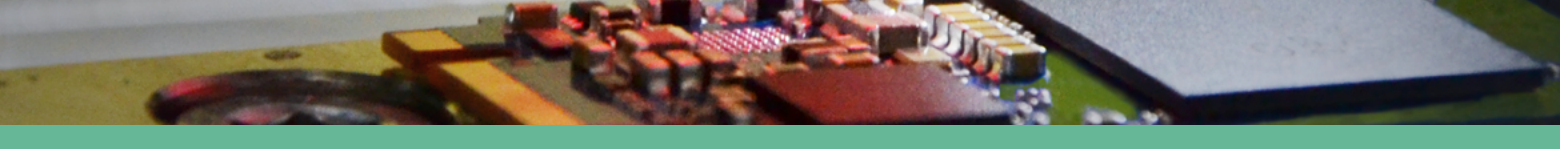
Because of the complexity of some substrate layer structures, the thermal feedback of an assembly is difficult to define before the process. In order to realize a safe and robust debonding and bonding process, the temperature is controlled by thermal sensors showing the highest measurement dynamics. The sensors are used to monitor the whole processing area and to control the laser almost instantaneously. An example of a thermal and temporal LAdB profile, as well as the modulated power density distribution for the removal of a 0.12mm x 14mm x 14mm Si chip populated with 250µm SAC305 solder bumps from a 3D chip stack, is shown in **Figure 2**.

The possibility of reusing the removed chip directly, or of placing a new chip on the assembly to be repaired, depends primarily on the quality of the remaining solder depots. Solder interfaces that do not require a new soldering process are advantageous because additional thermal loads are prevented and as a consequence, an increased lifetime of the assembly can be expected.

Using the laser-assisted process developed by PacTech for separating faulty semiconductor assemblies, an even split of the solder volume can be achieved for solder bump interfaces and Cu-pillar interconnections [3]. An example of the removal process of a defective PoP using LAdB is shown in **Figure 3**. Homogeneous solder depots showing height variations of ≤5% can be realized, which means the interface can be bonded afterwards without requiring any further preparation steps.

We have also developed a laser-assisted process for the subsequent homogenization of the solder depots in the event of a highly inhomogeneous residual solder structure on the contact surfaces of the removed microchips. The process of a laser-assisted transfer of solder material from a solid-state solder layer for mask-less formation of micro-solder depots is not only suitable for creating new solder deposits, but also for homogenization [3]. The process principle is as follows: 1) the chip with its contact structure is placed face-down on a solder-coated transfer substrate, for example a glass-wafer; then 2) a NIR laser is radiated onto the chip backside; and 3) the solder is liquefied in the interface between contact and solder in order to wet the contact metallization. A controlled vertical movement of the chip in and out of the solder material parallel to the laser reflow sequence enables the solder transfer and the forming of the solder bumps. Depending on the process dynamics and material thickness configuration of the solder layer, the solder volume to be transferred can be defined precisely. The correlation of initial solder layer thickness on the transfer substrate and the resulting solder height under constant process parameters for a Si-chip with 100µm octagonal ENIG pads and a Si-chip with a 50µm-large and 45µm-wide Cu pillar is shown in **Figure 4**.

The use of a laser tool for the described solder transfer process constitutes the superiority compared to conventional soldering or desoldering processes such as oven reflow, soldering iron, thermode bonding or debonding because of the very short thermal interaction times and the radiation selectivity. Moreover, the metallurgical characterization of the intermetallic phases, which were generated or reworked using a NIR laser, shows the advantages of the opto-thermal interaction explicitly. In previous work, it was shown by Kolbasow, et al. [4], that the intermetallic phases of a laser-generated ENIG SAC_305 interface grew by a factor of 3.5 less during a thermal



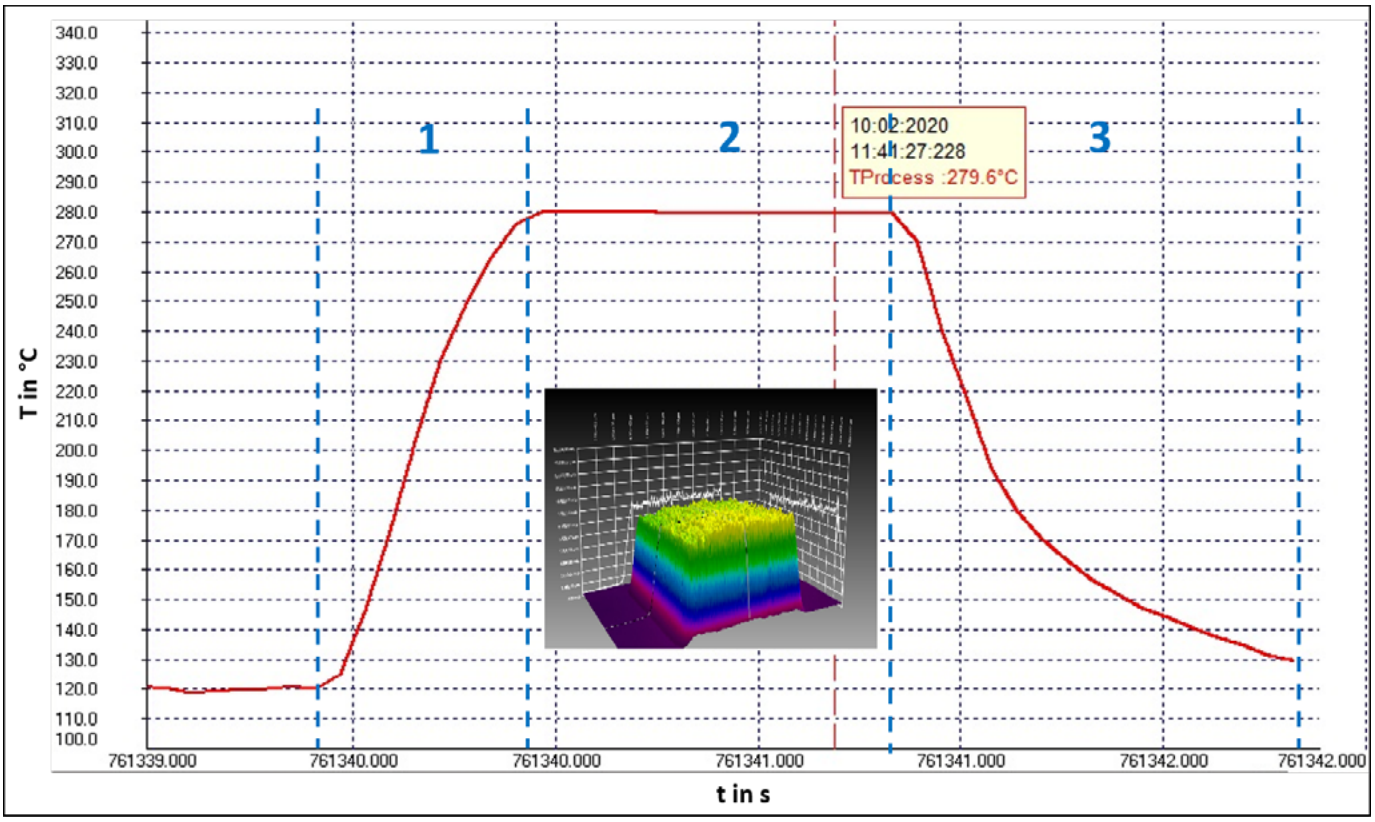


Figure 2: Thermal and temporal profile of the laser-assisted debonding process of a Si flip chip from a 3D package and the used spatial power distribution.

endurance test of 200 cycles (-40°C to 125°C, 35min cycle duration) compared to a thermode-generated interface with identical thermal bonding energies.

Special studies regarding the growth kinetic of intermetallic phases with repeated laser radiation exposure show that only minor changes in the geometric dimensions had occurred [2]. After 10 laser reflow steps, which correspond to five repair cycles of the same component, the phases have grown from 0.57 ± 0.37µm to 3.15 ± 0.22µm. The course of the measured values, which is shown in **Figure 5**, also indicates a saturation effect. The dimensions of the measured intermetallic phases of 2-3µm after 10 laser reflows, which already appear initially during a conventional reflow process, underline again the great advantage of using lasers. A structural change in the advantageous finger-like shape of the phases cannot be determined after the multiple laser-reflow cycles.

In addition to the metallurgical impact of the thermal loads during the repair process, the amount of inducing thermomechanical stress into a package is decisive for a successful repair. Especially for 3D packages, the underlying chip levels should not be affected by the repair process on the top level. On the one hand, the solder contacts could have an increased failure risk because of the introduction of additional mechanical stress, and on the other hand, the chip layers could collapse. Changing the stand-off during the repair step has a negative effect on the signal integrity of the module and consequently, it reduces the electrical performance. This problem can also be overcome by using a laser. Test series to remove several chip layers showed that no additional stress is induced in the 3D stack assembly [2]. The metrological proof could be provided by optical flatness measurements on the replaced chip layers. The measurement of the intermetallic phases, as well as the stand-off by means of a cross section analysis on the underlying chips, showed no changes compared to the initial state of the unprocessed sample. As a result, the presented LAdB process also shows a 3-dimensional selectivity of inducing the required thermal heat by optical radiation for the separation or bonding step.

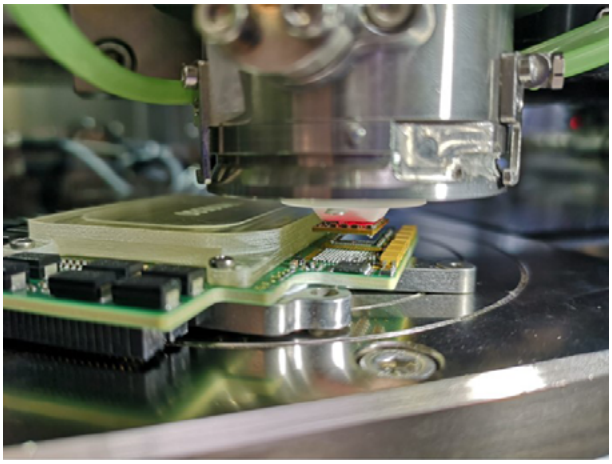


Figure 3: LAdB removal example of a defective PoP.

When selecting the repair method, another important aspect that needs to be considered is the layer integrity of the contact pad material of the semiconductor component to be repaired. With an increasing I/O count, the contact pad and pitch geometries are reduced, which increasingly

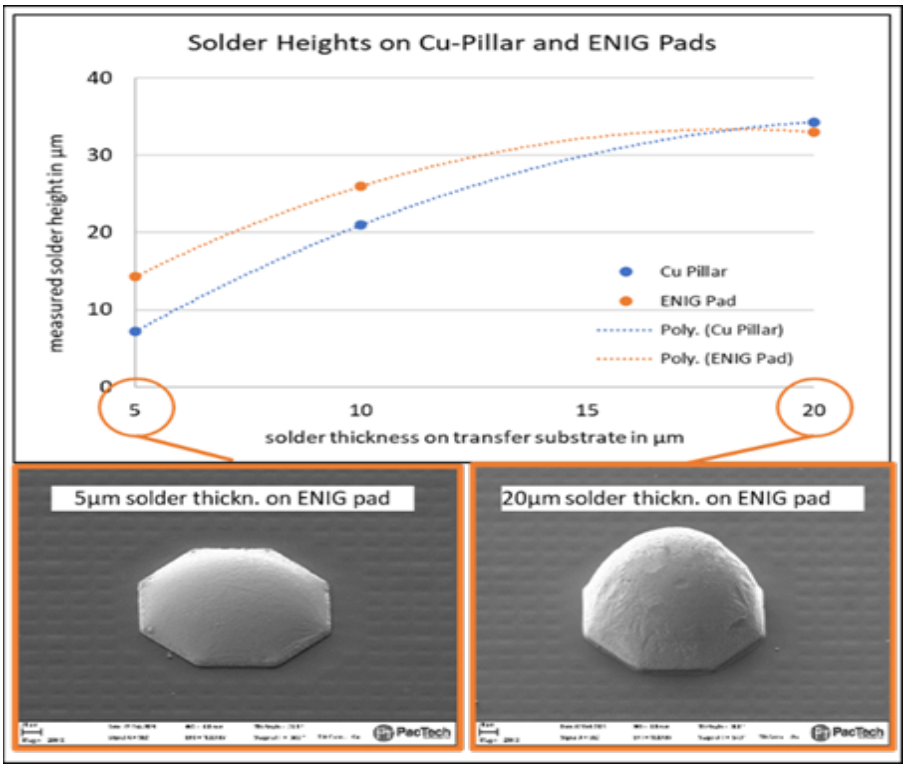


Figure 4: Correlation between the resulting solder cap height and the initial solder for a 5µm ENIG UBM and 45µm-high Cu pillar [3].

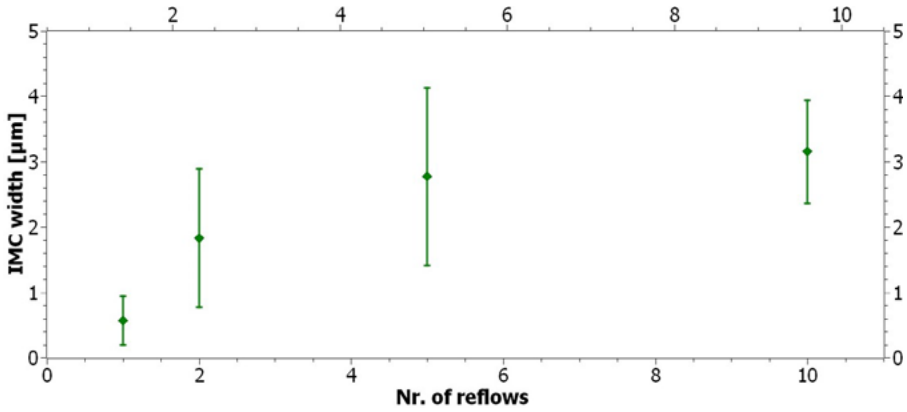


Figure 5: Progression of intermetallic compound (IMC) widths of a flip-chip device showing a 5µm ENIG pad SAC_305 solder interface after a given number of laser reflows [1].

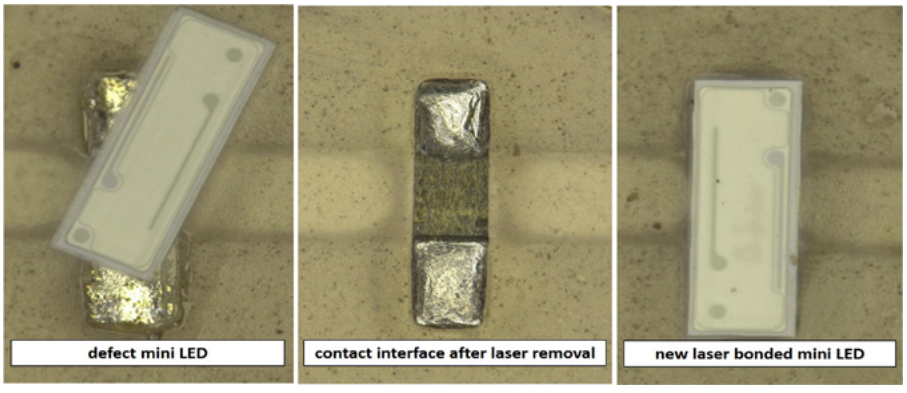
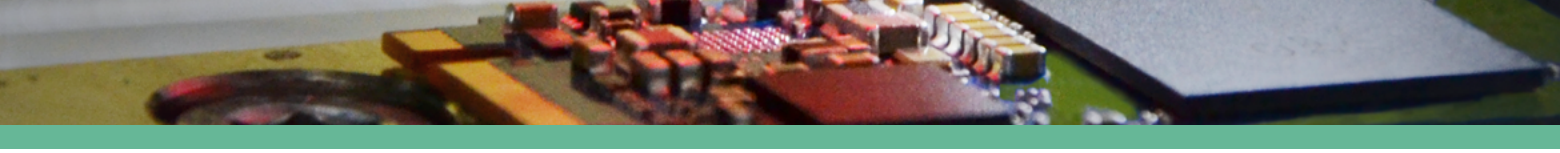


Figure 6: Result of a laser-assisted repair of a mini-LED pixel.

limits the choice of available plating processes. Quality problems, such as parasitic layer growth or partial coating because of passivation errors, increase accordingly. In combination with the cost pressure, layer structures are reduced, and layer thicknesses are minimized. The results are reduced material diffusion budgets that can be consumed during the reflow processes. This relationship is particularly present in the area of manufacturing displays with mini- and µ-LEDs. For a suitable rework of defective pixels and sub-pixels on a display, the process must show minimal thermal loads to limit diffusion effects by realizing in parallel a sufficient wetting and IMC formation. The combination of PacTech's laser-assisted bonding and debonding processes is also an ideal solution for this application.

Using suitable tooling and appropriate beam modulation, the laser is scaled to the size of a mini- or µ-LED. LEDs with an edge length of at least 40µm can be processed currently. The defective LEDs are removed without mechanical contact using a "step and repeat" method. The suction capillary is moved a few microns above the LED matrix and stops at the positions with defective components; the laser pulse is then activated and the LED is sucked out of the liquefied solder interface. The pulse times generally used are in the range of a few milliseconds, and therefore minimize diffusion processes within the contact structure. Thanks to the homogeneous splitting of the solder depots, a new LED can be placed directly afterwards. The solder depot of the replacement LED usually does not show an adapted solder volume to compensate the portion removed with the defective LED. Based on our experience, and due to the size of the small rectangular contact pad geometries in the range of 10µm to 30µm, the amount of solder material lost through the removal of the defective LED can be neglected.

For a repair process within the pixel matrix, the selectivity of the repair process is extremely important. Surrounding pixels should neither be thermally stressed, nor contaminated, by degassing effects. In particular, the beam modulation and the ability to control the laser reflow profile on the very small assemblies are the keys to success. An example for the removal of 150µm x 450µm mini-LEDs from an organic display panel is shown in **Figure 6**.



Summary

PacTech's laser-assisted bonding and debonding technologies are highly selective and thermally sensitive, and therefore are ideal methods for a sustainable, functional and economic rework of faulty semiconductor devices. The dynamics and characteristics of the laser-assisted process results in minimal thermal interaction with the soldered interface. The optical-thermal energy works primarily at the joint interface. Thermally-induced mechanical stress into the packages is negligible, and diffusion effects are limited to a minimum. Companies that want to implement a repair process for their state-of-the-art semiconductor products should consider the use of a laser.

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Biography

Matthias Fettke is a Business Unit Manager at PacTech – Packaging Technologies GmbH, Nauen, Germany. He is an expert on laser-assisted bonding technologies for semiconductor packages and electrostatic chucks used in the field of extreme ultraviolet (EUV) lithography. He holds a Master's degree in Laser- & Optotechnologies from the U. of Applied Science Ernst Abbe; email fettke@pactech.de

Enabling the 5G RF front-end module evolution with the DSMBGA package

By Curtis Zwenger [Amkor Technology, Inc.]

With the rise of 5G wireless technology, cellular frequency bands have increased considerably, requiring innovative solutions for the packaging of radio frequency (RF) front-end (RFFE) modules for smartphones and other 5G-enabled devices. Our double-sided molded ball grid array (DSMBGA) is an example of such solutions. Double-sided packaging technology has vastly increased the level of integration for RF front-end modules used in smartphones and other mobile devices. Common RF front-end modules consist of a low noise amplifier (LNA), power amplifier (PA), an RF switch, RF filters and duplexers.

Advanced system in package (SiP) design rules and DSMBGA technology enable the integration of additional components – such as antenna tuners and passive components – freeing up premium device motherboard real estate.

5G overview

5G is the fifth-generation technology standard that cellular phone companies began deploying worldwide in 2019. It includes three distinct classifications as noted below.

Low-band 5G Internet of Things (IoT). Low-band 5G uses a similar frequency range to 4G cellphones, 600–850MHz, delivering download speeds a little higher than 4G: 30–250Mbps. Low-band cell towers have a range and coverage area similar to 4G towers. In this range, packaging can be similar.

Mid-band 5G sub-6. Mid-band 5G sub-6 is an upgrade of 4G technology and involves incremental innovation in packaging. Operating at frequencies below 6GHz, the minor modifications of current RF packaging architectures result in minimal changes to the bill of materials (BOM).

5G millimeter Wave (mmWave). 5G mmWave technology is a disruptive innovation. The introduction of mmWave frequencies greater than 24GHz provides opportunities for the adoption of new packaging architectures and platforms. An example is the integration of the antenna into the package. To do this, major design changes and new low-loss materials are required.

5G technology enables advancements in products in all the major integrated circuit (IC) market segments, including: 1) Mobility; 2) IoT; 3) Automotive (advanced driver assistance systems (ADAS)); 4) High-performance computing (HPC)/networking; and 5) 5G network topologies. 5G is more than a new generation of technologies. It denotes a new era in which connectivity will become increasingly fluid and flexible. 5G networks will adapt to applications and performance and will be tailored precisely to the needs of the user.

For 5G, small cells are low-powered cellular radio access nodes that operate in licensed and unlicensed spectrums that have a range of 10 meters to a few kilometers. Small cells are critical to 5G networks because 5G radio waves cannot travel long distances due to 5G's higher frequencies [1].

In a technique called beamforming, the base station computer will continuously calculate the best route for radio waves to reach each wireless device and organize multiple antennas to work together as phased arrays to create beams of millimeter waves to reach the device [2].

Edge computing occurs by locating servers closer to the ultimate user. This distributed computing reduces latency and data traffic congestion. For the 5G ecosystem, cloud data centers provide the computing core. **Figure 1** shows the architecture of these mmWave-enabled changes.

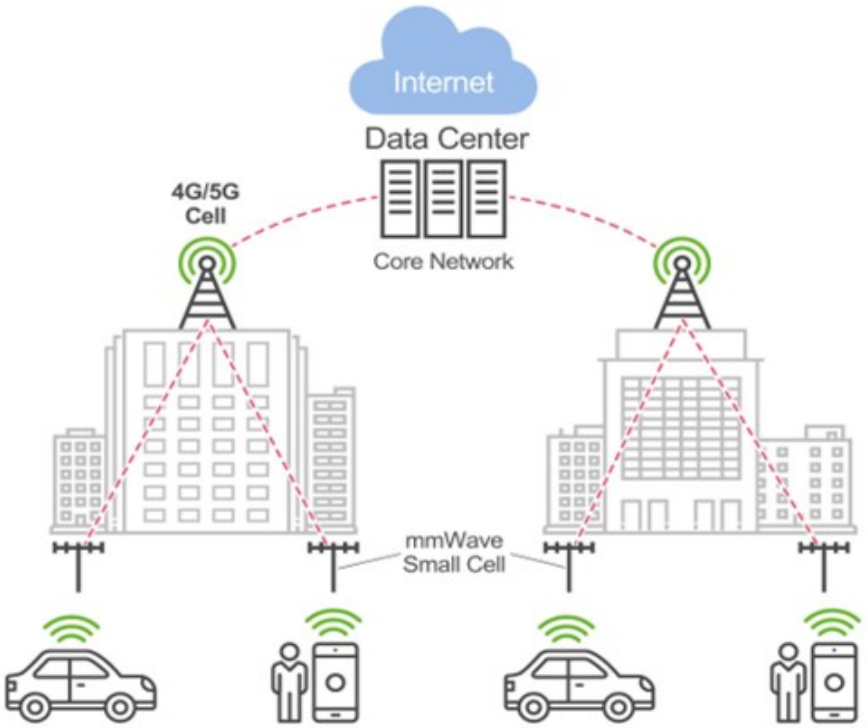

Figure 1: Small cells connected by beamforming technology link to data centers in 5G-enabled communications.

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Outlook on 5G market growth

By 2025, 5G networks are likely to cover one-third of the world's population. The impact on the mobile industry and its customers will be profound [1]. In addition, by 2026, 5G will have more than 3.5 billion subscriptions and will grow faster than 4G in most regions, per the Ericsson Mobility Report, June 2021 [3].

The advanced packaging market for 5G RFFEM is projected to reach US$2.3 billion by 2026, representing a 30% compound annual growth rate (CAGR) according to Yole Développement (Yole), SA, an industry consulting firm [4].

"There has been a change in frequencies with the arrival of 5G, adding frequency bands above 3GHz in FR1, and mmWave in FR2," according to Antoine Bonnabel, Technology & Market Analyst, RF Devices and Technology at Yole [5]. "This and the system-level trend have had a profound impact on both the number of components and the technology platforms on which they are built."

RF front-end integration history

The next sections discuss the challenges associated with 5G packaging along with the associated "toolbox" available to enable solutions.

5G IC packaging challenges. Advanced packaging for 5G systems requires the integration of RF, analog, and digital functions along with passives and other system components into a single module. Called heterogeneous integration (HI), the advanced SiP designs that accomplish this integration become more important for 5G because of several reasons, including:

a) Integration of antennas with transceiver ICs and other circuitry;
b) Addition of the sub-6GHz frequency range 1 (FR1) in the near-term through advances in packaging technologies;
c) New mmWave bands frequency range 2 (FR2) drive the integration of RF circuitry, including filters, diplexers, broadband power amplifiers and switches; and
d) The add-on modules to the existing RFFE require optimum miniaturization and component integration.

Further reduction of package size and losses requires close proximity of the transceiver and front-end module. Package-level integration of antennas or antenna in package (AiP) designs within the RF module as well as simultaneous modeling of heat dissipation to keep active components within acceptable thermal limits address these needs. The integration of power amplifiers with antenna arrays to address the design issues of size, cost and performance is a critical step. For package designers, the solution to these challenges incorporates multi-layer fabrication with fine-line features and precise layer-to-layer registration, advanced low-loss materials to reduce conductive losses and co-simulation of circuit, device, package and thermal performance.

The transition to 3D package integration at higher power levels and frequencies requires exceptional isolation between the various circuit blocks. In addition, for high-volume deployment, the manufacturing costs of high-power amplifiers and large antenna arrays in millions of base stations must be addressed [6].

5G RF packaging technology toolbox. To meet the technical demands for complex 5G RF front-end modules, advanced package integration techniques must be deployed. An advanced SiP technology toolbox addresses these demands. Figure 2 identifies the key attributes of an effective 5G technology toolbox.

The growing number of new frequencies, combined with the variety of multiplexing methods, significantly increases the complexity of the RF front-end. Integration using SiP methodology enables customers to design, tune and test RF sub-systems, allowing for a reduction in design iterations and an accelerated time-to-market.

Advanced SiP package integration is being utilized for 5G packaging for a myriad of reasons [7]:

- More flexibility for system designers – to mix and match IC technologies, optimize performance of each functional block and reduce cost.
- Faster time to market (compared to the system on chip (SoC) approach).
- Reduced motherboard complexity – by migrating signal routing complexity to the package substrate.
- Better performance – various ICs and passives placed close together means shorter line length, which reduces resistor (R), inductor (L) and capacitor (C) losses leading to higher signal integrity and lower power consumption.
- Lower system cost – compared to discrete packages, optimized SiP solutions result in overall system cost reduction.
- Small form factor – sub-system size is reduced by integrating multiple dies and passives into a single SiP.
- Improved reliability – better solder joint connections compared to discrete components assembled on a board/printed circuit board (PCB) result because the SiPs are molded, which alleviates stress in the joints.

The introduction of DSMBGA

To meet the high levels of integration required for 5G front-end modules, an extension of existing single-sided SiP package technologies was pursued. The combination of several enabling package features and assembly processes resulted in the double-sided molded ball grid array (DSMBGA) package. Package development began in 2018 and the first product was released to production in

Figure 2: An advanced RF packaging technology toolbox incorporates many different tools.

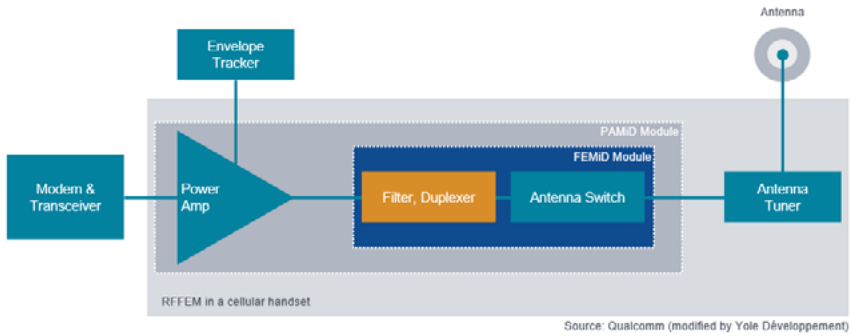

Figure 3: Integrated FEMiD and PA in the cellular handset PAMiD. IMAGE SOURCE: Yole Développement SA.

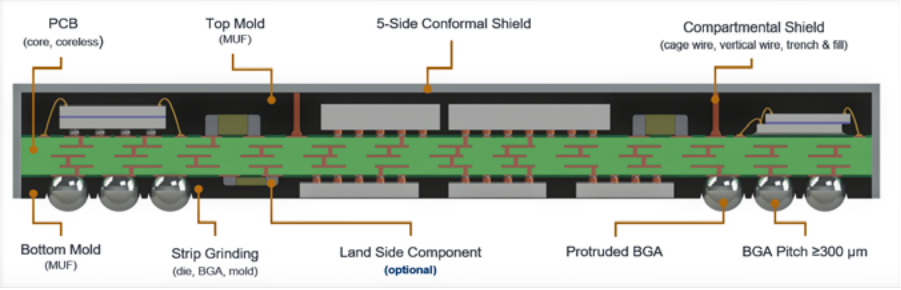

Figure 4: DSMBGA enabling technologies include both top and bottom molded underfill.

May 2020. **Figure 3** shows a typical block diagram of a DSMBGA front-end module with integrated duplexer (FEMiD) and a power amplifier module with integrated duplexer (PAMiD).

To provide the high level of integration noted above, several enabling technologies were combined to create a DSMBGA front-end module. By utilizing strip grinding, molded underfill (MUF) and double-sided molding, combined with industry-leading design rules, significant advancements in package size reduction were achieved. Other improvements include state-of-the-art conformal and compartmental shielding for electromagnetic interference (EMI) isolation and attenuation and implementation of in-line RF testing to deliver robust and cost-effective assembly technology. **Figure 4** illustrates the extensive technologies applied to create this RF front-end package with key performance attributes. With additional power amplification and filtering circuitry, the DSMBGA package improves signal integrity and reduces losses, resulting in improved Rx/Tx amplification, which translates into reduced system power requirements.

Advanced SiP design rules

A critical benchmark for any IC package technology is its design rules. For DSMBGA, the most advanced SiP design rules are applied to enable a highly integrated and small form factor package. **Figure 5** illustrates the typical SiP design rule attributes for package miniaturization. The minimum spacing for packages and components is directly related to the

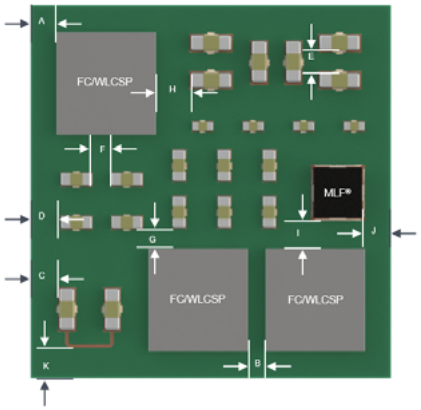

Figure 5: Typical SiP design rule attributes.

substrate supplier's process capability (e.g., for solder mask registration) coupled with the package/component physical tolerances, assembly process robustness and assembly materials used. For example, to prevent component tombstoning, the substrate bond pad geometry, solder paste stencil design and solder paste material all interact and must be optimized for high-volume manufacturing. Molded underfill (MUF) is commonly used to reduce process cost and decrease package spacing requirements. For a robust MUF process, the molding technique (e.g., compression vs. transfer molding), the mold process parameters (e.g., transfer time, pressure, temperature) and the mold compound material must be carefully chosen and optimized to ensure a high-yielding production process. Substrate solder mask thickness control and strategically located solder mask keep-out zones help ensure the molded underfill's process quality and the package's long-term reliability are as robust as possible.

Advanced design rules are rigorously validated through extensive process optimization, workmanship analysis and component/board-level reliability testing. **Figure 6** represents a typical advanced SiP test vehicle (TV) that

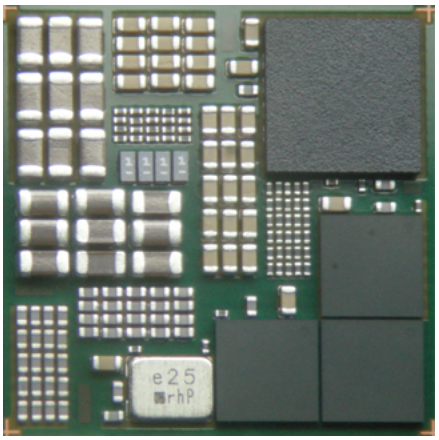

Figure 6: Example of an advanced SiP design rule validation test vehicle.

contains various sized flip-chip chip-scale packages (CSPs) and passive components. Solder mask-defined and non-solder mask-defined bond pads are incorporated into the TV to validate the effect on component/package stand-off, tombstoning and MUF performance. The assembled test vehicle is then subjected to the typical battery of component-level reliability tests, including high-temperature storage (HTS), preconditioning, temperature cycling (TC), and unbiased highly accelerated stress test (uHAST). Board-level reliability is also verified through temperature cycling and drop shock testing.

EMI shielding

Maintaining signal integrity within the DSMBGA package was essential to guarantee system performance. To minimize any electrical disturbances and resulting signal degradation in an IC and its surrounding circuitry, innovative electromagnetic interference/radio frequency interference (EMI/RFI) shielding needed to be integrated in the structure. **Figure 7** illustrates some of the EMI shielding techniques that have been incorporated into the DSMBGA package.

By leveraging industry-leading physical vapor deposition (PVD) tools, a thin metal stack-up is applied to the external surfaces of the package and coupled to an exposed ground plane in the DSMBGA's organic substrate. This conductive EMI coating is referred to as conformal shielding. By applying state-of-the-art masking techniques, a conformal shield can be applied to select areas of the package, if needed. Compartmental shielding is another EMI suppression technology utilized in the DSMBA package. These compartmental shielding techniques showcase adaptable designs for internal component-to-component shielding with in-package partitioning.

The original compartmental shielding technique was known as trench and fill. Laser ablation was used to create a trench within the mold compound to reveal ground connections on the underlying substrate. A conductive epoxy was dispensed in the trench to form an electrically conductive wall to create the EMI shield partitioning needed. More advanced compartmental shielding techniques have been developed that utilize sophisticated wire bond technologies to create a wire fence, a wire cage or a vertical wire structure within the molded package. Strip grind or laser ablation processes are used to reveal the encased wire. Conformal shielding is then applied to create a Faraday cage effect, whereby the wire structure serves to block electric fields and electromagnetic waves [8]. These EMI shielding structures are shown in **Figure 8**.

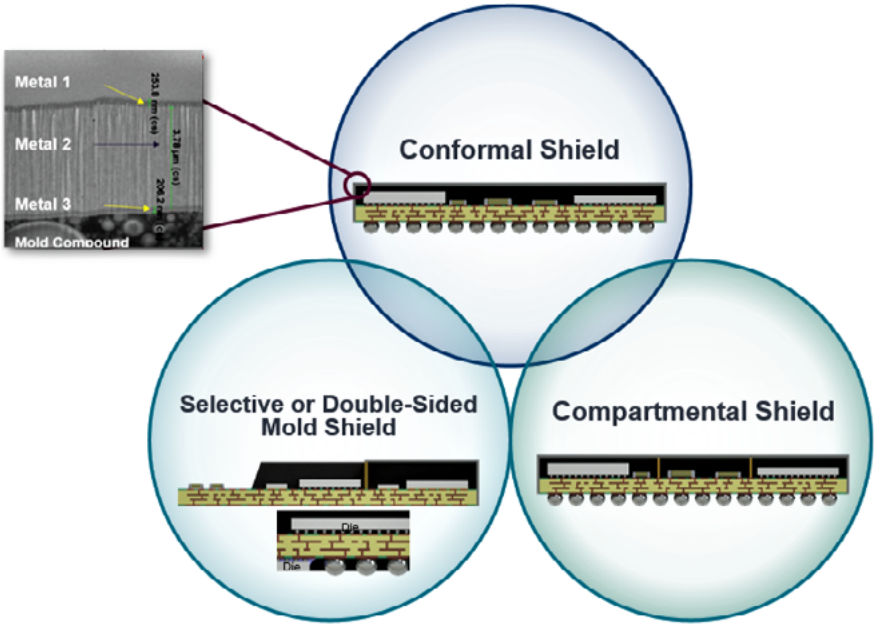

Figure 7: EMI/RFI shielding techniques minimize electrical disturbances in and near the package.

The conformal shielding technology requires strict controls to ensure process quality and yield. To enable this capability, PVD was adapted to package-level processing. **Figure 9** illustrates the PVD conformal shielding technique. A focused ion beam (FIB) cut is used to validate the metal stack thickness. For a 5-sided application, the PVD must be optimized to get accurate and repeatable top surface and sidewall coating to ensure effective EMI shielding. **Figure 9** also compares the EMI shielding effectiveness between an unshielded and a shielded package.

5G front-end module evolution and roadmap

Virtually any 5G RF system circuitry needing component-level integration can benefit from the size, cost and performance benefits offered by the DSMBGA package. The majority of DSMBGA packages being used today are for PAMiD products. Historically,

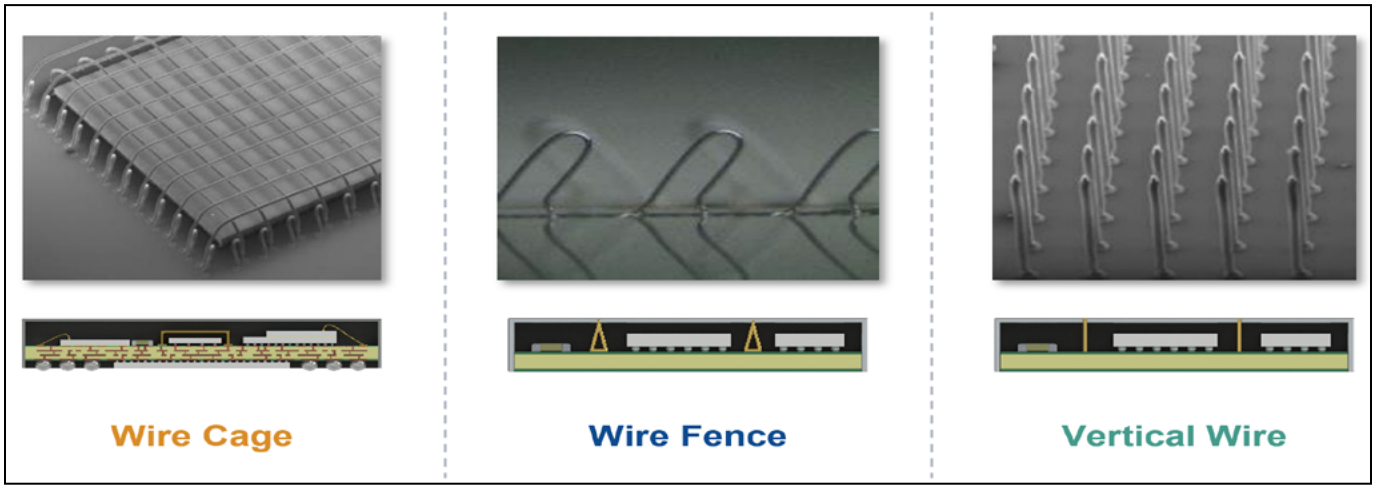

Figure 8: EMI shielding techniques for DSMBGA packages to achieve improved system performance.

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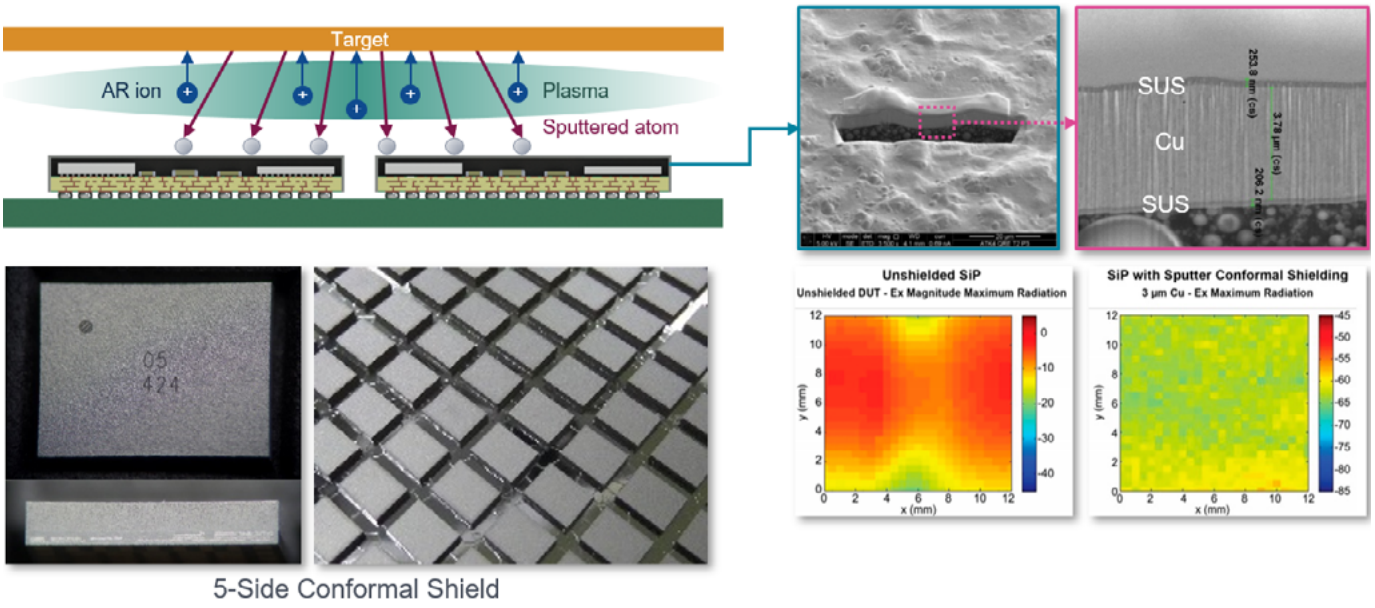

Figure 9: Conformal shielding and EMI radiation suppression effectiveness.

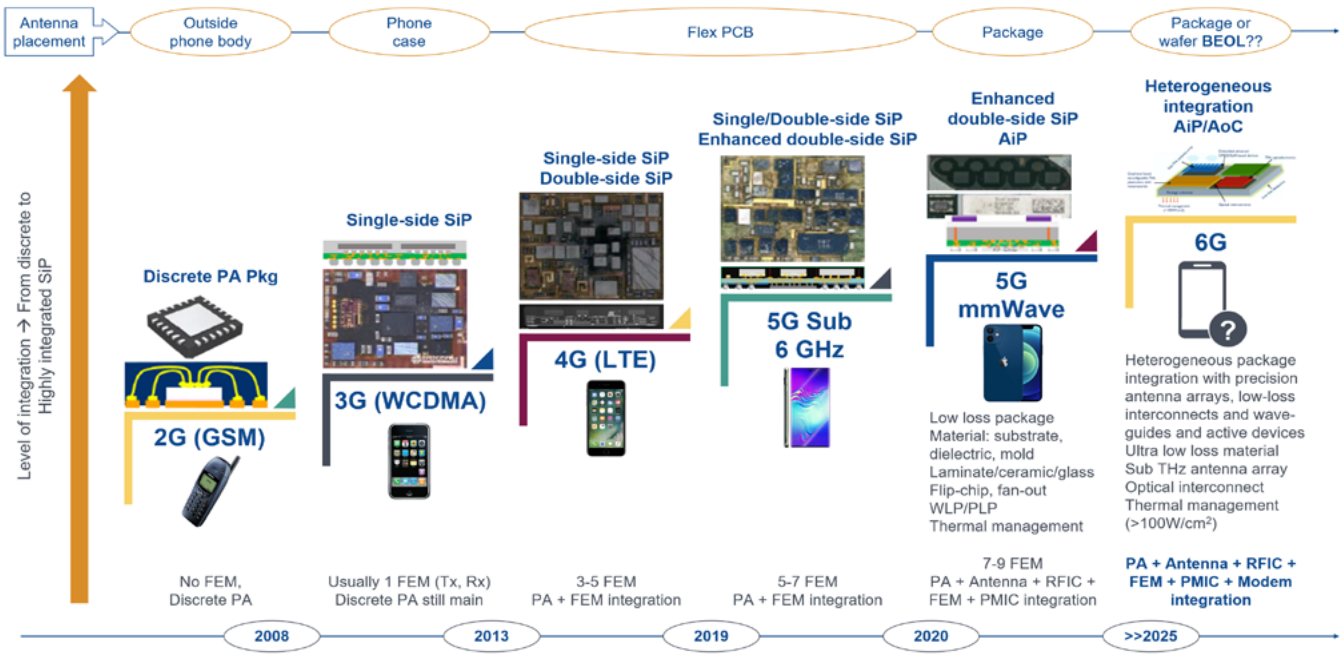

Figure 10: Packaging integration evolution and trends in smartphones. SOURCE: [9]

these products were served by single-sided SiP designs because the front-end module circuit complexity was not very demanding (e.g., for 3G applications).

With the advent of 4G LTE, medium- and high-band power amplification and filtering circuity became more demanding with up to five RF front-end modules required in a single handset. This led to the evolution of DSMBGA's predecessor, the DSBGA (double-sided BGA) package where ICs were mounted to the bottom of the structure. This allowed for significant module size reduction for the equivalent circuitry in a single-sided SiP structure. Then, with the evolution of the 5G cellular spectrum, front-end module complexity further increased with the introduction of ultra-wideband (UWB) circuitry.

To support these multiple bands, up to seven and nine front-end modules were required for 5G sub-6GHz and 5G mmWave applications, respectively. This resulted in the advent of the DSMBGA package. The latest version of the DSMBGA package is almost 50% smaller than the first mid-/high-band PAMiD. Thanks to innovations such as EMI shielding, flip-chip PA and double-sided molded BGA packaging, PAMiD suppliers managed to integrate the same system in a smaller footprint [9]. **Figure 10** illustrates the evolution and roadmap for RF front-end module integration for 5G smartphones. **Figure 11** shows an example 5G PAMiD product in a DSMBGA package.

Figure 11: Example of a PAMiD DSMBGA product showing layout a) (left) before MUF; b) (middle) top; and c) (right) bottom after MUF and EMI shielding.

Summary

The advanced SiP double-sided molded BGA platform has become an industry technology standard in this domain. Applying leading-edge design rules for 3D component placement and double-sided molding, together with conformal and compartmental shielding and in-line RF testing, delivers integration levels in a small form factor with high yield.

In addition to formidable SiP capacity and DSMBGA technology, an extensive toolset has been developed to maximize performance and to address the sophisticated packaging formats required to productize 5G applications. Some of these tools include AiP, substrate-embedded die, wafer-level SiP and a variety of RF shielding design options. This toolset, combined with expertise in RF module design, characterization and bench test, enables us to serve customers who want to outsource the challenges (including the substantial investment) associated with combining multiple ICs with advanced package assembly and test technologies for 5G networks.

As demand for packages that support 5G climbs, we are well underway with the successful implementation of DSMBGA technology having been in production for high-volume markets for more than a year.

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Biography

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Test interface solution for mmWave and AiP applications

By Collins Sun, Ryan Chen, Hayden Chen [WinWay Technology]

Since the launch of 5G new radio (NR) communication technology, many countries such as South Korea, China, and Japan have dedicated their initial 5G roll-out to the 3GPP-defined FR1 bands (4.1GHz to 7.1GHz). Other countries/regions, like the United States and the European Union, are focusing on the FR2 bands of mmWave frequencies (24.25GHz to 52.6GHz) [1]. The major reasons for choosing FR2 bands are the availability of spectrum and wider bandwidth operating at mmWave bands. The next-generation wireless networks are required to be faster, ultra-reliable and reactive. According to the 3GPP standard, 5G FR2 signals also have a wider synchronization signal block (SSB) – 28.8MHz and 57.6MHz, respectively – because these have subcarrier spacing up to 240kHz, compared to only 30kHz and 60kHz for FR1. FR2 signals also have more SSB beams. All 5G NR base stations transmit SSB beams through the transmission of a sector antenna, but FR2 radios use up to 64 beams, whereas FR1 radios are limited to a maximum of 8 beams. With 64 beams, the radio can transmit narrower beams with high power, which improves the efficiency of the radio and helps avoid interference because of high signal to noise ratio. However, more beams require decoding multiple bits from the physical broadcast channel (PBCH) in order to read out all 64 beam indexes in the correct location. Having more beams also requires a greater number of antenna elements in the antenna array, which enable better superposition of waves using beam-forming technology. This makes it difficult to do connected testing and verification of the radios, forcing the test engineer to do testing over-the-air (OTA). High-frequency signals have shorter wavelengths, which will cause higher propagation losses through both air and most physical objects. This means 5G FR2 service will require more radio density and strategic placement at the package and system levels. It will also make signals more vulnerable to interference, and requires test equipment with lower noise floors and faster sweep speeds in the mmWave bands.

Prior to discussing the test solution for antenna-in-package (AiP) and mmWave technology, it is helpful to consider why we need AiP in high-frequency design, instead of conventional external radio frequency (RF) circuit design. The answer is because the higher frequency results in a shorter wavelength with the roll-out of 5G FR2. On the other hand, the RF circuit design at mmWave frequencies considers the smaller form factor with more integration in the package technology, especially with respect to signal loss and cost tradeoffs. AiP is one option for achieving the goal of integration with shorter interconnections between the antenna and the RF chip (see **Figure 1**). Considering mmWave applications, signal loss becomes more critical at high frequencies and system design challenges increase rapidly in complexity. With AiP

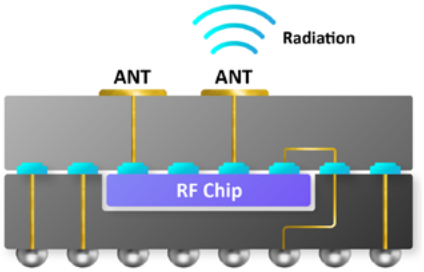


Figure 1: AiP cross section.

technology, the antenna is no longer a separate component within the wireless device, but is integrated into a system in package (SiP) with RF switches, filters, and amplifiers. A variety of AiP methodologies provide the required form factor and function for these applications and can include more than one antenna or an antenna array, such as flip-chip ball grid array (FCBGA)-based AiP, fan-out AiP, and AiP modules. The use of mmWave frequencies in AiP applications presents an extreme challenge for engineers in charge of characterization and validation of integrated designs who need to look for accurate OTA and coupling test solutions. The challenge is that engineers need to measure and validate package antenna performance by checking hundreds or thousands of data points in the test setup.

Test interface solutions

Under the complex package construction and electrical properties needed to handle the higher frequencies at 5G FR2, the data challenge noted above is especially true in mmWave applications. In such applications, the signals are especially vulnerable to interference given the higher amounts of path loss in transmission of conduction and radiation. This makes measurement accuracy and repeatability even more critical. Wavelengths in the mmWave range are extremely sensitive to cable and connector errors, so learning how to make multiple measurements per connection can help remove uncertainty from those measurements. In this article, we have shared valuable information on designing test interface solutions to help understand mmWave test solutions. Design considerations include mechanical design along with dielectric material selection, and socket solutions to fit the multiple test requirements, such as near/far-field defined in OTA, gain, error vector magnitude (EVM), etc. [2-5]. Therefore, the test interface in mmWave is a "multiphysics" problem, which is a term used to describe systems with mutual coupling interactions among physical fields.

To test the mmWave AiP package, the design with a manual lid that has a wide opening area and low dielectric loss material (see **Figure 2**) is one of the effective testing solutions used in the beginning stage of

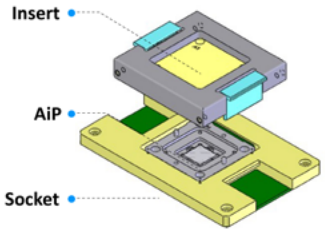
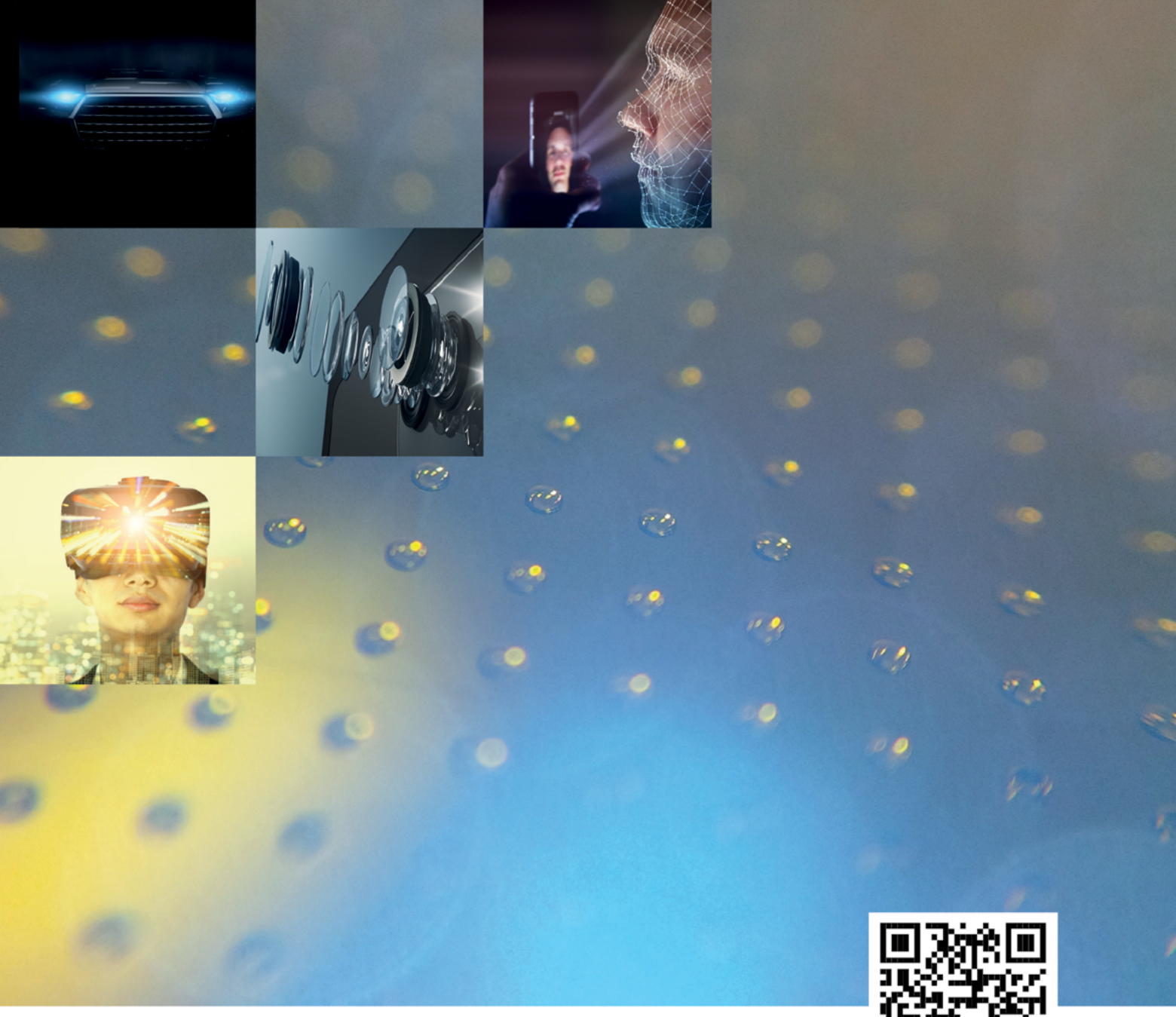


Figure 2: Manual lid socket design.



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Tensile Strength (MPa)	96 ~ 140	110 ~ 163	86 ~ 110	1.6 ~ 3.7
Elastic Modulus (MPa)	6480 ~ 10480	3923 ~ 4000	3447 ~ 5500	75 ~ 180
Electrical				
Dielectric Constant (Dk)	5.3 ~ 7.9	3.3 ~ 3.7	3.3 ~ 4.1	1.04 ~ 1.1
Loss Tangent (Df)	0.16 ~ 0.22	0.001 ~ 0.004	0.003 ~ 0.005	0.0002 ~ 0.015

Table 1: Material properties of the insert design.

device characterization. The purpose of lid design (both the wide opening and the low dielectric loss material) is to ensure the least amount of radiation loss when radiation propagates through the lid material. In the semiconductor test field, advanced engineering plastic materials are designed for the socket housing to position the spring probe and as an insert to press the device into the socket test position. The plastic materials in Table 1 need to be considered in order to fulfill the test considerations, such as mechanical strength, electrical loss, thermal stability, chemical consistency, and anti-statistic properties. However, dielectric constant and loss tangent are more important than the other parameters and are very sensitive with respect to how they affect the measurement results in mmWave AiP testing. By combining the horn antenna, sophisticated instruments and printed circuit board (PCB) layout, a simple OTA test setup for mmWave AiP can be made (Figure 3). In this setup, radiation and conducting measurements can be performed at different conditions. The purpose of these measurements is to check the influence of different inputs so that data correlation will help determine solutions for high-volume production. The open top lid design with the engineering plastic material and low-loss insert material are compared (Figure 4) to show the radiation propagation interference in spatial radiation distribution and gain measurement. The mechanical strength of the low-loss material is much worse than that of the engineering

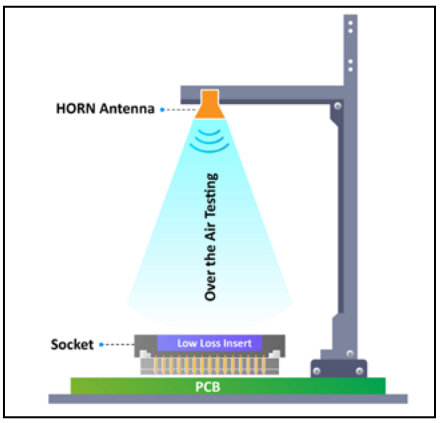

Figure 3: Antenna OTA testing schematic.

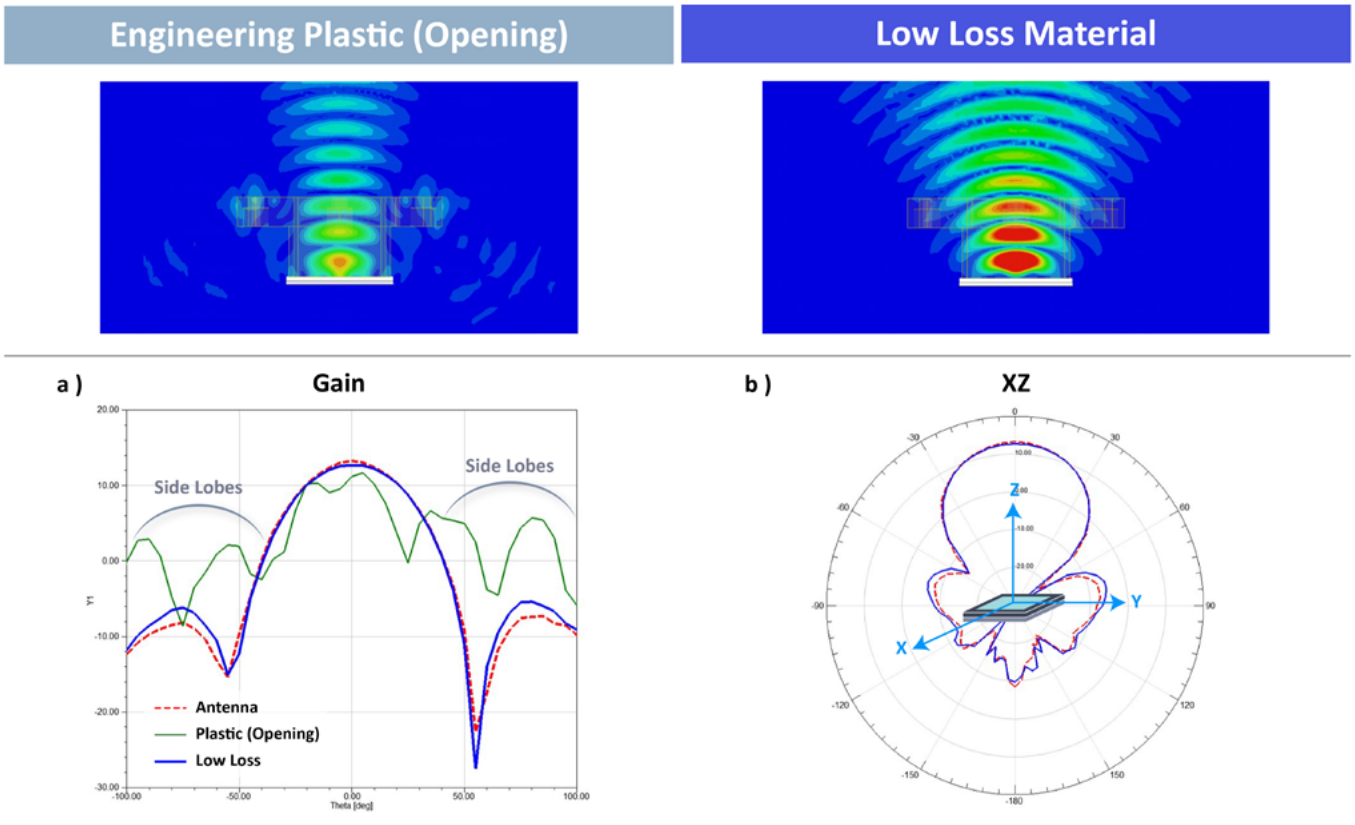

Figure 4: The influence of different materials on antenna radiation: a) effects on antenna gain; and b) effects on XZ radiation.

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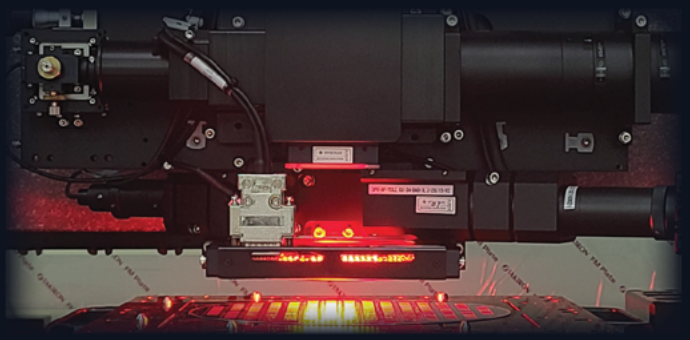

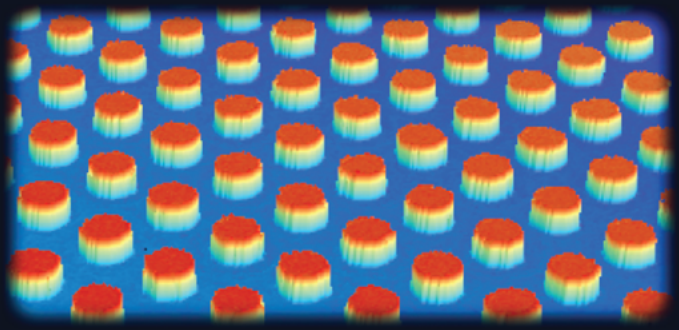

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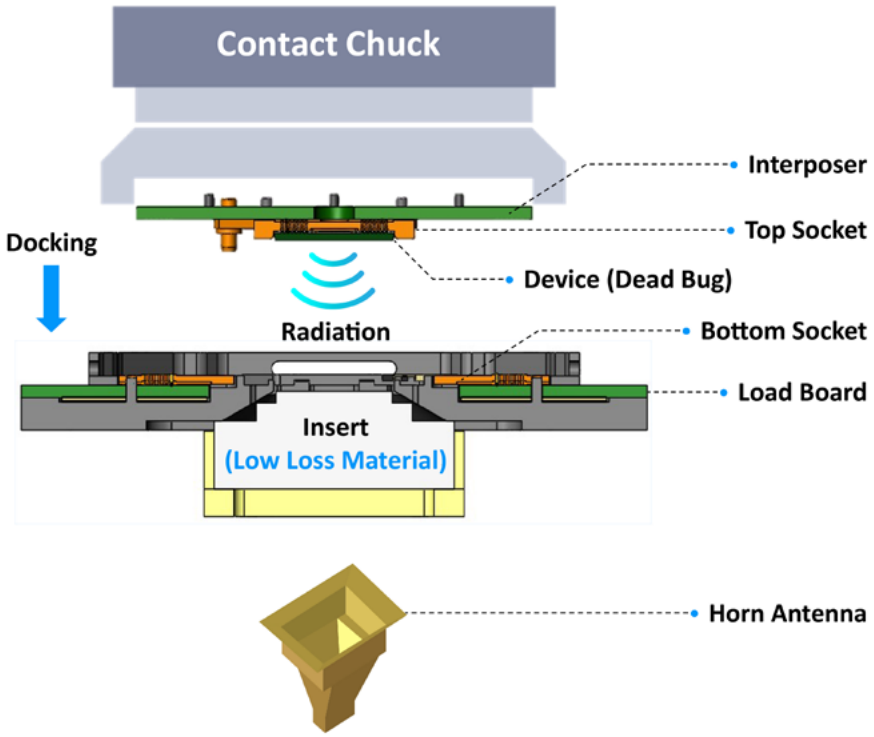

Figure 5: Production solution for AiP testing.

plastic material because of the porosity structure of the foam, which is a tradeoff for long-term operational reliability and high-frequency measurement accuracy. To better ensure a comprehensive design consideration, it is suggested that the design and material selection be simulated by using electromagnetic (EM) field characterization software and that there be a review of the frequency-dependent radiation distribution generated from the top side antenna array of the AiP package.

Regarding a production solution design: "dead bug" testing of the AiP package is one of the solutions for adapting the device's package format to the pick and place handlers. However, the bottom side of the package design needs to be considered as part of the keep out area for the nozzle (see **Figure 5**). The pros of conducting "dead bug" testing are that it will easily establish the OTA test environment rather than a test using a "live" device because the radiation is propagated down the entire side of the test setup. Therefore, the transmitted signal will not interfere with the mechanical pick and place parts of the handler. In general, all those parts are made of metal and will block or reflect the radiation. The cons of "dead bug" testing are that there is a longer trace loss through the top socket and interposer, and through the loopback to the bottom socket and load board. A customer's major concern with this kind of testing is how to control the loss or frequency shift within the expectation for these particular measurement environments. Therefore, 3D model co-simulation including the package, socket, and PCB will be preferred instead of cascading the individual component's S parameter both in signal integrity (SI) and power integrity (PI). As an example, **Figure 6** shows that impedance behavior will be significantly violated by different simulation setups, and the insertion and return loss will become uncontrollable if impedance is not matched. As previously mentioned, the difficulties and the different kinds of mmWave testing include the use of a smaller signal wavelength that will induce more realistic setup issues on the measurement results, such as pad size, via size and location, as well as manufacturing tolerance. The fine-tuning process in the simulation model compared with the actual manufacturing parts in the measurement system will be crucial to success of the process.

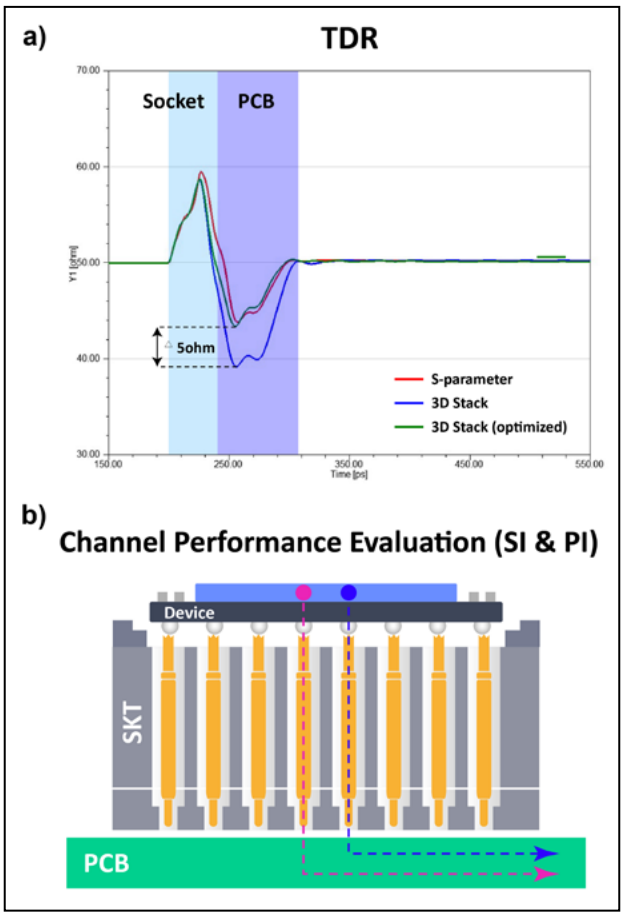

Figure 6: a) Channel simulation results between a 3D stack and an S-parameter cascade; b) Channel performance evaluation (SI and PI).

The housing and contact elements of the test socket are the most critical components in semiconductor testing. These components seriously influence the SI among electrical test interfaces. As previously noted, in the conduction and radiation setup, a mmWave test solution needs to seriously consider the fragile signal transmission path. In **Figure 7**, the experimental results of return losses up to 100GHz using various socket solutions were verified by using an impedance optimizing spring probe in 5G FR2 and automotive radar, and in a so-called RF socket, Brownie coaxial socket [6], and the recently launched contact pin solution, eHORN. How should one design a suitable mmWave test socket? The answer is highly dependent on the customer's requirements for the socket. Requirements include the package type and the preference for mass production hardware

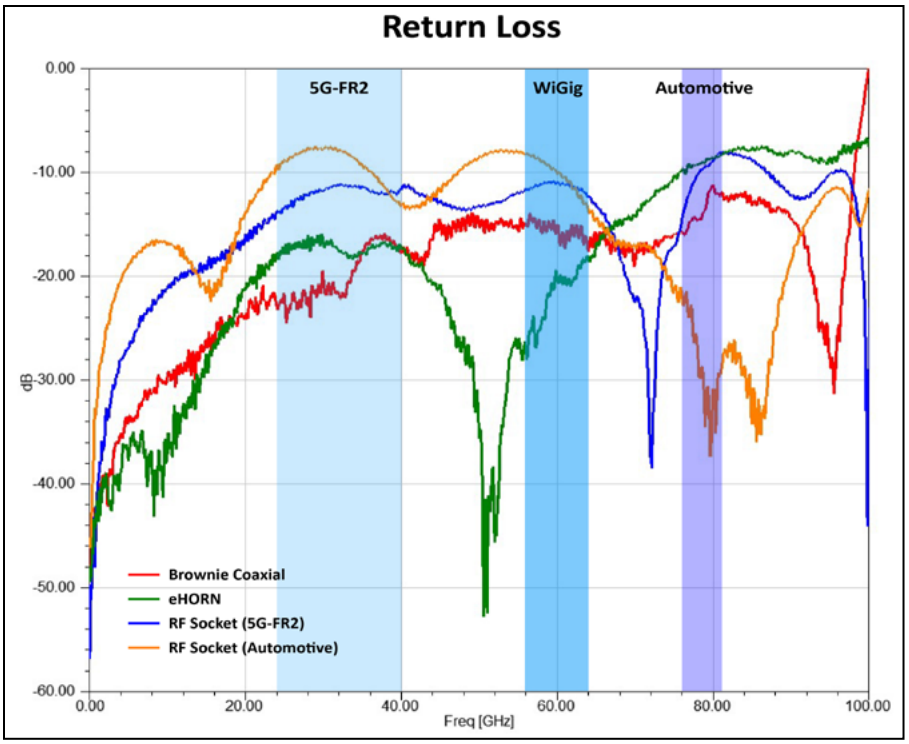

Figure 7: Measurement results for various mmWave socket solutions.

Socket Solution	RF Socket (5G-FR2)	RF Socket (Automotive)	eHORN	Brownie Coaxial
Contact Element	Spring Probe	Spring Probe	Contact pin	Spring Probe
Housing Material	Engineering Plastic	Engineering Plastic	Engineering Plastic	Metal
Pin Length (mm)	2.8	2.2	1.32	2.5
Travel (mm)	0.4	0.35	0.125	0.4
Avg. DC Resistance (mΩ)	< 60	< 60	< 20	< 85

Table 2: Socket solution comparison.

selection. Regarding the RF socket: the electrical performance can be adjusted based on the specific pin map that is used to achieve the target by changing design parameters, and for which the housing material is engineering plastic. In general, an extremely short probe (less than 2mm) is a preferred option for testing at high frequencies, but not necessary. Not only impedance matching in design, but also impedance matching with the test interface is a more realistic procedure. A Brownie coaxial socket is made by using a metal housing and can adjust the individual probe's impedance to optimize for the best performance. To deal with the quad flat no-leads (QFN) package, the newly developed contact element, eHORN, can support up to 80GHz and has the smallest scratch length (~0.08mm) on the device pad to satisfy the smaller package outline along with a shrinking pad size. The comparison table of socket solutions is listed in detail in Table 2.

Summary

The test interface solution for mmWave and AiP applications is a very hot topic because of the high-volume devices coming to market. What we have provided is a total test interface solution to analyze the radiation and conduction measurements including engineering and mass production solutions. By carefully checking the design factors for mmWave test requirements, mechanical considerations with proper material selection and socket solution need to be verified by 3D simulation before being released to manufacturing. The cascading S-parameter of each component is not suitable for high-speed and high-frequency applications. 3D simulation is a more straight forward way to analyze the properties from the component to the system level. At frequencies above 6GHz, channel simulation including package, socket, and PCB will be a recommended method to design the test solution, which creates a barrier for semiconductor test market entry.

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Biographies

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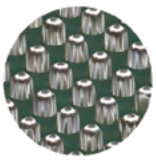
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From wafer to panel: the evolution of an electroplating tool for advanced packaging

By Richard Hollman, Jon Hander, Robert Moon [ASM-NEXX]

Panel processing is now firmly established in volume production for advanced packaging. Several of the top-tier semiconductor manufacturers, their outsourced semiconductor assembly and test suppliers (OSATS) and substrate suppliers, have panel process lines in operation. And, as evidenced by numerous presentations at this year's Electronic Components and Technology Conference (ECTC), the emphasis has shifted from tool set development to process optimization. In this article, we will view this progress using the example of electroplating, or ECD (electrochemical deposition), which has a central position in any advanced packaging process flow.

Background

Serious development activity directed at the use of panel substrates began before 2015 [1,2]. There were several market and technology forces driving this effort. With the slowdown in Moore's law (i.e., constantly increasing integration on a single chip), this has focused greater attention on heterogeneous integration, or the integration of several dies produced by different processes in the same package. The introduction of 5G frequency bands for mobile applications adds at least two different pressures to the mix: greater integration of radio frequency (RF) components within the same package as logic and memory, and the tremendous sensing and data infrastructure required to realize the full potential of 5G for the Internet of Things (IoT), driverless vehicles, and other applications. The increasing reliance on online communications during the pandemic accelerated these trends and provided added motivation to make panel processing a reality.

In packaging for mobile devices, overall size remains a critical factor, but for the infrastructure, packaging with increasingly large substrate areas turns out to be advantageous. Interposer dimensions of 100mm or larger are routinely reported, and this presents a problem for fan-out processing using 300mm round substrates (i.e., reconstituted wafers), as illustrated in **Figure 1**. In this example, only 6 such devices can fit on a 300mm wafer, while a 500 x 515mm panel could accommodate 40. And, while a 450mm wafer would have over 61% of the area of the panel in this example, only 16 of these devices could be fabricated on it.

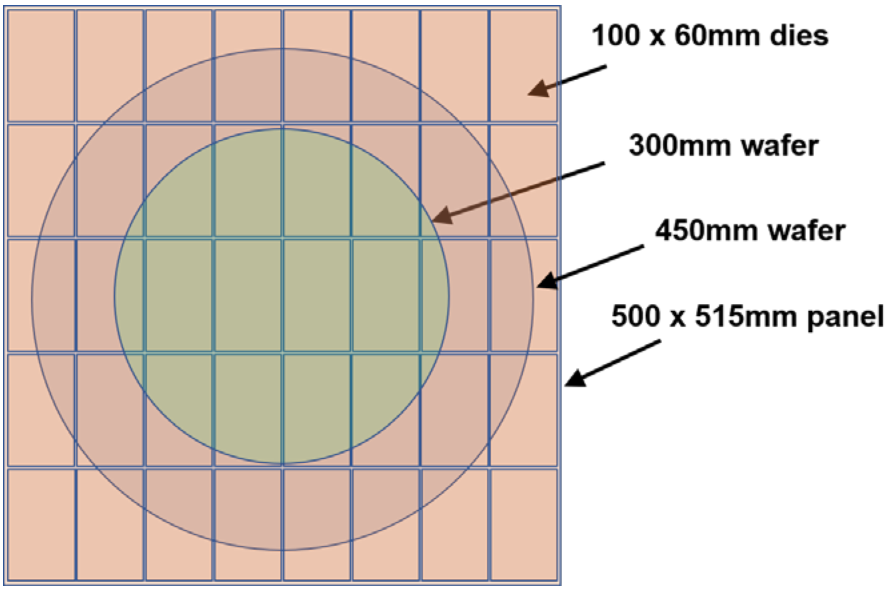

Figure 1: Layout of large dies on a 300mm wafer and on a 450mm wafer vs. a 500 x 515mm panel.

As recently as 2015, there was still interest in developing 450mm wafer processes as an alternative to panel substrates. Either 450mm round substrates, or larger rectangular substrates, would require a new set of process tools. But in the case of rectangular panels, there was a head start: there were already existing tool sets from printed circuit board (PCB) manufacturing and flat panel display manufacturing.

The process requirements for advanced packaging are generally more stringent than for either PCB manufacturing or flat panel displays. Minimum feature sizes are considerably smaller (2µm or less compared with 25µm for the most advanced PCB processes). With reduced feature size comes a greater need for particle control and process control in general. Advanced packaging is carried out in cleanrooms that are less restrictive than front-end wafer fabs, but considerably more restrictive than the typical PCB process line. So, not all existing process tools would be compatible with the advanced packaging manufacturing environment, and for some process steps a new category of process tools was required.

Example: ECD

Electrochemical deposition (ECD), or electroplating, has a central position in all advanced packaging process flows (**Figure 2**). With a broad spectrum of metal deposition processes available,

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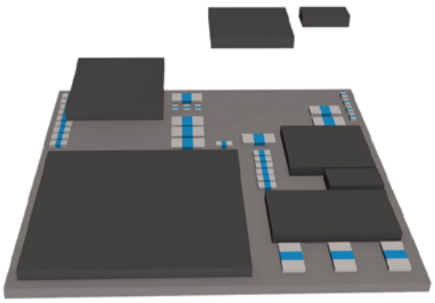

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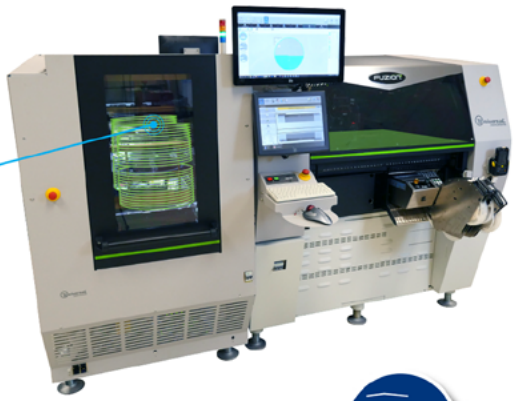

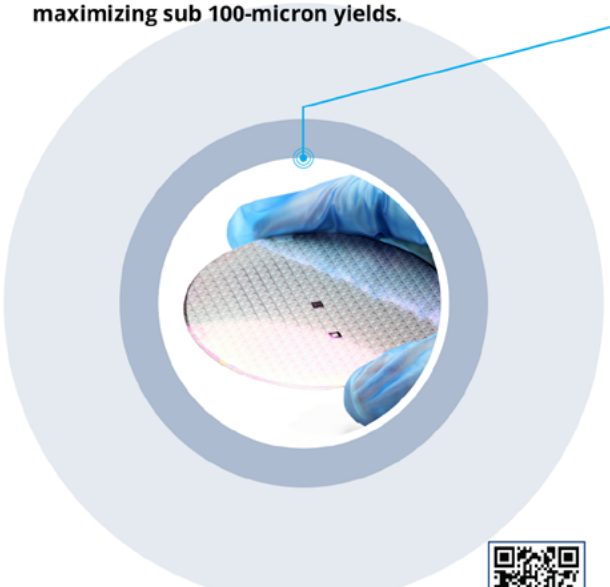

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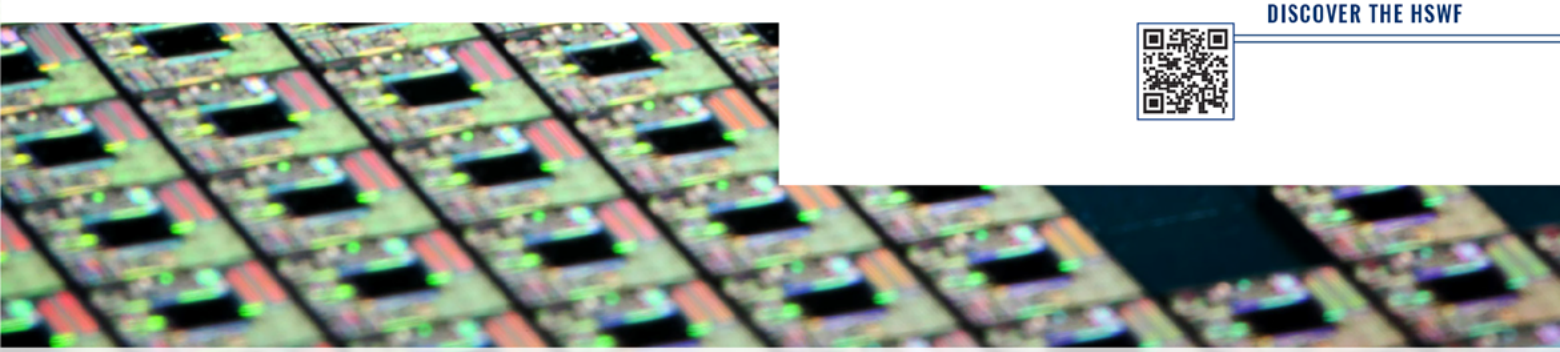

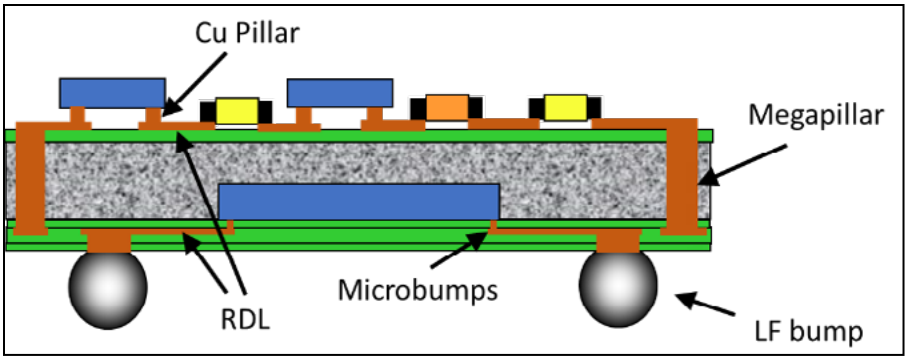

Figure 2: Electroplated features in a fanout architecture.

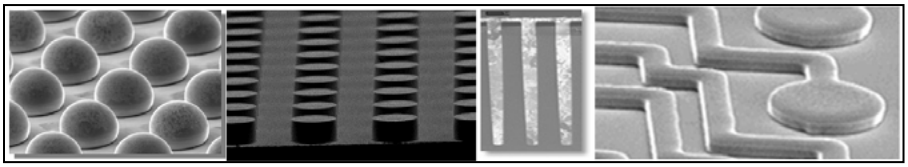

Figure 3: Typical device features fabricated by ECD: C4 bump, Cu pillar, TSV, RDL.

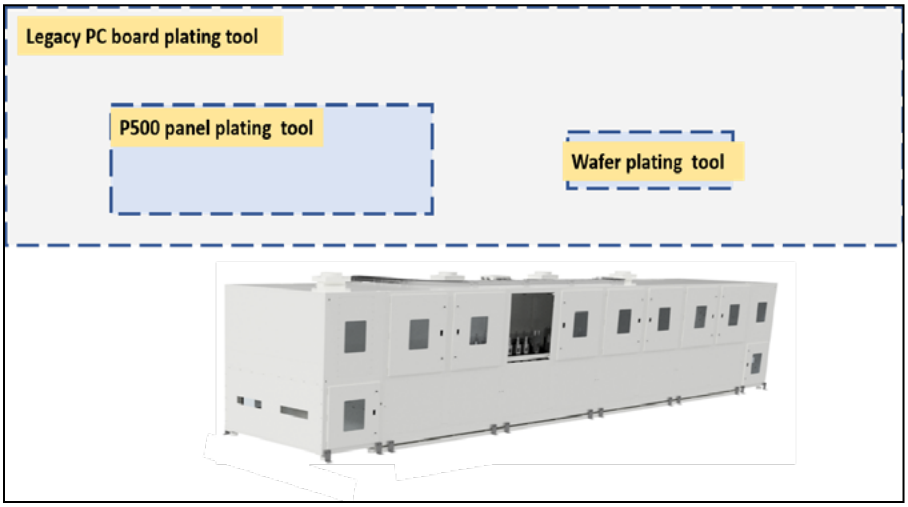

Figure 4: Floor outlines of P300 and P500 plating tools and a VCP legacy PCB plating tool.

ECD remains the method of choice for layers thicker than a few tenths of a micron, and where high throughput and tight control of deposited metal properties are necessary. For manufacturing, it has the advantages of fast deposition rate, no need for vacuum, ambient temperature or only slightly above, and the availability of numerous process variables allowing control of metal properties such as roughness and stress.

ECD is used in advanced packaging for depositing a variety of metals in a variety of structures, as illustrated in **Figure 3**. As packaging processes evolve for 5G with more RF signal interconnects within the package and low-loss substrates such as glass in increasing use, ECD remains central to all proposed solutions.

Although electroplating is part of the PCB process line, the equipment is not ideally suited to an advanced packaging environment. **Figure 4** shows one reason: footprint. Here we see the outline of a PCB plating tool, alongside a tool (the ASM NEXX P500) that adapts wafer processing technology to panel substrates. A typical 300mm wafer plating tool is outlined for reference. Although the P500 is considerably larger than the wafer tool, it is still considerably more compact than the vertical continuous plating (VCP) tool found in PCB manufacturing lines. The result is a more than 3X improvement in panels per hour per unit floor space, in addition to the other process benefits.

A panel plating tool for advanced packaging

To meet the requirements for advanced packaging on panel substrates, adapting a back-end or advanced packaging wafer plating tool was a more realistic path than modifying existing PCB plating tools. This is not only for the footprint and throughput reasons, but also because the wafer tool was already cleanroom compatible and allowed for excellent process control in advanced packaging applications. So, the same design elements just needed to be scaled up to panel dimensions, or adapted for handling rectangular substrates.

The starting point was the P300 wafer plating tool, incorporating a vertical plating cell design. Wafer plating tools can have vertical or horizontal plating cells, and there are examples of both in production. However, the vertical architecture is particularly well suited to plating panels, and allows a very compact arrangement of cells and straightforward transport from load port to plating cell and from cell to cell (for multi-metal stacks). Also, where horizontal wafer platers rely on spinning the substrate for rinse and dry following deposition, spinning of rectangular panels is not a practical option.

The panel plating cell is essentially a scaled-up version of the wafer plating cell, but with some notable differences, which will be described below. One major difference in the mechanical handling of the rectangular substrates involves the clamping needed to provide both electrical contact at the panel edge and the sealing of the clamped area from the corrosive chemicals in the plating

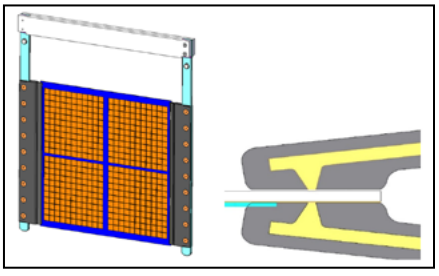

Figure 5: Electrical contact, chemical seal and mechanical support for a panel substrate in an ECD tool.

bath. For wafers, the contact and seal are made all around the circumference of the wafer, by clamping the wafers to a holder (**Figure 5**). In the panel tool, the contact and seal are made on two of the

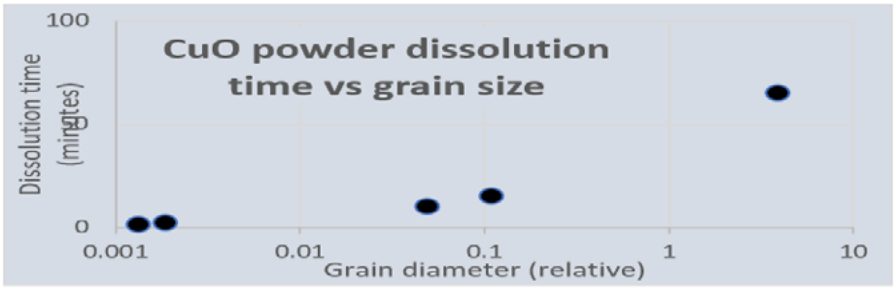

Figure 6: CuO powder dissolution time. Surface area per gram is inversely proportional to the square of the grain size.

four edges of the rectangle. The clamping mechanism provides a convenient frame to move the panel from the loading station to the various cells used in the process.

One feature of the panel plating tool that is qualitatively different from the wafer tool is in the area of bath maintenance. Consider the example of Cu, which is by far the most common metal deposited in advanced packaging processes. In most wafer plating scenarios, the plating cell contains a solid Cu anode, which not only provides the current for ECD, but also continually replenishes the metal that is removed from the bath in the deposition process. Although there are other chemical components of the bath that require monitoring and maintenance, the only action required to maintain the Cu concentration in a bath with a solid Cu anode is to replace the anode when it has lost too much of its volume.

In the panel tool, insoluble anodes are used. There are three reasons for this: 1) a solid Cu anode of this size would be extremely unwieldy to install and replace; 2) the segmented anode design described below requires anodes that do not change dimensions over time; and 3) the volume of metal deposited in the plating process is considerably greater than what is seen in wafer tools, and therefore it makes sense to replenish the metal in a more continuous fashion.

The Cu plating process is known to have high current efficiency. Therefore, the consumption of Cu ions from the bath can be reliably calculated from the accumulated charge (current * time). The Cu metal is replenished in the bath in the form of copper oxide (CuO) powder. This replenishment is a critical function because the overall volume of chemistry is kept to a practical minimum, so any component of the bath that is consumed in the plating process must be managed on a continuous basis.

Replenishment of Cu metal in the form of CuO powder introduced some new technical challenges. Most obviously, the cleanroom environment must be protected from the powder, requiring specialized equipment to contain and dispense the powder. Also, the specifications on the powder are critical: the grain size has a significant influence on the rate at which it dissolves in the solution (**Figure 6**). Clearly, a very fine powder is required for this application. Several

auger designs were tested to find one that would reliably dispense a predictable volume of such a fine powder. Finally, it was discovered that the speed of dissolution of CuO powder was enhanced by raising the bath temperature from 25°C to 35°C. This temperature increase was found to improve plating speed as well, by allowing higher concentrations of metal ion, with consequent improvement in via filling process times.

For wafer plating applications, uniformity of metal deposition across the substrate is one of the most critical performance parameters. There are several well-known ways in which nonuniformity can occur. One, known as the "wafer terminal effect" is the result of the ohmic voltage drop as the plating current is passed from the interior of the wafer surface to the edge. As a consequence of this, the center of the wafer presents a higher potential than the edge relative to the bath. This potential difference can be enough to cause a faster deposition at the edge than in the center. In wafer plating, this is straightforward to correct by placing properly designed barriers between anode and wafer to compensate for this effect. In panel plating, the situation is more complicated. The distances traveled by the plating current through the seed layer are greater, as are the total currents, which can lead to much greater ohmic potential drops. Also, the lack of cylindrical symmetry makes this distribution more complicated to correct.

The first step in correcting this mode of nonuniformity is a segmented anode (**Figure 7**). Rather than presenting a uniform anode surface at a fixed potential, the current supplied by each anode segment is individually controlled. Using finite element modeling, the optimum current distributions can be calculated for a given bath, seed layer conductivity, and exposed pattern.

Figure 7 shows an anode with five main segments. The number of segments has since been increased to 10, allowing even greater control of uniformity across the panel, and incidentally allowing for increased total plating current per panel, which can reduce the deposition time for some processes.

Another way in which deposition can become nonuniform is through variations in the pattern density. Where there are areas of dense pattern in close proximity to areas with sparse pattern, the sparse pattern will tend to plate faster than the dense simply because the uneven distribution of current near the wafer surface generates a slight potential difference, which affects the deposition rate. To deal with this, a close-edge shield methodology has been developed for use on the panel plating tool. This is a dielectric sheet held within a few millimeters of the panel to be plated, with an arrangement of perforations defined by performing a finite element analysis on the actual device pattern (**Figure 8**).

Another feature of the wafer plating tool that was incorporated in the panel plater, was shear plate agitation. Generating turbulence close to the plating surface has been shown to decrease the boundary layer thickness and allow for more efficient transport of the metal ions

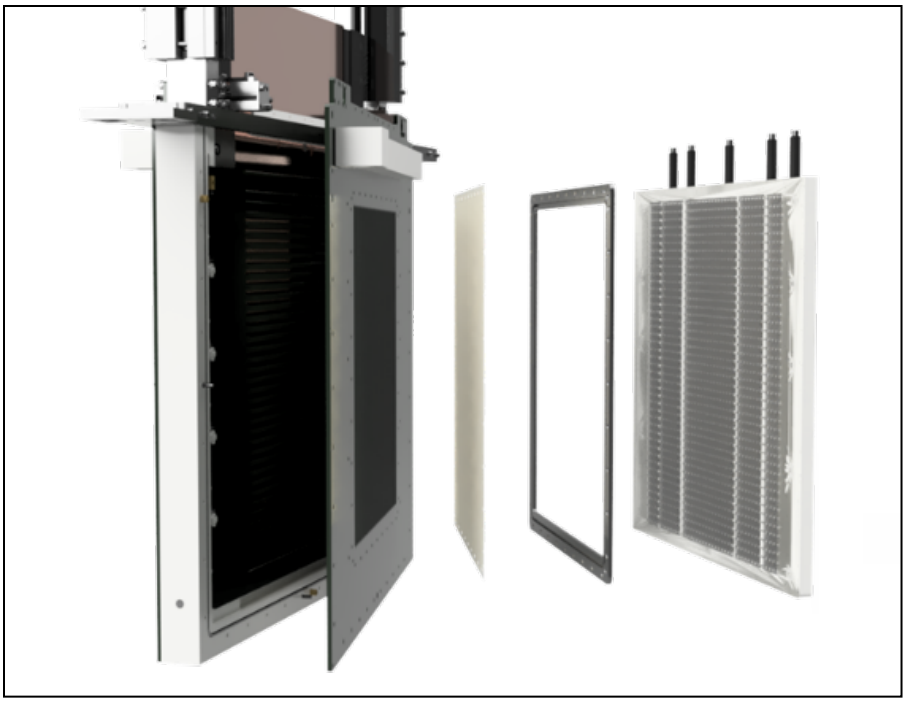

Figure 7: Contents of one side of a plating cell, including segmented anode and close-edge shield. The panel holder is shown on the left side.

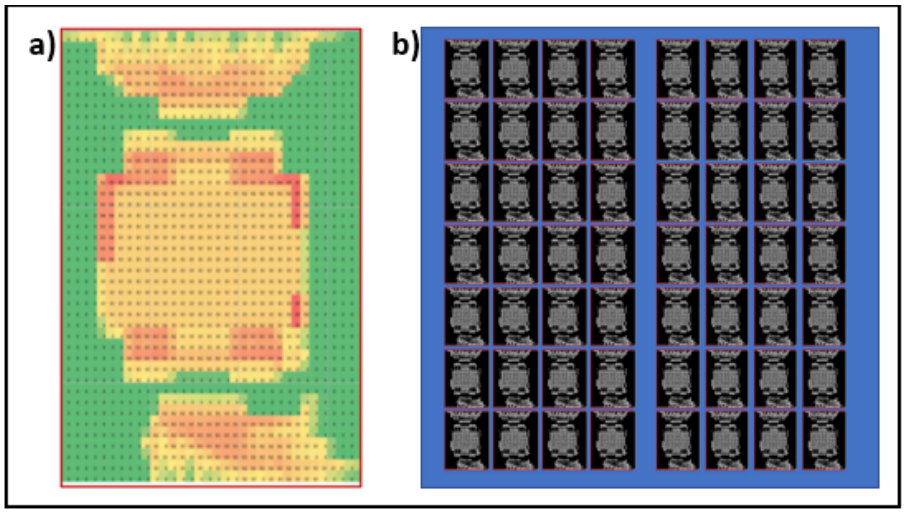

Figure 8: a) "Heat map" generated from the device pattern to be plated, and b) used to create a close-edge shield.

to the active surface. The distance from the shear plate to the substrate surface is a key parameter in the effectiveness of this agitation. In the initial design, this distance was 15mm, but has since been reduced to less than 6mm.

Summary

In the span of a few short years, advanced packaging processes using rectangular panel substrates have become practical, with a full set of effective process tools that can meet the same tight specifications as the corresponding processes on wafers. This includes electroplating processes, which are an essential part of all advanced packaging process flows. Developing an ECD tool for panel processing was in part a straightforward scaling of a wafer tool with vertical architecture, but also required rethinking some aspects of the tool to deal with the rectangular format and the large volumes of chemistry and currents involved.

Although the specific demands of advanced packaging have driven the development of the panel process and the P500 ECD tool in particular, a manufacturing tool with significantly improved productivity and process control may find applications in the world of PCB manufacturing, as this segment of the industry looks for ways to extend its technical capability.

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Biographies

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Jon Hander is Assistant VP of Panel Products for ASM NEXX, Billerica, MA USA. He has worked at NEXX since 2011 and in the semiconductor industry since 1996. He has a BS in Engineering Technology from Texas A&M U., and an MBA from U. of Phoenix.

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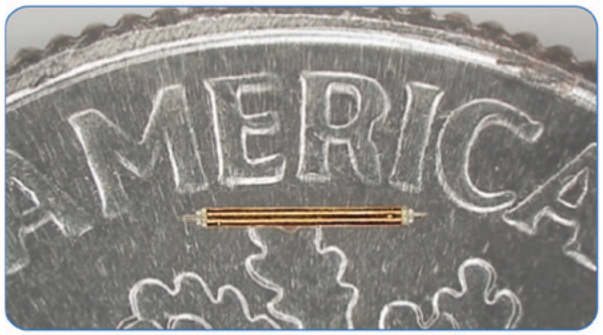
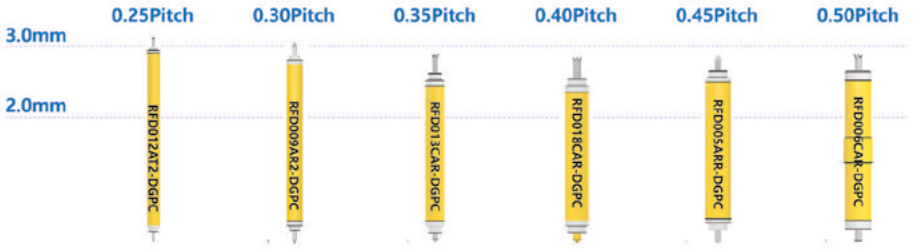
Specification

Frequency : 80GHz(BGA),
100GHz(QFN, LGA)
Pitch : 0.25mm ~
Crosstalk : -60dB
Impedance : 50Ω±10%





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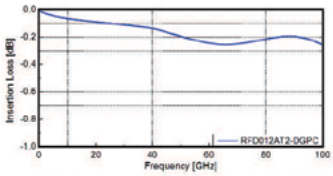
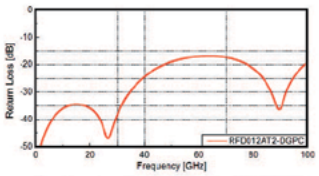
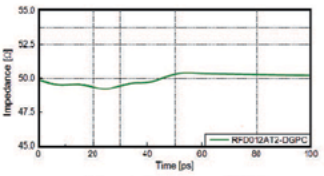


Insertion Loss(-1dB): Up to 100GHz

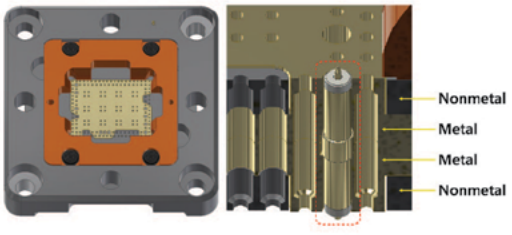


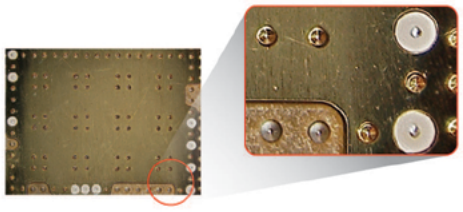
Return Loss(-10dB): Up to 100GHz



Impedance:49.2Ω

Coaxial Probe Socket Structure





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Silicones for chip packaging: stress management, device reliability and assembly considerations

By Jayden Cho, Manabu Sutoh, Roderick Chen [Dow]

The electronics of today and tomorrow will require more complex chips with smaller design parameters in packages that are physically larger, but also denser and more tightly integrated. Current integrated circuits (ICs) support multi-function chips in both side-by-side (2.5D) or stacked (3D) packages using flip-chip ball grid array (FCBGA), flip-chip chip-scale package (FCCSP), wafer-level ball grid array (WLBGA), fan-out system in a package (FOSiP) and fan-out wafer-level package (FOWLP) types. Advanced approaches to packaging now include integrated fan-out system on wafer (InFoSoW) for high-performance computing and superconducting multi-chip module (SMCM) for cryogenic electronics.

Despite the fact that current design parameters are as small as 5 nanometers (nm), researchers are working on 3nm, 2nm and even 1.4nm designs that will package more on-chip components more tightly together. To support the requirements of current and future designs, engineers can no longer consider the chip, package and printed circuit board (PCB) separately. Instead, an integrated approach is required. In addition to a growing and developing emphasis on device reliability, especially under demanding conditions, on-chip engineers are also tasked with considering assembly efficiency and environmental sustainability. Plus, changes in responsibility during the design process mean that on-chip engineers need to consider who is responsible for managing chip stress (**Figure 1**).

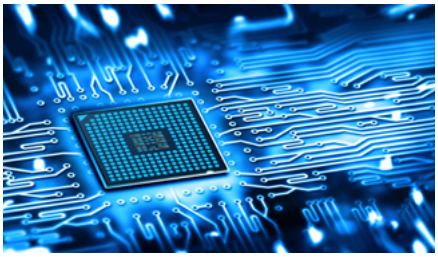

Figure 1: Complex and smaller chips in electronics today and tomorrow require reliable stress management.

Chip design and stress management

With the increased siliconization of electronics, it is now the job of the on-chip engineer (instead of the off-chip engineer) to manage stress-related problems caused by challenging integrations. Stress management is more than just a mechanical problem, however. It is also an electrical problem and a thermal problem – and all three problems are interrelated (**Figure 2**). Although there are many causes of chip stress, heat is especially problematic because high temperatures can cause electronics to fail prematurely or perform unreliably. Heat can also cause secondary stresses that degrade device performance over time or result in sudden failure.

The increased use of integrated packages provides several examples of heat-related challenges. Because there is more active device switching, larger chips have localized hotspots that change the stress profile across the entire chip. Thinner chips within flip-chip packages can warp, and stress-related problems such as die cracking, underfill delamination and package warping may occur. With 3D ICs, stacked dies need a longer path to dissipate heat; however, as the top die disperses its heat, some of this heat moves to the die below, which also requires heat dissipation. This heat transfer

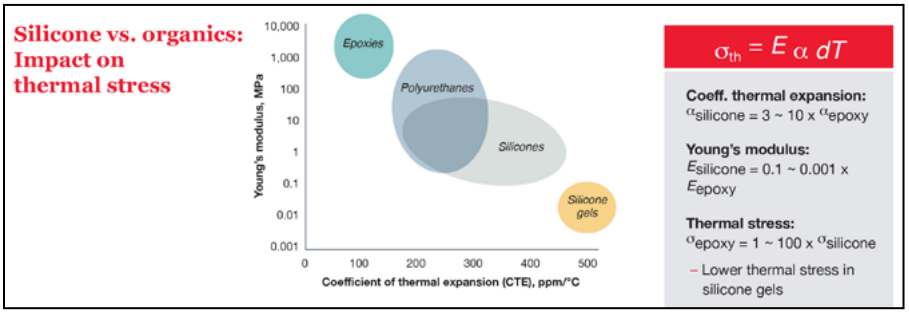

Figure 2: Relative thermal stress for 25ºC to 125ºC.

imparts new stresses to the bottom die that can result in cracking within the entire package, allowing the ingress of moisture and contaminants.

Both current and future designs need to withstand the high temperatures associated with densely-packed, heat-generating electronics. Yet, high temperatures alone are only a part of the thermal management challenges that on-chip engineers face. Thermal shock – a mechanical load caused by a rapid change in temperature – can occur because of rapid heating and cooling as the package dissipates heat. Plus, the different materials that are used in electronic devices each have a different coefficient of thermal expansion (CTE), a material property that indicates the extent to which a material expands with heating. Because these different materials expand (and contract) at different rates, stresses are imparted that can affect device reliability.

Heat, stress and modulus

To understand why differences, or mismatches in CTEs occur in chip packaging, consider the many different materials that are used in today's electronics. The package itself can be made of plastic, ceramic or glass. The bonding wires can be made of gold or copper, and the interconnects may use these same materials or aluminum, silver-palladium or indium-tin-oxide instead. Some PCBs are made of ceramic or glass, but others use epoxy, glass fiber-reinforced epoxy, polyimide, phenolic, BAKELITE® or melamine. The PCB includes metal heat sinks and a variety of electronic components, many of them surface-mounted, including a proliferation of sensors. During the design process, there are different CTEs to consider.

Effective thermal management requires interface materials that can resist high temperatures, withstand thermal shock, and absorb some of the stresses caused by these CTE mismatches. Elasticity is also important because electronics face physical shock and vibration, such as when a laptop computer or smartphone is dropped. In addition, environmental resistance to moisture, sunlight, dust and other contaminants is needed for device reliability. Sealants, encapsulants, adhesives and other thermal interface materials (TIMs) are used for heat-related challenges, but not all chemistries have the ideal modulus—a measure of resistance to elastic deformation when stress is applied. Consequently, not all chemistries can provide optimal stress management.

Stress management and material selection

On-chip engineers can choose silicones or epoxies for use as sealants, encapsulants, and adhesives, as well as coatings and other thermal materials. Both silicones and epoxies can resist high temperatures, but there is more to consider than heat resistance because of the relationship between thermal, electrical and mechanical stresses. Because they have a high modulus, epoxies have lower levels of elastic deformation when stress is applied. In other words, epoxies remain more rigid and, because they are less flexible, provide less stress relief when different materials expand at different rates. By contrast, silicones have a lower modulus that enables them to absorb some of the stresses that occur when electronic materials have different CTEs.

There are other reasons to use silicones as well. These well-balanced and stable elastomers adhere to many different packaging materials, including metal, glass and plastics. They are also self-leveling, which is important because chips are not perfectly flat. Silicones' elongation and compression properties provide protection and cushioning against shock and vibration – and across a wide range of temperatures as well. Because the density of polydimethylsiloxane (PDMS) polymers is approximately 1.0g/ml, silicones can support lighter-weight designs for portable electronics. Additional benefits include silicones' resistance to moisture, dust, and sunlight. Thermally conductive silicones can also work with heat sinks for improved heat dissipation.

Silicones, chip packaging and electronic assembly

The advantages of silicones extend to chip packaging and electronic assembly—areas where manufacturers are seeking to improve operational efficiency and meet environmental sustainability goals. To enhance production efficiency, manufacturers can use automated equipment instead of manual labor to apply thermally-conductive silicones in liquid form to chip packaging. Along with their long pot life, primer-less bonding and ease of mixing and handling, these silicones come in viscosities that support high flow rates for efficient filling and dispensing. They also support screen printing and can produce thinner bond lines for more effective heat transfers. Unlike greases and compounds, curable materials also remain in place.

Silicones can shorten production times through more efficient curing, a chemical process that converts a material from a liquid to a solid and imparts end-use properties. There are four main curing methods for liquid silicones: evaporative, moisture, heat and ultraviolet (UV). Evaporative curing and moisture curing both occur under ambient conditions. They do not require the use of specialized equipment, but throughputs are slower because cure times are longer. Thermal curing uses infrared lamps or thermal ovens to initiate or accelerate curing. Ultraviolet curing uses a UV light source and, typically, a secondary curing mechanism for "shadowed" areas that aren't reachable by the UV lamp.

Advanced silicones that use thermal curing are now available that cure at lower temperatures for greater energy efficiency. There are also room-temperature curing silicones where the application of lower-temperature heat can accelerate curing for high-volume assembly. Both the heat-curing and UV-curing silicone adhesives are available in solvent-free formulations that reduce or eliminate emissions of volatile organic compounds (VOC) such as benzene, toluene, ethylbenzene and xylene (BTEX). These advanced silicones promote environmental health and safety (EH&S) while helping to reduce the risk of fire because many solvents are flammable or combustible. Solvents are also closely regulated and may even be subject to greenhouse gas reporting requirements.

Solving chip packaging challenges today and tomorrow

With their well-balanced properties, silicones combine thermal stability and high-temperature resistance with strong environmental resistance to sunlight, water, dust, and other airborne contaminants. Their low modulus provides effective stress management and makes them well-suited for complex chips with smaller design parameters in larger but tightly integrated packages. Importantly, silicones help to relieve the stresses that occur when heat causes different materials to expand at different rates.

Advanced silicones can also improve assembly efficiency and help manufacturers to meet their environmental sustainability goals. They cure more rapidly, have lower energy expenses, and come in formulations that are free from solvents. As reliability becomes increasingly important and electronic devices become more expensive to purchase and repair, silicones are already supporting technologies such as 5G. These advanced materials are also well-positioned to support emerging technologies such as 6G and augmented reality wearables.

Summary

For on-chip engineers, the management of stress-related problems caused by challenging integrations will become a growing concern. By choosing a technology partner with a robust portfolio of products and advanced application experience, these engineers can strengthen their ability to support both today's designs and tomorrow's technologies.

Biographies

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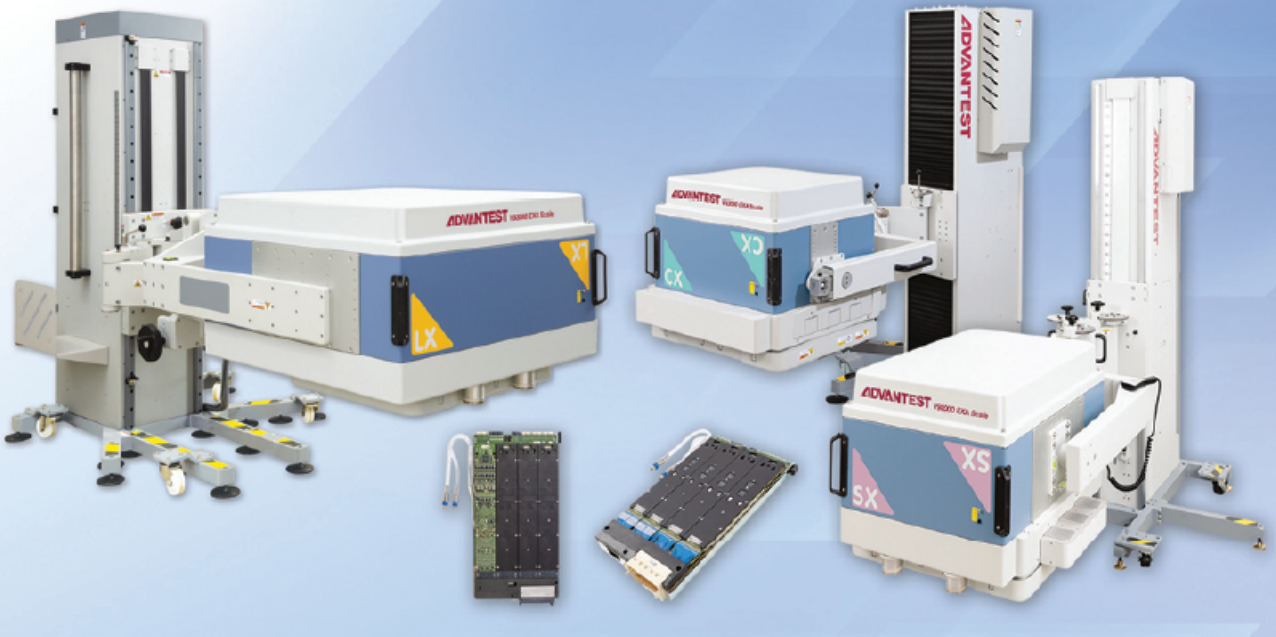

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