Chip Scale Review®

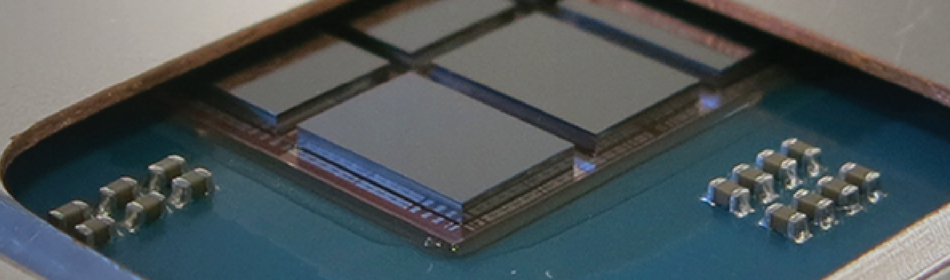
ChipScaleReview.com

The Future of Semiconductor Packaging

Volume 25, Number 2

March • April 2021

Heterogeneous 3D integration for high-performance computing
page 8



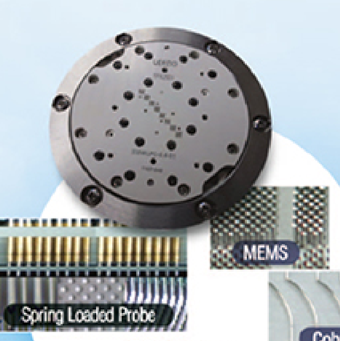
- Enabling wafer thinning using a glass carrier
- Packaging trends for automotive LIDAR applications
- Fan-out embedded bridge packaging for chiplet integration
- Hi-resolution dry-film PID material for high-density packaging
- Silicon die bonding using a photostructurable adhesive material
- Automating RF PA device manufacturing to accelerate 5G wireless rollout

Subscribe

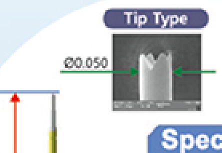
LEENO
Total Interface Solutions

90um Pitch ~

Spring Contact Probe



90um Pitch~
Probe Head

Tip Type


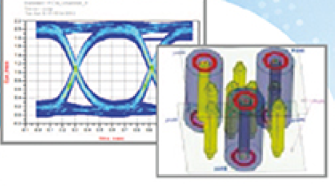
Specification
Pitch : Min.120um
Spring Force : 8.0g@250um
Current Rating : 1.3A
Inductance : 0.3nH
RF Probe for Fine Pitch Probe Head

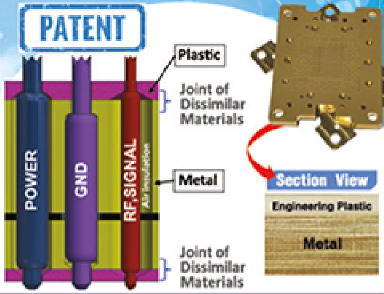
0.18mm Pitch~
RF Coaxial Spring Probe & Impedance Controlled Socket

Logic Test Socket

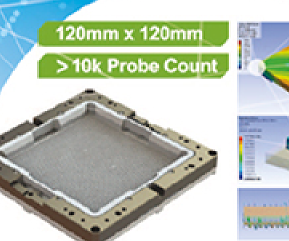
High Speed
Frequency : >20GHz
VSWR : < 1.2
Automatic Coaxial Probe

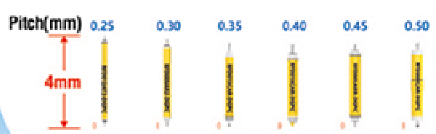
5G


Electrical Analysis
CCC Test, HFSS, TDR
Eye Diagram
4Port VNA Test

PATENT


MP Socket

120mm x 120mm
>10k Probe Count

Large Device Socket

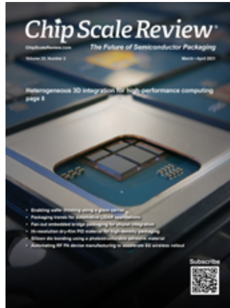
Specification
Frequency : 80GHz(BGA), 100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%


Coaxial Probe for 100GHz

LEENO LEENO INDUSTRIAL INC.

CONTENTS

March • April 2021
Volume 25, Number 2



CEA and IRT Nanoelec demonstrate a chiplet-based Active Interposer proof-of-concept, IntAct. Using advanced 3D technologies, such as TSV-middle and fine-pitch die-to-die interconnect, the IntAct demonstrator exhibits state-of-the art performance. 150,000 die-to-die interconnects are used, mostly for power and grounds, while 30,000 µbumps are used for 3D plug connectivity delivering throughput density up to 3TBit/s/mm². This circuit implements 96 cores with a scalable cache coherent architecture, delivering 220 GOPS peak.

Photo courtesy of CEA-Leti

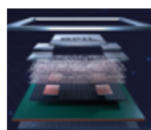
DEPARTMENTS

6 INDUSTRY NEWS
ECTC 2021 will bring key technologists and scientists together – virtually
By Ibrahim Guven, 71st ECTC Program Chair
[Virginia Commonwealth University]

FEATURE ARTICLES

8 **Heterogeneous 3D integration for high-performance computing**
By Séverine Chéramy, Emilie Bourjot
[CEA-Leti]
Johanna M. Swan
[Intel]

16 **Fan-out embedded bridge packaging for cost-effective chiplet integration**
By C. Key Chung, Shuai-Lin Liu, Jackson Li
[Siliconware Precision Industries Co., Ltd.]



Enabling the Future

As the original pioneers of the OSAT industry, Amkor has helped define and advance the technology, manufacturing and test landscape.

We deliver innovative packaging solutions with the service and capacity global customers rely on.

Amkor Technology®

amkor.com ▶ sales@amkor.com

© 2021 Amkor Technology, Inc. All Rights Reserved.

DIE-TO-WAFER (D2W) BONDING SOLUTIONS

- Fusion and hybrid bonding for next-generation heterogeneous integration
- Collective D2W bonding enabled by extensive knowledge in carrier preparation and die handling
- Direct placement D2W activation and cleaning complete solution with EVG®320 D2W
- Production-ready equipment solutions for successful integration of chiplets
- Heterogeneous Integration Competence Center™ serving as leading-edge incubation center for customers and partners

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

EVG® 320 D2W

Chip Scale Review

ChipScaleReview.com *The Future of Semiconductor Packaging*

STAFF

Kim Newman Publisher
knewman@chipscalereview.com
Lawrence Michaels Managing Director/Editor
lmichaels@chipscalereview.com
Debra Vogler Senior Technical Editor
dvogler@chipscalereview.com

CONTRIBUTING EDITORS

Steffen Kröhnert - Advanced Packaging
steffen.kroehnert@espat-consulting.com
John L. Lau, Ph.D - Advanced Packaging
john_lau@unimicron.com
Ephraim Suhir, Ph.D - Reliability
suhire@aol.com
Rao R. Tummala, Ph.D - Advanced Packaging
rao.tummala@ece.gatech.edu

EDITORIAL ADVISORS

Andy Mackie, Ph.D (Chair) - Indium Corporation
Rolf Aschenbrenner, Dipl.-Phys. - Fraunhofer IZM
Arun Gowda, Ph.D - GE Global Research
John Lau, Ph.D - Unimicron
Leon Lin Tingyu, Ph.D - National Center for Advanced Packaging (NCAP China)

SUBSCRIPTION—INQUIRIES

Chip Scale Review
All subscription changes, additions, deletions to any and all subscriptions should be made by email only to
subs@chipscalereview.com

Advertising Production Inquiries:
Lawrence Michaels
lmichaels@chipscalereview.com

Copyright © 2021 Haley Publishing Inc.
Chip Scale Review (ISSN 1526-1344) is a registered trademark of Haley Publishing Inc. All rights reserved.

Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry.
Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at Gilroy, Calif., and additional offices.

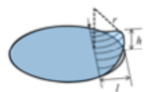
POSTMASTER: Send address changes to Chip Scale Review magazine
P.O. Box 2165
Morgan Hill, CA 95038
Tel: +1-408-846-8580
E-Mail: subs@chipscalereview.com

Printed in the United States

Volume 25, Number 2
March • April 2021

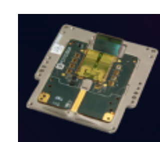
FEATURE ARTICLES *(continued)*

22 **Enabling wafer thinning using a glass carrier**
By Julia Brueckner, Andreas Gaab, Steven Lin, Erica Chang, Toshihiko Ono, Varun Singh, Jay Zhang [Corning Incorporated] Sebastian Tussing, Walter Spiess [SÜSS MicroTec]



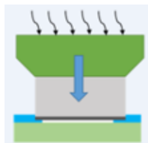
28 **Automating RF PA device manufacturing to accelerate 5G wireless rollout**
By Limin Zhou, Julius Ortega [MRSI Systems, Mycronic Group]

35 **Packaging trends for automotive LIDAR applications**
By Ajay Sattu, Weilung Lu, Mike Sleiman, Burt Barber [Amkor Technology, Inc]

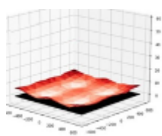


44 **Estimating BGA reliability of 2.5D packages using coupled thermal-mechanical simulation**
By Manish Nayini, Janak Patel [Marvell Semiconductor] Timothy Horn, Lloyd Burrell [GLOBALFOUNDRIES]

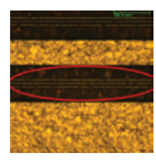
48 **Silicon die bonding using a photostructurable adhesive material**
By Kai Hollstein, Kirsten Weide-Zaage [Institute for Microelectronic Systems, RESRI Workgroup]

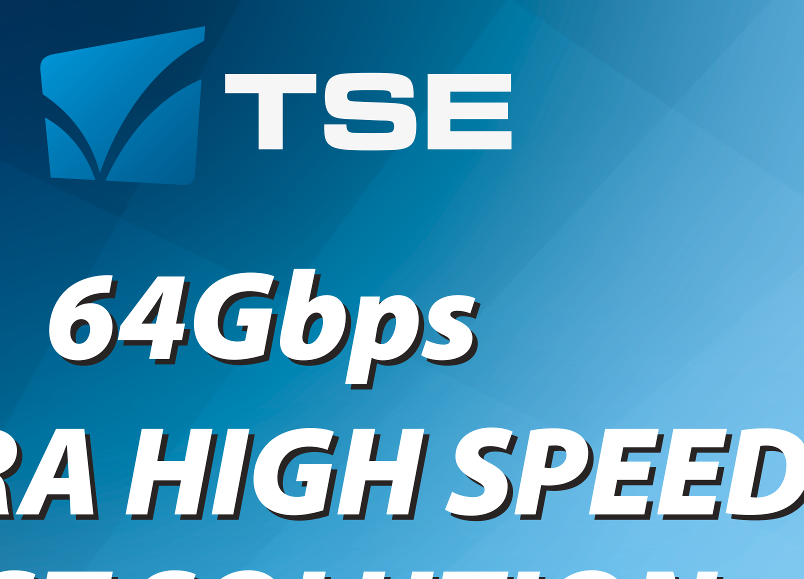


53 **Effects of FOPLP layouts on large-area thermal chucks**
By Debbie Claire Sanchez, Klemens Reitinger, Sophia Oldeide, Wenxuan Song [ERS electronic GmbH]



58 **Hi-resolution dry-film PID material for high-density packaging**
By Yuya Suzuki, Chihiro Funakoshi, Daisuke Shibata, Daichi Okamoto, Yoko Shibasaki [Taiyo Ink Mfg. Co.., Ltd.]





ULTRA HIGH SPEED
TEST SOLUTION

HSIO LC Component

ELTUNE
(Low CTE and Dk Elastomer Socket)

MRC
(MEMS Rubber Contact)

FlexTUNE
(Coaxial Spring Pin Socket)

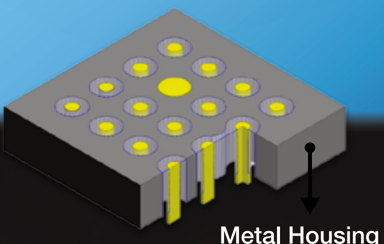
Load Board

TSE

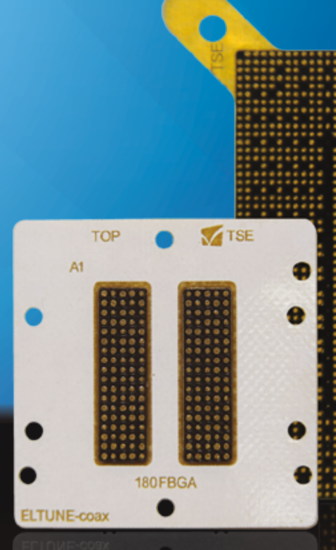
COAXIAL ELASTOMER SOCKET

ELTUNE-coax™

Conventional Elastomer Socket



ELTUNE-coax



GDDR6
(18Gbps)

CPU/GPU
(32/64Gbps HSIO,112Gbps PAM4)

• Mechanical Specification

(unit: mm)

0.80mm pitch	Spring Pin	Elastomer	ELTUNE-coax
Over-drive	0.40	0.25	**0.25**
Test height	3.50	0.60	**0.60**

• Electrical Specification

(unit: GHz)

42.5Ω, 0.80mm pitch		Spring Pin	Elastomer	ELTUNE-coax
Insertion Loss S_{21} @-1dB	Single Ended (G-S-G)	13.93	27.81	**>100**
	Differential (G-S-S-G)	25.39	28.94	**>100**
Return Loss S_{11} @-10dB	Single Ended (G-S-G)	10.98	15.89	**>100**
	Differential (G-S-S-G)	20.77	25.20	**48.21**
Crosstalk S_{31}, @-20dB	G-S-S-G	8.50	9.43	**>100**

Contact | sales@tse21.com | **Korea** (Headquarters) +82-41-581-9955 | **USA** +01-408-731-0030 | **China** +86-512-67617299 | **Taiwan** +886-3-657-6616 | **Singapore** +65-9623-2650

ECTC 2021 will bring key technologists and scientists together – virtually

By Ibrahim Guven, Virginia Commonwealth University, 71st ECTC Program Chair

On behalf of the Program and Executive Committees, it is my pleasure to invite you to IEEE's 71st Electronic Components and Technology Conference (ECTC). We are very excited about the 2021 program and welcome our colleagues from all over the world to join us. The 71st edition of ECTC, sponsored by IEEE/EPS, will take place virtually from June 1 until July 4, 2021.

Considered the premier electronic packaging conference of the industry, ECTC is continuing its tradition of bringing the latest developments in IC packaging, components, and microelectronic system technologies. This annual international conference brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses and foundries, outsourced semiconductor assembly and test (OSAT) service providers, substrate makers, equipment manufacturers, material suppliers, research institutions, and universities—all under one roof. ECTC typically attracts more than 1,500 attendees from over 25 countries. Last year's 70th ECTC, originally scheduled to be held in-person in Lake Buena Vista, Florida, was converted to an online platform because of the pandemic. The virtual conference had over 7,500 attendees from more than 55 countries around the world with 346 video presentations featured in 45 technical sessions. Additionally, there were seven special sessions with 60 invited presentations.

The 71st ECTC will continue with the same tradition of being the premium venue to showcase all the latest developments in the electronic components industry where packaging has become a way to achieve device and system performance scaling. More than 200 experts from broad-ranging technical areas have put together an exceptional program consisting of more than 350 technical papers in 46 technical sessions, 14 Professional Development Courses and several panels, special sessions, and networking opportunities. The conference will address various important topics and industry trends, from mobile, 5G, medical wearables and automotive applications including autonomous driving, flexible and printed electronics, to high-speed communications, wireless, LiFi, photonics, high-performance and quantum computing, and artificial intelligence (AI) hardware. The technical presentations and panel discussions will feature a wide range of packaging technologies, from wire bonding, wafer- and panel-level packaging, flip chip, 2.5D and 3D integration, to advanced substrates and interposers, embedded technologies, system in package and heterogeneous integration. New ideas, designs, characterizations, simulations and reliability studies will bring new perspectives and challenges with respect to materials and processing, integration, interconnections, assembly and manufacturing. Authors from over twenty-five countries are expected to present their work at the 71st ECTC, covering ongoing technology developments within established disciplines or emerging topics of interest for our industry.

The virtual platform will allow for recorded presentations of all technical session talks to be available on-demand throughout the conference. During the last two weeks of the conference, a live teleconferencing meeting for each session will be held by the session chairs; all the presenters in the session will be available live to field questions from the attendees. The special sessions will be held in a slightly different manner (see the **Table**). Special sessions will be held live during the first two weeks of the conference. Each panelist will pre-record their talks for the session; these talks will be broadcast live and immediately followed by a live panel discussion during which attendees will be able to ask questions. The special sessions will be recorded and made available for on-demand streaming from the date of the session until the end of the conference.

Sam Naffziger, Senior Vice President of AMD, will deliver the keynote speech entitled, "What the Chiplet-Based Future of Compute Means for Components and Technology." The conference will also feature a record ten special sessions (see the **Table**) with invited industry experts that will cover emerging technologies and applications. Session #2 will address market trends in the semiconductor industry, emerging applications, economic and geopolitical uncertainties, and the impact on the global supply chain for microelectronics packaging. Session #1 will be chaired by IEEE EPS President, Christopher Bailey, and IEEE EPS Vice President of Conferences, Sam Karikalan. Attendees of Session #1 will

Session #	Special Session Topics	Chair/Co-Chair
1	***IEEE EPS President's Panel*** - Future Vision of Electronics Packaging.	Christopher Bailey and Sam Karikalan
2	***ECTC Special Panel*** - Market Trends and Geopolitical and Economic Outlook	Rozalia Beica
3	***Plenary Session*** - Transformation of the Electronics Industry in a Post-Covid World	Jan Vardaman, Kimberly Yess, and Mark Poliks
4	***ECTC Diversity Panel*** - Diversity Does Matter and Can Drive Enhanced Business Performance	Allyson Hartzell and Kitty Pearsall
5	***ECTC Young Professionals Virtual Meetup***	Yan Liu and Adeel Bajwa
6	***IEEE EPS Seminar*** - "Latency: Are High-Bandwidth Optical Networks a Silver Bullet?"	Yasumitsu Orii and Shigenori Aoki
7	***ECTC Special Session***- Pathogen Detection and Eradication	Chris Bower and Mark Beranek
8	***ECTC Special Session*** - Low Temperature Solder (LTS) Packaging Challenges of a Next-Generation SMT Interconnect	Kevin Byrd and Keith Newman
9	***ECTC Special Session*** - Home Use Medical Devices and Packaging in Wearable Technologies	Kotlanka Rama Krishna and Ahyeon Koh
10	***ECTC Special Session*** - Materials and Technologies for Advanced Packaging (5G, RF, Power, Harsh environment)	Karsten Meier and Przemyslaw Gromala

hear from several leading companies who will discuss their future vision for advanced electronics packaging.

We are continuing our tradition and bringing back the young professionals networking event (Session #5). This is a great networking opportunity for young engineers, researchers, and students, to meet senior EPS members and professionals, learn more about industry activities, receive career guidance, and engage through a series of activities. The ECTC Diversity Panel (Session #4) – started a few years ago as a women-focused panel – has now evolved into a Diversity and Career Panel. Its focus will be on the correlation between diversity in the workplace and enhanced business performance. This year's ECTC Plenary Session (#3) will address the evolution and challenges of our industry in light of the pandemic, and the expectations that will drive packaging developments in the future. Our colleagues from Japan will be chairing Session #6, which will focus on the permissible latency in certain systems, and how high-bandwidth optical networks are critically important for satisfying latency requirements.

Following the industry trends and a growing interest in photonics, ECTC 2021 will feature a special session (Session #7) in which a panel of experts will provide their perspectives on the studies and technological improvements needed for safely detecting and eradicating pathogens on surfaces and spaces. A reliability-focused ECTC Special Session #8 will highlight LTS research areas most critical to component suppliers to improve compatibility with surface mount technology (SMT) LTS processing and to enhance solder joint reliability.

ECTC Special Session #9 will focus on some of the challenges associated with packaging sensors and the electronic signal chain into these emerging, at-home clinical-grade wearables. ECTC Special Session #10 will cover materials and technologies for advanced packaging.

In addition to the technical and special sessions and panels, the 71st ECTC event will offer several professional development courses (PDCs) and Technology Corner exhibits. Fourteen PDCs organized by PDC Committee chairs, Kitty Pearsall and Jeffrey Suhling, will be offered.

Whether you are an engineer, a manager, a student, or a business and marketing professional or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. As the Program Chair, I invite you to make your plans now to join us and be a part of all the exciting technical and professional opportunities offered at this event. I would also like to take this opportunity to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 71st ECTC a success. I look forward to virtually meeting all of you on June 1, 2021.

Heterogeneous 3D integration for high-performance computing

By Séverine Chéramy, Emilie Bourjot [CEA-Leti] Johanna M. Swan [Intel]

Following several years of continuous improvement and massive R&D efforts by chipmakers and research organizations, supercomputers will soon reach exascale-level computing performance. Traditionally, the ongoing increase in computing and memory performance, and the associated requirement to keep energy efficiency at a reasonable value, was achieved thanks to advanced computing devices, multi-core architectures, and power-optimized accelerators. In addition, high-performance computing (HPC) specifications also require the introduction of innovative hardware technologies around the processors themselves.

Meanwhile, new technologies supporting heterogeneous 3D integration allow product cost and time-to-market optimization. Through advanced packaging interconnects, performance enhancement may be obtained through power and area savings, as well as leading to quicker time-to-market and re-use of chiplets across a broader array of application-specific microelectronic solutions (Figure 1).

Intel's advanced packaging technologies

Going as far back as the early days of stacking memory and memory with logic for flash and wireless communications devices, Intel's Components Research organization has explored dense interconnect packaging. Over that time, a significant change in scaling occurred when applied to higher performance logic products. While many in the industry looked to silicon interposers and through-silicon vias (TSV) as a solution, Intel's Components Research organization took a different approach. They developed the first instantiation of a multi-die interconnect bridge using silicon within the package, now known as the embedded multi-die interconnect bridge (EMIB) [1]. Using small bridge dies embedded as part of the substrate, EMIB enables an order of magnitude increase in die-to-die interconnect density within the package, leading to much higher bandwidth between processor and memory.

More recently, Intel introduced Foveros [2], a 3D technology that allows the stacking of logic-on-logic die for the first time. Foveros helps to deliver higher flexibility for products fabricated with smaller chiplets such as I/O, static random access memory (SRAM), or power delivery circuits in the bottom base die and high-performance logic chips on top. It is

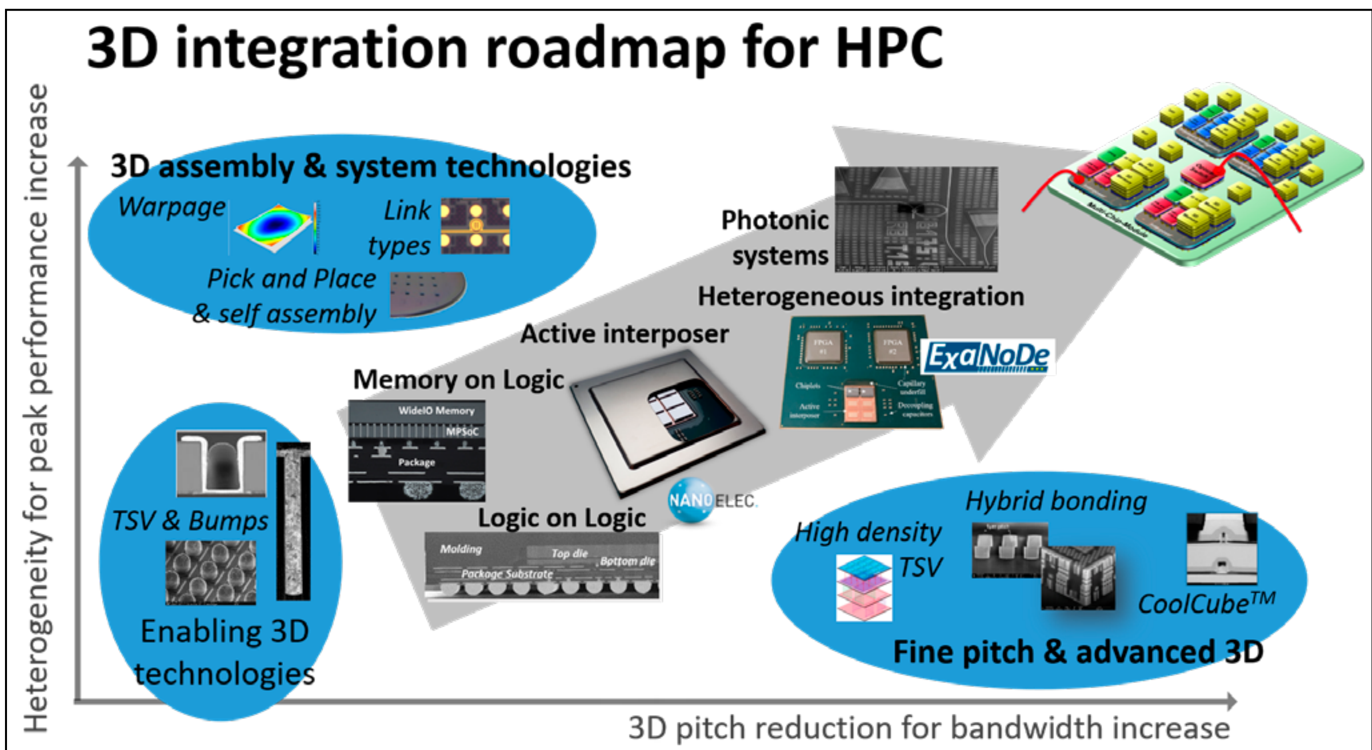


Figure 1: CEA-Leti's 3D integration roadmap for high-performance computing. © CEA-Leti

SCREEN

Solutions for Miniaturization and IoT

Leading-edge Devices Wafer size 300mm

SU-3300
Single Wafer Cleaner

SB-3300 NEW
Wafer Back-side Cleaning System

DT-3000
Coat/Develop Track

SP-2100 NEW
Spin Processor

LA-3100
Flash Lamp Annealer

RE-3500
Ellipsometric Film Thickness Measurement System

SS-80EX
Spin Scrubber

CW-2000
Compact Wet Station

ZI-3500
Wafer Pattern Inspection System

VM-2500
Spectroscopic Film Thickness Measurement System

SK-80EX
Coat/Develop Track

DW-6000
Direct Imaging System for Panel Level Packages

5 nm
7 nm
10 nm
14 nm
28 nm
45 nm
65 nm
90 nm
130 nm
250 nm

IoT Applications Wafer size 200mm

Power Device | SAW Device | LED | CMOS Sensor | MEMS

SCREEN Semiconductor Solutions Co., Ltd.

High-throughput flexible direct imaging for packaging/MEMS fabrication
As featured in Chip Scale Review January-February 2021 issue

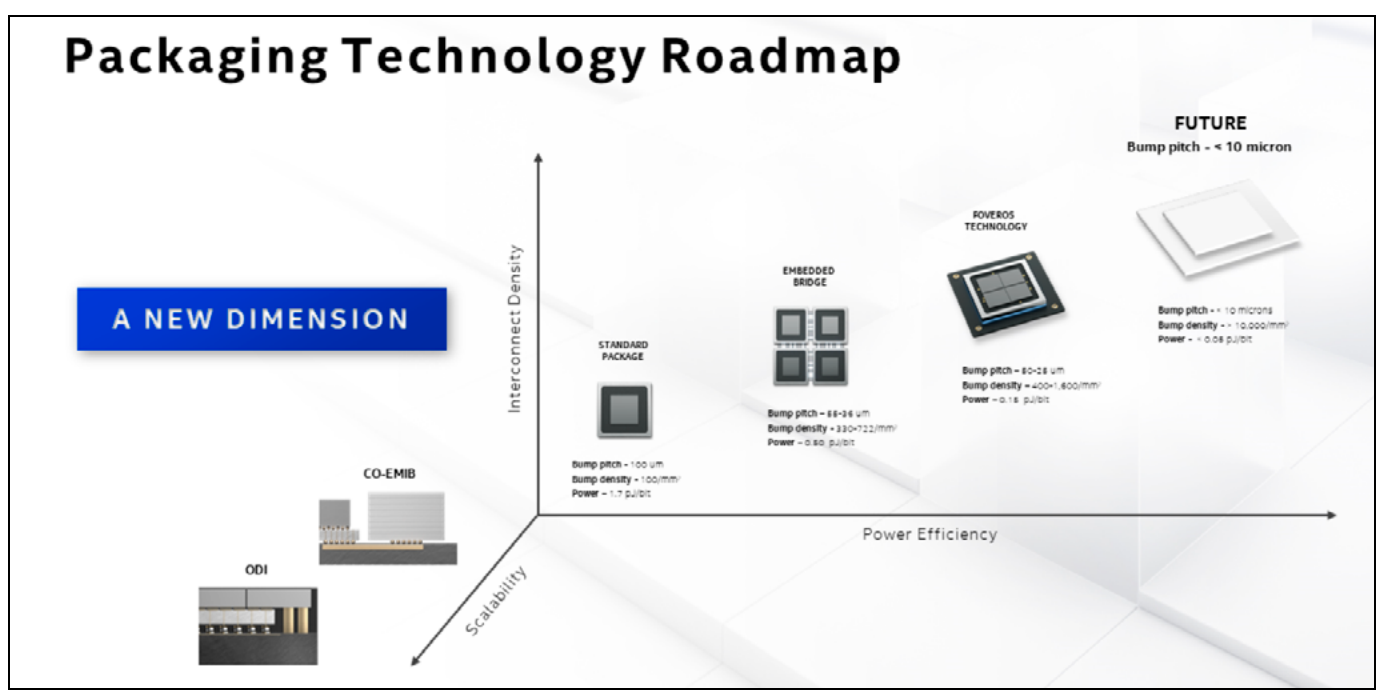
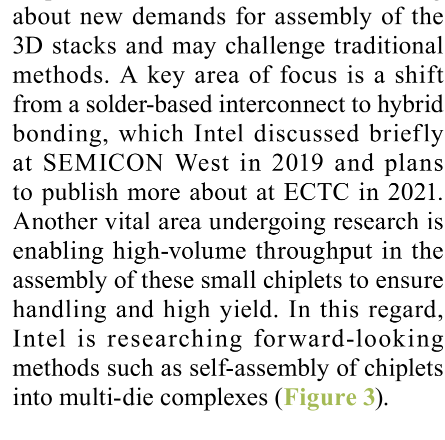


Figure 2: Intel's packaging technology roadmap. © Intel

envisioned that the combination of EMIB with Foveros, or co-EMIB, will enable increased partitioning opportunities by interconnecting larger than reticle-sized base die and their respective stacked-die complexes (Figure 2).

As a next step in optimizing performance, Intel's Components Research introduced the omni-directional interconnect (ODI) at SEMICON West in 2019 [3]. This new building block is complementary to EMIB and Foveros because it offers additional degrees of freedom for interconnecting die together for even higher performance. For example, ODI allows top-side chiplets to take advantage of 3D stacking's high bandwidth while maintaining the benefits of direct power delivery from the package, thereby avoiding losses that can accompany TSVs.

Beyond these architectural developments, Intel researchers are also working to scale the vertical interconnect pitch between die. The shrinking of the pitch enables much higher interconnect density or die size area reduction, or a combination of both. The ever-smaller chiplets and denser interconnects bring about new demands for assembly of the 3D stacks and may challenge traditional methods. A key area of focus is a shift from a solder-based interconnect to hybrid bonding, which Intel discussed briefly at SEMICON West in 2019 and plans to publish more about at ECTC in 2021. Another vital area undergoing research is enabling high-volume throughput in the assembly of these small chiplets to ensure handling and high yield. In this regard, Intel is researching forward-looking methods such as self-assembly of chiplets into multi-die complexes (Figure 3).



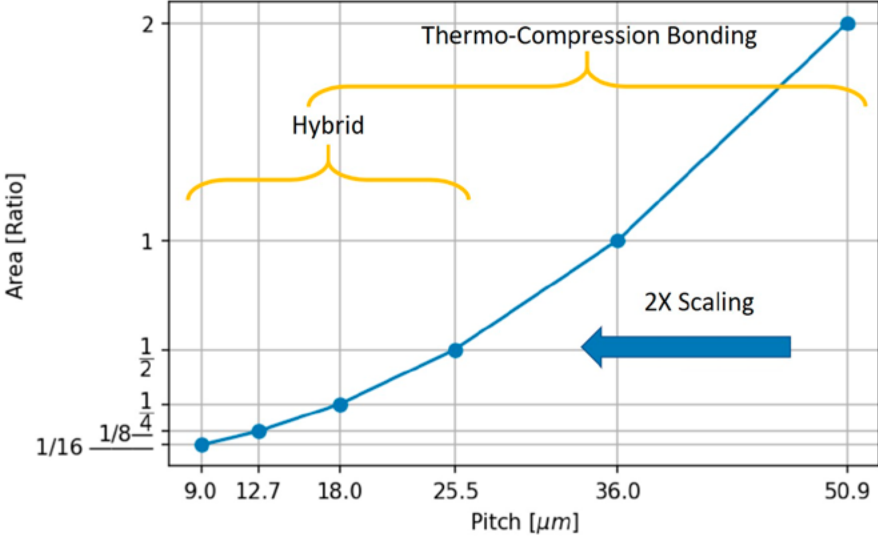
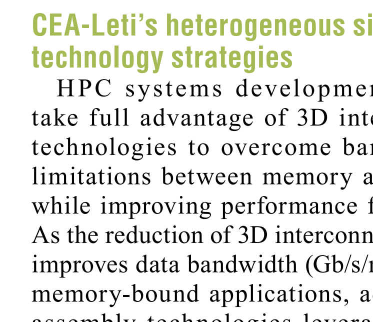


Figure 3: Interconnect technologies versus required pitch. © Intel

CEA-Leti's heterogeneous silicon technology strategies

HPC systems development must take full advantage of 3D integration technologies to overcome bandwidth limitations between memory and CPU while improving performance for each. As the reduction of 3D interconnect pitch improves data bandwidth (Gb/s/mm²) for memory-bound applications, advanced assembly technologies leverage tight heterogeneous integration with a low energy profile (pJ/b), which is useful for compute-bound applications.



Pursuing this objective, CEA-Leti introduced IntAct in 2019 at IEEE ECTC [4], a proof-of-concept demonstration integrating a 96-core architecture comprising six chiplets (fully-depleted

Seriously Fast.

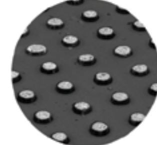
WX3000™ Metrology and Inspection Systems for Wafer-Level and Advanced Packaging

Powered by Multi-Reflection Suppression™ (MRS™) Technology

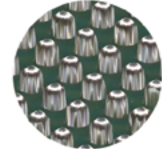
- **Improve Yields**
  High-Resolution & High Accuracy.
- **Increase Throughput**
  2-3X Faster Than Alternative Solutions.
- **Improve Processes**
  100% 3D and 2D Inspection in a Single Pass.

Copper Pillar

Flip Chip (c4)



Micro Bump



BGA Ball

2-3X Faster with High Resolution and High Accuracy

WX3000 3D and 2D metrology and inspection system provides the ultimate combination of high speed, high resolution and high accuracy for wafer-level and advanced packaging applications to improve yields and processes.

Powered by Multi-Reflection Suppression (MRS) Sensor Technology

The 3-micron NanoResolution (X/Y resolution of 3 micron, Z resolution of 50 nanometer) MRS sensor enables metrology grade accuracy with superior 100% 3D and 2D measurement performance for features as small as 25-micron.

100% 3D and 2D metrology and inspection can be completed simultaneously at high speed (25 300mm wafers/hour and 55 200mm wafers/hour) as compared to a slow method that requires two separate scans for 2D and 3D, and only a sampling process.

www.cyberoptics.com

Copyright © 2020. CyberOptics Corporation. All rights reserved.

silicon on insulator [FDSOI] 28nm node) three-dimensionally stacked on an active silicon interposer (complementary metal-oxide-semiconductor [CMOS] 65nm node). The work described technologies such as TSV-middle and die-to-die fine-pitch interconnects (20µm).

In 2020 at IEEE ISSCC [5], CEA-Leti and its partners unveiled the architecture of this HPC demonstration, as well as its performance metrics (**Figure 4**). Working together within the IRT Nanoelec 3D program framework, the team jointly demonstrated world-class figures of merit, such as 3D network-on-chip (NOC) communications at 1.2GHz while achieving up to 3Tbits/s/mm² in efficiency. As for power consumption, the demonstration showed how an astonishingly low 1.1W for 3.2Tb/s could be achieved. The work paves the way for future high-efficiency systems supporting HPC.

Convinced that HPC systems can fully benefit from the development of two technological tracks, one being new integration schemes and processes for reducing 3D interconnects pitch, and assembly technologies being the other, CEA-Leti pursued a technology roadmap that combines historical techniques with newer options such as direct hybrid bonding, in addition to die-to-wafer approaches for reaching a die-to-die interconnect pitch of 5 to 10µm, or even lower.

Figure 4: IntAct interposer. © CEA-Leti

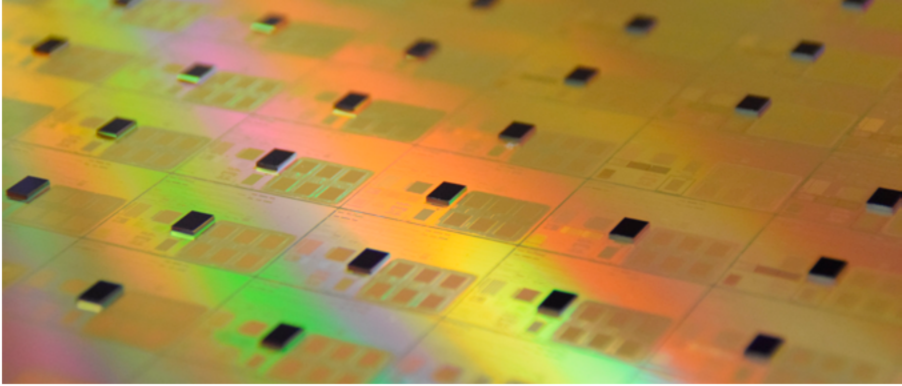


Figure 5: Die-to-wafer: make connection with 3D technology. © CEA-Leti

CEA-Leti initiated a direct hybrid-bonding variant more than ten years ago, now well-known at wafer-scale, in a die-to-wafer integration [6] (**Figure 5**). What is now considered a mainstream technology for heterogeneous integration was at that time quite exotic. In addition to developing the process and integration, the institute also initiated collaboration with equipment suppliers. SET, a French leader in accurate flip-chip bonding, and CEA-Leti together demonstrated in the 3D IRT Nanoelec program both the technical feasibility of the approach, as well as the industrial relevance of such an integration.

Consider an example: Whatever its promise in terms of die-to-die bandwidth and reliability, the die-to-wafer approach, particularly compared to wafer-to-wafer integration, only makes sense if dies can be selected prior to the bonding, making a known-good-die (KGD) strategy mandatory. Even if evident on paper, it is not so plug-and-play from a practical point of view. Design-for-test (DFT) features are also required (demonstrated by CEA thanks to the IntAct interposer). Furthermore, test methods, classically used for wire bonding or thermo-compression interconnect, must be adapted in order to be compatible with direct hybrid bonding topology and contamination constraints.

At the end of 2020, CEA-Leti successfully demonstrated proof-of-concept for the KGD approach that is compatible with direct hybrid

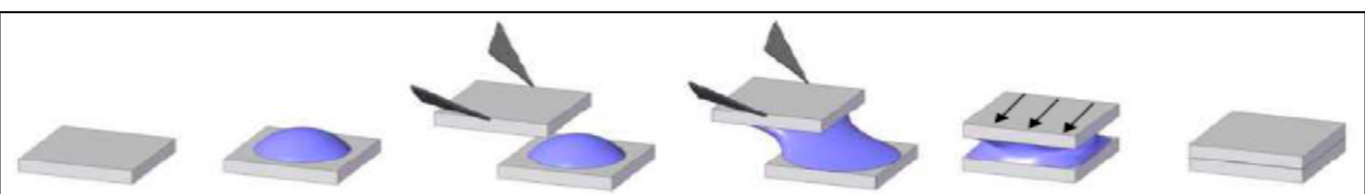


Figure 6: The self-assembly principle. © CEA-Leti

KOSDAQ LISTED COMPANY

SEMICONDUCTOR PACKAGE INSPECTION WITH REAL INTELLIGENCE

INTEKPLUS AI Technology improves Production Yield
by reducing Over-rejection and accurately classifying Defect Types for Yield Enhancement.

AI DEEP LEARNING

· ZERO UNDER-REJECTION · MINIMUM OVER-REJECTION

INTEKPLUS CO.,LTD.

#263,Techno 2-ro, Yuseong-Gu, Daejeon, 34026 Korea
Tel : +82-42-930-9900 Fax : +82-42-930-9999

For more information
www.intekplus.com / sales1@intekplus.com

bonding, which involves selecting high-topography tested chips (>2µm) and transferring them to direct bonding that tolerates a maximum topography of 10nm [7]. This was made possible thanks to researchers' deep expertise in planarization.

Intel Components Research/CEA-Leti collaboration

The semiconductor industry widely recognizes 3D integration technology and heterogeneous architecture as a solution for advancing chip design. Intel and CEA-Leti share the vision that advanced 3D integration and packaging technologies will strengthen IT solutions, especially in the area of HPC. They signed an R&D agreement in 2016 on several strategic research programs, including the Internet of Things (IoT), high-speed wireless communication, security technologies, and 3D displays [8]. They extended this collaboration in 2020, where Intel's Components Research organization and CEA-Leti are working together on 3D heterogeneous technologies for HPC.

The collaboration will allow both organizations to continue to investigate future opportunities for the heterogeneous integration roadmap thanks to a combined broad base of 3D technologies involving both chip packaging and interconnectivity. The work should ultimately pay off in solutions that offer flexibility in building large, high-performance, power-efficient systems out of smaller functions.

Self-assembly technologies: the new deal

CEA-Leti published an approach at IEEE ECTC 2019 [9] that combines advantages of die-to-wafer hybrid bonding and high throughput in the pursuit of anticipating coming challenges. The so-called self-assembly technology relies upon the engineering of the surface tension between two areas to be bonded and the use of an intermediate liquid in order to rearrange the physical orientation (in the three dimensions x, y, z) between them. Figure 6 describes the concept in the case of two chips to be assembled.

This technology could offer an alternative to mechanical alignment between the two areas, which could be decisive in reaching high bonding throughput and ultimate accuracy as pick-and-place bonders still have challenges to leverage throughput, alignment accuracy, and ultra-small dies bonding.

Summary

The collaboration between CEA-Leti and Intel on silicon interconnect technologies between chiplet and active interposer and, more specifically, on self-assembly, aims to overcome many of the challenges involving material, processes and integration, and equipment. Nevertheless, the early proof-of-concept released by CEA-Leti is very encouraging. With Intel's support and the expected collaboration with different players in the supply chain, particularly equipment suppliers, this technology may be a must-have technology for low-cost, high-performance heterogeneous integration in the future.

References

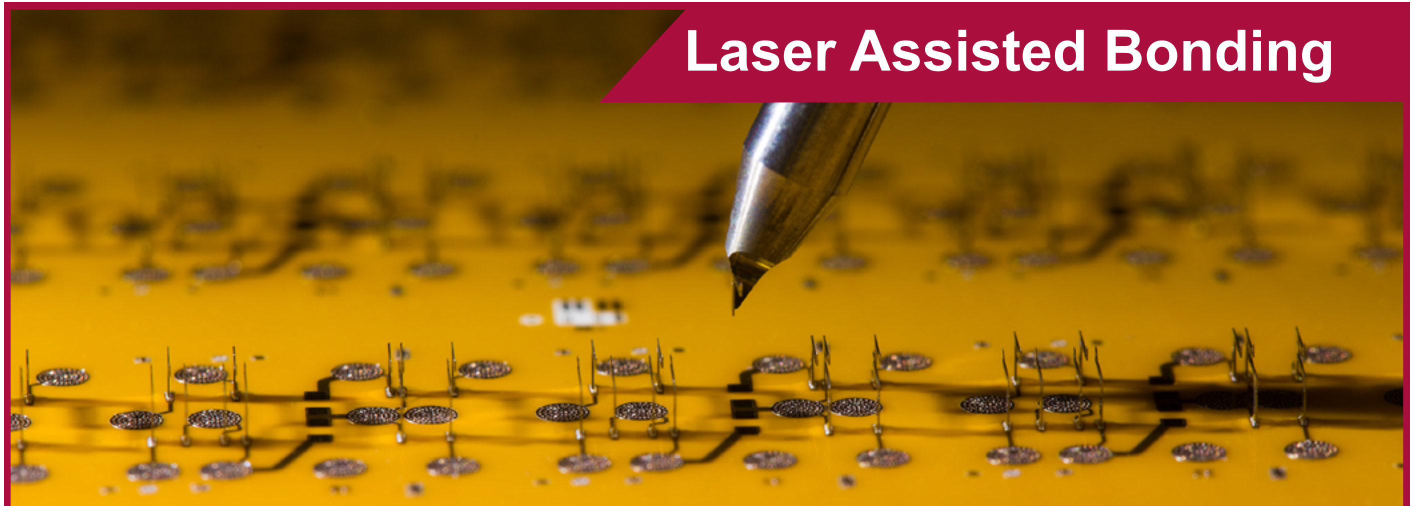
1. https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7545486
2. https://newsroom.intel.com/news/new-intel-architectures-technologies-target-expanded-market-opportunities/#gs.rp34uv
3. https://newsroom.intel.com/news/intel-unveils-new-tools-advanced-chip-packaging-toolbox/#gs.qov5x0
4. P. Coudrain, et al., "Active interposer technology for chiplet-based advanced 3D system architectures," 2019 IEEE 69TH Elec. Comp. and Tech. Conf. (ECTC), pp.: 569-578 (DOI: 10.1109/ECTC.2019.00092).
5. P. Vivet, et al., "A 220GOPS 96-core processor with 6 chiplets 3D-stacked on an active interposer offering 0.6ns/mm latency, 3TBit/s/mm^2 inter-chiplet interconnects and 156mW/mm2@82% peak-efficiency DC-DC converters," 2020 IEEE Inter. Solid-State Circuits Conf. (ISSCC), pp.: 46+ (DOI: 10.1109/ISSCC19947.2020.9062927).
6. A. Jouve, et al., "Die-to-wafer direct hybrid bonding demonstration with high alignment accuracy and electrical yields," 2019 International 3D Systems Integration Conference (3DIC), Sendai, Japan, October 8-10, 2019. Pages 1-7 (DOI: 10.1109/3DIC48104.2019.9058905).
7. E. Bourjot, et al., "Known good dies (KGD) strategies compatible with direct hybrid bonding," 2020 IEEE International Workshop on Testing Three-Dimensional, Chiplet-Based, and Stacked ICs 3D&Chiplet Test, session 2.
8. https://www.leti-cea.com/cea-tech/leti/english/Pages/What's-On/News/The-CEA-announces-expanded-collaboration-with-Intel-to-advance-cutting-edge-research-and-innovation-in-key-digital-areas.aspx
9. A. Jouve, et al., "Self-assembly process for 3D die-to-wafer using direct bonding: a step forward toward process automation," 2019 IEEE 69TH ECTC, pp.: 225-234 (DOI: 10.1109/ECTC.2019.00041).

Biographies

Séverine Chéramy is Director of the Institute of Technological Research (ITR) 3D program and is also responsible for 3DIC integration strategy and business development at CEA-Leti, Grenoble, France. She joined CEA-Leti in 2008 as 3D Project Leader, and was promoted in 2012 to 3D Integration Laboratory Manager. She holds an Engineering Degree in Materials Science. Email Vincent Barral, Business Development Manager at vincent.barral@cea.fr

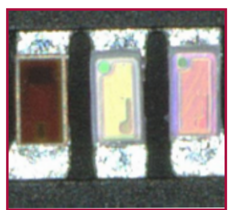
Johanna M. Swan is an Intel Fellow and the Director of Package Research and Systems Solutions in Components Research within Technology Development at Intel Corporation, Chandler, Arizona, USA. She leads an interdisciplinary team of researchers charged with developing novel technologies and package architectures to enable continued semiconductor scaling such as the recent Omni-Directional Interconnect for 3D IC interconnects. Email johanna.m.swan@intel.com

Laser Assisted Bonding



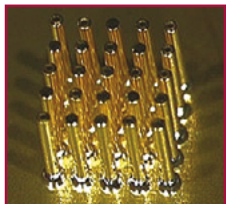
SMD

- SMD placement on ultra-thin flex



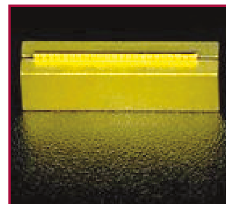
LED

- Mini & Micro LED assembly for repair and mass transfer



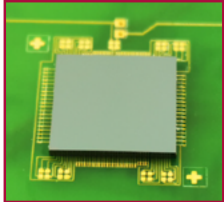
Pin bonding

- Single & multipin attach on various substrate material



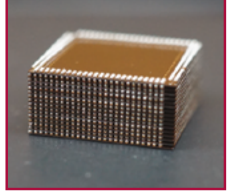
VCSEL

- diode assembly in between cooling block



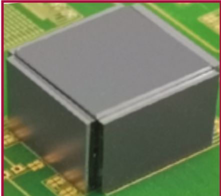
2D - 2.5D Packaging

- Chip on wafer, chip on board, chip on chip, package on package



3D Packaging

- In-situ die placement & reflow
- Lowest thermal & mechanical stress
- High chip stack uniformity



3.5D Multilayer Die Stacking

- Horizontal & vertical chip assembly
- No requirement for TSV structures
- Simplification of complex package design

Selective Chip Rework

- Selective removal of bad die
- In-situ replacement & reflow
- Cost saving for high density fan-out packaging

Fan-out embedded bridge packaging for cost-effective chiplet integration

By C. Key Chung, Shuai-Lin Liu, Jackson Li [Siliconware Precision Industries Co., Ltd.]

With transistor scaling reaching both physical and economic barriers, transistor performance and cost have been increasingly lagging behind the historical Moore's Law trajectory. However, demand for silicon remains incessant with the growth of transmission rate. Development of electronic devices has increasingly required greater high-density package integration. The electronic industry's response to this demand on package integration is to use chiplet-based devices for improving yield and lowering the total cost. Chiplet packaging has now become a key technology to continue Moore's Law. Intensive research has resulted in the development of multiple chiplet packages, such as multi-chips on a Si interposer using through-silicon via (TSV) (2.5D), die-to-die stacked on each other (3D), fan-out multi-chip module (FOMCM), and embedded multi-die interconnect bridge (EMIB). These packages were developed for the server, high-performance computing, router, and switcher markets.

In this paper, we introduce a scalable chiplet package technology, called fan-out embedded bridge (FOEB). This advanced package improves upon the 2.5D package by lowering the package cost, improving the electrical signals, and having better reliability performance. In this article, we present a demonstration of an FOEB test vehicle in which chips are integrated as follows: one application-specific integrated circuit (ASIC) die and 4 high-bandwidth memory (HBM) dies with four embedded bridge dies on a mold-based interposer, and one layer of an RDL. The embedded bridge dies are fabricated using 65nm node technology with 0.56µm Cu line and space. By comparing the warpage of a 2.5D package with a similar package size, we show that the FOEB chip module has a similar warpage shape to the substrate, and the final package assembly with the substrate—so the warpage value is identical to the 2.5D package. Therefore, it has much lower stress residues as compared to a 2.5D package. Because of this finding, the FOEB package has been validated: it has a 2x longer temperature cycle without a single failure as compared to a 2.5D package. This finding allows us to scale the package to a much higher I/O density, with finer L/S, a greater number of RDL layers, and a greater number of dies that nicely fit Moore's Law trends for packaging.

Introduction

By now, Moore's Law has clearly ended with respect to Si scaling [1], and the role of advanced packaging to extend this trend is of utmost importance. The growth of semiconductors has been driven by the demands of smartphones and tablets, but these markets are now slowing down and being overtaken by high-performance computing (HPC) and big data computing (BDC). HPC and BDC demand very high-frequency and high-speed transmission with lower latency, high-bandwidth and power efficiency requirements. These requirements have created a different level of packaging complexity and challenges. One solution to meet these demands is to integrate multiple dies into an electronic package. These packages are designed either homogeneously or heterogeneously with integrated devices [2-4]. Over the years, electronic assembly houses have developed a plethora of chiplet packages for multi-chip integration.

Figure 1 shows the evolution of advanced packaging over time. The first 2.5D package was developed by TSMC with two purposes: 1) for die partition, which was a homogeneously-integrated

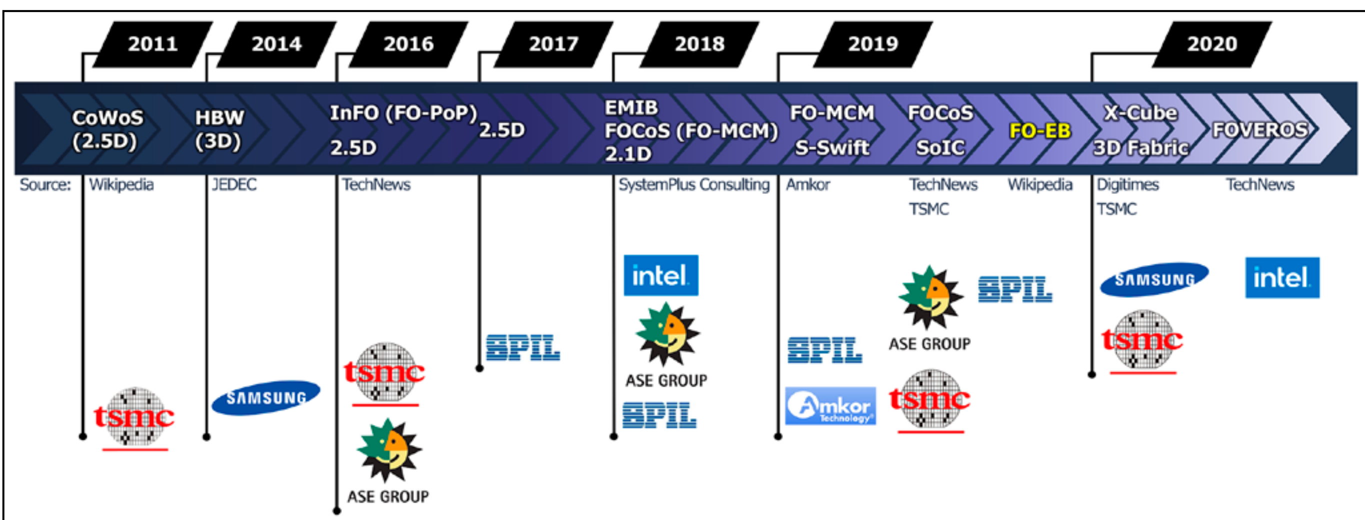


Figure 1: Evolution of advanced packaging in high-volume manufacturing.

package; and 2) for a heterogeneously-integrated package that was to integrate the HBW memory with system on chip (SoC) dies within the same package. The 2.5D package was introduced in early 2011 to immense interest on the part of many design houses. Amkor then announced its Silicon-less Integrated Module (SLIM™) and its Silicon Wafer Integrated Fan-Out Technology (SWIFT®) package, which was a fan-out MCM—but this technology had some limitations and did not take off into production. Then, TSMC introduced the integrated fan-out (InFO) package for Apple's A8 processor, which was a fan-out package on package (FO-PoP). Subsequently, ASE also certified its 2.5D package for AMD at 2016. In 2017, SPIL overtook other outsourced semiconductor assembly and test suppliers (OSATS) as the first such supplier to manufacture 2.5D packages in high volume. In 2019, many semiconductor companies were offering different versions of advanced packages, which were actually the extension of 2.5D, FOMCM, and 3D packages. In 2020, SPIL introduced its FOEB that has been certified in 2019 and started low-volume manufacturing in 2020.

2.5D IC with through-silicon via (TSV) technology is the package that has been developed to satisfy the need for a matured platform in the near term. Research has shown that a Si interposer can provide the fine-pitch technology to match the shrinking die pitch trend, and further implement the high-density interconnection needed between SoC and high-bandwidth memory (HBM) [5,6]. In view of the escalating demand for the enhanced performance and cost efficiency, assembly houses have devoted resources to the development of 3DIC [7-9] and fan-out technology that feature multiple layers of an organic interposer [3,4,10]. To achieve enhanced performance, using 3DIC TSV technology to directly stack logic on logic or logic on memory has advantages for providing improved computing ability and electrical properties, as well as wide I/O with less than 20µm pitch to achieve an ultra-high density interconnect [7-9]. However, whether 2.5D or 3DIC technology is used, either Si interposer or active dies with TSV has critical drawbacks in terms of parasitic resistances and expensive fabrication manufacturing processes [2,11]. Therefore, fan-out technologies with multiple RDL layers of an organic interposer have been developed to provide the die to die interconnection feasibility and cost benefit without having to use TSVs. Flexible and scalable designs that use more than three RDL layers for high I/O density provide sufficient signal and power/ground line distribution [3,4]. But, as the chip module is getting larger, the thermomechanical stresses generated between the die to die interfaces will break the RDL traces [10,12].

The fan-out technology called FOEB provides localized high-density wiring through the use of an embedded silicon bridge [13-19]. The partial bridge interposer is applied in the specific area of the high I/O density interconnection that is used for the integration of HBM dies, which is in comparison to 2.5D packaging in which the whole piece of Si interposer is used. Intel also demonstrated that the fan-out basis of EMIB technology is capable of supporting high-bandwidth interconnects with high-quality power networks to the satisfaction of signal/power integrity demand [20-22]. In signal integrity, both the insertion loss and near-end crosstalk show excellent agreement, and the link power efficiency can be as low as 0.7pJ/b at 1.2V [22]. The solution not only offers high bandwidth, but also consumes low power. For the SPIL FOEB package, instead of placing the embedded die inside the substrate, we introduce the embedded dies inside the organic interposer [13-19].

FOEB package technology

The FOEB architecture is described in Figure 2a. The thin Si bridge dies are embedded within the organic interposer and RDL layers are fabricated on the organic interposer. The range of the Cu line/space (L/S) goes from 2/2 to 10/10µm. The RDL layers can be either one or more in number, depending on the design needs. Within the organic interposer, there are embedded bridge dies that are fabricated with Cu wire with L/S values ranging from 0.56~0.8µm. The Cu microbump pitch is 40µm. The ASIC die is connected to the adjacent HBM dies via the bridge dies. Figure 2b shows that the Cu posts are built up with C4 bumps for the vertical transmission of signal, ground and power from the top dies to the substrate. FOEB technology is highly flexible for advanced package design in terms of the Cu wire inside the bridge dies and RDL layers. It can be customized for the various die combinations with as many as 19 dies (with 9 bridge dies), and the basic 2.5D structure with three dies (with one bridge die), as illustrated in Figure 2c.

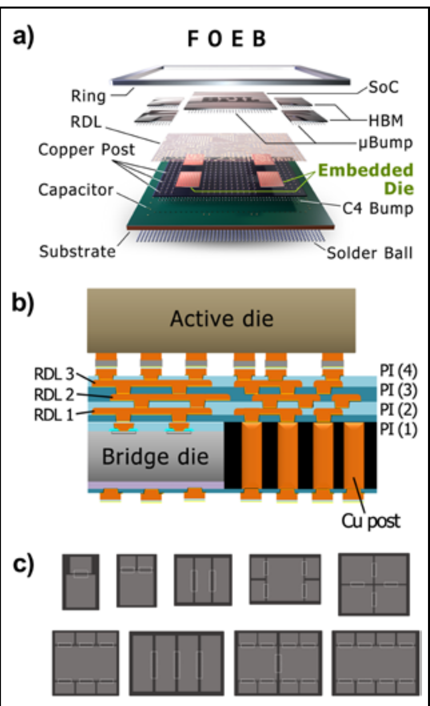


Figure 2: FOEB Illustration of a) elements of the architecture; b) a section view; and c) possible scalable features.

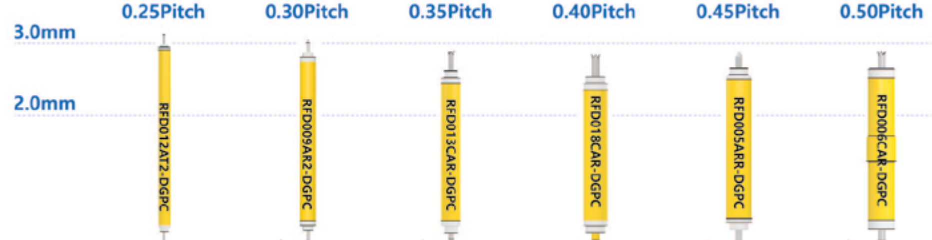
The FOEB process flow is briefly introduced in Figure 3. The first layer of RDL is fabricated on the glass carrier, and then the Cu post is built up using standard lithographic technology and plating. In parallel, the embedded bridge die is fabricated with microbumps and then die bonding on the first RDL layer as depicted in Figure 3a. The assemblies are molded in wafer form and then grinding is to expose the Cu post and the Cu bump as shown in Figure 3b. With that, the organic interposer is built up; Figure 3c shows the build-up of RDL layers and forming the micro pad. After that, Figure 3d-f illustrate the processes to attach SoC die and HBM dies on the micro pad by reflow joint, underfill dispensing and the curing process. Then, a second molding is applied to cover the entire wafer, and the wafer form assemblies are ground away so as to expose the die surface. The glass carrier is removed by laser ablation, and C4 bumping fabrication is plated up accordingly. These wafer form

LEENO

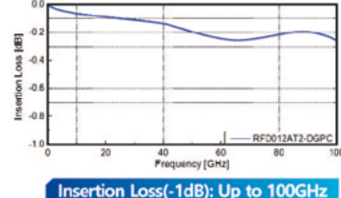
Coaxial Probe for 100GHz

Specification

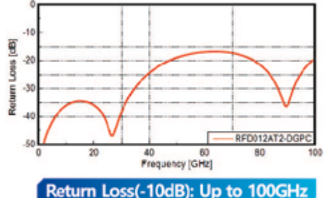
Frequency : 80GHz(BGA),
100GHz(QFN, LGA)
Pitch : 0.25mm ~
Crosstalk : -60dB
Impedance : 50Ω±10%



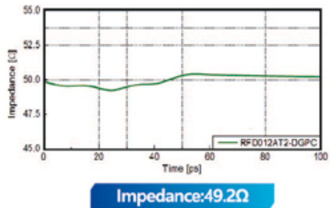
RFD012AT-DGPC(0.25P) S-Parameter & Impedance



Insertion Loss(-1dB): Up to 100GHz

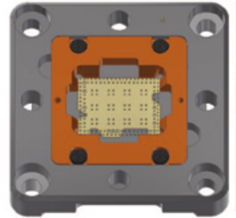


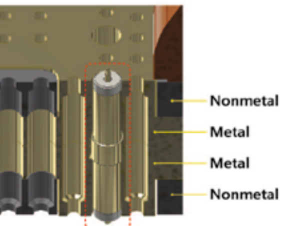
Return Loss(-10dB): Up to 100GHz

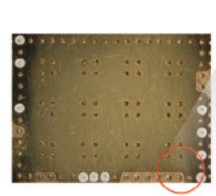


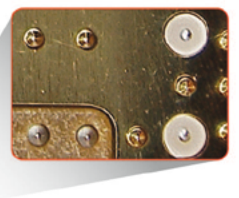
Impedance:49.2Ω

Coaxial Probe Socket Structure









For More Details, Please Contact Us.
We are Always Ready to Visit You.

GLOBAL LEADER LEENO

HEAD OFFICE
10 105beon-gil MieumSandan-ro Gangseo-gu, Busan, Korea

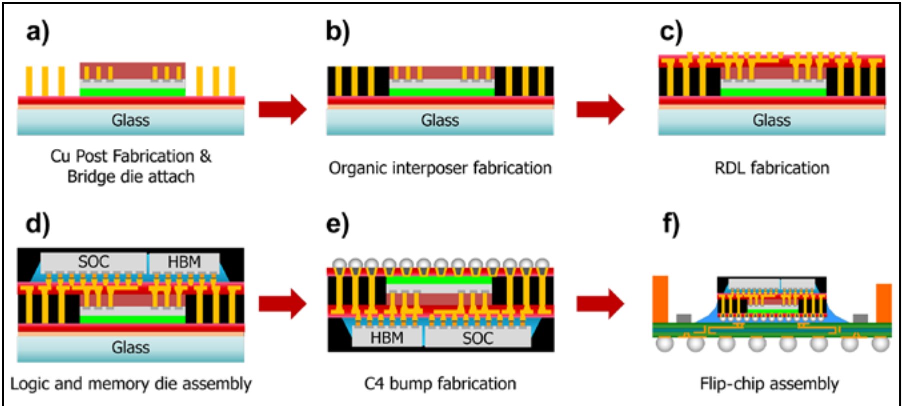


Figure 3: FOEB process flow.

chip modules are then singulated into individual units. The final process step is the attachment of the chip module on the organic substrate using conventional flip-chip processes.

Results

The FOEB package is the alternative solution providing cost efficiency and better electrical performances as opposed to 2.5D technology [22]. According to our certification, the mechanical strength and package reliability can be comparable and even better than that for 2.5D. The thermal moiré results indicated that FOEB chip module warpage has the same deformation behavior with the organic substrate at high temperature (see Figure 4a). As a result, the well-matched contact for solder wetting was expected and the attachment of the FOEB chip module on substrate had 2x lower residue stress than for the 2.5D case [10]. At the finished package level, Figure 4b shows that FOEB package warpage is similar to that for the 2.5D package. The similar coplanarity indicated the low risk in the surface mount technology (SMT) process of packaging on a PCB. Owing to this result, the benefit of the lower internal stress could make the FOEB platform useful to the product application in larger package sizes. It passed the reliability test up to TCG 2500 cycles, the unbiased-highly accelerated stress test (HAST) of 264hrs, and the high-temperature storage life (HTSL) test (1000hrs) [13-19]. Owing to these reasons, the FOEB package has a great chance to supersede the 2.5D package as it has better design flexibility, scalability, and the benefit of a lower cost.

One of the technologically certificated FOEB devices comprises 1 SoC + 4HBM package structure with a package dimension of 5,075mm^2 with a fan-out module size of 1,250mm^2. The structure passed JEDEC standard reliability tests. The packages were first preconditioned using moisture soaking level 4 (MSL4) requirements, and then subsequently stressed for temperature cycling under -40 to 125°C for 1200 cycles and then subjected to the unbiased high accelerated stress test at 130°C for 264 hours. The HTSL test was done at 150°C for 1000 hours [19]. In order to certify the structural strength under severe conditions, we tightened the TCJ cycle test up to 3000 cycles. Again, the units passed based on the open/short (O/S) test as tabulated. The units were then cross-sectioned and examined under SEM. The integrity of the package was well intact. Figure 5 shows the cross section details after TCJ 3000 cycles.

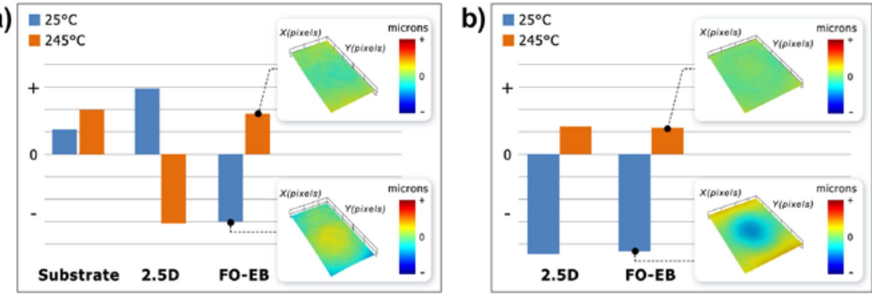


Figure 4: Thermal Moiré results: a) chip module and substrate; and b) package level.

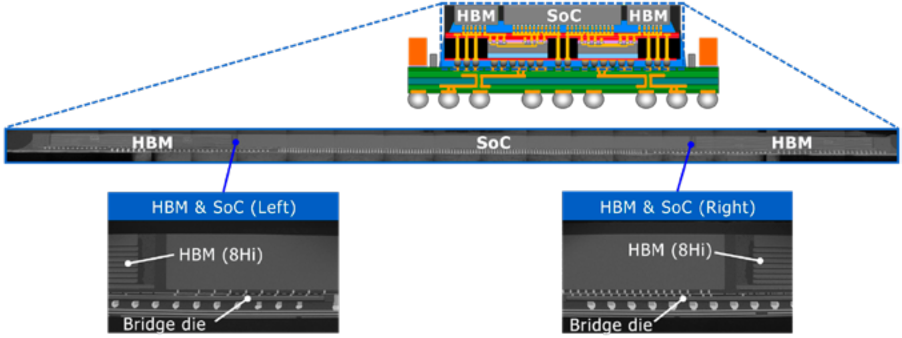


Figure 5: Cross sections of FOEB package integrity after 3000 cycles of TCJ testing.

Summary

The FOEB platform has been demonstrated as a new package paradigm that provides a localized high-density interconnection between two or more dies that are being integrated. In the flourishing industry of artificial intelligence (AI), 5G applications, and cloud computing, the fundamental infrastructure is being developed for the higher speed and terabyte/s bandwidth needed for the large amounts of data being transmitted. The FOEB package not only provides an alternative and acceptable cost/benefit solution for chiplet integration, but it also provides the mechanical performance that well exceeds the mature 2.5D technology. With the advantages of controllable warpage and less internal stress, FOEB technology is the proper platform to build up a much larger package size for the integration of greater numbers of multiple dies. In addition, FOEB meets the scalability and design flexibility needed for the customized requirements. We are now converting the bridge dies to active dies for vertical communication and better functionality.

References

1. R. R. Tummala, "Moore's Law for packaging to replace Moore's Law for ICs," *Chip Scale Review*, vol. 23, pp. 31-34, Jan-Feb 2019.
2. X. Zhang, et al., "Heterogeneous 2.5D integration on through-silicon interposer," Appl. Phys. Rev. 2., 021308 (2015).
3. J. Lau, "Redistribution layers for heterogeneous integrations," *Chip Scale Review*, vol. 23, pp. 20-25, Jan-Feb 2019.
4. J. Lau, "Recent advances and trends in fan-out wafer/panel-level packaging," J. of Elec. Packaging, vol. 141, pp. 1-27 (2019).
5. F. Shoo, S. Elisabeth, "3D packaging is breaking new ground," Yole Développement 2020 (WebCast).
6. C. Lee, et al., "An overview of the development of a GPU with integrated HBM on silicon interposer," 2016 IEEE 66th Elec. Comp. and Tech. Conf. (ECTC), Las Vegas, NV, 2016, pp. 1439-1444, doi: 10.1109/ECTC.2016.348.
7. M. Koyanagi, "New 3D integration technology and 3D system LSIs," 2009 Symp. on VLSI Tech., Honolulu, HI, 2009, pp. 64-67.
8. M. Chen, F. Chen, W. Chiou, D. C. H. Yu, "System on Integrated Chips (SoIC™) for 3D heterogeneous integration," 2019 IEEE 69th ECTC, Las Vegas, NV, USA, 2019, pp. 594-599, doi: 10.1109/ECTC.2019.00095.
9. A. Podpod, et al., "High-density and high-bandwidth chip-to-chip connections with 20µm pitch flip-flop chip on fan-out wafer-level package," IEEE Inter. Wafer Level Packaging Conf., IWLPC 2018 doi: 10.23919/IWLPC.2018.8573262.
10. Y. Lin, et al., "Multilayer RDL interposer for heterogeneous device and module integration," 2019 IEEE 69th ECTC, Las Vegas, NV, USA, 2019, pp. 931-936, doi: 10.1109/ECTC.2019.00145.
11. P. Yu, et al., "Coaxial through-silicon vias using low-κ SiO_2 insulator," IEEE 70th ECTC, Orlando, FL, USA, 2020, pp. 1167-1172, doi: 10.1109/ECTC32862.2020.00187.
12. J-K. Fang, M-L. Huang, H-J. Tu, W-L. Lu, P. Yang, "A Production-worthy fan-out solution - ASE FOCoS chip last," IEEE 70th ECTC, Orlando, FL, USA, 2020, pp. 290-295, doi: 10.1109/ECTC32862.2020.00055.
13. C. Key Chung, et al., "Alternative solution for 2.5D package using FO-MCM and FOEB," IEEE 22nd Elec. Packaging Tech. Conf. (EPTC), Singapore, Dec 2-29 2020 (Invited Talk, virtual).
14. C. Key Chung, et al., "Silicon bridge using fan-out," 2020 IEEE 14th Inter. Microsystems, Packaging, Assembly and Circuits Tech. Conf. (IMPACT-EMAP), Taipei, Taiwan; Oct 23-25, 2019 (invited speech).
15. C. Key Chung, et al., "Advanced packaging solutions for high-performance computing and big data processing," IEEE 15th Inter. Microsystems, Packaging, Assembly and Circuits Tech. Conf. (IMPACT-EMAP), Taipei, Taiwan; Oct 21-23, 2020 (invited speech).
16. C. Key Chung, Y. L. Huang, "Back-end based chiplet integration solutions & roadmap," IEEE 40th Symposia on VLSI Tech. and Circuits, Hawaii, USA. Jun 15-19, 2020 (invited short course, virtual).
17. C. Key Chung, "Low-cost solution for 2.5D using fan-out embedded bridge," Symp. by Yole Développement and NCAP on Advanced Packaging Semiconductors (SYNAPS), Wuxi, China, Sept. 15, 2020 (keynote, virtual).
18. C. Key Chung, "Recent progress of chiplets integrated packages in semiconductor industry," 2020 SEMICON Taiwan, Heterogeneous Integration Innovation Zone: Fan-out Packaging Technology Seminar, Taipei, Sept 23, 2020 (invited speech).
19. J. Lin, C. Key Chung, C.F. Lin, A. Liao, Y. J Lu, J. S. Chen, D. Ng., "Scalable chiplet package using fan-out embedded bridge," IEEE 70th ECTC, Orlando, FL, USA, May 26-29, 2020; pp. 14-18, doi: 10.1109/ECTC32862.2020.00015 (virtual).
20. R. Mahajan, et al., "Embedded multi-die interconnect bridge (EMIB) -- A high-density, high-bandwidth packaging interconnect," IEEE 66th ECTC, Las Vegas, NV, 2016, pp. 557-565, doi: 10.1109/ECTC.2016.201.
21. R. Mahajan, et al., "Embedded multi-die interconnect bridge—A localized, high-density multi-chip packaging interconnect," IEEE Trans. on Comp., Packaging and Mfg. Tech., vol. 9, no. 10, pp. 1952-1962, Oct. 2019, doi: 10.1109/TCPMT.2019.2942708.
22. R. Viswanath, A. Chandrasekhar, S. Srinivasan, Z. Qian, R. Mahajan, "Heterogeneous SoC integration with EMIB," 2018 IEEE Electrical Design of Advanced Packaging and Systems Symp. (EDAPS), Chandigarh, India, 2018, pp. 1-3, doi: 10.1109/EDAPS.2018.8680869

Biographies

C. Key Chung is a Senior Director at Siliconware Precision Industries Co., Ltd., Corporate R&D, Taichung, Taiwan, R.O.C. He received his PhD from National Taiwan U. and has 26 years experience in the industry focused on packaging, substrate and assembly material. His team has won several advanced packaging businesses including FO-PoP, FOMCM, FOEB, 2.5D, and 3DIC. He received 20 issued patents, published 45 papers, and delivered multiples invited talks at conferences. Email keychung@spil.com.tw

Shuai-Lin Liu is a Deputy Manager at Siliconware Precision Industries Co., Ltd., Corporate R&D, Taichung, Taiwan, R.O.C. He received his MS in Engineering Management from U. of Texas at Arlington, and has 10 years in the industry on material research and packaging.

World Class Full Turn Key WLCSP Solution Provider

UTAC's New Wafer Bumping Process in Singapore.

Scan to view our website, utacgroup.com

Enabling wafer thinning using a glass carrier

By Julia Brueckner, Andreas Gaab, Steven Lin, Erica Chang, Toshihiko Ono, Varun Singh, Jay Zhang [Corning Incorporated] and Sebastian Tussing, Walter Spiess [SÜSS MicroTec]

Wafer thinning is an industry trend driven by functional requirements or form factor considerations. For example, 3D stacked memory uses silicon (Si) that is thinned to <50µm to enable through-silicon via (TSV) interconnection. Insulated-gate bipolar transistor (IGBT) chips rely on very thin wafers for vertical structural realization. Many components used for mobile devices are thinned before packaging to accommodate the height constraints imposed by design or aesthetics. When the final wafer thickness is greater than 100µm, backgrinding tapes are typically used to support the wafer during the thinning process. Thinning beyond this thickness often necessitates the use of a more rigid support, such as a carrier wafer.

Wafer thinning is often accompanied by post-thinning processing that happens at elevated temperatures, e.g., metal or dielectric deposition. Differences in the coefficient of thermal expansion (CTE) of the carrier and that of the wafer can cause shape distortion, resulting in undesirable consequences such as lithography errors, or even wafer breakage. For convenience, we use the term warp in this article to describe shape distortion.

An ideal carrier wafer for wafer thinning should have a CTE matched to that of the wafer to be thinned. In this article, we will also discuss other levers that may be used to minimize shape distortion during thinning and post-thinning processing.

This article will explain why glass is an ideal carrier material. We will also demonstrate why glass carrier wafers are not only ideal for laser debonding, but that they can also be used with automated, mechanical debonding tools.

What impacts wafer warp?

We begin by first developing the fundamental understanding of what impacts wafer warp. In a previous article in this journal [1], we showed a simplified formula that can be used to estimate bi-layer warp as a function of material and

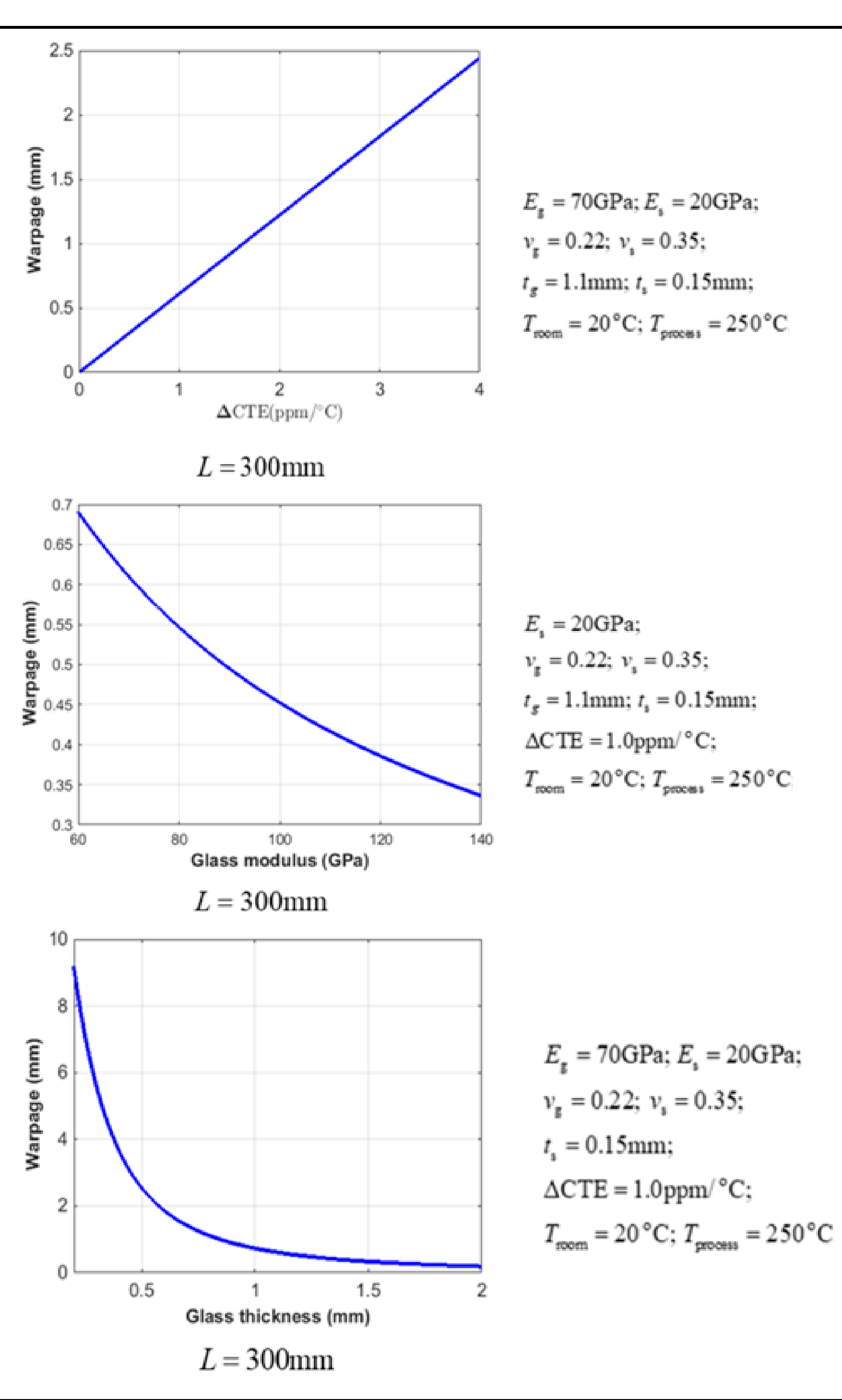


Figure 1: Warp as a function of ΔCTE, carrier Young's modulus, and carrier thickness.

sheet properties. If we assume the post-thinning wafer layer is significantly thinner than the carrier, the warp expression is:

$$\approx 0.75 L^2 \Delta\alpha\, \Delta T\, \frac{E_s\left(1-v_g\right)}{E_g\left(1-v_s\right)} \frac{t_s}{t_g^2}$$

Here we use subscript *s* to designate the material properties of the semiconductor wafer to be thinned: E_s for Young's modulus, t_s for the wafer thickness, υ_s for Poisson's ratio, and α_s for the thermal expansion coefficient. For the carrier glass, we use subscript *g* for the same parameters accordingly. L is the size of the carrier.

From the simplified formula shown above, we can see the trends clearly. The warp is linearly proportional to CTE mismatch, as well as the temperature differential between bonding and operation; it is inversely proportional to the carrier's Young's modulus; and the warp is also inversely proportional to the square of the carrier thickness. When we use the typical conditions encountered in wafer thinning and post-thinning processing, we see these trends in **Figure 1**.

Benefits of glass as a carrier

The discussions above focused on three levers for a carrier to help manage warp. We discuss specific requirements and constraints for each of the three below.

CTE is the most important attribute. **Table 1** shows the CTE of the most commonly used wafer types. These include Si on the low-CTE end, all the way to $LiTaO_3$ on the high-CTE end. Glass can cover the entire CTE range, and if the market warrants the investment, a glass company can design and make glass with very fine granularity, down to ~0.2ppm/°C.

Wafer type	Si	SiC	GaN	GaAs	Sapphire	$LiTaO_3$
Applications	IC, Memory	Power IC, LED	RF, LED	RF, LED	LED	SAW filter
CTE (RT-300C)	~3	~4.0	3-5.6 *	~6	5-7 *	4-16 *
* significantly dependent on crystal orientation						

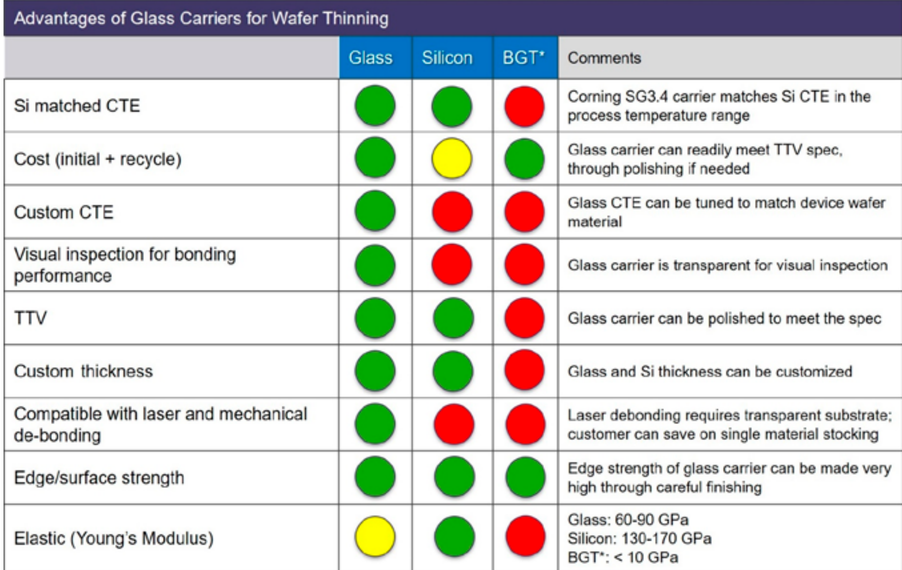
Table 1: CTE values of commonly used wafer types.

Young's modulus. Young's modulus is an effective lever to control warp when a perfect CTE match is not possible. While popular glass compositions typically show Young's modulus in the 65-75GPa range, a highly technical glass can exhibit Young's modulus as high as 140GPa. In the real world, compromises must be made between performance and manufacturability, which translates into cost.

Carrier thickness. Carrier thickness is another lever available to the user. The thickness-squared relationship makes it highly effective in controlling warp, especially in the 0.5-1.0mm range.

Glass is an ideal carrier wafer material because it can offer a CTE that matches the wafer to be thinned, its Young's modulus engineered to be relatively high, and its thickness to be optimized within the constraints of the application. The transparent nature of glass makes laser debonding possible, and the same transparency also makes bonding quality control simple and straightforward. Other glass benefits include: the ability to reach a very low total thickness variation (TTV), its reusability, etc. **Figure 2** compares glass to Si and the backgrinding tape (BGT) used for wafer thinning.

Figure 3 shows the availability of glass wafers that cover the range of 3-13ppm°C from Corning. Corning's Advanced Packaging Carriers (APC) product was engineered to have a relatively high Young's modulus and a wafer thickness of up to 2mm.



Advantages of Glass Carriers for Wafer Thinning

	Glass	Silicon	BGT*	Comments
Si matched CTE	green	green	red	Corning SG3.4 carrier matches Si CTE in the process temperature range
Cost (initial + recycle)	green	yellow	green	Glass carrier can readily meet TTV spec, through polishing if needed
Custom CTE	green	red	red	Glass CTE can be tuned to match device wafer material
Visual inspection for bonding performance	green	red	red	Glass carrier is transparent for visual inspection
TTV	green	green	red	Glass carrier can be polished to meet the spec
Custom thickness	green	green	red	Glass and Si thickness can be customized
Compatible with laser and mechanical de-bonding	green	red	red	Laser debonding requires transparent substrate; customer can save on single material stocking
Edge/surface strength	green	green	green	Edge strength of glass carrier can be made very high through careful finishing
Elastic (Young's Modulus)	yellow	green	red	Glass: 60-90 GPa Silicon: 130-170 GPa BGT*: < 10 GPa

Figure 2: Comparison of substrates used for wafer thinning and their bonding properties.

Mechanical debonding of a glass carrier

Because of their excellent transparency, glass carrier wafers are often associated with laser debonding. This does not have to be the case. Glass carriers provide benefits for the mechanical debonding process as listed below.

Enabling visual inspection. Glass carriers add value to the mechanical debonding by enabling visual inspection

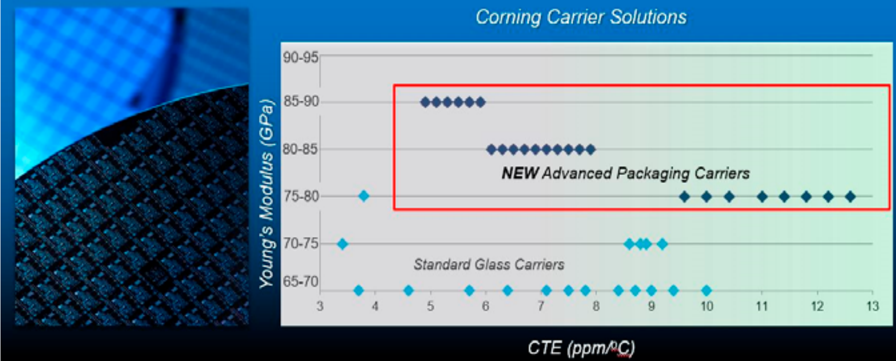


Figure 3: CTE and Young's modulus of APC wafer products from Corning Incorporated.

World No.1 Specialized IC Packaging Company

Wafer Bumping
RDL
WLP
Test
COG/COF

Look Beyond
Your Current Needs
to Make your Future Business Successful

▶ Webpage QR code
www.lbsemicon.com

www.facebook.com/lbsemicon

138, Cheongbuksandan-ro, Cheongbuk-eup, Pyeongtaek-si, Gyeonggi-do, Korea
TEL +82-31-680-1600 FAX +82-31-680-1798

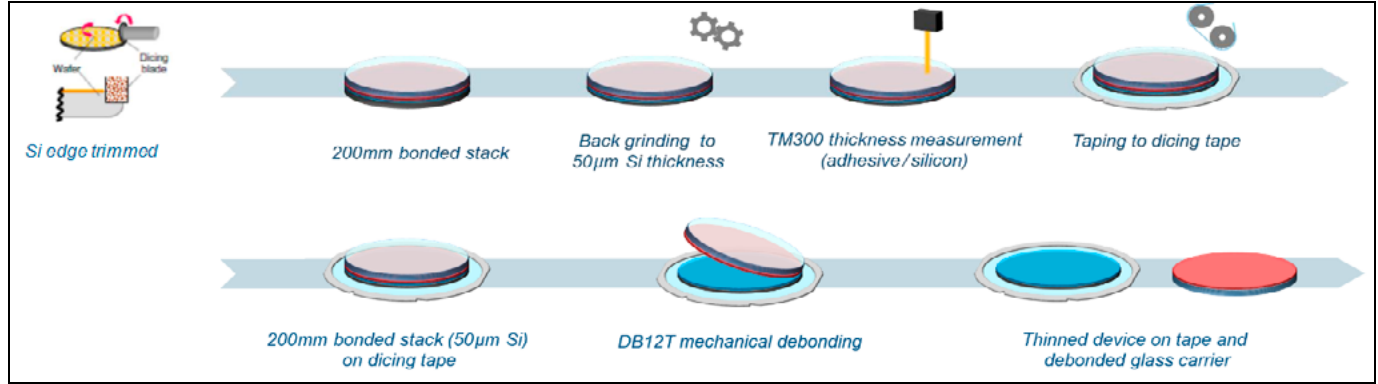


Figure 4: General process flow: edge trimming, bonding, backgrinding, taping, debonding.

after the device wafer has been bonded to the carrier. Bonding performance can be inspected by simply looking through the carrier (optical defect inspection) instead of sophisticated inspection tools required with Si carriers.

Flexibility. As the trend in the industry asks for thinner substrates, we believe that laser debonding will become essential moving forward. Having the flexibility now to use a carrier that can work with current mechanical debonding processes, and that aligns with the future thinning roadmap, can help companies save on development time and cost.

Below, we describe a demonstration of Corning glass carriers working with SUSS MicroTec's mechanical debonding tool.

General process flow. In order to demonstrate the ability to mechanically debond glass carriers, Corning's SG3.4 glass wafers (200mm diameter, 0.5mm thickness) were bonded to Si wafers (200mm diameter and 0.525mm thickness) (see **Figure 4**). The CTE of this glass is well matched with that of Si in the typical temperature range used for Si thinning and post-thinning processing. In order to conduct a meaningful experiment and mimic real-world semiconductor process conditions, we performed thinning down to a 50µm final thickness. The study started with Si edge trimming prior to wafer/glass bonding to prevent edge chipping during the grinding process. A C-type chamfer was used as the edge finish for the glass wafer. Wafer stack bonding was performed with a SUSS XBS300 temporary bonding system and two different market-proven, commonly used adhesive systems for mechanical debonding (one with device release, one with carrier release). Edge trimming and grinding details are discussed in the next section.

The subsequent metrology step controls the backgrinding process to ensure that the final Si thickness of 50µm is within the expected tolerance. In addition, the uniformity of the adhesive thickness can

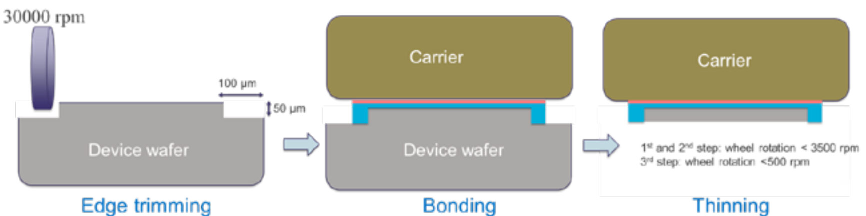
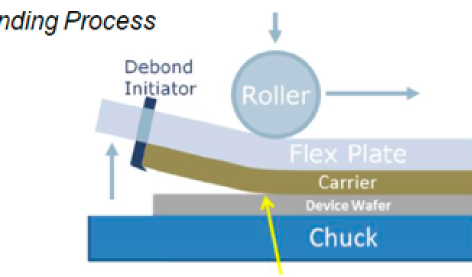


Figure 5: Cross-sectional view of edge trimming, temporary bonding, and backgrinding.

Tool Model:
SUSS XBC300 Gen2 Debonder (fully automated)



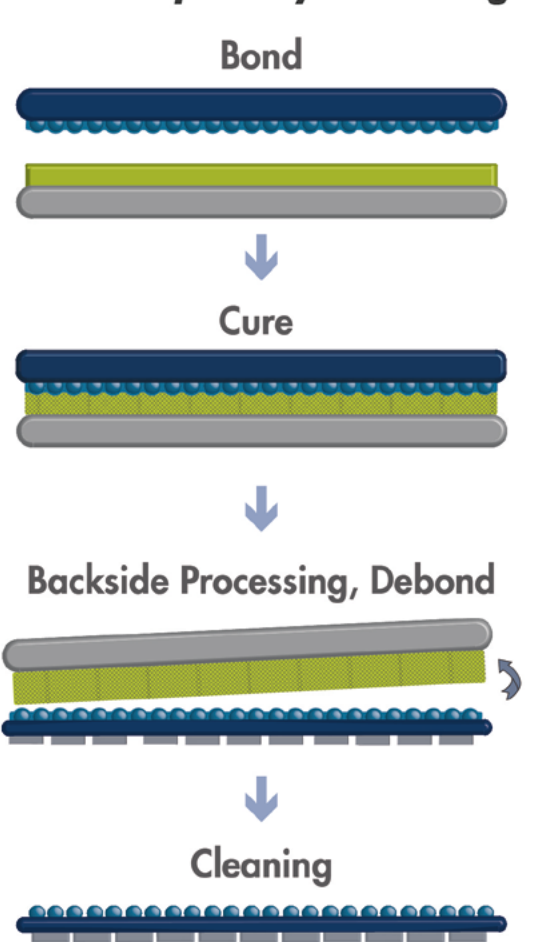
Debonding Results

Slot	Adhesive Interface	Glass Edge Type	Debonded Device	Debonded Carrier	Glass status
A1	Material A	c-shape	No traces	Adhesive traces at initiator	Ok
A2	Material A	c-shape	No traces	Adhesive traces at initiator	Ok
A3	Material A	c-shape	No traces	Adhesive traces at initiator	Ok
B1	Material B	c-shape	Traces of initiator	Adhesive traces at initiator	Ok
B2	Material B	c-shape	Small traces of initiator	Small adhesive traces at initiator	Ok
B3	Material B	c-shape	Small traces of initiator	Adhesive traces at initiator	Ok

Figure 6: Summary of debonding results.

Dual-Layer Solution

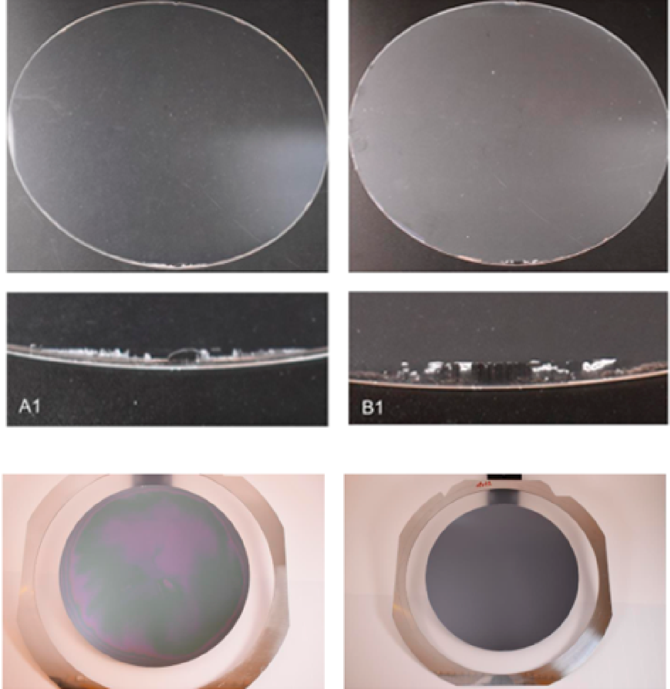
A path-changing direction for temporary bonding



Our unique dual-layer solution for high-temperature & high-stress applications found within the semiconductor industry

www.brewerscience.com

©2020 Brewer Science, Inc.



A and B device wafers with no damage

Figure 7: Successful debonding using a mechanical debonder. The carrier can be reused.

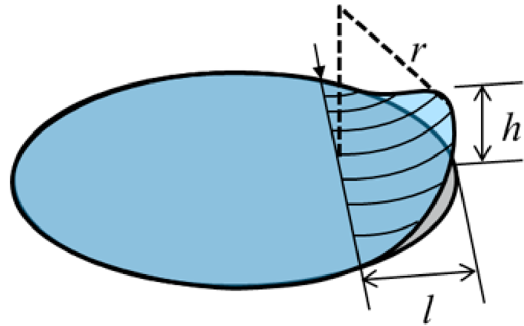


Figure 8: Schematic illustration of glass bending during debonding.

be monitored. In the next step, the device wafer is attached to the dicing tape before the final mechanical debonding process takes place. Finally, mechanical debonding is performed on a SUSS XBC300 Gen2 mechanical debonding system. This is a critical part of the study that needs to be established for a glass carrier to succeed as a material for mechanical debonding processes. Here, the wafer stack is placed with the silicon side on a vacuum chuck. A wedge-shaped initiator is used to initiate the separation between the carrier and device wafer. The initiator is lifted and positioned at a specific height, h. A flex plate is placed on top of the glass carrier, and with the help of a roller that moves away from the initiator point, the debonding continues until the carrier is fully separated. **Figure 6** shows a picture of the debonding tool, as well as a schematic showing the flex plate in action. Please refer to the stress calculation in the sub-section entitled "Stress calculation" that shows that the induced stress is much lower than the strength of the glass. The result shows the thinned device on tape and the

debonded glass wafer that can be cleaned to remove adhesive residues and recycled multiple times, which is common practice for glass wafers used in laser debonding processes.

Edge trimming and grinding conditions. Before bonding, an edge trimming process was applied to the Si wafer using a dicing saw tool (DFD6361) from Disco (see **Figure 5**). The purpose of edge trimming is to reduce the risk of interfacial delamination and edge chipping during the backside thinning process. The edge trimmed profile is 100µm in width and 50µm in depth. After bonding, a multi-step, backside thinning process was performed using the Disco grinder (DGP8761). The first step is to use a coarse wheel grit to remove the bulk of the excess wafer thickness until it reaches 92µm. The second step is to use the finer wheel grit to grind the Si thickness from 92µm to 52µm. The final step is to use the finest grit to precisely and slowly polish the Si thickness to the target thickness of 50µm.

Results. The debonding results are summarized in **Figure 6**. All samples were successfully debonded, independent of the adhesive system used, and no damage was observed on the wafers. The images in **Figure 7** show the intact carrier and device wafers with some imprints in the remaining adhesive layer at the initiator position, which is typical for mechanical debonding. The bulk adhesive is on the glass for material A (device release) or on the device for material B (carrier release). Adhesive residues or imprints of the initiator can be removed in the subsequent cleaning step. As mentioned above, the debonded glass carriers are in excellent condition with no mechanical flaws. After removing the adhesive traces on the glass surface, the carrier can be easily reused with no issue.

Stress calculation. The bending stress on the wafer during the debonding process can be calculated and compared

radius [mm]		l [mm]		
		35	40	45
h [mm]	1	613	800.5	1013
	2	307.3	401	507.3

Table 2: Calculated radius from typical lifting height and pivot distance values.

to the edge strength to assess the risk of glass failure due to bending. The bending stress generated on the glass edge can be

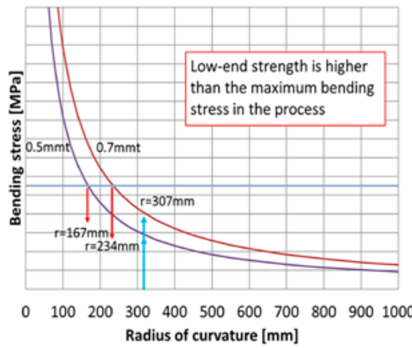


Figure 9: Relation between the radius of curvature and the bending stress.

estimated from the radius of curvature with beam bending theory as **Eq. 1** below:

$$\sigma = \frac{t}{2}\frac{E}{r} \qquad \text{Eq. 1}$$

where t is the wafer thickness, E is Young's modulus of the glass wafer, and r is the bending radius during the debonding process.

The bending radius, r, is obtained from the lifting height, h, and the distance at pivot from lifter, l, as shown in **Table 2**. **Eq. 2** is based on the assumption that the deformation is simply cylindrical.

$$r = \frac{l^2 - h^2}{2h} \qquad \text{Eq. 2}$$

The calculated radius of curvature r from the typical lifting height h and the pivot distance are listed in **Table 2**. The smallest radius is 307mm when the lifting is 2mm and the pivot distance is 35mm. **Figure 9** plots the relationship between the radius of curvature and the bending stress of glass wafer for two thicknesses, 0.5mm and 0.7mm. A horizontal, blue line indicates the typical, low-end edge strength value of glass wafers made by Corning. The low-end strength value is much higher than the stress generated by the tightest curvature 307mm during the debonding process (blue arrow marks). Therefore, the glass wafer can be used in the debonding process without failure. From the low-end strength line and curvature, the allowable bending curvatures are 167mm and 234mm for 0.5mm and 0.7mm thick glass, respectively.

Summary

For semiconductor wafer thinning, glass is an ideal carrier material because of the following: 1) its ability to deliver variable CTE to match the wafer CTE; 2) flexible thickness to minimize shape change during thinning and post-thinning processing; 3) transparency to enable bonding quality control; and 4) compatibility with multiple debonding technologies. This paper demonstrated successful debonding.

Acknowledgements

We thank Hsiang-Hung Chang of Industrial Technology Research Institute (ITRI) in Taiwan for providing Si wafer edge trimming and thinning. We also thank MK Cornfield of Corning Incorporated for providing editorial support to this article.

Reference

1. J. Zhang, Y. Xiao, A. Teng, I. Dutta, V. Singh, L. Yang, M. Li, "Advanced packaging carriers for WLFO applications," *Chip Scale Review*, pp. 20-26, Jul/Aug, 2019.

Biographies

Julia Brueckner is the Sales & Business Development Manager at Corning Incorporated, Wiesbaden, Germany. She joined Corning in 2019 to support the Precision Glass Solutions (PGS) business unit and is responsible for customers in the EMEA region. She received her PhD in Physical Chemistry from Heidelberg U. Email BruecknеJ@corning.com

Jay Zhang is the Business Development Director at Corning Incorporated in Corning, NY, USA. He joined Corning in 2000 and is responsible for new business development as well as program management. He obtained his PhD in Applied Physics from Yale U. and an MBA from Cornell U.

Automating RF PA device manufacturing to accelerate 5G wireless rollout

By Limin Zhou, Julius Ortega [MRSI Systems, Mycronic Group]

The successful rollout of 5G wireless depends on the deployment of a significant quantity of base stations with a higher density of radio frequency (RF) power amplifiers (PA) compared to the older 4G technology. Each 5G base station has more channels, and each channel needs one RF PA device. These devices are key components that boost the RF power signals in base stations.

Before the 5G era, silicon-based lateral double-diffused metal oxide semiconductor (Si-LDMOS) was the mainstream solution in the RF PA market for 4G long-term evolution (LTE) technology. Those devices are now regarded as almost commodities with a high level of technical maturity. Traditional Si-LDMOS performs well at 3.5GHz and below, but is unable to meet the higher frequency requirements for 5G applications. The operating frequency of gallium arsenide (GaAs) applications is mainly within 8GHz, suitable for medium- and low-power devices for 5G cell stations. In the high-power RF application, gallium nitride (GaN) has obvious advantages and is a necessary material for 5G macro stations. GaAs and GaN are on the rise to replace silicon as the backbone of power switching technology thanks to better power systems efficiency, performance, and cost, of GaAs and GaN. As wide-bandgap (WBG) semiconductor materials, both GaAs and GaN devices are more efficient than Si. GaAs/GaN devices are replacing Si-LDMOS devices in 5G base stations, radar, and avionics, as well as other broadband applications. In future network designs, GaAs/GaN and other WBG materials will replace most of the existing Si-LDMOS devices due to limitations of their physical properties [1]. Generally speaking, 5G base stations will incorporate GaAs/GaN-based PAs for the higher frequencies, while Si-LDMOS will remain just a part of the mix for lower bands [2]. According to Yole's report [3], the total GaN RF market will increase from $740 million in 2020 to more than $2 billion by 2025, with a compound annual growth rate (CAGR) of 12%. Telecom infrastructure and military radar are the main drivers for RF GaN. The telecom infrastructure market segment for 5G wireless will enjoy a 15% CAGR.

This article discusses an essential element in automating RF power amplifier device manufacturing—a fully automated die bonding solution to support the flexible, high-precision, high-volume manufacturing required for large-scale deployment of RF PA devices in 5G applications.

Manufacturing requirements and challenges

RF PA devices have two major die bonding assembly methods: eutectic and epoxy. The eutectic process, which is the most common die bonding technique for power electronic devices, has historically been the only method for making higher power RF PA devices used in base stations. The eutectic alloy between the die and the heat sink is typically gold-silicon (AuSi) or gold-tin (AuSn), which gives the best thermal conductivity and lowest possible void rate after bonding. On the other hand, the traditional epoxy process may be cheaper, but has lower thermal conductivity and a higher void rate after bonding. This may be sufficient for some low-power/low-reliability devices. In recent years, some new die bonding adhesive materials and processes have been developed to replace AuSi/AuSn solder for cost reduction for high-power devices. For example, the pressure-less nanosilver sintering materials are expected to have good thermal conductivity for high-power devices and to be able to adapt the standard epoxy dispensing equipment and process. The materials and processes have not yet matured enough for RF PA devices.

There are five major challenges to achieving a good die bonding process using a fully-automated solution in order to enable multi-process and multi-die manufacturing required for RF PA device production for 5G base stations. The sections below discuss these challenges.

RF PA chip handling. Electrostatic discharge (ESD) is a major factor that can potentially destroy or damage the RF PA chips. To solve this problem, the die bonder should be properly grounded and periodically tested for ESD compliance for all work surfaces that contact the product to minimize or eliminate ESD risk during production.

These RF PA chips have unique characteristics—they may be larger than other chips, with an aspect ratio of more than 10. They are long and thin dies (thickness can be as little as 30µm), with air bridges or sensitive structures on the top that can be damaged if excessive force or stress is applied to the top. These characteristics require delicate handling including placement force control that is only achieved with real-time force feedback. The die pick and place process uses vacuum collets that hold the chip edges. GaAs and GaN are naturally brittle materials. The bonding force ranges from 10g to 100g, which must be tightly controlled to avoid damage and for the best bonds.

GaAs and GaN eutectic processes. Gold-tin (AuSn 80/20) is the alloy most commonly used in the industry for bonding GaAs and GaN chips, because of its compatibility with gold-based components and its long-term stability. The backsides of GaAs and GaN chips are plated with a gold layer to provide a good thermal and electrical interface and allow flexibility in the die attachment method. The solder preforms (12~50µm in thickness) are often used in this process. The solder preform size is determined experimentally. Al_2O_3, Cu-W, Cu-Mo, and Si and SiC, etc., are the common materials for substrates.

The lowest melting point of the AuSn 80/20 alloy is 280°C. A 2% decrease of

Advanced Packaging Carriers

from Corning Precision Glass Solutions

- Wide range of customizable CTEs
- High-stiffness properties to reduce in-process warp
- All wafer sizes available in a wide range of thicknesses
- Glass portfolio with alkali-free options
- 4-6 week lead time for samples

Learn more at www.corning.com/carrier

©2021 Corning Incorporated. All Rights Reserved.

tin to 18% increases the melting point to 350°C. The eutectic reflow temperature should be 20-40°C higher than the melting point. Because of reliability concerns, a maximum reflow temperature of 320°C for a maximum of 30 seconds is recommended for GaAs and GaN. The temperature profile is dependent on the eutectic stage, the size and number of dies, and the substrate, etc. The first step of the process is to pick and place the solder preform while at a pre-heating temperature. The second step of the process is to pick and place the die. The die are placed on top of the solder preform either at the reflow temperature, or just before reaching it. The die are placed with a force of 10~100g and scrubbed according to some preprogrammed parameters. In some cases, the preform is pre-deposited on either the substrate or the PA chip.

LDMOS eutectic process. AuSi is used for ultra-high thermal demand applications, such as silicon-based LDMOS. The packaging or substrate materials of LDMOS RF PA devices are Cu-W or Cu-Mo. With AuSi bonding, an additional alloy material is not included. Instead, the process relies on the diffusion of gold and silicon that occurs at a high temperature. This process is done in the presence of forming gas with 5-10% hydrogen.

AuSi eutectic bonding occurs at a high melting temperature of 363°C. In order to maintain the LDMOS performance, the bonded chip-on-substrate (CoS) needs to be processed quickly and removed from heat as soon as possible. The bonding force of the eutectic process may be set to 30~100g. Scrubbing must be applied during die attachment to eliminate voids.

Void-free processing. Solvent cleaning of solder preforms and substrates/packages is recommended to remove any existing surface contaminants (from machining, packaging, handling, etc.). GaAs and GaN can be cleaned using an oxygen or plasma cleaning process before the eutectic process. During the eutectic process, an inert gas (nitrogen or nitrogen with 5-10% hydrogen) is used to surround the parts and remove oxygen during reflow, preventing oxidation of the interconnect surface.

Reliable eutectic die attach of high-power/high-frequency devices requires nearly a void-free attachment. A better than 95% void-free attachment is achievable with a scrub assist. An oxygen level >10,000ppm contributes to voiding poor quality solder joints. The oxygen level in the eutectic chamber of <5000ppm is necessary to achieve a low void rate. The oxygen level should be controlled <1000ppm to have a buffer for different eutectic processes. For process control, the amplitude of the scrub cycle, time of scrub, and force, must all be optimized to form a good void-free attachment. Scrub-assisted automatic die attach is a common process that relies on "scrubbing" of the die into the gold or package surface to break up the oxidation layer and have good mixing to form the eutectic alloy. The scrubbing process usually is a 5-10 cycle scrubbing movement under a certain amplitude and frequency in X-Y-Z directions. During the eutectic process, the scrubbing process distributes the solder and removes the gas bubbles that are among the main reasons for void generation.

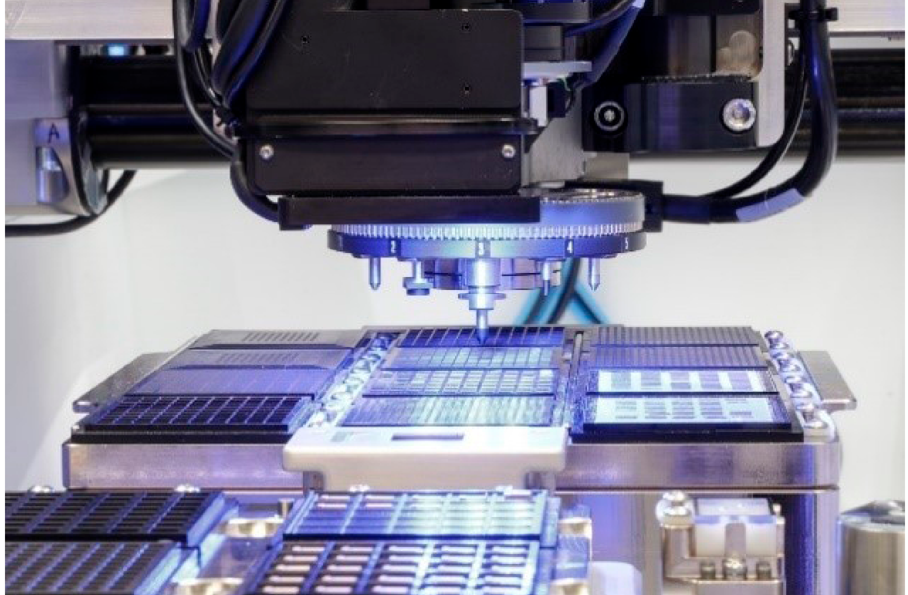


Figure 1: MRSI's "on-the-fly" tool changer.

Epoxy process. The epoxy process has mostly been used for attaching passive components, such as capacitors, but not active components in RF PA devices. In recent years, new adhesive materials have been developed to replace AuSn. Silver micron-particle sintering joining technology developed by Prof. Katsuaki Suganuma of Osaka University has enabled pressureless die bonding in ambient temperature at a low cost. Because this technology showed high reliability at high temperatures over 250°C, its use is spreading as a key next-generation power semiconductor die bonding technology. There is a lot of ongoing research and development work on the pressureless nano Ag sintering materials and sintering processes [4]. Potentially, the new materials will be used for high-power RF PA [5-7].

The thinner the epoxy bond lines, the higher their thermal conductivity. Achieving these thin bond lines requires a careful design of the dispense pattern, die placement and process parameters during the epoxy process. A thicker bond line may help mitigate CTE mismatches between the chip and the substrate, especially for GaN dies (that can handle a slightly higher mismatch), but the resulting increase in thermal resistance may not be an acceptable trade-off. High-performance stamping and dispensing functions, as well as bonding force control, provided by the die bonder are necessary for a satisfactory bond line control.

MRSI automation solution

MRSI has developed fully-automated die bonding solutions to enable multi-process and multi-die manufacturing of RF PA devices for 5G base stations. These systems have the flexibility and high throughput required for this high-mix and high-volume manufacturing environment and solve the challenges outlined above. The sections below summarize the bonding solutions.

Automation solutions for RF PA. Our new assembling solutions have two platforms, the 1.5µm MRSI-H-LDMOS

DISCOVER THE HSWF

Advanced Packaging enables the world's most innovative products for 5G, AI, Edge Computing, AiP, and Integrated Power Management.

Consumer, Automotive and IoT devices are getting smaller and thinner, 2.5D and SiP multi-die packages are becoming more complex, InFO and Panel Fan-Out are driving large-format batch processing, and volume demands are rising.

These new challenges demand a comprehensive solution that breaks traditional boundaries for efficient multi-die assembly.

Introducing the **High-Speed Wafer Feeder** from Universal Instruments – **The world's fastest rapid-exchange multi-die feeder**. Combined with Universal's FuzionSC™ Platform, it is the **ultimate multi-die solution for heterogeneous integration**.

- 16K cph dual-wafer tables, low-force pick heads
- Up to 52 unique wafers types at once; 4", 6", 8", 12"
- One-step "wafer-to-placement" handoff
- Synchronous wafer stretch and storage
- Maximum panel sizes up to 635mm x 610mm
- Maximum die size range with thinnest die

WAFER CAPACITY
to minimize replenishment rate

4" 6" 8" 12"

SPEED
to meet volume requirements

LARGE SUBSTRATE
to reduce manufacturing costs

MULTIPLE DIE TYPES
to maximize utilization

THIN DIE
to maximize sub 100-micron yields

uic.com

and the traditional 5µm MRSI-705 with horizontal turret. Both platforms support AuSi and AuSn process requirements and have high-performance stamping and dispensing options.

Both of our products come with an integrated turret that can hold up to 12 tips. The turret enables "on-the-fly" tool changing to achieve zero-time between tip changes. **Figure 1** illustrates our "on-the-fly" tool changer. Any version of custom die pick up tip or epoxy stamping tip can be used in the turret. It can flexibly handle multiple dies, multiple processes, and multiple products in one machine. This helps users to create flexible production lines that can be rapidly reconfigured for different products.

Furthermore, high-volume production is aided by the in-line eutectic die bonding system we developed. By utilizing a progressive heat stage system that indexes through heat zones, eutectic die attach can be performed on parts transported in "boats" or carriers that are loaded, processed, and unloaded to cassettes automatically. The in-line eutectic system is a "Universal" Progressive Indexing Conveyor (**Figure 2**). It is a modularly-designed common architecture across multiple machine platforms (MRSI-705, MRSI-M3, MRSI-H), and supports both AuSn and AuSi eutectic processes. This in-line mode is also applicable to the epoxy process.

Temperature profile control. To achieve eutectic bonding, a heating station is typically employed that can ramp up and ramp down the temperature rapidly and precisely to maintain good temperature uniformity on the hotplate. Our eutectic station is a pulsed heating station, with a maximum temperature of 450°C, a temperature control accuracy of <±1°C, a temperature ramp-up speed of up to 40°C/s, and a cool-down speed of 30°C/s.

Oxygen environment control. The eutectic process is performed in an inert environment to prevent oxidation of the bonding surfaces, as the RF PA device is subjected to heat. We used a specially designed gas cover over the eutectic station. The flow of forming gas is carefully managed to create an oxygen-free environment for the eutectic process. The standalone eutectic station can achieve a <100ppm oxygen level environment and the indexing eutectic station can achieve a <500ppm oxygen level environment, using pure nitrogen forming gas. Both cases far exceed the process requirements mentioned earlier.

Scrubbing process. Scrubbing is a critical process step in the formation of a common material (bond) between AuSi and AuSn by forcing out air to reduce voiding. Also, the solder is better distributed across the die and the pressure assists the diffusion process. As a starting point, our software includes a pre-programmed library of scrub patterns to guide users as they quickly develop their process. The scrubbing parameters are completely programmable for customization to the specific process. Scrubbing consists of applying vertical and lateral forces to a chip during its placement. The chip is usually moved in a figure eight pattern that is repeated for several cycles. Movements in alternate directions are also possible. Rotational scrubs are sometimes employed. Scrub parameters consist of amplitude, speed, and frequency in the x, y, and theta directions. Parameters are determined by process requirements, such as the surface area of the chip, and process constraints, such as proximity to adjacent die.

Bond line control for the epoxy process. Our epoxy stamping process uses a rotating stamping-well with multiple epoxy grooves presenting epoxy for stamping. The dispensing process uses time-pressure dispensing units with precision fluid control technology. The substrate surface is measured by a three-point laser height system that maps the plane to ensure that the gap between the needle and surface is maintained at all locations. We also provide an option for a confocal height sensor to measure bond line thickness. Consistent bond lines are achieved through a combination of precision epoxy volume control and closed-loop force control.

RF PA process results

Below, we share the performance results achieved using the MRSI-H-LDMOS. This system included an indexing conveyor for high-volume manufacturing. We used 60 industry standard glass dies to test the machine's pick and place accuracy, the 3σ results of x<1.21µm and y<0.84µm surpassed the machine specification <1.5µm @3σ. The machine oxygen level at the eutectic bonding station was tested by using a Pro OX-100 Digital Oxygen Purge Monitor. The results show the oxygen level at the eutectic bonding area is <100ppm.

The real AuSn process was done for two different size GaN chips bonding on a substrate by using AuSn solder preforms. Chip sizes were about 3 x 1mm and 4 x 1mm. Both chips were 100µm thick. Au-Sn solder preform sizes were slightly smaller than the chips. As the carriers were indexed through the machine, parts were heated to a pre-heat temperature before arriving at the bond station. The bond station was ramped from the preheat to reflow temperature during the processing. Optimal force and scrub parameters were found through process development. Metrology revealed that the bonding process accuracy met the requirements well. The results are shown in **Figure 3**. The left image shows 15 samples, the right image shows the real size sample. These

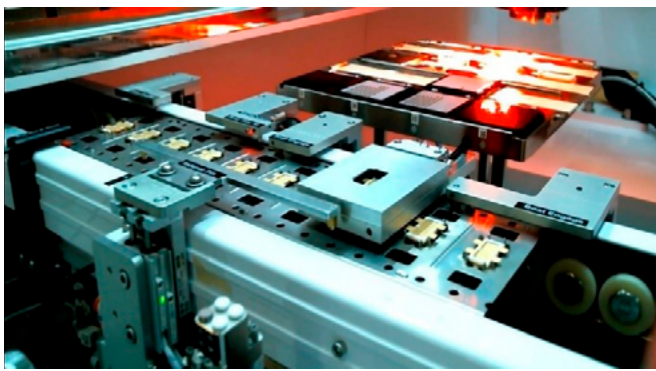


Figure 2: "Universal" progress indexing conveyor.

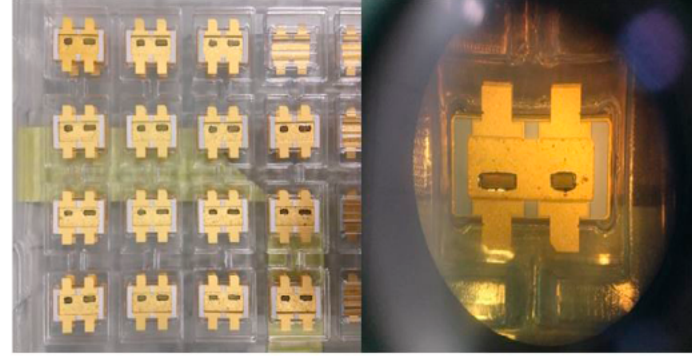
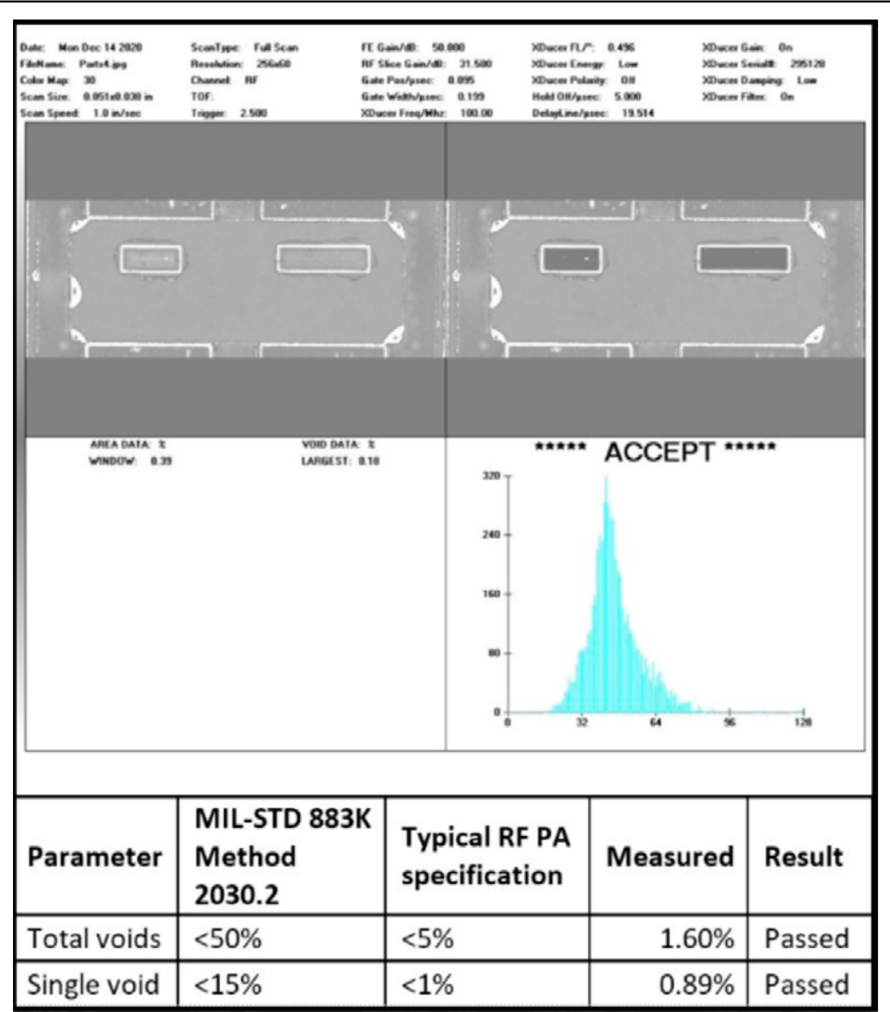


Figure 3: 15 samples show solder flowed evenly without oxidation.



Parameter	MIL-STD 883K Method 2030.2	Typical RF PA specification	Measured	Result
Total voids	<50%	<5%	1.60%	Passed
Single void	<15%	<1%	0.89%	Passed

Figure 4: Voiding results by scanning acoustic microscope results for the five samples.

images show that all of the 15 samples of the solder flowed evenly without oxidation.

After the build, five samples were tested for voiding through the use of a scanning acoustic microscope (SAM). The average total void is 1.6% and the average single void is 0.89%. The results are shown in **Figure 4**.

Summary

We have developed a highly flexible automation solution to support multi-die, multi-process production for RF PA devices for 5G base station applications. The tests show that the machines achieve high die bonding accuracy and very low void percentage with high production throughput to support the GaN AuSn eutectic process. The machines also support the AuSi eutectic process by using different pre-heat and eutectic temperatures and can be configured to add epoxy dispensing and epoxy stamping. Our fully-automated solution for RF power amplifier device manufacturing meets the challenges posed by the accelerated deployment of 5G at an attractive return on investment for users.

References

1. M. Di Paolo Emilio, "RF power semiconductors for 5G shift to WBG materials," September 4, 2020, Electronic Products.
2. Mark LaPedus, "Power Amp Wars Begin For 5G," Aug. 24, 2020, Semiconductor Engineering.
3. "GaN RF market applications, players, technology, and substrates 2020," Yole Développement report, May 2020.
4. Paul Shepard, "Pressureless sinter joining for next-gen GaN & SiC power semis," Sept. 01, 2017, EEPower.
5. H. Yang, et al., "Improvement of sintering performance of nanosilver paste by tin doping, 22 Jan. 2020, J. of Nanomaterials.
6. XiaominWang, et al., "Pressureless sintering of nanosilver paste as die attachment on substrates with ENIG finish for semiconductor applications," Volume 777, 10 Mar. 2019, pp.: 578-585, J. of Alloys and Compounds.
7. K. S. Siow, *Die-Attach Materials for High Temperature Applications in Microelectronics Packaging, Materials, Processes, Equipment, and Reliability*, pub. Springer, 2019.

Biographies

Limin Zhou is a Senior Director of Strategic Marketing at MRSI Systems, Mycronic Group, MA, USA. Prior to joining the company in 2019, he was Senior R&D Director at NeoPhotonics, China, NPI & Product Engineering Director in Oclaro Asia, and NPI Operation Director in both JDSU and SAMN-SCI China. He also worked in Sebit as co-founder of a start-up laser company. His career began at Chartered Semiconductor. He has a PhD in Automation from Xi'an Jiaotong U.; Email limin.zhou@mycronic.com

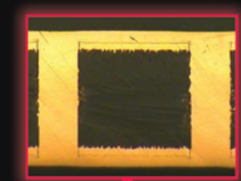
Julius R. Ortega is a Principal Applications Engineer at MRSI Systems, Mycronic Group, MA, USA. He joined the company in 2000 and started his career at Texas Instruments (Baguio City, Philippines) as Test Equipment Engineer (Manufacturing); he was also a Field Service Support Engineer for Schlumberger (Semiconductor Test and Assembly Division) supporting Intel (Philippines, Malaysia & Israel) Asia. He has a BS in Electronics & Communications Engineering from Saint Louis U. (Baguio City, Philippines).

IC substrate designs are becoming increasingly diverse.

WE HAVE YOUR SOLUTIONS.

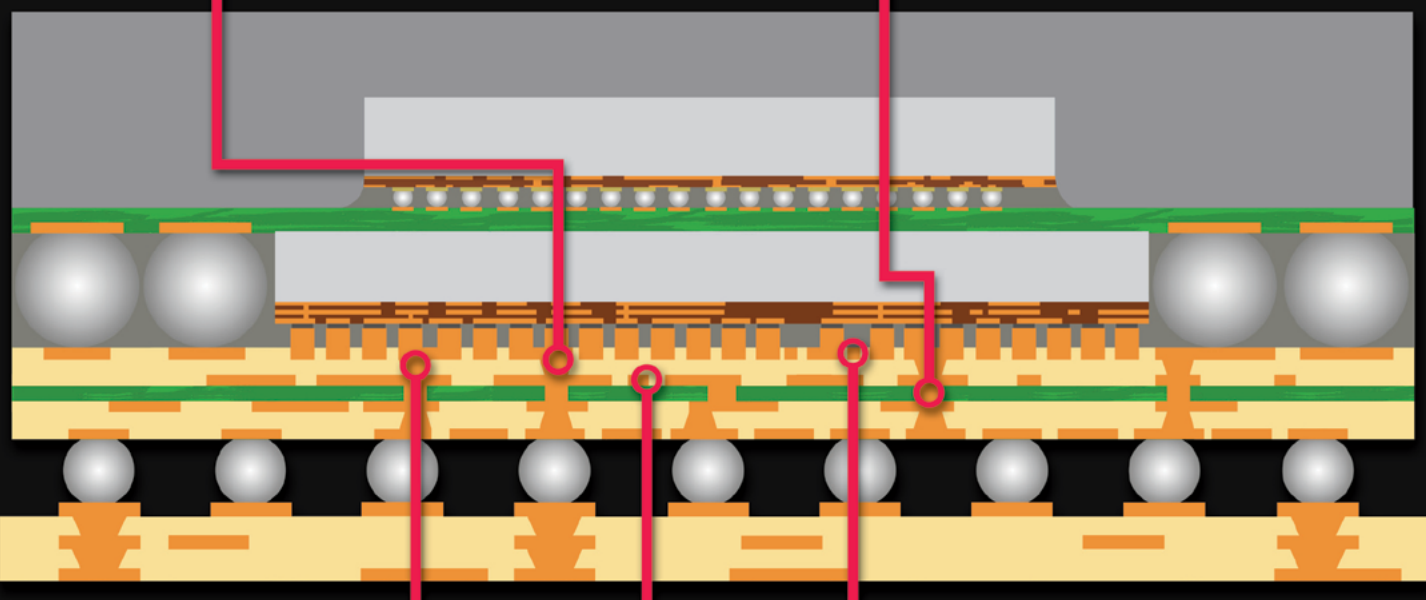
Systek UVF 100 2-in-1 Plating for RDL

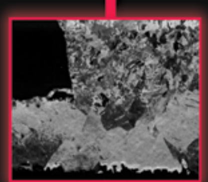
Ultra via filling process for IC substrate RDL that fills micro vias and copper traces with excellent co-planarity and feature uniformity



MacuSpec THF 100

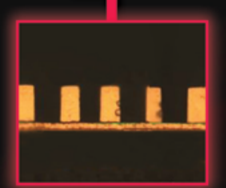
Single step copper through hole filling for core layer that provides enhanced thermal and mechanical design options





Systek SAP

High-performance semi-additive build-up process allows enhancements for high speed signals and very fine line routing



Systek ETS

Embedded trace substrate plating 5/5 micron line/space enabling next generation miniaturization of IC substrate RDL

CircuEtch 200

High-performance flash etching process for circuit formation that enables vertical trace sidewalls without undercut

macdermidalpha.com

© 2021 MacDermid, Inc. and its group of companies. All rights reserved. "(R)" and "TM" are registered trademarks or trademarks of MacDermid, Inc. and its group of companies in the United States and/or other countries.

Packaging trends for automotive LIDAR applications

By Ajay Sattu, Weilung Lu, Mike Sleiman, Burt Barber [Amkor Technology, Inc]

Revolutionizing the safety of the modern car will reduce road traffic fatalities and associated costs. Each year, approximately 1.35 million people die due to road traffic crashes worldwide. And, these accidents cost most countries 3% of their gross domestic product [1]. Human error is the leading cause for a majority of these traffic fatalities. According to the National Highway Traffic Safety Administration's (NHTSA) annual report for 2018 (published in 2020), nearly 34,000 crashes resulted in fatalities in the United States; additionally, 1.9 million crashes resulted in injury and 4.8 million crashes resulted in property damage [2]. While automotive car manufacturers (original equipment manufacturers [OEMs]) have integrated the modern car with a suite of sensors, such as radio detection and ranging (radar), cameras, inertial measurement units (IMU), and an anti-lock braking system (ABS), continued improvements will further automate driving tasks.

In recent years, light detection and ranging (LIDAR) technology has gained viability for applications such as advanced driver assistance systems (ADAS) and autonomous driving (AD). As the automotive industry pushes the safety envelope of the newer vehicles with ADAS and AD capabilities, the variety of state-of-the-art solutions is promising. Most OEMs and system (Tier 1) suppliers believe a combination of LIDAR, radar and cameras is essential for a robust safety platform.

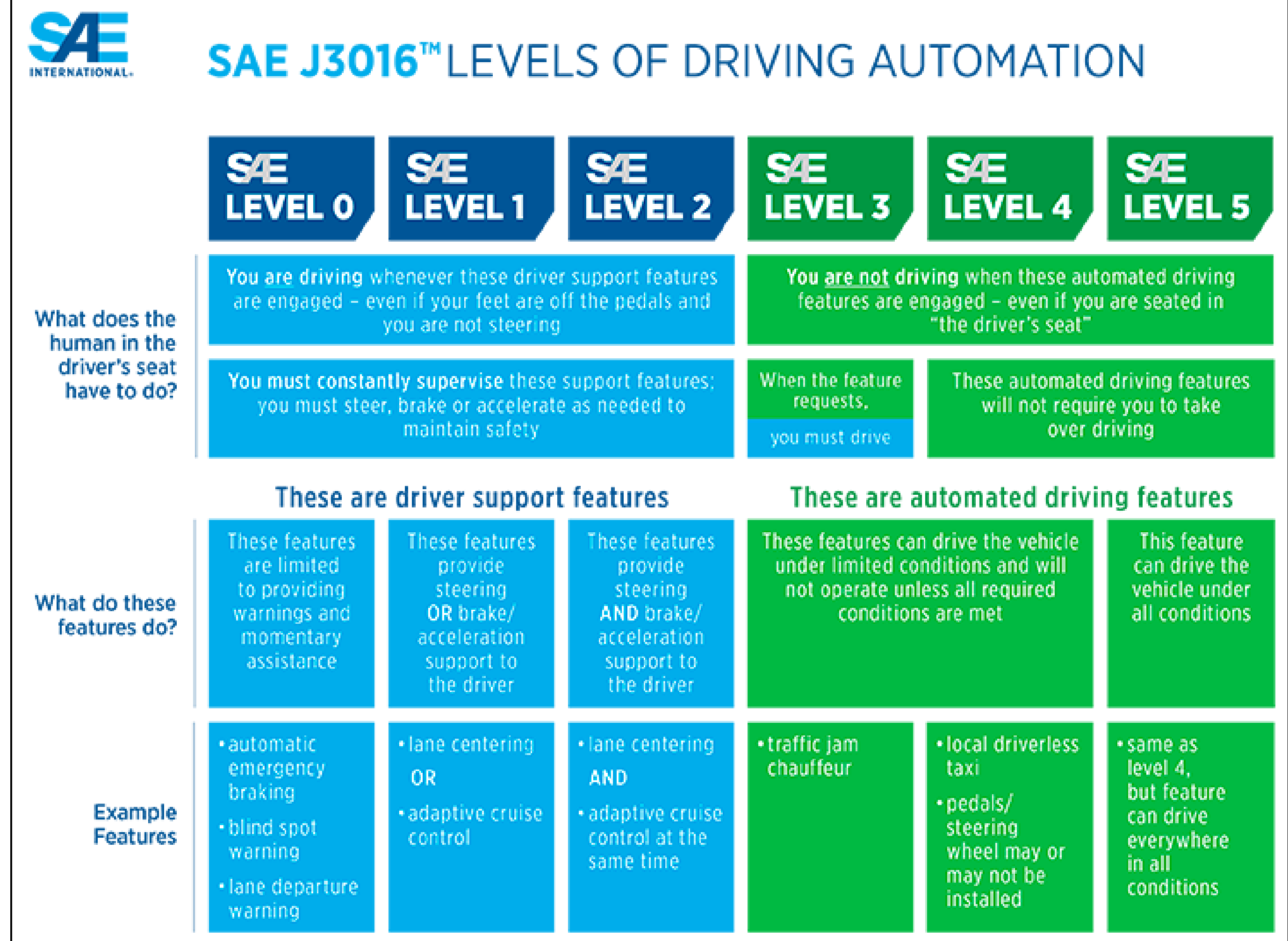


Figure 1: SAE autonomous driving levels. SOURCE: SAE International

Figure 2: Light vehicle forecast and ADAS levels. SOURCES: Yole, IHS Markit

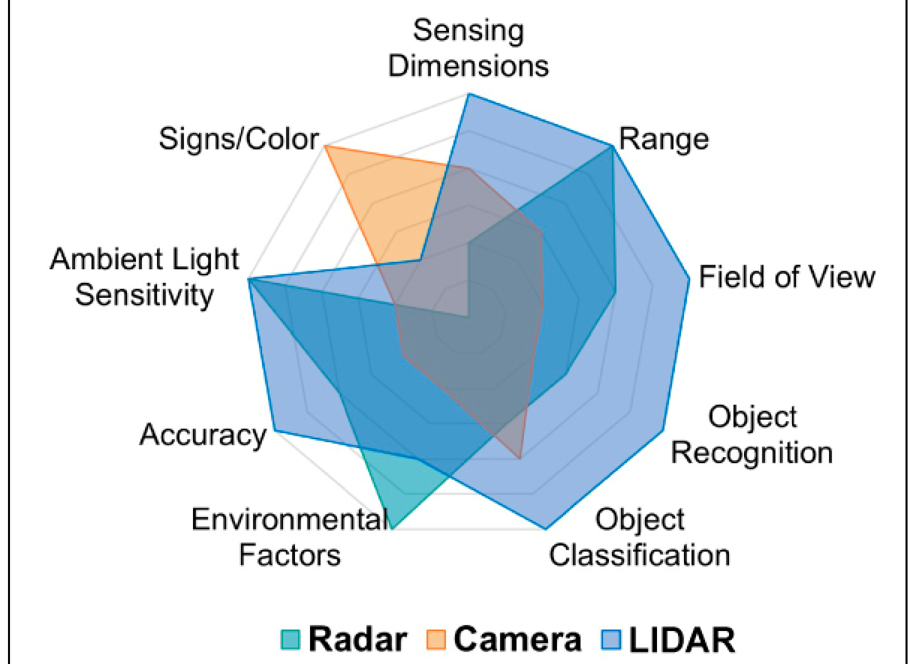


Figure 3: Relative comparison of radar, camera and LIDAR. SOURCES: Quanergy, Velodyne

Industry trends

According to SAE International (formerly the Society of Automotive Engineers [SAE]), the automated driving capabilities of vehicles can be defined from Level 0 to Level 5. The general description and guidelines of various levels, according to the SAE J3016 standard, are seen in **Figure 1**. Some of the key driver assistance features each of these levels enable are discussed below. For example, Level 1 includes automatic emergency braking (AEB) and lane departure warning system (LDWS) features, while Level 2 further enables safety options such as lane keeping assist (LKA) and adaptive cruise control (ACC). For some extended periods of time, a driver can take his/her hands off the steering wheel and foot off the pedals in Level 2 vehicles, enabling partial automation. Though Level 2 features can intervene in certain driving scenarios, the driver is expected to remain attentive on the driving environment. As such, bigger challenges remain in enabling Level 3 as vehicles migrate from partial to conditional automation.

Vehicles with Level 3 will enable features such as traffic jam assist (TJA) and driver monitoring system (DMS) as the driver-to-machine transition occurs. Unlike Level 2, Level 3 places the burden of monitoring the surroundings on the vehicle's sensor suite. However, the shift from Level 2 to Level 3 has been granular, as the industry defined an intermediate level called 2+. Level 2+ is empowered by high-definition maps with foresight of the horizon in both optimal and sub-optimal driving conditions. Essentially, Level 2+ heightens a vehicle's understanding of its path, especially during absence of lanes and unfamiliar driving destinations. Beyond Level 3, ADAS Levels 4 and 5 will include autopilot (AP) on highways and everywhere else, with high and full automation capabilities that are a must for robotic vehicles.

Most vehicles manufactured today are Level 0, however, it is expected that the adoption of Level 1 and above will increase as shown in **Figure 2**. For example, in 2019 one in every six cars sold was equipped with Level 2 and above capability. However, towards the end of the decade, nearly one in two cars is expected to be at Level 2 and above capability. The typical approach of most OEMs has been to design Level 2 using multiple radar and camera sensors. While this has been acceptable so far, relying on just radar and camera sensors may not be sufficient to enable Level 3 and higher levels. Other sensors such as LIDAR are gaining attention because of their complementary nature to radar and cameras. **Figure 3** shows a comprehensive view of how each of these sensors compares against each other under similar measurement conditions.

Qualitatively, cameras require significantly more computing power due to the image processing for the acquired images. On the other hand, LIDAR sensors rely on analog detection or statistical methods to generate point cloud images. So, fewer number of compute cycles are required with LIDAR. While LIDAR sensors have better range, resolution and accuracy than cameras, LIDAR cannot replace cameras because of a camera's ability to recognize road traffic signs and different colors. Alternatively, both LIDAR and camera sensing benefit from using radar as an antecedent technology for ADAS systems. For example, operation of camera sensors can be impaired by snow, while weather conditions can change the refractive index of the propagation medium and reduce the possible range of LIDAR.

PROCESS SOLUTIONS, EQUIPMENT AND SERVICES

Keeping It *Cool* for "Beyond Moore" Advanced Packaging

Lower Temp Cure with Vacuum

Your roadmap looks cooler than ever.

YES's industry-leading vacuum cure lets you take the temperature down, to make those advances real. Reduce stress/warpage in 3D stacks. Leverage the all-copper interconnect trend. Wafer or panel, R&D lab or high-volume fab – we've got you covered. YES supports your move to low-temp technology with unrivalled film quality, excellent yield and superior throughput.

Yield Engineering Systems, Inc.

Call: **1-510-954-6889** (worldwide) or **1-888-YES-3637** (US toll free)

www.yieldengineering.com

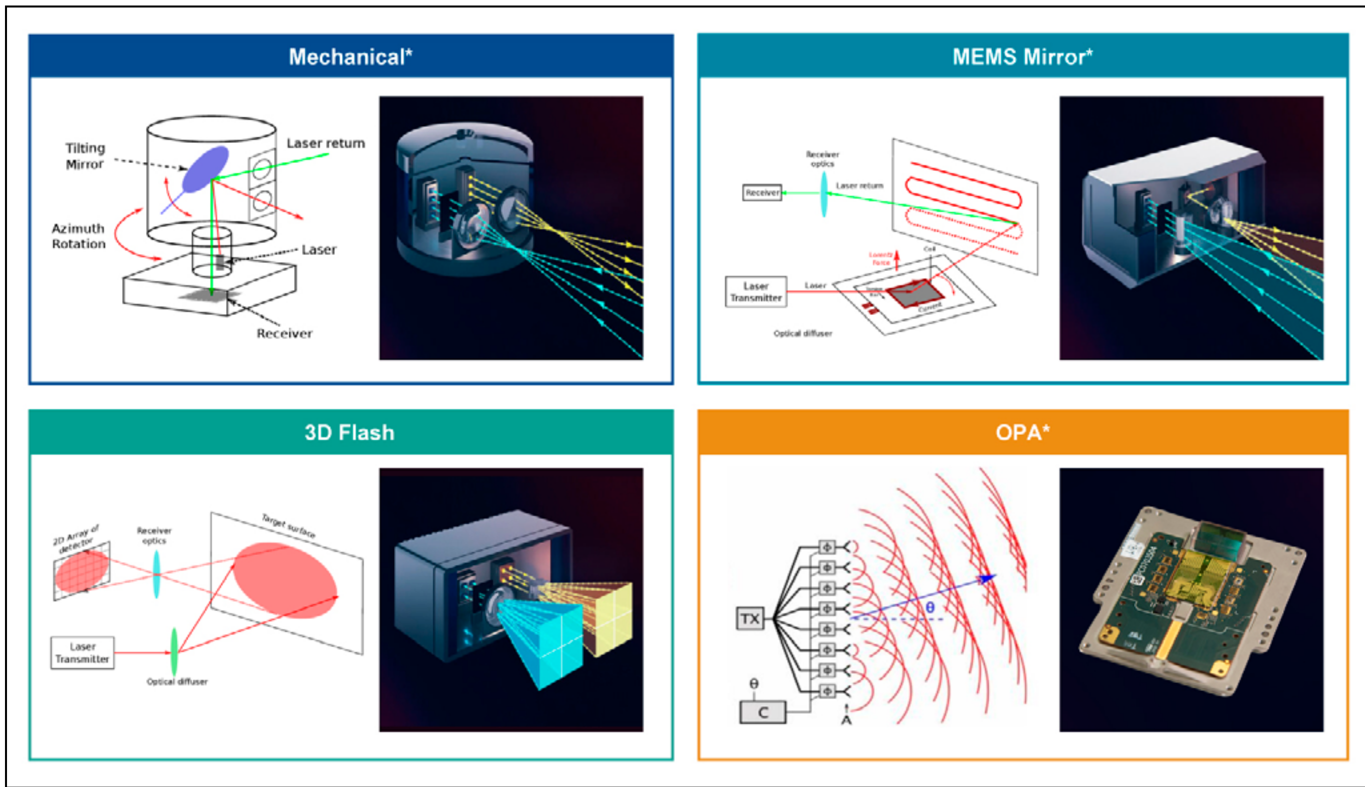


Figure 4: LIDAR beam-steering technologies [3]. (* Indicates scanning mechanism.)

LIDAR sensor landscape

To understand the underlying driving forces, the current landscape of the LIDAR sensor market can be broadly divided into four segments: measurement technique, emitter source, detector, and beam steering. From a measurement perspective, two dominant approaches are being pursued: time of flight (ToF) and frequency modulation continuous wave (FMCW). In ToF, range is measured by determining the difference in time of transmission and time of arrival of the pulse. The pulses used in such systems tend to be of very high power, but with narrow pulse width. Detectable range is directly proportional to the peak power of the pulse. In this measurement technique, range of the object is measurable, but not velocity.

With ToF, signal-to-noise ratio (SNR) issues are higher, especially in bright conditions. Because of achievable receiver sensitivities of current ToF systems, range is often limited to 100-200m. On the other hand, FMCW is relatively immune to SNR problems because this technique relies on the number of transmitted photons, not on the peak laser power. Additionally, because of the coherent detection nature, only the relevant wavelengths are amplified for signal processing. FMCW enables detection of both range and velocity of objects at a relatively lower power.

In terms of emitter technology, most designers prefer laser diodes over fiber lasers or other types because they offer better cost, performance and system-level integration. Among the oft-used laser diode designs, edge-emitting lasers (EELs) and vertical-cavity surface emitting lasers (VCSELs) are being discussed extensively. Because light is emitted from the side in EELs, they are better suited as discrete elements rather than arrays. However, for a wider field of view (FoV) and longer range, arrays are preferred over discrete diodes and emitters operating at high peak powers. This often results in higher costs for cooling systems. VCSELs, on the other hand, can be manufactured as arrays because of their top emission. Though VCSEL technology is an emerging area, its cost/watt is expected to improve with its adoption in automotive applications. Range is believed to be up to 500m from EEL sources, however, illumination is a disadvantage given the elliptical nature of the beam. Alternatively, the usable range of VCSEL sources can be up to 300m with a beam shape that is tighter compared to EELs. Finally, the wavelength of emission is another key factor to consider in emitter sources. In the context of maximum permissible exposure, most of the emitters used today are around 905nm near-infrared (NIR), which are relatively unsafe for the human eye at elevated powers. Because of this concern, emitters around 1550nm short-wave infrared (SWIR) wavelengths are garnering a lot of attention because of better eye-safe levels.

On the receiving side, FoV is essential to ensure that returning light is captured effectively and processed via analog detection or statistical detection. The active area of the photo detector, focal length of the lens, and placement of the optical bandpass filter determine the FoV. In principle, a wider FoV is preferred, but it is achieved at the cost of larger photo detector die, resulting in higher terminal capacitance and higher noise. There are different types of detectors that are used in LIDARs today, such as photodiodes (PDs), avalanche photodiodes (APDs), silicon photomultipliers (SiPMs), and single-photon avalanche diodes (SPADs). Detectors paired with NIR emitters are silicon based and, as a result, cost is not a concern. However, SWIR detectors

are not based on silicon and relatively expensive, resulting in higher system cost at around 1550nm wavelengths. While sensitivity and infrared detection performance is acceptable among all of these detector types, gain is much higher in SiPMs and SPADs. For effective detection, the receiving signal power cannot be increased without increasing the aperture of the collecting lens or using a detector with high photosensitivity. Another challenge is the design of bandpass filters that need to work at wavelengths of sun during the day, and streetlights and headlights during the night. Consequently, analog detection still has a lot of challenges. Some designers have opted for statistical detection using SPADs because SPADs work on the principle of received pulses and histogram development.

Finally, the key beam-steering technologies that are being implemented and researched today (as shown in **Figure 4**) include: mechanical, microelectromechanical systems (MEMS), Flash, and optical phased arrays (OPAs) and discussed more in depth in reference [3]. Mechanical LIDARs are primarily used in robotic cars today. These are multi-channel devices with multiple lasers and detectors that rotate 360°. The mechanical designs are bulky, costly and present aesthetic problems for the average customer, limiting its implementation in light passenger vehicles. MEMS LIDAR uses a microscanning mirror integrated with actuators on silicon that steer the laser beam during illumination. These designs are relatively cheaper, compared to mechanical LIDARs, but reliability concerns persist under all terrain conditions. In Flash LIDARs, instead of scanning over an entire area, the laser beam is illuminated all at once. There are no moving parts in such LIDARs, offering better reliability for automotive use cases. Obviously, an array of detectors is needed to form an image. A slight variation of the Flash concept is sequential Flash where illumination of an entire scene is not done at once, but rather, column by column. Lastly, OPA steers the illumination by controlling the phase of an array of lasers. Similar to Flash LIDARs, there are no moving parts and therefore, OPA offers good reliability as well.

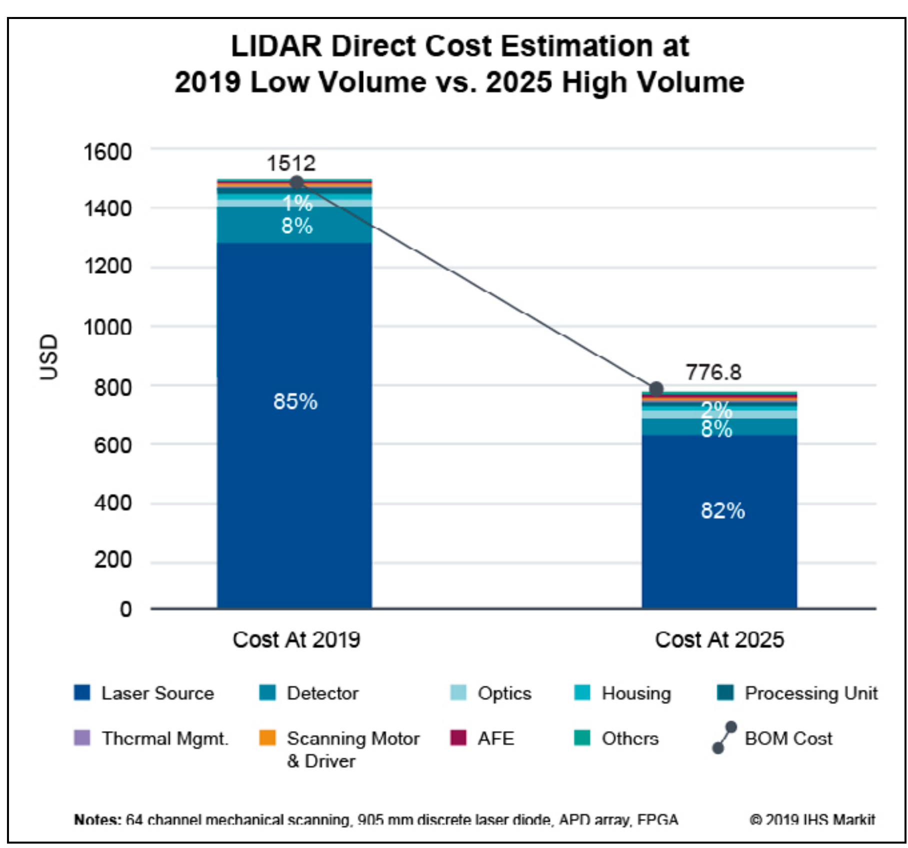


Figure 5: LIDAR cost breakdown and trends. SOURCE: IHS Markit

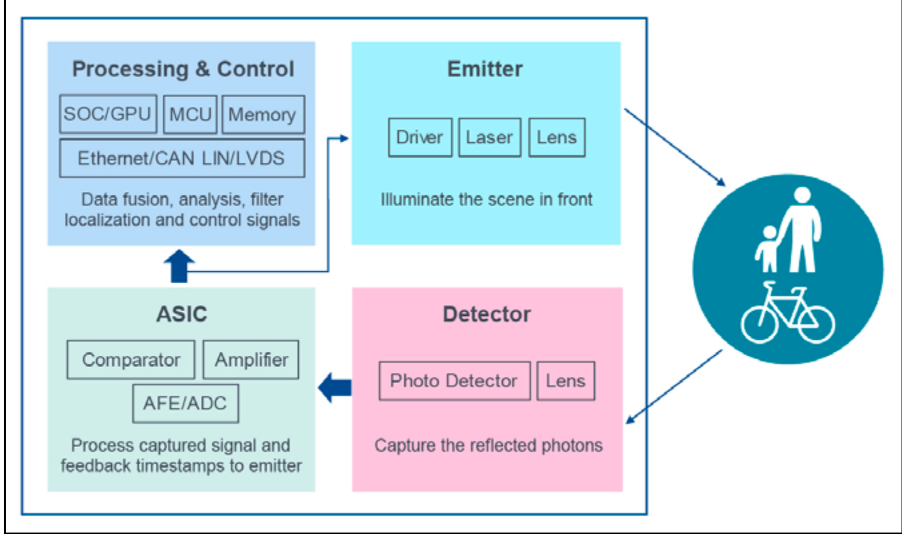


Figure 6: LIDAR building blocks. SOURCE: IHS Markit

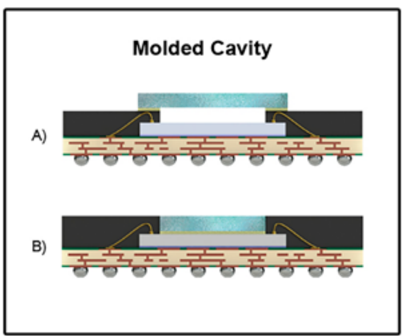
Packaging solutions

Lacking government mandates for LIDAR, vehicle OEMs have chosen the path of redundancy to ensure safety in autonomous driving. Cameras, radar and LIDAR not only complement each other, but also compete in some applications as shown in **Figure 3**. We are able to provide package solutions for the emerging LIDAR sensors of the ADAS market. Because of the varying requirements of LIDAR customers, the market consists of highly fragmented solutions. Today, however, the cost of LIDAR systems is higher because of the lack of economies of scale and inherently expensive incumbent technologies for mass markets such as

automotive. One example of the cost breakdown of a mechanical LIDAR is shown in **Figure 5**. According to IHS Markit, the cost of a mechanical LIDAR system with 64-channel scanning could reach a price point below $800 by 2025. If achieved, such a price point for a LIDAR module might be affordable for OEMs focusing on mobility as a service (MaaS) with ADAS capabilities higher than Level 4. For personal use vehicles, cheaper LIDAR solutions may be preferred.

Being an outsourced semiconductor assembly and test (OSAT) supplier, we bring knowledge and economies of scale to offer cost-effective solutions. For example, successful cost reduction has been demonstrated by using a standardized process flow through our MEMS sensors platform. Cavity ball grid array (BGA)/land grid array (LGA) and molded cavity BGA/LGA standardized packages can target many market categories such as biometric authentication, automotive, human interface, environmental and healthcare/fitness. Standardization also offers faster time to market. Though most of the current laser diode and detector packaging uses high-cost ceramic substrates, leveraging suppliers' continued development of laminates, lid and mold compounds can ensure quality and performance for low-cost solutions. To further understand the levers to reduce cost and improve functionality, one needs to understand the building blocks for a LIDAR system (**Figure 6**). The current building blocks for a LIDAR system contain an emitter that illuminates the scene, a detector to capture the reflected light, an application-specific integrated circuit (ASIC) to process the signal, and a processing unit to analyze the data. While most of the solutions today are in discrete form, integration of multiple chips in a single package or multiple packaged parts on a single substrate could be possible future trends.

With system-in-package (SiP) modules being so successful in other automotive applications, as well as applications such as infotainment, it begs the question of how integrated a LIDAR package solution can be and the possibility of integration trends. For example, an integrated APD and a trans-impedance amplifier (TIA) or an integrated SPAD with an ASIC can be packaged either in a side-by-side or as a chip-on-wafer (CoW) solution. Further, a digital signal processing (DSP) die can be co-integrated through a possible hybrid solution on a printed circuit board (PCB) or monolithic system on chip (SoC) detector solution. Both have their own advantages and disadvantages. For example, monolithic solutions offer low NIR sensitivity and better speed of detection, while hybrid solutions offer higher NIR sensitivity and have a better aperture ratio.



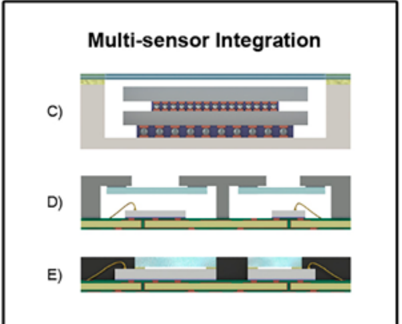


Figure 7: Amkor's packaging solutions.

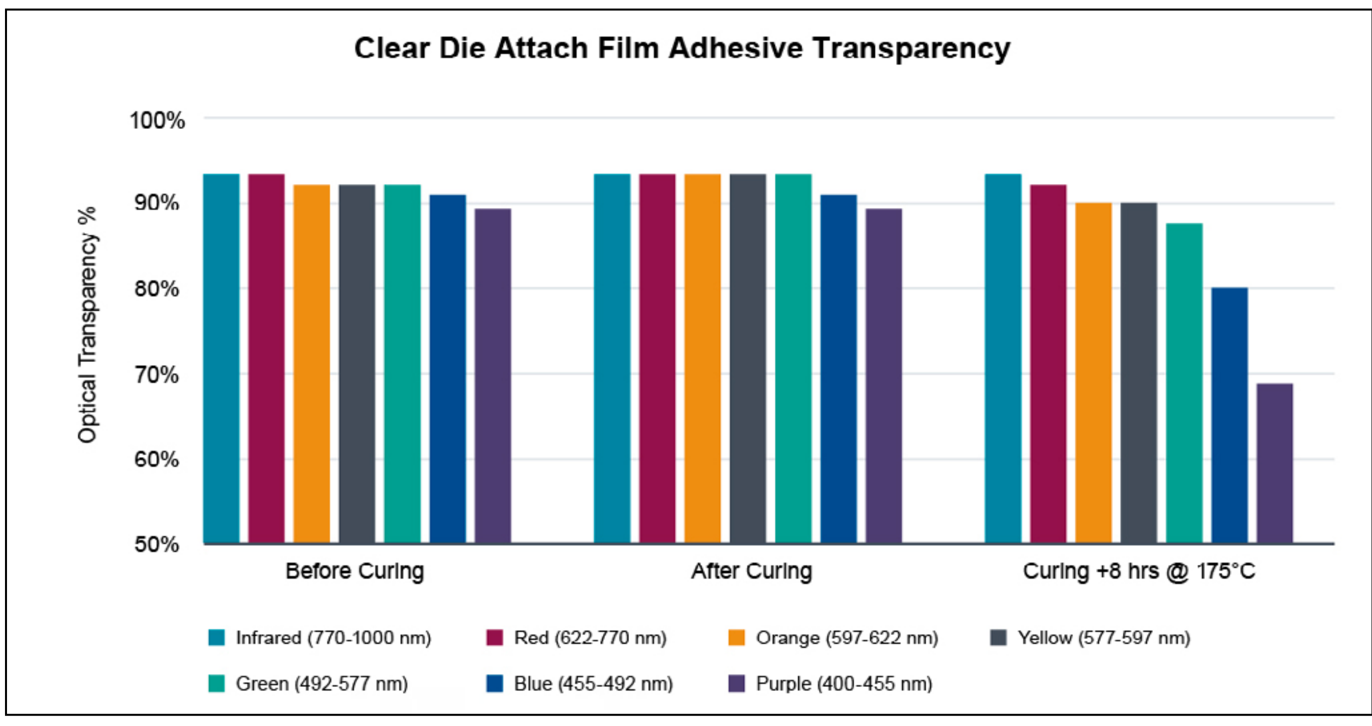


Figure 8: Clear die attach film transparency spectrum. (SOURCES: Loctite, Henkel Adhesives

SUSS EQUIPMENT SOLUTIONS ENABLING LEADING-EDGE PACKAGING TECHNOLOGIES

SUSS MicroTec is a leading supplier of equipment and process solutions for the semiconductor industry enabling state-of-the-art packaging technologies from R&D to high volume production.

With next generation lithography solutions for FOWLP and leading edge wafer bonding technologies for 2.5D and 3D stacking, we contribute to the advancement of innovations in the key areas of packaging and system integration.

Always be one step ahead — with solutions from SUSS MicroTec.
Contact us for more information!

SUSS MicroTec
info@suss.com
www.suss.com

With low inductance being a priority, especially for ToF applications in the detectable range, high-power short-pulse is a requirement and a transition from long-lead, through-hole laser packages (with high inductance) to surface mount packages with an array of laser diodes will be key. Beam quality is another requirement that will depend heavily on reducing package electrical losses. To find the right path forward, the successful technology achievements in optical fingerprint sensors and MEMS sensors can be leveraged to offer improved packaging solutions for LIDAR customers.

In addition, molded-cavity fingerprint sensor packaging (**Figure 7**, structures A and B) has been successfully qualified for automotive applications under the Automotive Electronics Council's AEC-Q100 Grade 2 specifications. While automotive grade packages need to undergo more stringent requirements than consumer fingerprint sensors, we have been able to use a standardized process and qualify them specifically for automotive complementary metal-oxide-semiconductor (CMOS) image sensors, ToF and LIDAR applications. The current molded-cavity structures can be modified to meet customers' needs including, flip-chip/copper pillar bonds instead of wire bond, LGA instead of BGA and varying glass attach epoxies for different applications.

As an example of the discussion above, consider that a ToF sensor within the cabin of a vehicle for a gesture control application might not need an extremely clear and precise image, so by eliminating the need for an air gap and attaching the glass using a clear die attach film (DAF), pressure buildup within the package might be reduced. **Figure 8** shows the transparency at different wavelengths for a clear DAF solution adhesive that offers over 93% transparency in the infrared spectrum (770-1000nm wavelength). Structure B (**Figure 7**) utilizes a clear DAF to attach the glass while structure A uses an ultraviolet (UV) curable epoxy to attach the glass to create an air gap. A UV-curable epoxy aids in mitigating pressure buildup within the cavity that would be increased with a thermal cure epoxy. By utilizing similar technologies, multiple sensors can be integrated into one package and continue to evolve into the future. As shown in **Figure 7**, structures C, D and E show three different solutions for combo-sensors including a ceramic substrate with a stacked die solution on top (structure C). Because of the high average power of approximately 12-25W for long range LIDAR, a ceramic substrate such as the top solution might be required. The top solution is also optimal for many ToF applications where a large amount of heat is produced because it poses the best thermal performance and least warpage. Structures D and E both utilize wire-bond interconnects with a laminate substrate. The difference is one utilizes a molded solution (E), while the other a liquid crystal polymer (LCP) lid (D). Both solutions are optimal for lower power applications. An example of this might be short-range LIDARs where the typical power output may be <6W. These packages can be used to bring a lower cost, high-quality LIDAR solution to the market through strategic partnerships with the supply chain and customers.

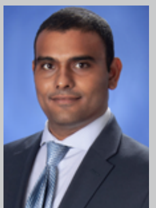
Summary

Driven by environmental, economic and social factors, demand for sophisticated automotive safety solutions will increase. Affordable safety being a priority, LIDAR is being developed as a major component for ADAS. We are positioned to provide package solutions for each segment of ADAS, including cameras, radar and LIDAR. Utilizing geographically dispersed factories, services are strategically implemented to customers worldwide in automotive, industrial and consumer applications. While focused on delivering products from the existing portfolio of packages in the photo detector portion of the LIDAR block, innovative solutions in the form of system-in-package (emitter and receiver) that further spearhead integration in a single package/module will be developed as LIDAR continues to evolve towards cost-effective solutions. Going forward, we will rely on our strong technology know-how and customer partnerships to deliver advanced solutions to these challenges.

References

1. "Road Traffic Injuries," World Health Organization, https://www.who.int/news-room/fact-sheets/detail/road-traffic-injuries
2. "Traffic Safety Facts Annual Report Tables," NHTSA, https://cdan.nhtsa.gov/tsftables/tsfar.htm
3. Y. Li, J. Ibanez-Guzman, et al., "Lidar for autonomous driving: the principles, challenges, and trends for automotive Lidar and perception systems," IEEE Signal Processing Magazine, Vol. 37, Issue: 4, July 2020.

Biographies



Ajay Sattu is Sr. Manager, Automotive Product Marketing at Amkor Technology, Inc., Tempe, AZ. He is focused on automotive electrification, ADAS and infotainment product marketing and strategy. Prior to joining Amkor, he worked for Infineon, managing technology and product development of wide-bandgap semiconductors. He has published several peer-reviewed articles and presented at industry conferences. He holds a PhD in Electrical Engineering from U. of South Carolina and an MBA from UCLA Anderson. Email ajay.Sattu@amkor.com

Burt Barber is a MEMS and Sensors Consultant at Amkor Technology, Inc., Tempe, AZ. With more than 20 years' experience in the global semiconductor supply chain, he has served in various key marketing and business/product development positions at MEMC/Sun/Edison, Texas Instruments, Alcatel, Xilinx and Hitachi Semiconductor. He holds a BS in Electrical Engineering from Santa Clara U. and an MBA from U. of San Francisco.

Your trusted partner in IC testing

Vertical Probe Card

- Hign pin count > 30,000pins
- C4 pad pitch down to 75um

WLCSP Probe Card

- Maximum pin count up to 3000
- Minimum pitch down to 120um

Coaxial Socket

- SerDes 112Gbps PAM4
- Pitch down to 0.35mm

Burn-in Socket

- 850W heat dissipation capability
- Creative lid design

Thermal Control System

- 800W heat dissipation solution
- Mass production for handler

sales@winwayglobal.com

www.winwayglobal.com

Estimating BGA reliability of 2.5D packages using coupled thermal-mechanical simulation

By Manish Nayini, Janak Patel [Marvell Semiconductor] Timothy Horn, Lloyd Burrell [GLOBALFOUNDRIES]

Silicon interposer technology, or 2.5D, is a type of system-in-package (SiP) that provides an opportunity to integrate several heterogeneous integrated circuit (IC) devices in the same package. Placing multiple IC chips next to each other on a passive silicon interposer allows for short and dense interconnection between the chips. This configuration enables lower power, lower latency and higher bandwidth compared to traditional 2D packages [1]. 2.5D technology is seen as an important solution to overcome limitations of Moore's Law scaling and finds use in several high-performance applications such as networking, graphics, artificial intelligence (AI)/machine learning, etc. 2.5D packages consisting of logic die and high-bandwidth memory (HBM) stacked die are one of the most common configurations to increase the performance of the logic die.

Motivation

With the increasing bandwidth requirements, the logic die size, number of HBMs and, by extension, interposer size, organic laminate size, are increasing. This has necessitated the move to low coefficient of thermal expansion (CTE) organic laminates to improve the package coplanarity and also maintain ultra low-k (ULK) layer, underfill, and C4/micro-pillar reliability. However, this move to low CTE organic laminates results in an increased CTE mismatch between the package and conventional FR4 printed circuit board (PCB). The low CTE organic laminate combined with large package sizes (higher distance from neutral point [DNP]) leads to lower ball grid array (BGA) solder joint reliability, especially in thermal cycling.

2.5D packages are used in many applications and each application has different temperature excursions due to unique environment, power management, etc. The JEDEC TC-J test is considered an industry standard test to evaluate thermal cycling fatigue reliability of BGA solder balls. The test is a uniform temperature cycling with a fixed profile and the test results need to be bridged to the field application case. Therefore, there is a need to model and predict the 2nd level interconnect reliability for different applications.

Several papers in previous literature have evaluated BGA solder joint reliability in both thermal and power cycling using finite element modeling (FEM). S. Shao, et al., [2] reported on a parametric study of 2.5D package board-level reliability in thermal and power cycling using combined computational fluid dynamic (CFD)-structural modeling. J. Wang et al., [3] discussed the effects of package geometry and material properties on board-level solder joint reliability of a 2.5D package in accelerated thermal cycling. Various authors, such as B. Rodgers, et al., [4], L. Yin, et al., [5] have investigated thermal cycling and power cycling using coupled thermal-mechanical modeling techniques. Few papers such as those by L. Garner, et al., [6], T-C. Chiu, et al., [7], P. Bhatti, et al., [8] have analyzed the effect of heat sink load on solder joint reliability.

In this study, we discuss a mix of FEM simulations and test data to understand BGA fatigue reliability in accelerated thermal cycling and field-like cycling conditions. The JEDEC standard TC-J thermal cycling reliability test procedure for a large body lidless 2.5D package with reticle stitched interposer, reticle size application-specific integrated circuit (ASIC) and two HBMs, is detailed. Two configurations are evaluated in this test: with and without heat sink. The data collected from these tests are used to validate the FEM simulation of the thermal cycling. The coupled thermal-mechanical simulation technique is then used to predict BGA lifetime in field-like cycling conditions using the TC-J thermal cycling lifetime as a reference.

TC-J reliability test

The reliability test boards are designed as a 20 plus layer, 10" x 8", 147.2mil-thick, copper metal and FR-4 dielectric build-up layers with non-solder mask defined (NSMD) pads. For monitoring of high-risk connections in the board, electrical connections are made to a 540-pin connector (interval measurement only) and a 4-pin connector (in situ measurement only). In situ measurements are the primary focus of this study because of their capability to sense the exact time to fail under stress, enabling more precise estimation of the BGA life. 2.5D packages joined to the test boards are assembled with a 30PSI heat sink (**Figure 1**). A total of 26 assemblies are monitored in this assessment: 13 with heat sinks, and 13 without.

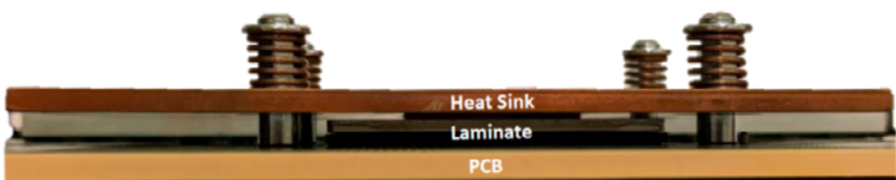


Figure 1: Package, PCB and heat sink assembly.

The assemblies are subject to thermal cycling between 0°C to 100°C, with set points at -5°C and 105°C, respectively. A ramp rate of less than 20°C/min is applied. Worst case dwell time is set at 11 minutes. The thermal cycling profile

is according to the industry standards JEDEC TC-J condition [12], and IPC-9701A [13]. The thermal chamber used for the assessment is a Thermotron SE-600-10-10, single-zone chamber. Target failure criteria is a 100 ohm shift from time zero set points for greater than 50% of the hardware.

Modeling methodology

The simulation in this study aims to analyze and compare BGA reliability in two different thermal cycling conditions. The first case is the JEDEC standard TC-J thermal cycle, which is uniform temperature cycling. Within this case, we have two configurations: one with and one without a heat sink. The second case is a representative field-like cycle. We call it a field-like cycle because the actual cycling conditions usually depend on the customer application. In this case, we analyze only the configuration with a heat sink. This condition is nonuniform temperature cycling and therefore it involves both thermal and mechanical models.

3D FEM models are generated using ANSYS Mechanical software (**Figure 2**). The model consists of a fully-assembled lidless 2.5D package with a stiffener ring, printed circuit board (PCB), backing plate (when a heat sink is used) and a full array of BGAs. The heat sink/pressure plate component of the assembly itself is not modeled and is instead replaced with an effective pressure or convection heat transfer coefficient. In order to model

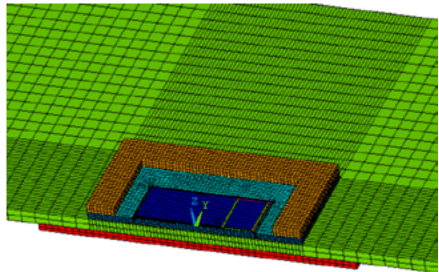


Figure 2: Global FEM model of a 2.5D package on a PCB with a backing plate.

the BGAs to a higher degree of accuracy without being computationally expensive, a global-local modeling approach is utilized [9,10]. The material properties in the global and local model are all temperature-dependent elastic properties except BGA solder. Anand's viscoplastic relation is used to define the constitutive behavior of solder.

The TC-J cycling condition applies a uniform temperature distribution across the entire package on board assembly, and therefore only requires a mechanical model to complete the analysis. A total of six TC-J thermal cycles (0°C to 100°C) are run in the model to achieve stability in the plastic strain/ plastic work accumulated per cycle. For the field application model, the temperatures within the package are a result of Joule heating inside the logic die and HBM. The temperature distribution is also nonuniform because of the different dimensions and thermal properties of the package components. Therefore, a steady state thermal model is solved first to evaluate the temperature distribution across the entire assembly. These temperature values are then input into the mechanical model as thermal loads. The temperatures evaluated in this model correspond to the ON state of the module. For the OFF state, a uniform temperature of 25°C corresponding to room temperature is assigned. The thermal model is run only once for a given set of boundary conditions. Once the model is completed, the same temperature values stored in the results file are read into the structural model for each field cycle. Three different Tj_{max} (maximum junction temperature) conditions of 100°C, 115°C, and 160°C are analyzed. These correspond to different use conditions of the product in the field. A cycle time of 24 hours with 11 hours dwell at ON, OFF states and 1 hour transition times is considered. Similar to the TC-J cycling model, a total of six field cycles are run to achieve stability in the plastic strain/ plastic work accumulated per cycle.

Results and discussion

The following sections discuss results obtained from TC-J reliability testing, TC-J cycling simulations, and field cycling simulation.

TC-J reliability test. The normalized Weibull failure rate plot for the two configurations is shown in **Figure 3**. A clear difference is noted in the time to failure between the two configurations. The 63.2% Weibull characteristic life (η)

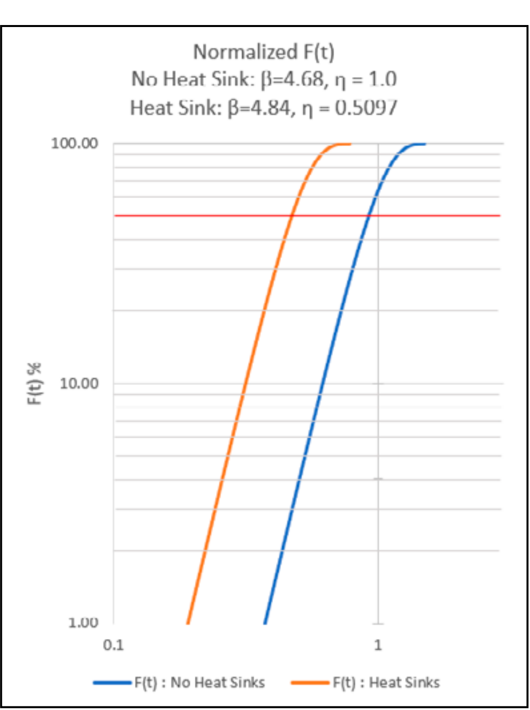


Figure 3: TC-J cycle Weibull failure rate plot.

Figure 4: Die and pry test showing failed BGAs at corners.

for assemblies with heat sinks is seen to be nearly half the characteristic life for the assemblies with no heat sinks. Using the 540-pin connector to isolate fails and further leveraging the dye and pry technique to characterize failures, the presence of BGA fails was observed at the corners of the module (**Figure 4**). Using this analysis, several corner failing BGAs were detected with pad rupture observed on surviving solder balls. Additionally, 100% failure was observed for the heat sink mounted hardware. There were no signs of electrical or physical failures in the interposer or chip shadow regions of the laminate.

TC-J thermal cycling simulations. Equivalent plastic strain is used as a metric to track the damage in solder. The location of the critical BGA is determined using

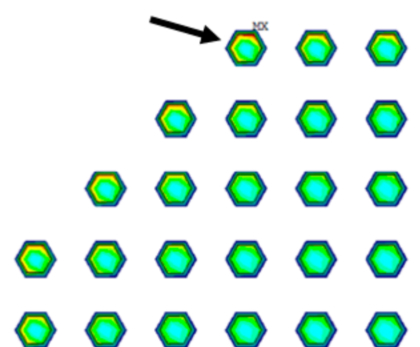


Figure 5: Equivalent plastic strain distribution in corner BGAs in global model showing critical BGA location.

the highest strain BGA at the end of the last cycle in the global model. Figure 5 shows the location of the highest strain BGA in TC-J thermal cycling for the case where heat sink is used. This matches the fail location determined using the dye and pry technique. The critical BGA location for both of the configurations – with and without heat sink – is observed to be at the package corner, which matches the fail data. This corner failing BGA indicates a shear dominant failure mode because of the higher CTE mismatch between organic laminate and PCB and high DNP as a result of the large package size. Once the critical BGA is identified, the local model is evaluated at that location. The plastic strain distribution in the local model BGA at the end of the last cycle indicates that the highest strain regions are towards the organic laminate side of the BGA near the copper pad.

Plastic strain accumulated ($\Delta\varepsilon_p$) for the last cycle in the local model is used as the metric to evaluate BGA lifetime. The Coffin-Manson strain-based relation (**Eq. 1**) [11] is used to calculate acceleration factors. Using one known data point from the test data, other lifetimes can be estimated using the acceleration factor.

$$AF = \frac{N_1}{N_2} = \left(\frac{\Delta\varepsilon_{p1}}{\Delta\varepsilon_{p2}}\right)^{-n} \quad \textbf{(Eq. 1)}$$

In this case, the characteristic lifetime (η) of the heat sink configuration is used as the reference point (N1). Using the Coffin-Manson relation, the lifetime of the configuration without the heat sink is calculated. The normalized values for the lifetime are plotted in Figure 6. The characteristic life of the configuration without a heat sink obtained from simulation is very close to the value

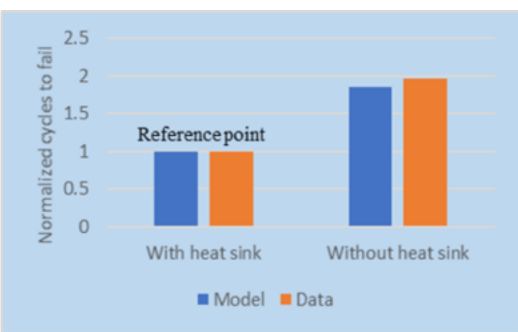


Figure 6: Normalized characteristic life in TC-J cycling obtained from model and test data.

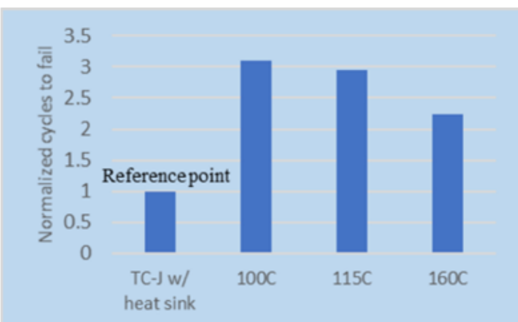


Figure 7: Normalized lifetime in field cycle with different Tj_{max}.

determined from test data (<10%) indicating good model-data correlation. The combination of heat sink load and backing plate is observed to significantly degrade BGA lifetime as it constrains the assembly from warp and channels the CTE mismatch between organic laminate and PCB into additional stress in the BGA.

Field cycling simulation. To estimate the characteristic lifetime for the field cycles, the same technique as described for the TC-J thermal cycling case is applied. The normalized characteristic lifetimes for the three field cycles are calculated using the Coffin Manson relation. The characteristic lifetime of the configuration with heat sink in TC-J cycle is used as the reference point in the Coffin Manson relation. Figure 7 shows that the number of cycles to fail for field cycles are, in general, higher than in the TC-J cycle. This can be explained by the lower overall stress in field cycle compared to the TC-J cycle for the critical BGA. Further, the lifetime values for the three different Tj_{max} cases show that as the Tj_{max} value is lowered, the lifetime increases. A smaller ΔT between the hot and cold ends of the cycle results in a less stress-inducing condition. There is also lower strain accumulated because of the lower temperatures at the high temperature end of the cycle.

Summary

As bandwidth requirements in high-performance applications keep increasing, robust and reliable 2.5D packages have become pertinent technology to address the needs. The JEDEC standard TC-J test is a standard test to evaluate BGA solder fatigue reliability in thermal cycling. But the results need to be bridged to the end application use conditions. Using the coupled thermal-mechanical simulation technique, field lifetime for a product can be evaluated using the accelerated testing lifetime. In this study we review a simplified method of modeling field cycles. Further work in this area needs to be carried out to model actual field cycles, which can be more complex.

Acknowledgment

This article was revised from its original version, which was originally presented at the IEEE Electronic Components and Technology Conference (ECTC) 2020 (virtual conference).

References

1. G. J. U. Knickerbocker, S. P. Andry, E. Colgan, et al., “2.5 D and 3D technology challenges and test vehicle demonstrations,” Proc. of 62nd Electronic Comp. Tech. Conf. (ECTC), San Diego, CA, 2012, pp. 1068-1076.
2. S. Shao, Y. Niu, J. Wang, et al., “Comprehensive study on 2.5D package design for board-level reliability in thermal cycling and power cycling,” 68th ECTC 2018, pp. 1668-1675.
3. J. Wang, Y. Niu, S. Park, A. Yatskov, “Modeling and design of 2.5D package with mitigated warpage and enhanced thermo-mechanical reliability,” 68th ECTC 2018, pp. 2477-2483.
4. B. Rodgers, J. Punch, J. Jarvis, P. Myllykoski, T. Reinikainen, “Finite element modeling of a BGA package subjected to thermal and power cycling,” Inter. Society Conf. on Thermal Phenomena, 2002, pp. 993-1000.
5. L. Yin, Y-L. Tsai, T. Chou, et al., “Second-level interconnects

reliability for large-die flip-chip lead-free BGA package in power cycling and thermal cycling tests," 61st ECTC 2011, pp. 921-926.
6. L. Garner, C. Zhang, K. S. Beh, K. Helms, Y. L. Tan, "Effect of compression loads on the solder joint reliability of flip-chip BGA packages," 54th ECTC 2004, pp. 692-698.
7. T-C. Chiu, D. Edwards, M. Ahmad, "Ball grid array solder joint reliability under system-level compressive load," IEEE Trans. on Device and Materials Reliability, vol. 10, no. 3, Sep. 2010, pp. 324-337.
8. P. K. Bhatti, M. Pei, X. Fan, "Reliability analysis of SnPb and SnAgCu solder joints in FC-BGA packages with thermal enabling preload," 56th ECTC 2006, pp. 601-606.
9. X. Fan, M. Pei, P.K. Bhatti, "Effect of finite element modeling techniques on solder joint fatigue life prediction of flip-chip BGA packages," 56th ECTC 2006, pp. 972-980.
10. G. Gustafsson, I. Guven, V. Kradinov, E. Madenci, "Finite element modeling of BGA packages for life prediction," 50th ECTC 2000, pp. 1059-1063.
11. L. F. Coffin, "A study of the effects of cyclic thermal stresses on ductile metal," ASME Trans., Vol. 76, pp. 931-950, 1954.
12. JEDEC STANDARD Temperature Cycling JESD22-A104E.
13. IPC-9701A, "Performance test methods and qualification requirements for surface mount solder attachments," IPC, 2006.

For Any PCB - GHz Bandwidth BGA/QFN Sockets

Quick-Turn Custom Sockets

• Use on any existing PCBs
• No mounting holes
• No soldering
• Patented placement/epoxy system
• 0.32mm larger than IC (per side)
• Bandwidth to 80 GHz
• 0.3mm pitch & up

Ironwood ELECTRONICS 1-800-404-0204
www.ironwoodelectronics.com

Biographies

Manish Nayini is Senior Engineer, Packaging Engineering at Marvell Semiconductor, USA, Hopewell Junction, NY. He works on thermomechanical simulations at the package- and board-level. He has been with Marvell for the past year; prior to that, he worked for 3 years at Globalfoundries in the Advanced Packaging Development Group. He has a Masters in Mechanical Engineering from Arizona State U., and a Bachelors in Mechanical Engineering from BITS Pilani, Goa, India. Email mnayini@marvell.com

Timothy Horn is a Packaging Reliability Engineer at GLOBALFOUNDRIES, USA. After completing his BS in Microelectronic Engineering at RIT in 2015, he pursued a passion for material characterization through his work as a reliability engineer at GLOBALFOUNDRIES, USA and by working on his MS in Materials Science at UVM (expected in May, 2021) as a part time endeavor.

Silicon die bonding using a photostructurable adhesive material

By Kai Hollstein, Kirsten Weide-Zaage [Institute for Microelectronic Systems, RESRI Workgroup]

This article addresses the usage of a photostructurable adhesive material for bonding a silicon chip onto a wafer surface. Such a process step is needed for a packaging technology currently under development. The process under analysis demands that a silicon chip be bonded face down onto a wafer substrate (**Figure 1**).

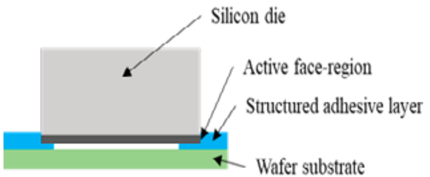


Figure 1: Build-up under analysis: silicon die bonded face down onto a structured adhesive layer.

The bonding layer should not have a thickness greater than 20µm. Furthermore, the adhesive layer needs to be structured. The combination of these varying requirements cannot be fulfilled using state of the art bonding technologies. This article introduces relevant literature, defines the research methodology to solve the project task, and presents corresponding results. **Figure 1** shows the schematic of the bonding task under analysis.

Common technologies like die bonding, pin transfer, jetting, etc., cannot be used because the adhesive volume has to be precisely controlled and the dimensions of the adhesive bond are too coarse for the application. The desired thickness of the adhesion layer can only be achieved using photostructurable materials.

Discussion

As an example of the above considerations, a similar process technology is applied in microfluidic applications, where bonding processes using photostructurable adhesives are commonly applied in order to build microchannel systems. The following literature provides an overview with respect to thin adhesive layers used in wafer-to-wafer or substrate-to-wafer bonding applications.

In [1], a photosensitive benzocyclobutene dielectric (BCB) is used to bond together a glass wafer and a silicon wafer. The resulting compound is analyzed using wedge-opening test and tensile methods. The successful implementation is shown for applications in RF system design and a microfluidics system.

In [2] and [3], a BCB material is used for a novel silicon photonic build-up. Here, a III-V substrate wafer is bonded onto a silicon-on-insulator (SOI) material. The comparable stress-free bonding process and reduced cleaning and sample preparation requirements are beneficial, but the material is not photostructurable and the bonding layer is very thin (below 50nm).

In [4], an adhesive bonding method for wafer bonding in microfluidic applications is introduced. This paper provides an overview of applicable wafer-to-wafer bonding technologies like adhesive bonding, fusion bonding, direct bonding, anodic bonding and eutectic bonding. Additionally, the authors concluded that SU-8 resist could be used as a bonding material. In order to selectively deposit the photoresist, an imprinting method is used because spin coating cannot be applied for this particular microfluidic application (microchannel system).

The authors of [5] bonded a glass lid on a glass wafer with lithographically-structured SU-8 on top. The resist has a thickness of 30µm and a minimum structure size of 5µm. The paper addresses the influence of pressure and bonding time on the bond quality, which is evaluated using microscopy and pull tests. Furthermore, the authors showed that

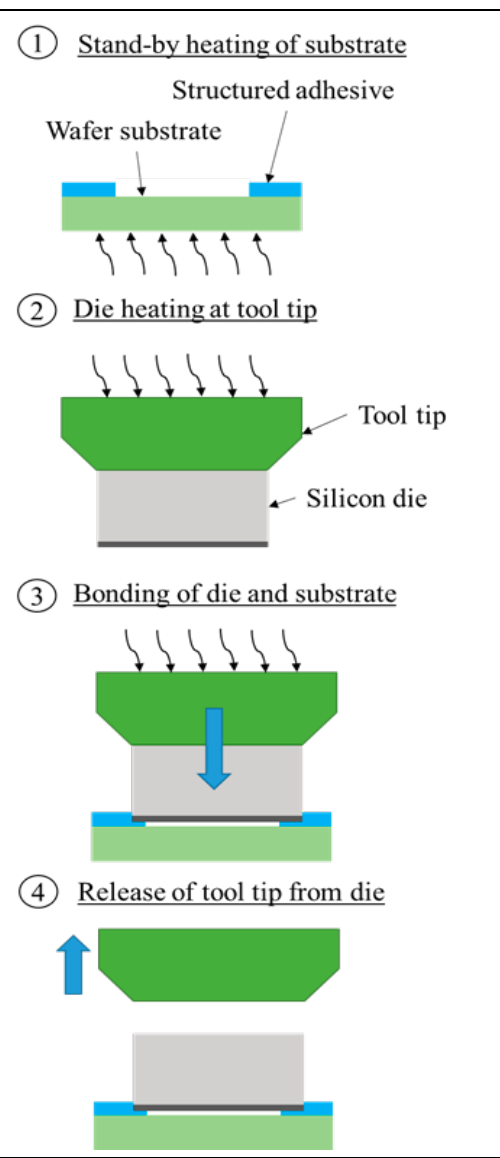


Figure 2: Process chain: bonding die onto the adhesive layer.

using a reactive ion etch (RIE) plasma clean is not beneficial for bond quality. The process is used for a microfluidic system.

In [6], several photostructurable materials for wafer-to-wafer bonding are compared. The underlying chemistry of the materials is either epoxy-based, siloxane-based, phenol-based or acrylic-based. The authors needed materials with a curing temperature below 250°C, so using BCB or a polyimide was not an option. In this study, a glass wafer and a silicon wafer were bonded to each other. The result was analyzed using optical microscopy and scanning electron microscopy (SEM) imaging. Thermogravimetric analysis was used to assess the thermal stability of the materials and Fourier transform infrared (FTIR) spectroscopy was applied to analyze chemical crosslinking of the materials. The bond strength was determined using tensile testing for all the materials that depend on the bonding temperature and bonding pressure. Cross-sectional SEM images conclude the paper. In [7], a similar comparison between BCB and SU-8 was done, and in [8], BCB was used for building a microfluidic device.

In the application analyzed in this article, the silicon chips are placed face down onto the adhesive layer. This process step is done using a standard die bonding machine. Both the substrate and the chip can be heated during this process step. A force needs to be applied on the chip in order to achieve sufficient bonding strength. The shape of the adhesive material at the edges is expected to be influenced by the process parameters. Furthermore, the resulting strength of the bond and the resulting shape of the adhesive with respect to their dependence on the process parameters have not yet been referenced in literature.

One of the main differences between the application under analysis and the microfluidic application is the resulting pressure field within the adhesive. Pressurizing the sandwich of two wafers and the adhesive layer results in a homogeneous distribution, whereas the single placement of the silicon die results in a local deformation and a local temperature change only. Therefore, the process parameters referenced in the given literature (like temperature and bonding force) cannot be used for this application and are analyzed in detail in the following sections.

Methodology

The material under analysis is expected to show the desired bonding behavior after the lithographical structuring process steps. Therefore, bonding temperatures above 150°C are needed. This process window will be used to place the silicon chip into the adhesive material. Furthermore, the reflowing of the material is expected to assist the covering of the edges. The build-up of wafer, adhesive layer and silicon dies can be cured accordingly after bonding. Because of the underlying chemistry, the material is expected to show high chemical and mechanical durability.

Figure 2 shows the applied process chain. First, the processed wafer is heated to a standby temperature of 50°C. This ensures a homogeneous activation of the adhesive material, but is still low enough for the material not to show any curing or outgassing effects. Second, the silicon die is picked up from a waffle pack and heated up to the required chip temperature, which will be analyzed later. A delay is implemented to ensure sufficient heat flow from the tool tip to the silicon component. Next, the component is placed onto the adhesive and pressure is applied. The influence of the applied pressure will be analyzed in detail in the results section.

The bond quality needs to be tested, therefore, standard die shear testing is used to quantify the bond strength. Standard light microscopy is used to analyze the resulting fracture after die shear

Parameter	Unit	Value
Temperature wafer	°C	50
Delay chip heating	s	10
Pressure application delay	s	10
Tool temperature	°C	160, 180, 200, 220,
Bonding Force Layout 1	N	0.6, 1.0, 1.4, 1.8, 2.2
Bonding Force Layout 2	N	1.0, 3.0, 5.0

Table 1: Variation of parameters under analysis.

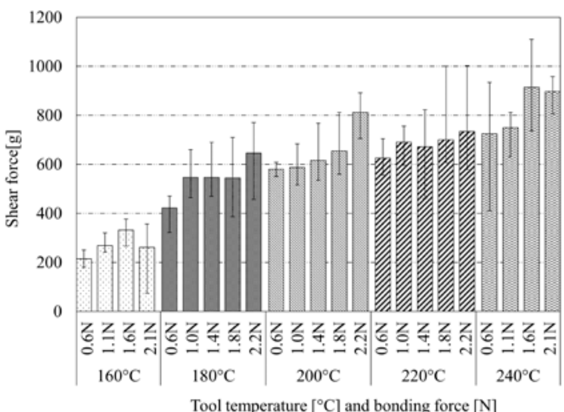


Figure 3: Shear testing results before curing with respect to temperature and bonding force variation.

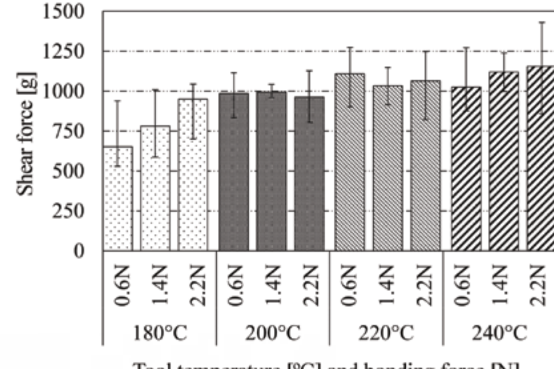


Figure 4: Shear testing results after curing with respect to temperature and bonding force variation.

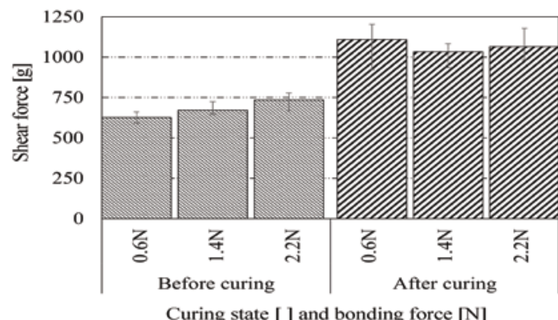


Figure 5: Direct comparison of shear values before and after curing at a 220°C tool temperature.

testing. Cross-section analysis provides further information about the resulting shape of the adhesive and its dependence on the process parameters.

In **Table 1**, the variations under analysis are given. The standby temperature of the wafer was kept constant at 50°C. The main parameters under analysis are the chip temperature and the bonding pressure. After pick-up, a delay of 10s is applied so that the die is able to reach a homogeneous temperature distribution. The temperature set points under analysis are 160°C, 180°C, 200°C, 220°C and 240°C. For each temperature, a bonding force of 0.6N, 1.0N, 1.4N, 1.8N and 2.2N is applied. For the second layout, fewer set points were analyzed (1.0N, 3.0N and 5.0N). The chips were shear tested before and after curing of the adhesive material. A total number of five shear tests were performed for each set point.

Results

First, the influence of temperature and applied force were analyzed. **Figure 3** shows the results before curing the adhesive material. Error bars represent minimum and maximum shear values. The results clearly show that a die temperature of only 160°C leads to a significant decrease in shear strength. Furthermore, it can be seen that increasing the applied bonding force results in an increased shear strength. A temperature of 240°C leads to the highest shear values, but the increased thermal load could likely damage the die.

The shear values after curing are shown in **Figure 4**. The bond strength seems to be less impacted by the variation in the process parameters. The influence of the applied force is not as significant as in the previous analysis before curing. Only for the lowest temperature of 180°C could a clear dependency on the applied force be seen.

A direct comparison of the values before and after curing is shown in **Figure 5** where one can see the increase in shear strength before and after curing. In order to better analyze the failure criterion, the resulting fracture has to be evaluated. **Figure 6** shows a representative result. The damage is occurring within the adhesive material.

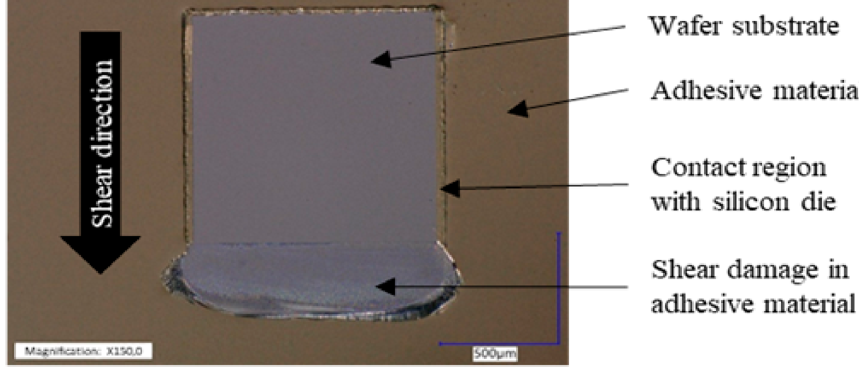


Figure 6: Resulting damage in the adhesive layer after shear testing (shear direction from top to bottom).

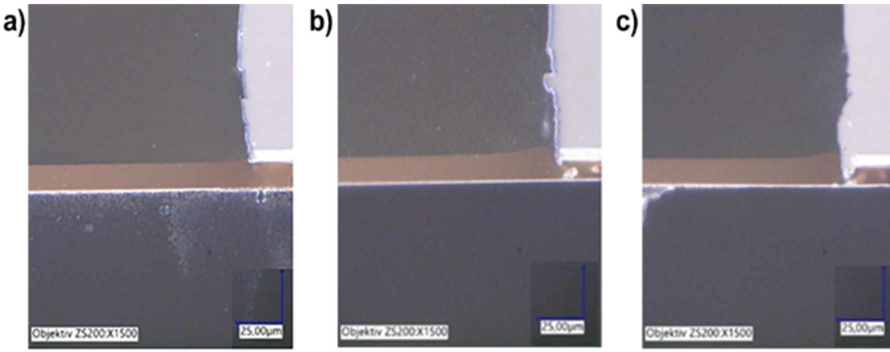


Figure 7: Cross-section images of the resulting adhesive layer shape after curing: a) 2.2N, 180°C; b) 2.2N, 200°C; c) 2.2N, 220°C.

The residue is still in contact with the silicon die after testing.

To achieve good bond quality, the covering of the edges of the die is another important factor to be considered. Therefore, cross-sectional images were taken in order to analyze the impact of the parameter variation on the resulting shape of the adhesive. **Figure 7** shows the result for a constant force of 2.2N and a variation in temperature. It can clearly be seen that higher temperatures are causing the die to be covered by the adhesive much better, however, the thickness of the remaining layer underneath the silicon die is decreasing accordingly. Depending on the application, this decrease needs to be considered when choosing the process parameters.

Another question under analysis is the influence of the adhesive thickness on the resulting shear strength of the bond. **Figure 8** shows the gathered results. A slight trend towards lower shear values for thinner adhesive layers is evident, but the temperature variation still proves to be more significant. Furthermore, an alternative adhesive design has been used. Instead of using the frame structure, the entire face area of the die is in contact with the adhesive material. **Figure 9** shows the results for a variation of applied force and temperature. Additionally, the cross-sectional image of a silicon

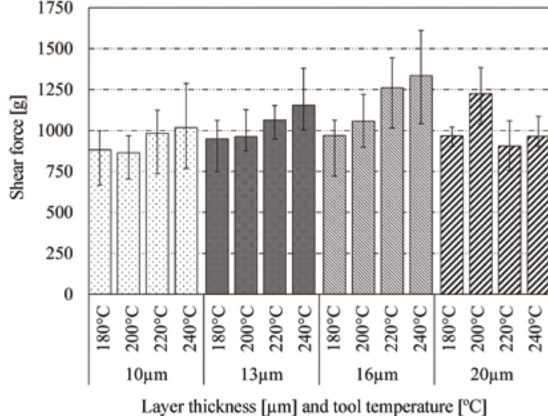


Figure 8: Resulting die shear strength for varying adhesive layer thicknesses after curing.

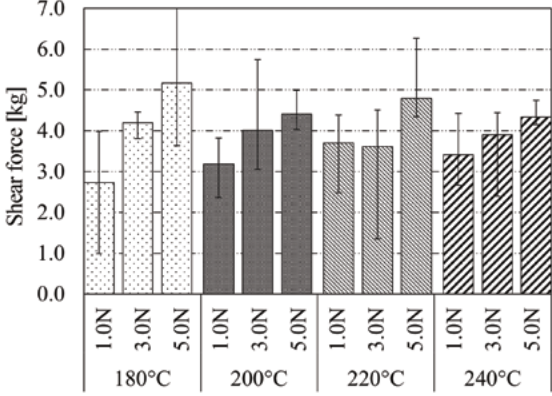


Figure 9: Resulting die shear strength for full contact between the silicon die and the adhesive layer after curing with respect to the variation of bonding temperature and applied force.

die bonded with 220°C and 3.0N is shown. The resulting shape of the adhesive material varies from the results of the previous analysis. The image in **Figure 10** shows that the edge of the silicon die is covered less, which is caused by the lack of possibility for the material to deform as a result of the applied pressure.

Discussion

It is shown that for variation 1, the temperature is the main influencing parameter on die shear strength. It is clearly evident that a threshold temperature needs to be applied in order to achieve sufficient bond strength. Because of the high spread of measured values, a higher sample count and more sub-steps need to be analyzed in order to better describe the dependency between bond strength and the applied temperature and bonding force. For full contact between the silicon die and the adhesive layer (second layout), the influence of temperature was much lower, but overall shear values have been much higher. The cross-sectional images clearly show that the edge covering is less for variation 2 when compared to layout 1. In order to better understand the flowing behavior of the material, temperature-dependent rheological measurements need to be conducted in the future.

Summary

This article introduced a bonding technology using a photostructurable adhesive layer with a thickness range of 10 to 20µm for a silicon die bonding application. Literature has been cited with comparable applications mainly in microfluidics. The available literature is not showing any application of these technologies for silicon die fixation on a wafer substrate. The work discussed in this article has shown the efficacy of the photostructurable adhesive for the application under analysis. Bonding parameters and adhesive layout and thickness have been varied in order to better understand the bonding process. The results were analyzed using die shear testing and cross-sectional imaging. Trends for the dependency between force and pressure could be demonstrated using die shear testing. Cross-sectional images of the first layout variation show a proper covering of the edges of the die for higher temperatures. For variation 2 the resulting shape of the adhesive material varies significantly showing less edge covering.

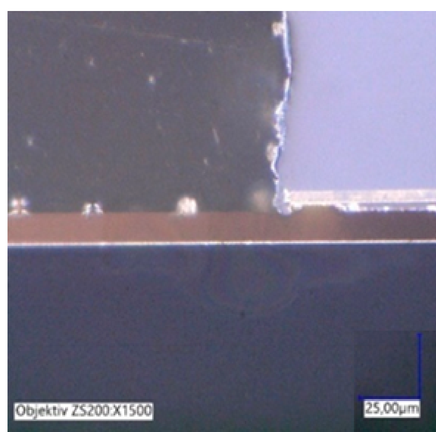


Figure 10: Cross-section image showing the resulting shape of the adhesive layer for full contact layout for 3.0N @ 220°C.

For additional analysis, a higher sample count at each set point needs to be applied and more set points need to be defined. Additionally, the material has to be further analyzed (e.g., rheological measurement, differential scanning calorimetry [DSC] analysis,

etc.) in order to better understand the bonding process. Further research needs to be done on the reliability of the bond. It is concluded that the proposed process technology is a possible solution for bonding silicon chips on a wafer substrate using a thin and photostructurable adhesive layer.

Acknowledgment

This article was previously published in the International Wafer-level Packaging Conference 2020 Proceedings. It has been edited and reformatted for publication in *Chip Scale Review*.

References

1. A. Polyakov, M. Bartek, J. N. Burghartz, "Area-selective adhesive bonding using photosensitive BCB for WLCSP applications," J. Electron. Packag., vol. 127, no. 1, p. 5 pages, 2005; doi: 10.1115/1.1846059.
2. S. Keyvaninia, M. Muneeb, S. Stanković, P. J. Van Veldhoven, D. Van Thourhout, G. Roelkens, "Ultra-thin DVS-BCB adhesive bonding of III-V wafers, dies and multiple dies to a patterned silicon-on-insulator substrate," Optical Materials Exp., vol. 3, no. 1, pp. 35-46, 2013; doi: 10.1364/OME.3.000035.
3. D. Liang, G. Roelkens, R. Baets, J. E. Bowers, "Hybrid integrated platforms for silicon photonics," Materials, vol. 3, no. 3, pp. 1782-1802, 2010; doi: 10.3390/ma3031782.
4. L. Yu, F. E. Tay, G. Xu, B. Chen, M. Avram, C. Iliescu, "Adhesive bonding with SU-8 at wafer level for microfluidic devices," J. of Physics Conf. Series, vol. 34, no. 1, pp. 776-781, 2006; doi: 10.1088/1742-6596/34/1/128.
5. S. G. Serra, A. Schneider, K. Malecki, S. E. Huq, W. Brenner, "A simple bonding process of SU-8 to glass to seal a microfluidic device," 3th Int. Conf. on Multi-Material Micro Manufacture, Borovets, Bulgaria, 2007; doi: 10.13140/2.1.2832.2082.
6. J. Kim, I. Kim, K.-W. Paik, "Investigation of various photo-patternable adhesive materials and their processing conditions," IEEE 61st Elec. Comp. and Tech. Conf. (ECTC), Lake Buena Vista, FL, USA, 2011; doi: 10.1109/ECTC.2011.5898765.
7. M. Wiemer, C. Jia, M. Toepper, K. Hauck, "Wafer bonding with BCB and SU-8 for MEMS packaging," Elec. System Integration Tech. Conf., Dresden, Germany, 2006; doi: 10.1109/ESTC.2006.280194.
8. F. Niklaus, P. Enoksson, P. Griss, E. Kälvesten, G. Stemme, "Low-temperature wafer-level transfer bonding," J. of Microelectromechanical Sys.; vol. 10, no. 4, 2001; doi: 10.1109/84.967375.

Biographies

Kai Hollstein is a PhD student at the Institute for Microelectronic Systems, RESRI Workgroup Hannover, Leibniz U. Hannover, Germany. His research focuses on package development, thermal and thermomechanical simulation of electronic packages and reliability analysis. Email kai.hollstein@ims.uni-hannover.de

Kirsten Weide-Zaage is extraordinary Professor at the Institute for Microelectronic Systems, and leader of the RESRI Workgroup Hannover, Leibniz U. Hannover, Germany. Her main research activities are in the field of microelectronic reliability with a focus on static and dynamical thermal-electrical-mechanical effects in interconnects, packages, and on boards, as well as on the effects of corrosion and radiation on customer owned tooling (COT) and TCAD simulations.

Effects of FOPLP layouts on large-area thermal chucks

By Debbie Claire Sanchez, Klemens Reitinger, Sophia Oldeide, Wenxuan Song [ERS electronic GmbH]

Complexities in integrated circuit (IC) applications and the drive toward miniaturization has put fan-out packages in the limelight. Many advantages have been noted for the fan-out structure, including high reliability and good electrical performance. The fan-out structure has enabled a multi-die configuration for 2.5D and 3D applications, allowing the packaging of high-density chips, as well as <5µm line/space redistribution layer (RDL) traces. These advantages, however, came with significant production costs. In an attempt to cut these costs, the idea of large-area packaging emerged.

Since the introduction of the fan-out package, however, several companies have been exploring the large panel-level space to provide a much more competitive cost solution. Companies like ASE, nepes, Samsung, and PTI have already either started investing in research and development, or have established a low-volume production line.

Despite the proof of economic advantage, fan-out panel-level package (FOPLP) processing was met with some skepticism from equipment suppliers because it required a new equipment design concept compared to fan-out wafer-level packaging (FOWLP) that uses standard semiconductor types of manufacturing equipment. The lack of panel size standardization has also played a significant role in the delay of mass utilization. FOPLP requires a new landscape for equipment makers, such as what type of handling and thermal control are needed to be able to create a robust and repeatable process for thermal debonding.

Fan-out in a nutshell

Fan-out structures can be categorized into two types: chip last and chip first. This investigation focuses on the chip-first type of structure.

The chip-first process (**Figure 1**) is more widely used by companies like Infineon, ASE, and Deca and has a reverse order compared to the chip-last process flow. The process starts with die bonding, molding, debonding and then RDL processing, respectively.

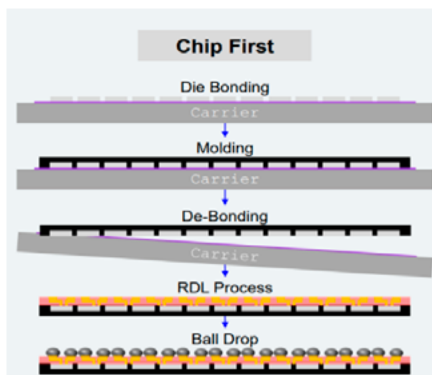


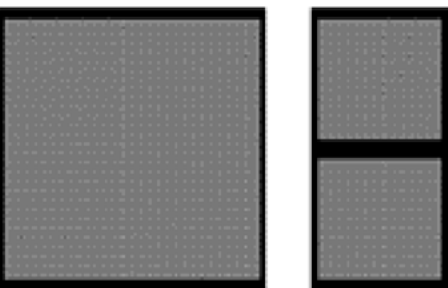
Figure 1: Chip-first structure.

Die bonding. Die bonding is the process of picking known good dies (KGDs) from a sawn silicon wafer, then placing them onto a temporary carrier laminated with thermal sensitive tape.

Molding. The compression molding process is commonly used for the chip-first structure. It starts with dispensing a specific amount of mold on top of the carrier with bonded dies. The machine then starts closing the cavity at a controlled speed, temperature, and timing.

Debonding. The debonding process is the separation of the reconstituted wafer from the carrier by applying heat or laser exposure. The sensitive (thermal or ultraviolet [UV]) tape layer softens and loses adhesion to aid the separation of the wafer from the carrier.

Photo, plating and etching processes. With the RDL built into the chip or



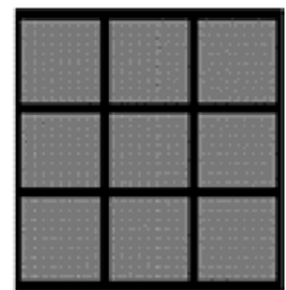


Figure 2: Panel format - array arrangement (e.g., single array, 2x2 array or 3x3 array).

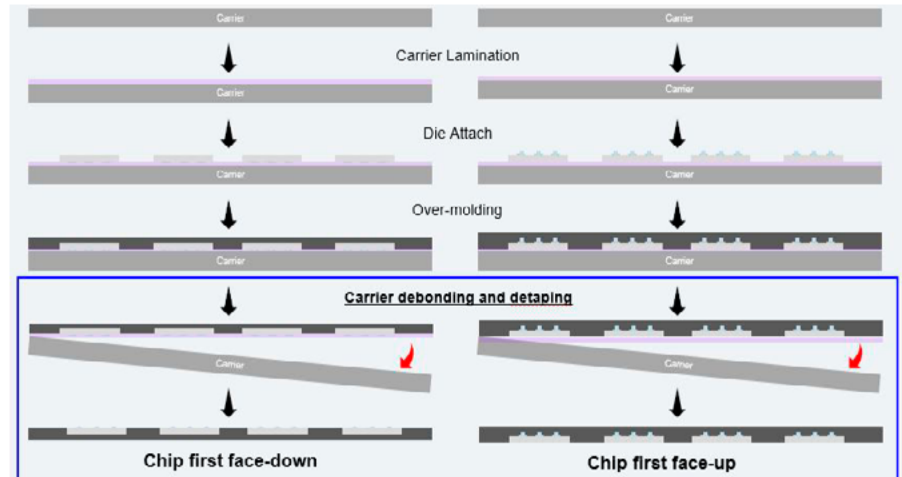


Figure 3: Fan-out wafer reconstruction process flow.

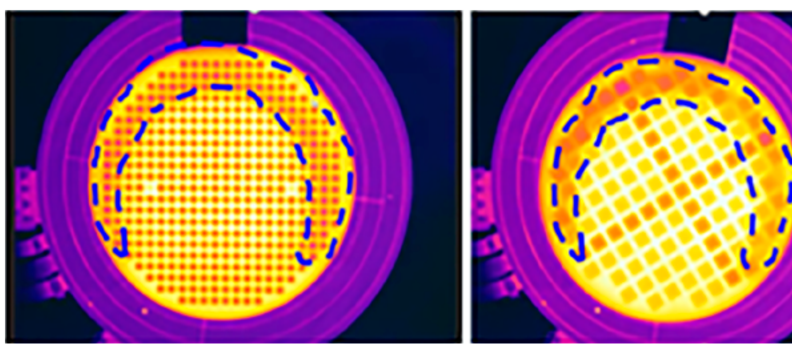


Figure 4: Thermal shot illustrating heat dissipation when a high-temperature wafer is in contact with a low-temperature object.

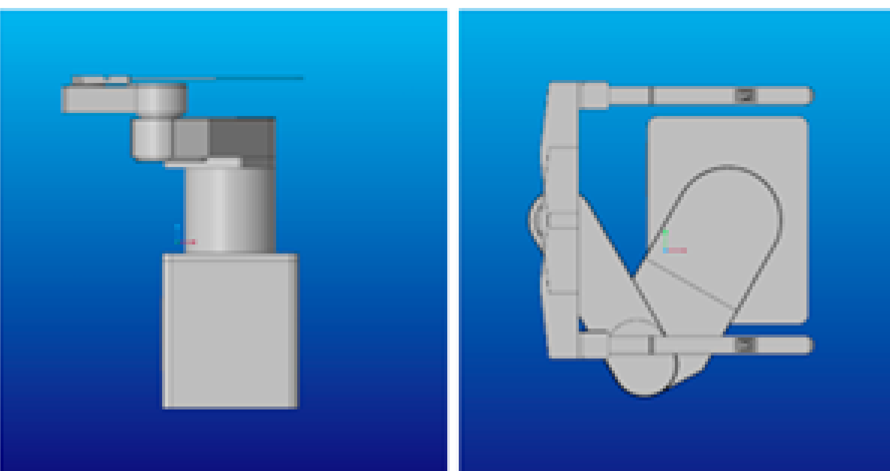


Figure 5: Standard pick and place robot with custom end effector design for panel handling.

carrier, the wafer or panel is now ready for final wafer processing involving ball drop, wafer thinning, laser marking, singulation, and tape and reel.

Common issues for fan-out packaging

As initially stated, fan-out architecture has an inherent yield issue because of the very structure of the package. The issues impacting yield are die shift and warpage.

Die shift. Die shift is the misplacement of the die with respect to its designed position. It can happen in several key processes of the panel reconstruction flow, like die bonding, molding, and thermal debonding. It becomes a problem when the shift is so high that it causes misalignment during the formation of the interconnects from the die bond pads to the redistribution layer.

Warpage. Warpage is caused by the mismatch of the coefficient of thermal expansion (CTE) between silicon and the epoxy molding compound (EMC). EMC, having a higher CTE value, results in an imbalance, which will cause the wafer or panel to warp.

Several pieces of research have been conducted to understand the effects of warpage as the wafer is processed through the line. Research has been done by John Lau, et al., [1] regarding the top six process stages that are hugely affected by the wafer/panel warpage. In wafers, warpage profiles can be categorized into a bowl shape (concave and convex) and taco

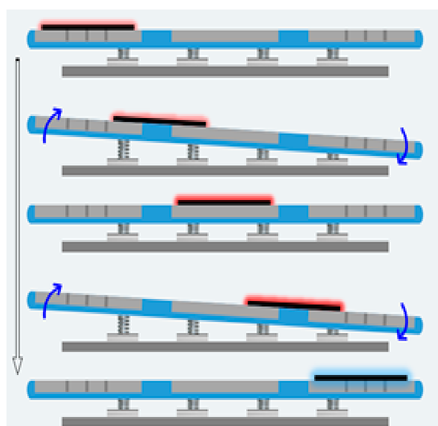
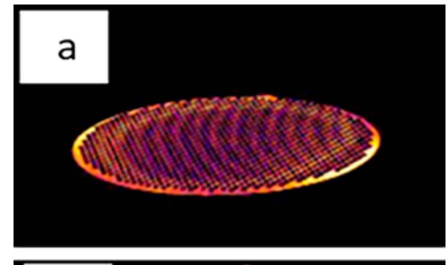


Figure 6: Contactless transport mechanism of the Tritemp slide system.

shape (smiling or frowning). The warpage profiles change depending on several factors such as silicon to mold density, die shape (i.e., square and rectangular), number of RDLs, and specifically for the panel format, the chip layout plays a significant factor (Figure 2).



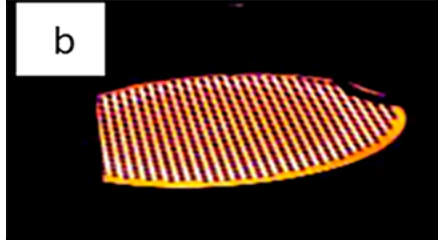
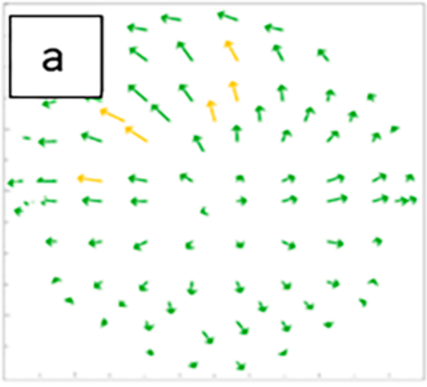


Figure 7: Thermal shot illustrating nonuniformity on thermal control: a) higher nonuniformity; and b) lower nonuniformity.



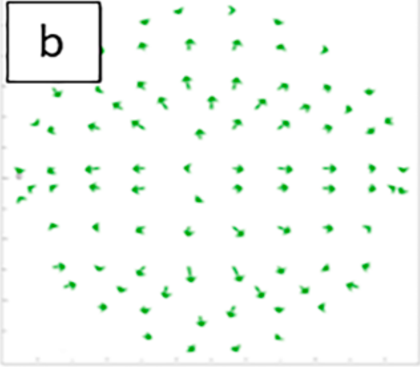


Figure 8: Die shift response in relation to nonuniform temperature on the chuck: a) higher die shift correlating to Figure 7a with high nonuniformity; and b) lower die shift correlating to Figure 7b with higher thermal uniformity.

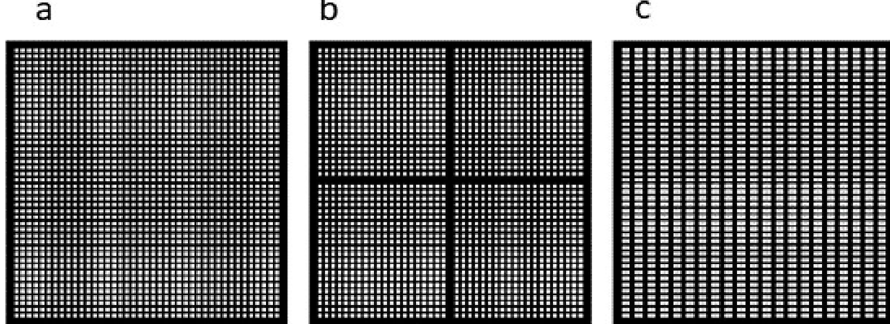


Figure 9: Defined test vehicle based on the panel layout: a) single matrix; b) 2x2 matrix; and c) single matrix with rectangular die.

Large-panel thermal debonding

In thermal debonding (**Figure 3**), process temperature, timing, and handling are defined as critical factors to ensure high yield. Panel handling is essential to ensure no excursion occurs. This is the first step where panel fragility (thickness, die placement layout, etc.) and weight will be a factor to consider in defining a handling mechanism.

Thermal control needs to be robust to maintain adequate uniformity across a larger surface. The thermal sensitive tape needs to activate across the entire

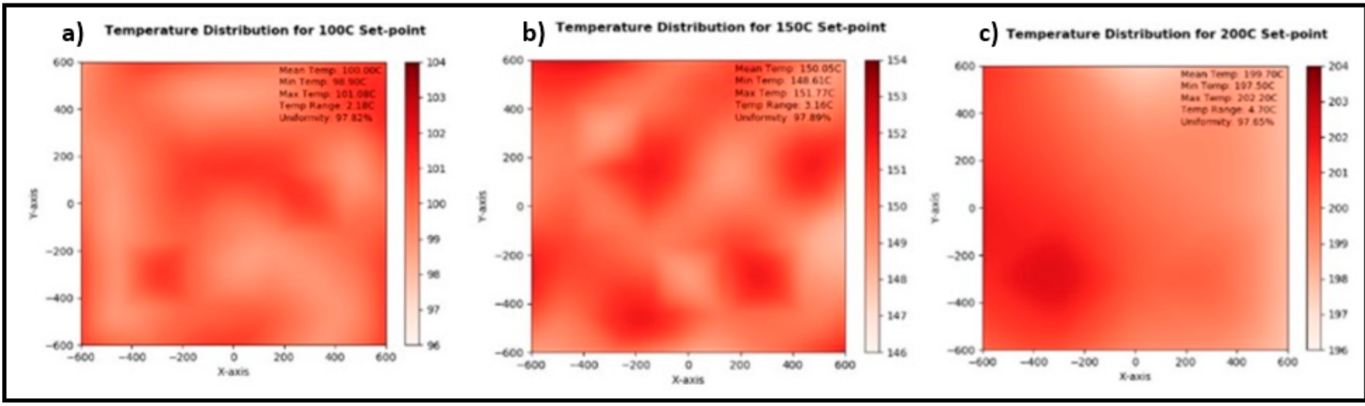


Figure 10: Temperature profile of the chuck measured at: a) 100°C; b) 150°C; and c) 200°C.

surface uniformly to eliminate not only potential cosmetic defects, but also excursion. The mechanical separation of the carrier and the panel can only happen when the thermal release tape has been fully activated uniformly across the whole surface.

Handling and transport. The handling method of molded wafers is critical in minimizing handling-induced warpage [2]. With a high-temperature molded wafer, any introduction of low-temperature objects will create

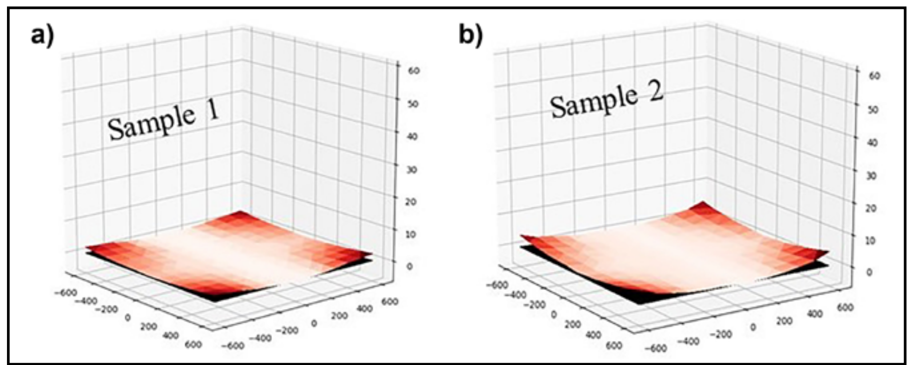


Figure 11: Warpage profiles for: a) sample 1; and b) sample 2.

thermal imbalance, causing the part in contact to shrink/contract resulting in warpage (**Figure 4**).

Handling is more complicated with a larger area. The end effector design, weight, and size of the panel will contribute to the overall warpage and the stability of the panel when transported. A common handling mechanism is pick-and-place using a robot with a customized end effector (**Figure 5**).

Another method is the air cushion mechanism (**Figure 6**), which is contactless transport whereby the panel is lifted with controlled air pressure on a tilted platform. Gravity then causes the panel to slide down. The panel, when moving, is not in contact with the handling robot; therefore, the elevated temperature is kept uniform across the panel while being transported. The mechanism to be applied for panel-level debonding is baselining the effectiveness on a 300mm format contactless transport.

Thermal control

A round 300mm thermal chuck surface is proven to be within the ±2°C for 200°C (tighter range on lower temperature), which is above the release temperature range of 175-195°C of the commercially-available thermal release tapes.

A previously presented paper [3] showed the effects of thermal nonuniformity on die shift. Wafers subjected to a high nonuniformity chuck vs. a chuck of 186°C ± 1°C showed significant yield performance (**Figure 7**). The wafer in **Figure 7a** showed high nonuniformity, while the wafer in **Figure 7b** has ±1°C uniformity. The corresponding die shift showed that with higher nonuniformity the die shift is larger in magnitude compared to a chuck with high thermal uniformity [3] (**Figure 8**).

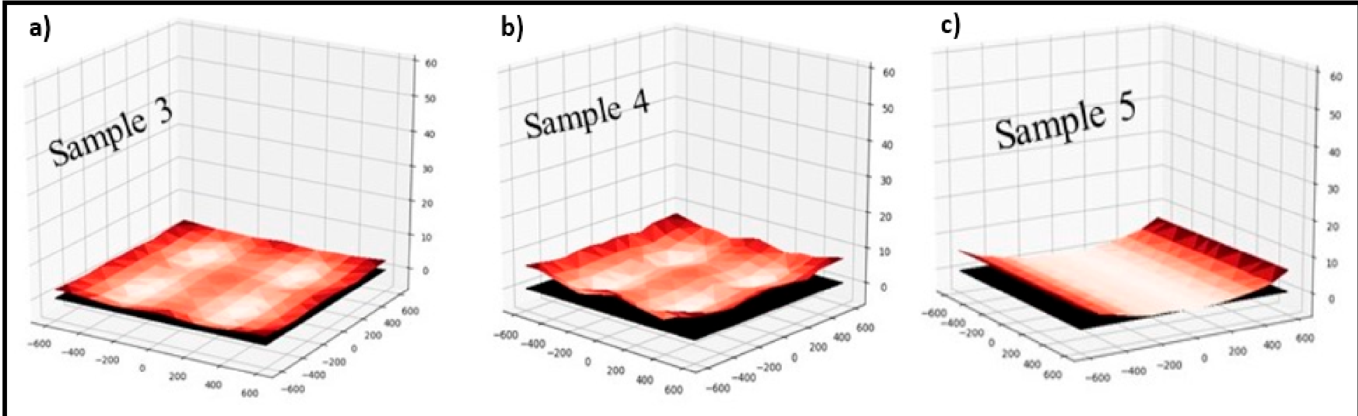


Figure 12: Warpage profiles for: a) sample 3; b) sample 4; and c) sample 5.

Maintaining heat for a 300mm round chuck is relatively more straightforward than for a 600mm square chuck. The power requirement difference and control mechanism needed to achieve setpoint temperature and maintain good uniformity, as well as the ramp-up rate, is significantly higher. As the surface is larger, tight planarity criteria are affected by the thickness of the chuck. Because power is directly proportional to volume, this also affects temperature. All aspects considered, temperature uniformity of ±3°C from 20°C to 200°C, is achieved.

Silicon Wafer Supplier
Spacer, Test, Monitor, Interposer, Reclaimed, Dummy Wafer
Competitive Pricing
High Pure Quality and Wide Range Options
An ISO9001 Certified
Heatsink sub-mount solutions for power devices
Provides high thermal conductivity ceramics substrates with thin thickness 100um and both side ground and polished.
With customer designed package circuit including metal deposition and patterning services for 3D TSV package in LED and power IC applications.
Contact: JHI CO.,LTD Taiwan james@jhtek.com.tw

Sample No.	Total Panel Thickness	Panel Layout	Die Shape
1	550µm	Single	Square
2	800µm	Single	Square
3	550µm	2x2	Square
4	800µm	2x2	Square
5	550µm	Single	Rectangular

Table 1: Overview of samples.

Thermal debond evaluation

Taking learnings from the FOWLP thermal debonding process flow, a manual panel-level system was made and optimized, baselining the contactless transport and ensuring good thermal control across a large surface area. Aspects of the evaluation are discussed below.

Scope of the experimentation. Different panel structures were evaluated with the system described above and warpage response was recorded. The thermal performance of the chuck was also examined to ensure good uniformity prior to processing the panels.

Methodology. A two-phase evaluation was performed as follows: 1) Checked the thermal performance of the large-area chuck in comparison with 300mm round chucks; and 2) Evaluated the performance of the thermal chuck plus the air-cushion handling mechanism to see the magnitude and profile of the output panel from the defined process flow.

An 81-point temperature mapping was performed on the chuck at three different temperatures: 100°C, 150°C, and 200°C.

Warpage was measured post-debond with a "shock and lock" treatment and compared to debonded panels through a pick-and-place debond method.

Samples preparation. A number of factors were hypothesized to affect warpage level as observed from wafer-level fan-out packaging and will also be tested for panel-level fan-out packaging. Five samples were prepared with a different structure configuration, taking into consideration the hypothesized warpage contributors. Samples 1 and 2 are single-matrix (Figure 9a) with 4x4mm^2 die size and thicknesses of 550µm and 800µm, respectively. Samples 3 and 4 have a 2x2 matrix panel layout with 4x4mm^2 dies, and thicknesses of 550µm and 800µm, respectively. Sample 5 is a 550µm-thick panel, single matrix with a 5x7mm^2 rectangular die.

Table 1 summarizes the data collected as listed above.

Results and observations

The temperature test performed on the large format chucks showed good thermal uniformity (Figure 10 and Table 2). The good thermal performance is evident with the uniform release of the thermal tape during the debond test vehicle runs. The debonding temperature was set to 190°C with 90 seconds soak time.

Setpoint Temp (°C)	100	150	200
Ave (°C)	100	150.05	199.70
Min (°C)	98.9	148.61	197.50
Max (°C)	101.08	151.77	202.20
Range (°C)	2.18	3.16	4.70
Uni %	97.82	97.89	97.65

Table 2: Observed temperature uniformity across the chuck surface.

Sample No.	Total Panel Thickness	Panel Layout	Die Shape	Warpage Response
1	550µm	Single	S	2-3mm
2	800µm	Single	S	5-6mm
3	550µm	2x2	S	3-4mm
4	800µm	2x2	S	5-6mm
5	550µm	Single	R	7-8mm

Table 3: Overview of warpage response data.

Warpage response

Table 3 shows warpage response data. Samples 1 and 2 showed a similar profile with different levels of magnitude. The thinner mold cap had less warpage compared to the thicker one (Figure 11).

Samples 3, 4 and 5 displayed different profiles to the first two samples (Figure 12).The warpage response of Samples 3 and 4 showed that the thinner panel was less warped than the thicker panel, matching the responses seen from Samples 1 and 2.

Summary

As we observed from wafer-level experience, mimicking the optimized methods, such as contactless transport, will result in an acceptable warpage level that succeeding processes can handle. Layout and thickness of the panel play a significant role in the output magnitude and profile of the panel warpage. High thermal uniformity >97% (+/-3°C) was achieved as tested up to 200°C for a large-panel chuck.

The manual thermal debonding system has been proven to overcome large-scale adoption from wafer-level format to panel-level format. The next action to take is to create an architecture with full automation.

References

1. J. H. Lau, et al., "Warpage and thermal characterization of fan-out wafer-level packaging," IEEE Trans. on Comp., Pkg. and Mfg. Tech. (CPMT), vol. 7, no. 10, pp. 1729-1738, Oct. 2017, doi: 10.1109/TCPMT.2017.2715185.
2. D. C. Sanchez, K. Reitinger, S. Oldeide, K. Zhao, W. Song, I. Khwaja, "A unique and robust technique to eliminate warpage for FOWLP and FOPLP during the thermal debonding process," 2019 Inter. Wafer Level Pkg. Conf. (IWLPC), San Jose, CA, USA, 2019, pp. 1-6, doi: 10.23919/IWLPC.2019.8914129.
3. S. Oldeide, R. Beckmann, L. Giai-Miniet, K. Reitinger, "Thermal debonding and warpage adjust of FOWLP - a crucial step in the evolution of advanced packaging?," IWLPC, San Jose, CA, 2018, pp. 1-6, doi: 10.23919/IWLPC.2018.8573267.

PLASMA ETCH
PROGRESS THROUGH INNOVATION
PLASMA IMPROVES BONDING!
Our fully automated plasma cleaners offer:
-Improved Markability
-Enhanced Adhesion
-Better Bonds
-Easier Assembly
-Surface Modification
100% removal of organic contaminants with a low environmental impact!
STARTING AT ONLY
$ 5,900 USD
TO LEARN MORE, VISIT WWW.PLASMAETCH.COM
OR CALL 775-883-1336

Biographies

Debbie Claire Sanchez is the Fan-out Equipment Business Unit Manager at ERS electronic GmbH based in Munich, Germany. She has worked for more than seven years in the field of wafer-level packaging (fan in and fan out), and is now driving the development of ERS' thermal debonding and warpage adjustment manufacturing equipment for fan-out applications. Prior to ERS, she worked for Deca Technologies. She holds a Master's degree in Physics from Mindanao State U. in the Philippines. Email: sanchez@ers-gmbh.de

Klemens Reitinger is CEO and CTO at ERS electronic GmbH based in Munich, Germany. He completed his Master's Degree in Mechanical Engineering at the U. of Applied Sciences in Vienna.

Hi-resolution dry-film PID material for high-density packaging

By Yuya Suzuki, Chihiro Funakoshi, Daisuke Shibata, Daichi Okamoto, Yoko Shibasaki [Taiyo Ink Mfg. Co.., Ltd.]

This paper reports a new dry-film type photo-imageable dielectric (PID) material for fine-pitch and high-density multi-layer RDL structuring. High-density packaging technologies are substantially required for high-speed signal transmission in a variety of applications, such as high-performance computing, artificial intelligence (AI), and 5G communications. To achieve high functionality, new integrated circuit (IC) packaging technologies including fan-out wafer-level packaging (FOWLP), fan-out panel-level packaging (FOPLP), and high-density substrates have been intensively studied and developed. These technologies endeavor to have high-density redistribution layers (RDLs) for signal routing with <5µm fine-pitch L/S Cu wiring and <10µm small interlayer via structures. Evolution in semi-additive process (SAP) technology has enabled 2µm L/S wiring formation by applying the latest materials and processing technologies. However, current mainstream laser processing for via formation by CO_2 laser or Nd-YAG laser cannot achieve ultra-small vias <10µm [1,2].

Although new laser processing such as short-wavelength solid lasers and excimer lasers have been developed to achieve <10µm via structures [3,4], installation of new laser tools requires a large investment, careful handling, and laborious maintenance. On the other hand, photosensitive dielectric materials can form small vias by existing photolithography stepper or mask aligner tools, so the materials are useful for high-density RDL manufacturing. Taiyo Ink has developed a new PID material, featuring: 1) Dry-film type for high surface planarity; 2) Low curing temperature (180°C); 3) Low coefficient of thermal expansion (CTE); 4) High resolution for 6-10µm via formation; 5) Resistance to organic solvents; and 6) High dielectric reliability. **Table 1** summarizes the material properties of the PID. The material has low CTE, which is enabled by organic-inorganic composite technology. Also, the PID has high tensile strength and elongation, which are beneficial for high resistance to mechanical stresses—especially when it is applied for a multi-layer RDL.

This paper first describes the benefits and challenges of our previous generation PID material (original PID), and then reports the technical development and evaluation of the latest PID material (new PID) with respect to solvent resistance and dielectric resistance. To demonstrate the reliability of the new PID, test coupons for line-to-line reliability and layer-to-layer reliability were fabricated, and biased highly-accelerated stress tests (BHAST) were conducted.

Properties	Unit	New PID
Tg (@TMA)	°C	180 - 185
CTE alpha 1	ppm/°C	35 - 45
Elastic Modulus	GPa	3.0 - 3.5
Tensile Strength	MPa	85 - 90
Elongation	%	7 - 8

Table 1: Material properties of a new PID.

PID material processing

PID materials are organic dielectrics with fine-patterning capability by photolithography processes (**Figure 1**). First, the PID is laminated on base substrate layers by vacuum lamination. After the lamination, photopatterning with ultraviolet (UV) exposure tools are performed, followed by polyethylene terephthalate (PET) film removal and development processes.

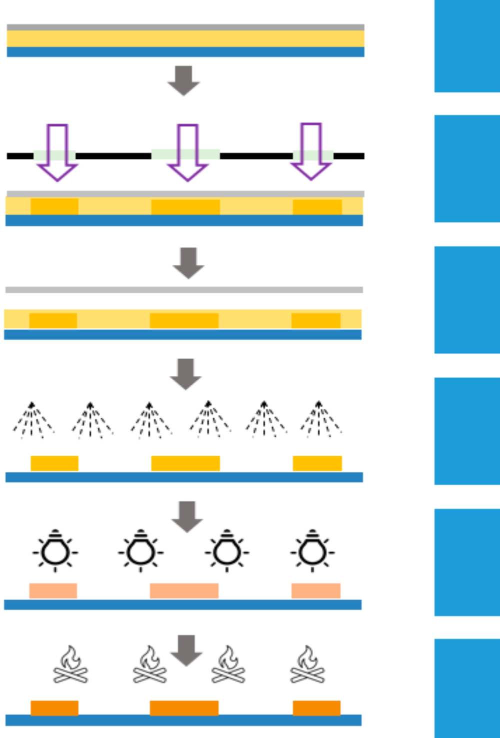


Figure 1: Process flow of PID patterning.

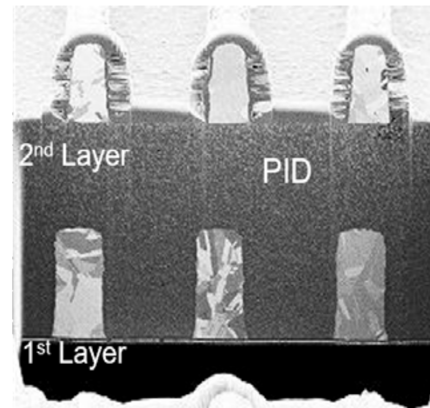


Figure 2: Multi-layer RDL formation in the original PID example with 4μm L/S/ structures.

The PID materials are negative tone, so the UV exposed area of the material undergoes the photoreaction by radical polymerization and becomes insoluble to developer chemicals. For developer chemicals, weak alkaline aqueous solutions such as Na_2CO_3 and tetramethyl ammonium hydroxide (TMAH) are used. Finally, UV cure with an excess amount of UV irradiation, and thermal cure at 180°C, are applied to complete photo- and thermal-polymerization reactions, respectively. The PID materials are dry-film format, and have high resolution and low CTE.

Many of conventional photodielectric materials are in liquid format, and they conformally cover the Cu wirings underneath, and form an uneven surface after the coating process. Such an uneven surface of dielectric layer limits the fine-pitch wiring formation on top. On the other hand, PID materials in this study are in a dry-film format, and a very flat surface is attained after vacuum lamination, even if there are Cu wiring structures under the PID layer. Therefore, it is beneficial for fine-Cu patterning, especially for multi-layer RDL. **Figure 2** shows a cross section of the demonstrated multi-layered RDL structure on the PID material. The highly uniform PID surface on top of the underlying Cu wirings made it possible to form 4μm L/S structures on top of the PID without any additional planarization processes.

The PID materials have excellent patternability and can form <10μm vias by photolithography. In addition to the high resolution, the PID materials have low CTE that is quite important for high reliability with reduced internal stress in packaging applications. A reduction in CTE of dielectric materials is generally attained by addition of inorganic filler particles. Meanwhile, addition of inorganic filler increases UV light scattering at the inorganic-organic interface, thereby exacerbating the photolithography resolution of PID. To overcome this trade-off, nano-sized filler was applied to minimize Mie scattering at a UV exposure wavelength (365nm). Consequently, the PID successfully enables both low CTE down to 35-45ppm/°C, and down to 6μm via resolution (**Figure 3**).

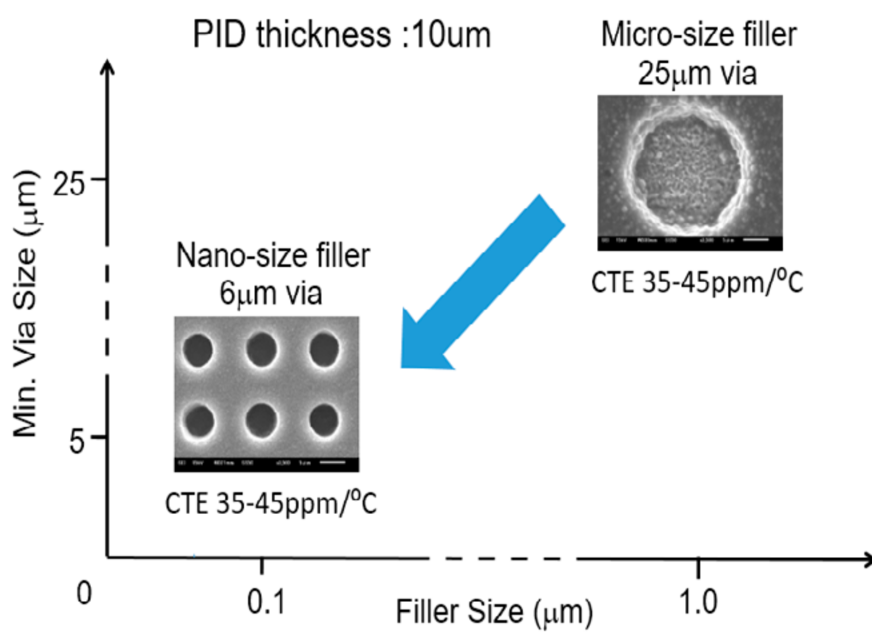


Figure 3: Filler size vs. PID resolution.

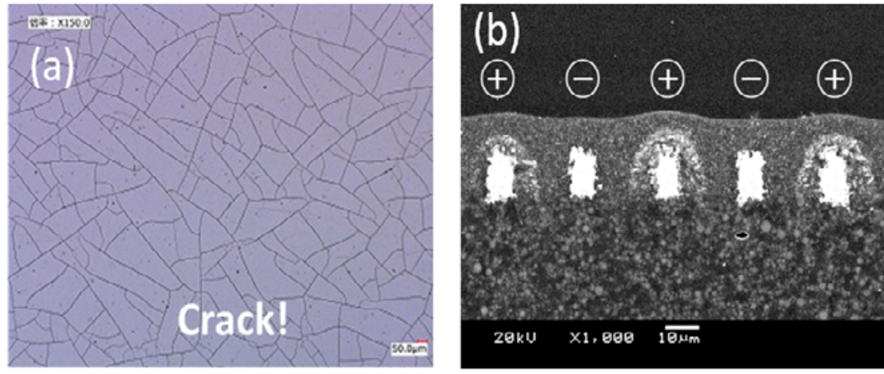


Figure 4: Challenges of the original PID example: a) Micro-cracks after acetone immersion; b) Cu migration with L/S=10/10μm after 100 hours of BHAST.

A dry-film format with low CTE and high resolution are quite useful features for IC packaging applications. However, the original PID had two technical challenges for high-density packaging applications, including FOWLP, FOPLP, and high-density package substrates (**Figure 4**): 1) limited resistance to organic solvents for photoresist stripping; and 2) insufficient BHAST reliability with very fine-pitch Cu wirings.

For fine-pitch Cu patterning by semi-additive processing (SAP), the latest photoresist materials with ultra-high resolution are applied. After Cu plating processes, these photoresist materials are stripped off by organic solvents. However, the original PID experienced severe damage by organic solvents, especially when acetone was used as a stripping agent. As a result, PID materials had microcracks after

30 minutes of dipping in acetone at room temperature. Another issue was BHAST reliability of the original PID. The original PID has acid-modified epoxy-acrylate as the main component, and a residual amount of raw material (epichlorohydrin) generated chloride ion in the final product. Chloride ion in the acid modified epoxy-acrylate catalyzes the Cu migration and leads to compromised dielectric reliability.

To overcome the technical challenges noted above, design of the material and evaluation of the impact of new formulation were investigated. First, a new material design for solvent resistance will be described. Then, chemistry design of the new PID for higher dielectric reliability will be studied, and finally, BHAST analysis to demonstrate the improved reliability will be reported.

Design of a new PID

The following sections discuss elements of the design of a new PID.

Solvent resistance for fine line SAP. Generation of microcracks in PID at solvent immersion is explained by the following mechanisms [5] (**Figure 5**): 1) Internal stress generation during the curing processes of PID; 2) The low crosslinking region in the PID has high permeability of solvent molecules such as acetone; and 3) Stress release initiates the microcrack.

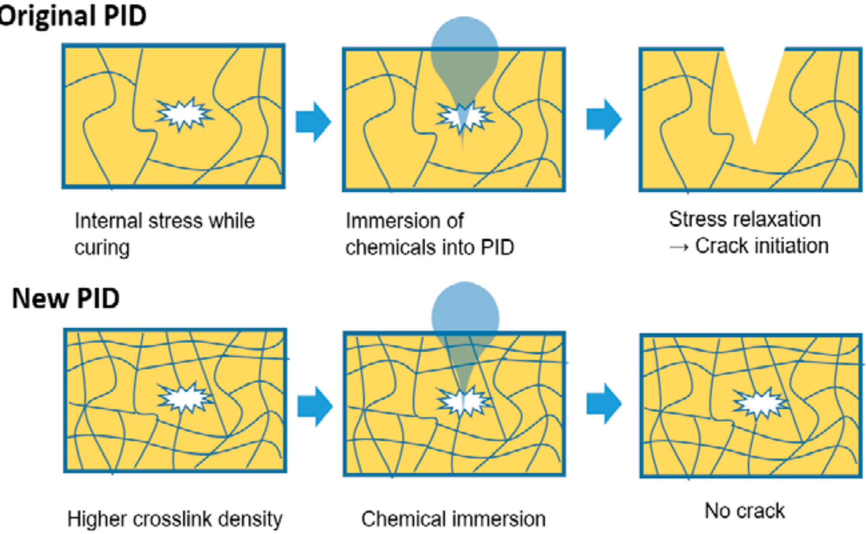


Figure 5: (upper) Mechanism of micro-crack generation in PID by solvent immersion; and (lower) Concept of improving solvent resistance.

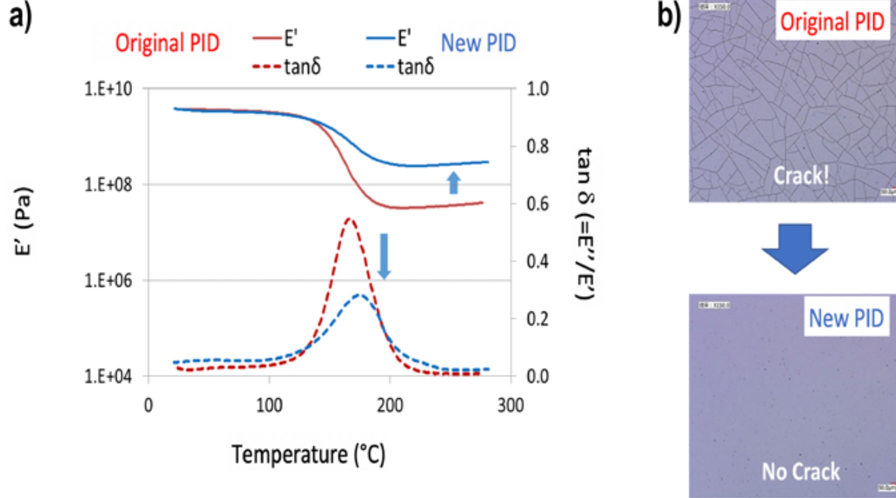


Figure 6: a) (left) DMA charts (E' and tanδ) of the original PID example (in red), and the new PID example (in blue), and b) (photos on the right) the improved solvent resistance.

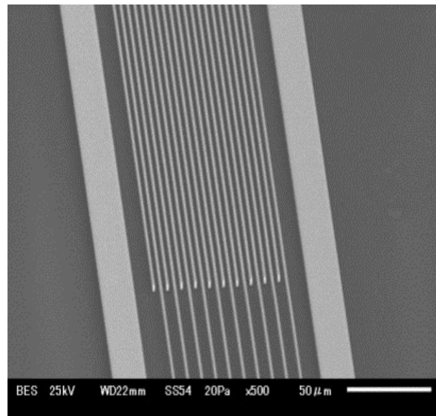


Figure 7: SEM images of L/S=2/2μm fine-Cu patterns on the new PID.

For improving solvent resistance, the amount of chemically reactive groups for crosslinking was increased in the new PID. As a result, the new PID is expected to have higher crosslinking density, which can lead to less permeability of solvent molecules in the material [6] and less microcrack generation (**Figure 5**).

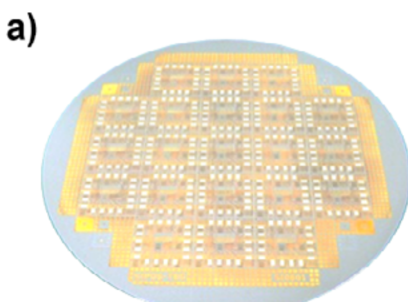
To evaluate the crosslinking density of the original PID and new PID materials, dynamic mechanical analysis (DMA) was applied in this study. In the DMA chart of cured polymer materials, the storage modulus (E′) value above the glass transition temperature (Tg) and the loss tangent (E″/E′ = tan δ) value at Tg indicate the crosslinking density of the material [7]. The Tg value of the material is generally understood to be at the temperature where the tan δ curve peaks out. The original PID has an E′ value around 10E+7Pa at temperatures above Tg, and a tan δ value of 0.55 at Tg. Meanwhile, the new PID with an increased crosslinking reaction group had an E′ of 10E+8 at temperatures above Tg, and a tan δ value of 0.28 at Tg. This higher E′ and lower tan δ peak strongly indicate increased crosslinking density in the new PID. After the DMA evaluation to confirm increased crosslinking density in the new PID, the material was immersed in acetone at the same condition as the original PID, and no microcrack was observed. This confirms the new material design successfully improved the solvent resistance of the PID (**Figure 6**).

After the demonstration, fine Cu-patterning by SAP on the new PID

Figure 8: Chemical reactions to produce resins for the: a) (left) original PID, and b) (right) new PID.

was performed. First, the new PID (10µm thick) was laminated on a 4" wafer by vacuum lamination. After the lamination, a UV dose of 1.0J/cm^2 was applied by an i-line exposure tool. Then, the PID was thermally cured at 180°C for 60 minutes. On top of the PID, Cu patterning was fabricated by SAP as follows: a Ti and Cu seed layer (50nm and 300nm, respectively) was first deposited with a sputtering tool. Photoresist was then coated on top of the seed layer by using a spin coating process at 5µm thickness. The photoresist layer was patterned with a photomask with a L/S = 2/2µm comb pattern, and then developed. After the photoresist patterning, electrolytic Cu plating was conducted to build 4µm-thick Cu patterns. Photoresist was then stripped off with organic solvent, and the seed layer was etched out. As a result, L/S=2/2µm Cu patterns were successfully formed without any residue of photoresist or seed layer (**Figure 7**). This fine-pitch Cu patterning can be achieved by improved solvent resistance of the new PID, which made it possible to select the latest photoresist for patterning.

Cu migration resistance for high BHAST reliability. Material design for better BHAST reliability at fine-pitch L/S was investigated by reducing chloride ion content in the PID material. Cu migration under BHAST conditions is catalyzed by the presence of chloride ion in the system. A Cu ion is stabilized by the presence of a chloride ion, which reduces the activation energy of Cu ion dissolution from the anode side, and a redeposition of Cu metal at the cathode side. Finally, as a result of Cu diffusion, Cu migration occurs. As the spacing between the Cu wirings



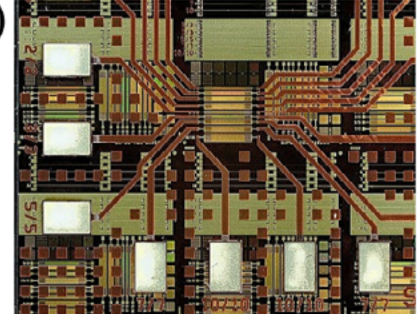
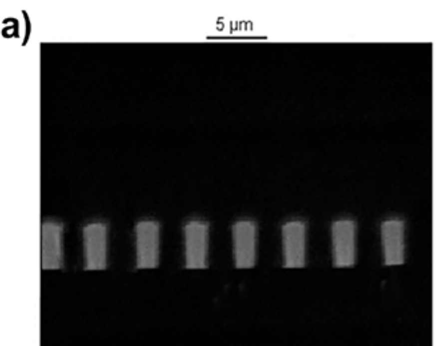


Figure 9: BHAST test coupon a) (left) overview, and b) (right) magnified image.



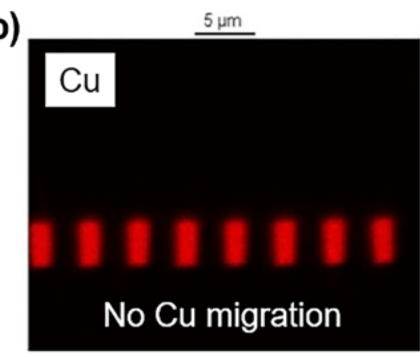


Figure 10: a) (left) Cross-section SEM image, and b) (right) EDS Cu mapping image of 2µm L/S structure after 300 hours of BHAST.

gets smaller, a stronger electrical field is applied in between the Cu wires, and they get more susceptible to electrical shorting. As discussed in prior sections, the original PID includes chloride ion as an impurity, because of the conventional chemical process to synthesize epoxy-acrylate resin. Therefore, a new synthesis of acid-modified resin was studied to eliminate the chloride impurity. First, alkylene-oxide was added to the phenolic resin, followed by dehydration between the alcoholic group and the acrylic acid. Then acid dehydrate reacted with the molecule to complete the reaction (**Figure 8**). Unlike the epichlorohydrin-based synthesize route, this new synthetic route does not have any chloride impurity. So, no chloride ion is expected in the new resin.

To validate this hypothesis, ion chromatography analysis was conducted to detect chloride ion contents in the conventional acid-modified epoxy-acrylate and in the new acid-modified resins. As

The 2021 IEEE 71st Electronic Components and Technology Conference

June 1 - July 4, 2021

Due to the COVID-19 pandemic, the 71st ECTC, electronic packaging's premier conference, will be held as a virtual event, enabling remote participation from anywhere in the world.

The only event that encompasses the diverse world of integrated systems packaging.

Visit ECTC.net for additional information.

350+ TECHNICAL PAPERS COVERING:

Fan-Out WLP & CSP
3D & TSV Processing
Heterogeneous Integration
Fine Pitch Flip-Chip
MEMS & Sensors
Advanced Substrates
Advanced Wire Bonding
Flexible & Wearable Devices
RF Components
Automotive Electronics
Harsh Environment
Bio/Medical Devices
Thermal/Mech Simulation
Interconnect Reliability
Optical Interconnects

HIGHLIGHTS

- 46 technical sessions with a total number of 350+ technical papers including:
  - 10 topical sessions hosted by the IP Subcommittee
- 5+ special invited sessions
- 50+ live Q&A sessions
- 14 CEU-approved Professional Development Courses
- Multiple opportunities for networking
- Technology Corner Exhibits, showcasing industry-leading product and service companies from around the world
- Various sponsorship opportunities for your company's visibility
- Great and professional digital platform solution

CONFERENCE SPONSORS:

OFFICIAL MEDIA SPONSOR:

Chip Scale Review

designed, no chloride ion was detected in the new resin, while more than 500ppm of chloride ion was included in the conventional resin. Once the synthesis of the new resin without chloride ion was established, the new resin was applied to the new PID formulation, and a BHAST reliability analysis was conducted.

Demonstration of BHAST reliability

Test coupons for BHAST analysis were L/S = 2/2µm comb-like Cu patterns, and they were fabricated on the first layer of the new PID by the same SAP processes as in the previous section. After the Cu patterning, the second layer of the new PID was laminated on top by vacuum lamination and cured to complete the test sample fabrication (**Figure 9**).

Fabricated test coupons were applied to the reliability testing with the following conditions:

- Preconditioning: 125°C/24h ⇒ 85°C/168h ⇒ Reflow 260°C/3 times; and
- BHAST: 130°C, 85% @5V (failure criteria : 1.0E+6 ohm)

For a BHAST chamber, a HASTEST® MODEL PC-R8D (Hirayama) was used, and for in situ electrical resistance measurement, a MIGRATION TESTER MODEL MIG-8600B (IMV) was used. There was no migration or electrical failure after 300 hours of BHAST condition. The cross-section analysis was then conducted, and the X-ray scanning electron microscope (X-SEM) images of 2µm L/S structures (**Figure 10**) also show no sign of Cu migration from the fine-pitch Cu wirings. Layer-to-layer BHAST reliability of a PID thickness of 5µm was also conducted and no failure after 300 hours was confirmed.

Summary

In this study, a new PID was developed based on the material design. The PID has low CTE (35-45ppm/°C) and high resolution (down to 6µm), which is beneficial for multi-layer RDL formation. The PID has high resistance to organic solvents for fine-pitch SAP, and no crack in the PID was formed by acetone dipping. As a result, very fine Cu line patterning of 2µm L/S was successfully demonstrated. A new synthetic method of acid modified acrylate resin with no chloride impurity was developed. The new PID applies the new resin, and BHAST evaluation showed more than 300 hours of electrical reliability with 2µm L/S and a 5µm thin PID layer. The PID material has fine-patterning capability, as well as excellent reliability, therefore it is a highly beneficial dielectric material for high-density packaging applications, such as FOWLP, FOPLP, and high-density package substrates.

Acknowledgements

The authors would like to acknowledge the technical support from Research Center for Three-Dimensional Semiconductors, in fabrication of test coupons for BHAST evaluations. The authors also thank Mitsui Mining & Smelting Co., Ltd. for its technical support in multi-layer RDL structure fabrication.

References

1. K. Yamanaka, K. Kobayashi, K. Hayashi, M. Fukui, “Materials, processes, and performance of high-wiring density buildup substrate with ultralow-coefficient of thermal expansion,” Comp. and Packaging Tech., IEEE Trans. on, vol. 33, pp. 453461, 2010.
2. T. Yamada, M. Fukui, K. Terada, M. Harazono, C. Reynolds, J. Audet, et al., “Development of a low CTE chip-scale package,” 63rd Elec. Comp. and Tech. Conf\. (ECTC), 2013, pp. 944-948.
3. Y. Suzuki, V. Sundaram, R. Tummala, M. Arendt, L. Seongku, H. Hichiri, et al., ”Embedded trench redistribution layers (RDL) by excimer laser ablation and surface planar processes,” 67th IEEE ECTC, 2017, pp. 884-889.
4. Y. Suzuki, J. Brune, R. Senczuk, R. Pätzel, R. Furuya, F. Liu, et al., “Demonstration of 20µm pitch micro-vias by excimer laser ablation in ultra-thin dry-film polymer dielectrics for multi-layer RDL on glass interposers,” 65th IEEE ECTC, 2015, pp. 922-927.
5. Y. Otake, “Troubleshooting of polymer materials,” Kogyo-Zairyo, 66 (8) Aug. 2018.
6. H. Kishi, T. Naitou, S. Matsuda, A. Murakami, Y. Muraji, Y. Nakagawa, “Relationships between mechanical properties and nano-structures of DICY-cured epoxy resins,” J. of the Adhesion Soc. of Japan 41(3), 84-92, 2005-03-01.
7. I. M. Barszczewska-Rybarek, A. Korytkowska-Walach, M. Kurcok, G. Chladek, J. Kasperski,”DMA analysis of the structure of cross-linked poly(methyl methacrylate) s,” Acta of Bioengineering and Biomechanics Vol. 19, No. 1, 2017, pp. 47-53.

Biographies

Yuya Suzuki is a Marketing Manager of Taiyo America, a sister company of Taiyo Ink Mfg. Co., Ltd., San Jose, CA. He has more than 10 years of experience in electronic materials for advanced IC packaging. Before joining Taiyo Ink, he worked for Zeon Corporation, and the 3D Packaging Research Center at the Georgia Institute of Technology. He has a PhD in Material Science from Georgia Institute of Technology. Email YuyaS@Taiyo-America.com

Chihiro Funakoshi is an Engineer at Taiyo Ink Mfg. Co., Ltd., Saitama, Japan, where, since 1994, he has been developing polymer-based products for IC packaging. He received BS and MS degrees in Chemistry from Toyo U., Japan. He has authored more than 10 patents on polymer materials.

ADVERTISER INDEX

Amkor Technology www.amkor.com 1

Brewer Science www.brewerscience.com 26

Corning www.corning.com/carrier 29

CyberOptics www.cyberoptics.com 11

DL Technology www.dltechnology.com 61

E-tec Interconnect www.e-tec.com 51

ECTC www.ectc.net 62

EV Group www.evgroup.com 2

INTEKPLUS Co., Ltd. www.intekplus.com 13

Ironwood Electronics www.ironwoodelectronics.com 47

JHI Co. Ltd. Taiwan www.jhtek.com.tw 56

Johnstech International www.johnstech.com/markets/automotive .... IBC

LB Semicon www.lbsemicon.com 24

Leeno Industrial www.leeno.com .... IFC, 18

MacDermid Alpha www.macdermidalpha.com 34

MRSI Systems www.mrsisystems.com 7

Pac Tech www.pactech.com 15

Plasma-Etch www.plasmaetch.com 57

Screen Semiconductor Solutions www.screen.co.jp/spe/en/products 9

Sonix www.sonix.com 52

SPIL www.spil.com.kr .... OBC

SÜSS MicroTec www.suss.com 41

TestConX www.testconx.org 64

TSE Co. Ltd www.tse21.com.kr 4,5

Universal Instruments www.uic.com 31

UTAC Group www.utacgroup.com 21

WinWay Technology www.winwayglobal.com 43

Yield Engineering Systems www.yieldengineering.com 37

May June 2021
Space Close May 5th
Materials Close May 10th

For Advertising Inquiries
ads@chipscalereview.com

Johnstech®

FULL-SPECTRUM AUTOMOTIVE SOLUTIONS

- ADAS Systems
- Body Electronics & Lighting
- Infotainment & Cluster
- Hybrid, Electric & Powertrain Systems

EXPERIENCE A CUT ABOVE

- Rapid Delivery Enabling Faster Time to Market
- High-Quality Test Solutions
- Extensively Experienced Field Service and Support

30th ANNIVERSARY

FOR MORE INFO, VISIT JOHNSTECH.COM

JOHNSTECH.COM/MARKETS/AUTOMOTIVE

© 2021 Johnstech International Corporation.

ADVANCED PACKAGING

FO-MCM

FO-EB

2.5D

RISING TECHNOLOGY OF THE NEW ERA

SPIL