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The Future of Semiconductor Packaging

Volume 25, Number 4

July • August 2021

A new era of computing performance with hybrid bonding

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- Low-temperature polyimide processing for next-gen backend applications
- 3D polylithic integration and thermal implications on BEOL RRAM performance

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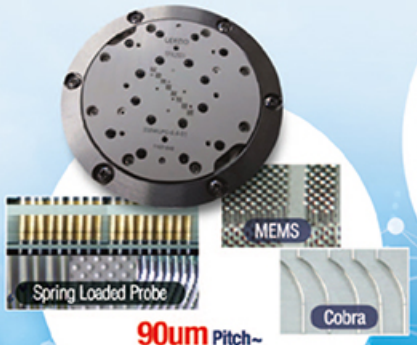
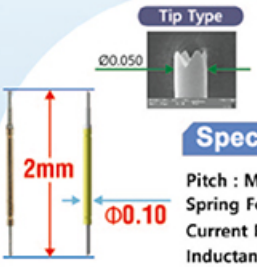
Probe Head



90um Pitch~

RF Probe for Fine Pitch Probe Head



Specification

Pitch : Min.120um
Spring Force : 8.0g@250um
Current Rating : 1.3A
Inductance : 0.3nH

RF Coaxial Spring Probe & Impedance Controlled Socket

0.18mm Pitch~

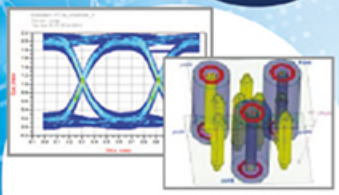
Logic Test Socket

High Speed Automatic Coaxial Probe

Frequency : >20GHz
VSWR : < 1.2

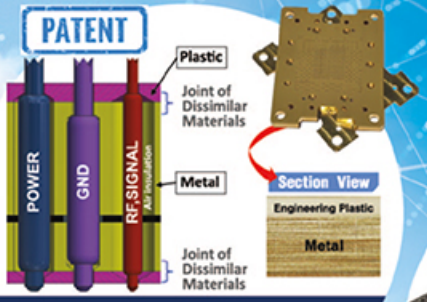
5G

Electrical Analysis

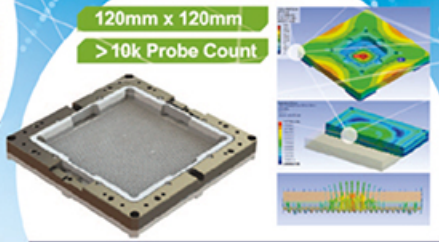


CCC Test, HFSS, TDR
Eye Diagram
4Port VNA Test

MP Socket



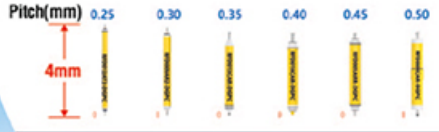
Large Device Socket



Coaxial Probe for 100GHz

Specification

Frequency : 80GHz(BGA),
100GHz(QFN, LGA)
Pitch : 0.25mm~
Crosstalk : -60dB
Impedance : 50Ω±10%



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Volume 25, Number 4

Beyond Moore's law, 3D semiconductors are the foundation for next-generation smart and connected devices. Hybrid bonding technologies enable 2.5D- and 3D-stacked integrated circuit (IC) solutions providing high-density chip-to-chip connectivity to boost the computing performance in data center, gaming, artificial intelligence (AI), machine learning, autonomous vehicle, 5G and Internet of Things (IoT) applications.

Cover image courtesy of Xperi/Invensas

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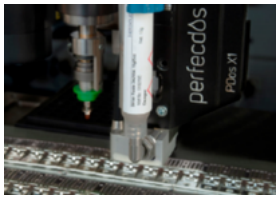

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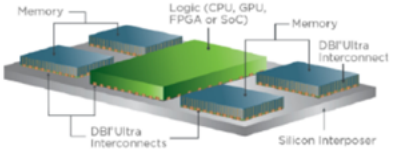

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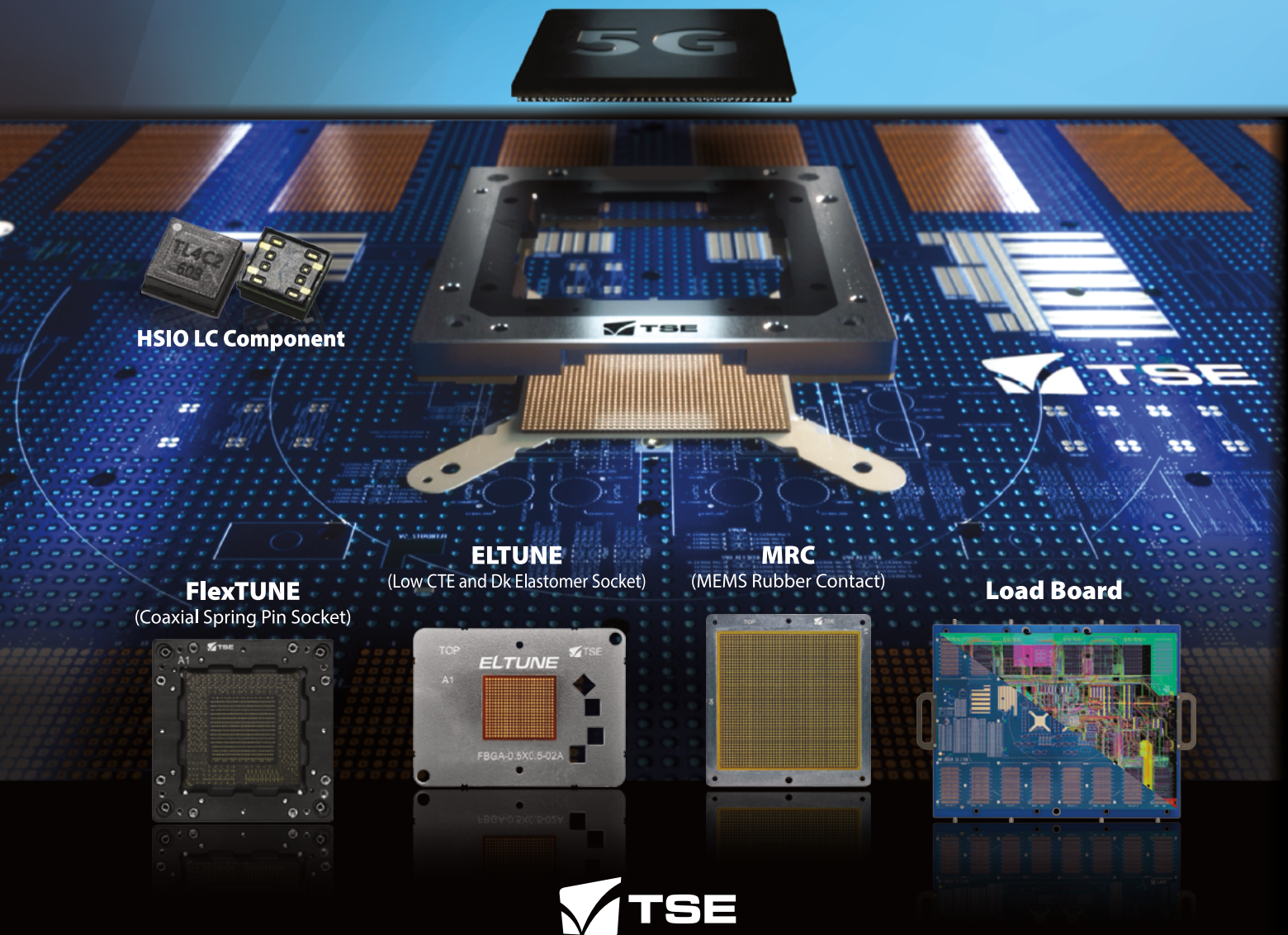
FEATURE ARTICLES *(continued)*

TSE

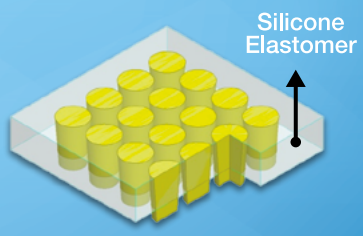
64Gbps ULTRA HIGH SPEED TEST SOLUTION



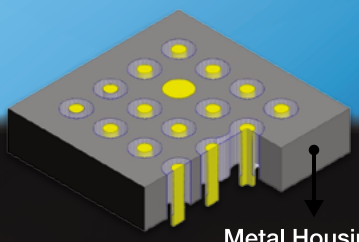
TSE

COAXIAL ELASTOMER SOCKET

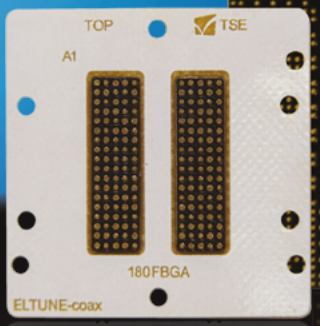
ELTUNE-coax™



Conventional Elastomer Socket



ELTUNE-coax



GDDR6
(18Gbps)

CPU/GPU
(32/64Gbps HSIO,112Gbps PAM4)

• Mechanical Specification

(unit: mm)

0.80mm pitch	Spring Pin	Elastomer	ELTUNE-coax
Over-drive	0.40	0.25	0.25
Test height	3.50	0.60	0.60

• Electrical Specification

(unit: GHz)

42.5Ω, 0.80mm pitch		Spring Pin	Elastomer	ELTUNE-coax
Insertion Loss S_{21} @-1dB	Single Ended (G-S-G)	13.93	27.81	>100
	Differential (G-S-S-G)	25.39	28.94	>100
Return Loss S_{11} @-10dB	Single Ended (G-S-G)	10.98	15.89	>100
	Differential (G-S-S-G)	20.77	25.20	48.21
Crosstalk S_{31}, @-20dB	G-S-S-G	8.50	9.43	>100

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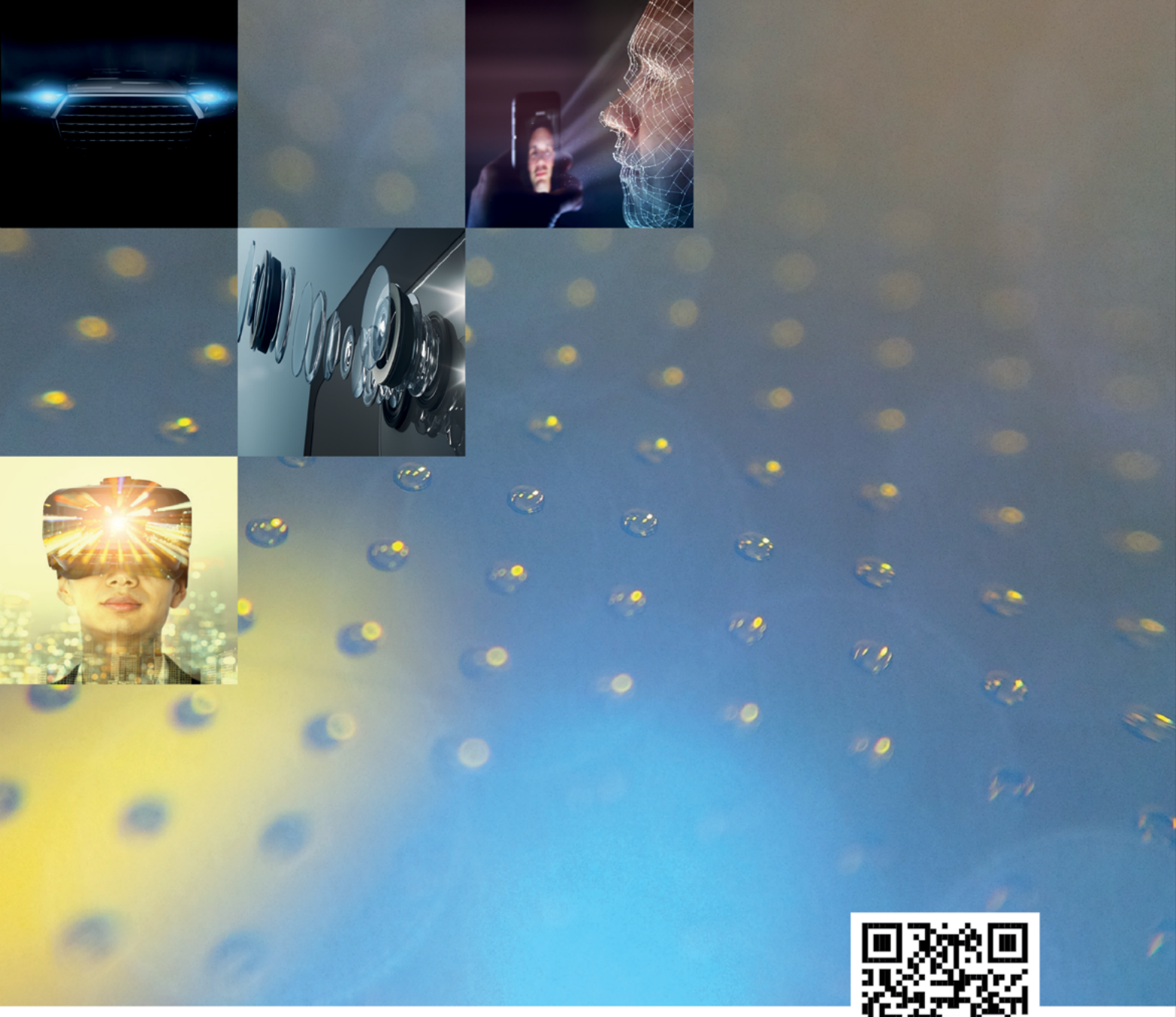

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Developments in jetting sinter paste

By Dennis Ang [Heraeus Materials Singapore Pte. Ltd.] Benjamin Kratz [perfecdos GmbH]

The global power electronics market is projected to grow from USD35.1bn in 2020 to USD44.2bn by 2025, at a compound annual growth rate (CAGR) of 4.7%. Energy-efficient power devices to build the backbone of power applications are in particular demand. Among them, a noticeable global trend is vehicle electrification where increasing adoption of battery-assisted or hybrid electric vehicles and construction of necessary charging infrastructure are registered. Power electronics plays a crucial role to distribute energy reliably while ensuring losses are kept to a minimum.

Most manufacturers of power electronics rely on soldering for their die attach process to assemble device packages. Lead-free solders of tin-silver (SnAg) alloy are commonly used for die attach of power modules, while smaller power devices necessitate the usage of high melting point solders where a lead-tin-silver (PbSnAg) alloy is widely adopted. Because the development of new power devices values flexibility, the tendency is to lean towards paste for die attach applications.

What is sufficient for many standard applications, however, is reaching its limitations in modern technologies. The demand for more powerful and innovative devices creates boundaries for manufacturers as they are tasked to develop more product variations at a faster pace.

Challenges of die attach

Electronic devices continue to shrink in size while increasing in power. Higher power densities increase device operating temperature and new processes and materials are necessary to provide greater reliability for longer device lifetime.

Solder, the most common type of die attach material, is at its limit to support the new device requirements. Sintering with silver is considered to be a viable solution. It can overcome higher operating temperature restrictions. A solid material until 961°C, silver has a significantly higher melting point than solders, whether lead-containing or lead-free. Sintering supports higher thermal operating temperatures of more than 250°C because it remains thermo-mechanically stable and shows almost no signs of aging. This is what makes high operating temperatures possible in modern power electronics.

Thinner gauge dies are a challenge for solder with fillet climb and die tilt. In comparison to soldering, the sintering process does not need to go through the liquidus transition phase, thereby minimizing the associated highlighted issues needed to hold die securely to the substrate while maintaining low bond line thickness.

When the precision of depositing paste increases — to maintain bonding layer quality — speed would typically be sacrificed. However, this begs the question of whether or not this is a bottleneck to meeting the growing power electronics market. Another question is how can manufacturers become faster without sacrificing quality, reliability, and performance? To meet these requirements, Heraeus, perfecdos and Infotech have come together to investigate viable solutions for realizing shorter cycle times. While soldering would continue to dominate, sintering has most of the attention. From the onset, the team decided to focus on sintering. We were keen to work with a non-pressure sinter process for applications to smaller packages. We, therefore, set about to identify the critical bottlenecks to attain higher device throughput to meet increasing power electronics demand.

The sinter paste

Sintering employs the principal of diffusion to produce a solid material bulk at below its melting point. Much attention is placed on applying silver (Ag) sinter paste for die attach (DA) of wide band gap (WBG) semiconductor devices. The greater power efficiency, higher switching frequency and increase in power density are benefits identified with a WBG semiconductor. The resulting increase in operating temperature necessitates a more superior die attach material to assure reliable operation throughout the device's lifetime.

Compared to a solder layer, Heraeus Electronics' non-pressure Ag sintered layer (**Table 1**) offers more than two times the thermal capacity increase and a high

Material Properties	Conductive Adhesive	Solder Paste (PbSn5Ag2.5)	mAgic Sinter Paste DA295A
Process Temperature (°C)	175 ~ 200	360 - 390	≥ 200
Ag Content (%)	75 ~ 85	2.5	100 (after sintering)
Electrical Resistivity (mΩ.cm)	≤ 0.1	0.046	≤ 0.008
Thermal Conductivity (W/m.K)	3-10	44	≥ 100
Residue-free	Yes	No	Yes
Pb-free	Yes	No	Yes

Table 1: Die attach material comparison chart.

Paste	Alloy	Metal Content	Application	Particle Size	Sinter Temperature	Compatible Surfaces	Sintering Atmosphere
DA295A	Silver	82%	Dispensing	≤ 25µm	≥ 200°C	Ag, Au	Air, N_2

Table 2: Heraeus sinter paste properties.

melting point of 961ºC. It is a compatible replacement candidate for WBG-based power packages. It requires a processing temperature at only 200ºC to form a low-voiding pure Ag interconnection between the die and substrate. The paste's stable rheology is fundamental to support a consistent paste deposit volume for extended high-speed dispensing operation (**Table 2**). It is already suitable for traditional time-pressure dispensing methods and can dispense consistently at 10mm/s for up to 12h. This widely adopted application technique is sufficient to meet prevailing production cycle time requirements.

Closely tracking the packaging trend of device miniaturization, it is desired to maintain flexibility balanced against a faster cycle time. The key lies in a complementary solution of equipment and sinter paste material to bring about accurate paste deposits onto reduced pad areas in a high-throughput production environment.

Sinter paste jet dispensing

In terms of dispensing, the sinter paste behaves comparably to a material with a very low surface tension and, at the same time, has a high density. During contactless dispensing, or jetting, the material fillers represent a further challenge as they influence the cut-off behavior, which in turn is different compared to most standard jetting materials.

The materials' outflow in contactless dispensing is achieved by generating a dynamic pressure, which is greater than that of static pressure, through movement of a closing element (tappet). One of the key objectives is to determine the parameter range that produces just the necessary dynamic pressure without accelerating the material. The fact that the flow resistance grows with increasing viscosity, nozzle length and decreasing nozzle diameter is yet another critical variable in the development's equation. As a result, a new nozzle/tappet combination was engineered to achieve a clean dispensing pattern. It is important to note that not only rheological material properties were taken into account, but also special chemical properties of the sinter paste that show corrosive action with some of the typically used steel alloys.

Perfecdos' micro-dispensing valve, PDos X1, enables the "ramps," which describe the movement of the tappet in the distance/time ratio, to be targeted precisely within a generous range. As a result, it was possible to achieve an end result with this newly developed nozzle/tappet combination that enabled high dispensing speed and clean application patterns.

On a classic time-pressure dispensing system, Heraeus sinter paste material has achieved a highest speed of 10mm/s. The same material coupled with perfecdos' jetting system has established a highest working speed of 30mm/s. There are even more advantages than the 3x faster cycle time. Contactless dispensing eliminates the need to move the valve in the Z-axis and therefore, not only shortens cycle times, but also minimizes the risk of collision with the lead frame, which is not an ideally flat surface (**Figure 1**). Another benefit is the consistency of the applied quantity. The classic pressure-time dispensing system works by contact, so that material carryover at the needle tip cannot be completely avoided. During jetting, the substrate to be coated is not touched with a drop adhering to the nozzle orifice. The overall result is a highly flexible production process that can be used where screen printing processes are not applicable, but high throughput rates are still required.

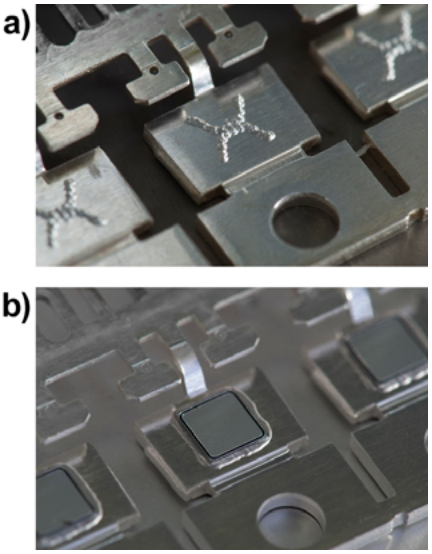

Figure 1: Lead frame dispensing: a) a dispensed lead frame; and b) a lead frame with a chip.

Production process

The sinter paste jet dispensing system is based on Infotech's Component Matrix, which is built on different cell sizes, Cartesian gantry systems, and a variety of machine components for jetting, assembling, die bonding, and many other process steps. The system's design displays multi-axis capability. Up to three dispensing axes, or up to six assembly heads, can be used in parallel on the same gantry. Each dispensing axis can also be equipped with its individual valve technology.

A universal interface is available so that the dispensing valves can be exchanged quickly and easily. Depending on the requirements for the dispensing result and the properties of the dispensing medium, jet valves, time-pressure valves or screw dispensing systems are used. For the application of the Heraeus sinter paste presented here, the perfecdos system described above provides the best results. Compared to other processes such as time-pressure, the jet dispensing process is much more flexible and less susceptible to fluctuations in the dispensing level, which is exactly the case with lead frames.

Axes control

The system achieves dispensing accuracy through integrated real-time controllers. The main portal axes are equipped with linear motors and

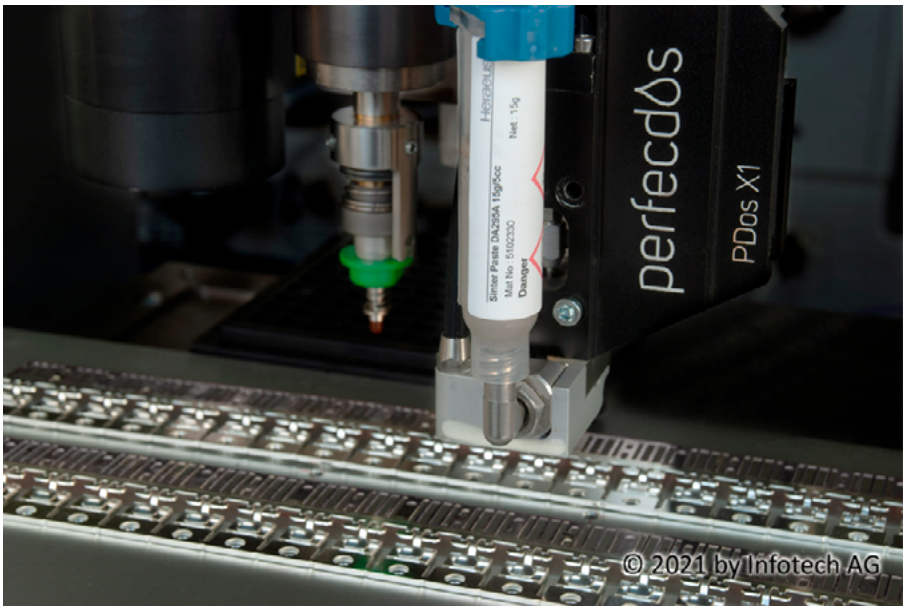

Figure 2: A jet dispensing process set-up.

encoders. The repeatability is specified at 10µm at 3 sigma, and the resolution of the main axes is 0.2µm. When approaching a defined position, it is crucial that the axis movement is permanently controlled with a closed loop.

Calibration of the dispensing system

A camera traveling with the robot head is used to detect the dispensing position and to calibrate the dispensing system. With X and Y offset calibration, it is not the needle or nozzle that is calibrated, but rather, the dispensed dot. For very precise applications, it is possible to dispense multiple dots onto one transparent film. The X- and Y-offsets are calculated by statistical filters based on the dot positions. Different illuminations, field of view sizes and image sensor resolutions are available depending on the particular application's requirements.

Process reliability

To ensure that a dispensing job that has been started is not aborted because of process fluctuations, various tools ensure process reliability. Both hardware and software incorporate functions for process monitoring. The dispensing result can be qualified by checking the dot size or line width. The results can be saved as a log file or further processed with traceability software. Connection to a line computer is available as an option.

The Interactive Media Finder is a timesaving, efficient and intuitive helper, especially for process development. Parameters can be changed during live dispensing, which has an immediate effect on the dispensing result, and can be observed or measured. Once the optimal parameters have been found, they can be saved in the database with a mouse click and called up in application programs. During dispensing, changes can be made in the software until the optimal parameters are found. In addition, there is the possibility of viscosity compensation. This is performed based on the measured dispensing results such as the dot diameter or weight of the material measured onto an integrated analytical scale. The corresponding dispensing parameters are then automatically adjusted. As a rule, two different dispensing parameters can be selected in the dispense set. In the case of an electro-pneumatic jet valve, this can be, as an example, the working pressure or the opening time. Viscosity compensation ensures compensation for the chemically-induced viscosity fluctuations of dispensing media and therefore, also ensures a precise dispensing result.

Other system attributes

The cleaning of the dispense needles or nozzles is performed fully automatically in the program, as required after a desired number of cycles, components, or after a defined period. Periodic cleaning of the entire dispensing system is an important aspect for precise and repeatable dispensing. If necessary, X, Y and Z offsets calibration is performed automatically in the manufacturing process.

The process steps that usually follow the application of sinter paste – for example pick & place or die bonding – can be integrated on the same system. In addition to a small footprint, this also guarantees minimized time spans between dispensing and placement processes. Chip bonding can be done directly from the wafer or from any other feeding system.

Biographies

Dennis Ang is the Global Product Marketing Leader for Solder and Sinter Pastes at Heraeus Materials Singapore Pte. Ltd., Singapore. A seasoned professional with more than 15 years of extensive experience in product management and engineering, he is enthusiastic about sintering as a thermal management solution for semiconductor packaging. Graduated with a bachelor's in electrical engineering, Mr. Ang is a Six Sigma Black Belt and practiced lean manufacturing. Email dennis.ang@heraeus.com

Benjamin Kratz is Manager and Application Engineer at perfecdos GmbH, Oberhaching, Germany. During his time at Liquidyn, Micro Dispensing Systems, which became Nordson EFD, he initiated many innovations. He broadened his experience at Mycronic by working with different dispensing systems for a number of applications. In 2019, Mr. Kratz founded perfecdos with colleagues from former Liquidyn.

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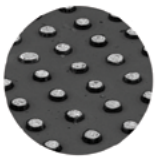
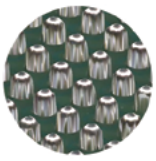
Copper Pillar


Flip Chip (c4)


Micro Bump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A new era of computing performance with hybrid bonding

By Laura Mirkarimi, Abul Nuruzzaman [Xperi Holding Corporation]

Deep learning and other artificial intelligence applications are driving the performance requirements of next-generation computing hardware. To meet the increasing demand for large-scale data analysis, data centers need low latency and significant memory bandwidth, combined with lower power consumption. Designers are integrating high-bandwidth memory (HBM) stacks with high-performance logic die to address this need, but interconnect density limitations are a significant obstacle.

The distributed processing capabilities of HBM, including bandwidth and efficiency, surpass all other off-chip memories. In particular, HBM offers substantially better power consumption. HBM2E (E=evolutionary) devices (5W at 2.8Gb/s bandwidth) consume about half as much power as a GDDR6 solution (10W in a 4-die stack) [1]. There is speculation that HBM3 will be designed with a low voltage swing interface rather than standard complementary metal-oxide semiconductor (CMOS) [2]. Although so far, HBM has been used primarily in niche markets, the HBM performance roadmap is aggressive. HBM3 is expected to double capacity over HBM2E (Table 1). High-bandwidth memory may serve as an intermediate step toward both chiplet-based system on chip (SoC) devices and 3D designs, thereby broadening its market applications [3]. This combination of low power and high bandwidth is highly attractive for compute-intensive applications.

	HBM1	HBM2	HBM2E
# Die/stack	4	2,4,8	4,8,12
Maximum speed	1 Gbps	2 Gbps	3.6 Gbps
Maximum density	4 GB	16 GB	24 GB
Bandwidth/chip	128 GBps	256 GBps	307 GBps

Table 1: HBM specifications comparison.

HBM adoption, however, has been relatively slow, at least partly due to the performance challenges facing the current Cu pillar/microbump technology and associated 2.5D package costs. Cu pillar/microbump technology has taken the industry a long way, but the scalability of established 2.5D and 3D packaging schemes like chip-on-wafer-on-substrate (CoWoS), embedded multi-die interconnect bridge (EMIB), and Foveros is limited by their use of flip-chip interconnects with solder microbumps to connect memory stacks to logic elements (Figure 1). Forming a solder connection flattens the solder

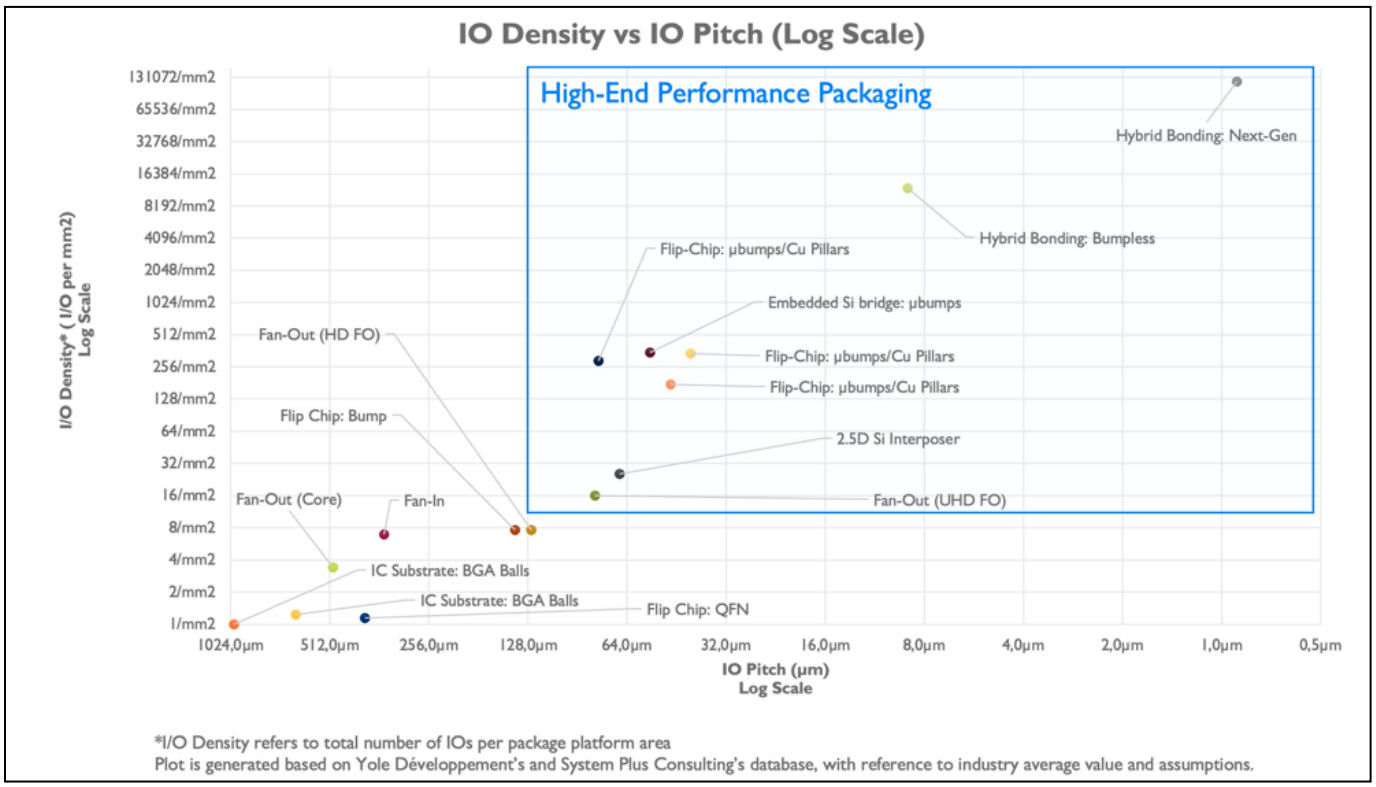

Figure 1: I/O density vs. I/O pitch for 2.5D and 3D packages. SOURCE: High-End Performance Packaging: 3D/2.5D Integration report, Yole Développement, 2020.

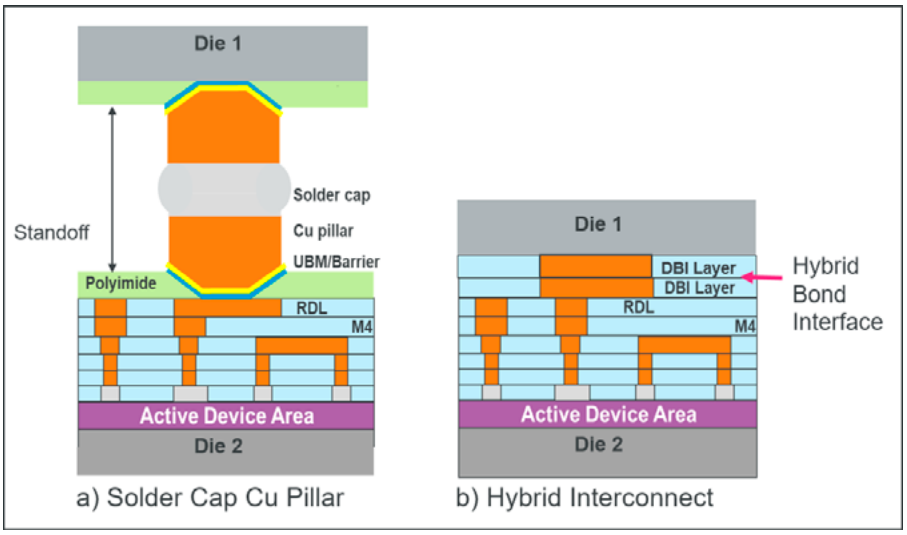

Figure 2: Schematic interconnect drawing for a Cu pillar with a solder cap in thermal compression bonding and direct metal-to-metal hybrid bonding.

bump: the ultimate width is larger than the nominal pitch (Figure 2). Solder bumps need to get smaller as the pitch shrinks, but eventually there simply isn't enough material to ensure a reliable electrical connection. Depending on the approach, the minimum interconnect pitch for solder-based technologies is between 30µm and 55µm. The resulting maximum interconnect density of about 1110 connections per mm^2 sharply limits the memory bandwidth that the package can support. Even Intel's high-density Foveros technology is limited to about 1000 connections per mm^2 [4].

Moreover, interconnect schemes based on copper pillars and microbumps create a 20-25µm separation between die in the stack. After deposition of the last layer of device metallization, additional process steps are required for either copper pillars or pads for solder bumps. Solder is a multicomponent material that is known to have thermo-mechanical stress during operation, which can cause cracking and lead to electrical failures. Organic underfill layers are routinely used to accommodate these stresses, but the high thermal resistance of these layers impedes heat dissipation. HBM die stack performance degrades quickly with heat. Each additional die adds to the thermal nonuniformity through the stack. Data intensive computations need an alternative interconnect scheme to support increasing bandwidth requirements without compromising thermal performance and yield [5].

How hybrid bonding works

The solution to the problem posed above is evident: a die bond layer free of any organic material with all-metal interconnect. Each such die stack will perform thermally like a single die. This hybrid bonding approach eliminates the chip-to-chip connectivity bottleneck by replacing solder bumps with high-density metal-metal 3D interconnects. Metal pads (usually copper) surrounded by dielectric contact each other directly. Before bonding, the metal is slightly recessed relative to the surrounding dielectric. Plasma treatment activates the dielectric surface, allowing a dielectric-to-dielectric bond to form on contact. Though the devices being connected have not yet made electrical contact, this bond is strong enough to allow handling, assembly of multi-chip stacks, and so on. Once the complete stack is ready, a final elevated temperature step causes the pads to expand, contacting each other and making a strong metal-to-metal bond.

In this structure, there is no solder material, no separation between the devices, and no need for an underfill layer. The inorganic dielectric provides mechanical support, protects the copper surfaces from contamination, and gives superior thermal conductivity. The direct copper-to-copper connection minimizes electrical resistance and maximizes heat dissipation.

Copper pad fabrication for hybrid bonding uses the same inlaid metal damascene process as the on-chip interconnect metallization used throughout the semiconductor industry. This mature, reliable process routinely achieves a 1µm pitch with potential densities approaching a million connections per mm^2. The net result is up to a 1000x interconnect density increase, while still improving thermal performance and reducing cost of ownership (Figure 3) [6]. While hybrid bonding does not require through-silicon vias (TSVs), it can exploit them to support complex multilayer stacks. The inlaid copper pads on the frontside of one die can contact TSVs directly on the backside of another, simplifying the manufacturing process and providing unmatched versatility.

Xperi's Direct Bond Interconnect DBI® wafer-to-wafer hybrid bonding technology is well established in image sensor applications. It has demonstrated 2.2µm bond pitch in high-volume manufacturing, and can achieve a 1µm pitch or lower. The hybrid bonding motto is, "If you can print it and align it, we can bond it."

The next-generation DBI® Ultra process brings die-to-wafer hybrid bonding to high-performance memory and integrated multi-function packages. The efficacy of hybrid bonding has been demonstrated in various test vehicles.

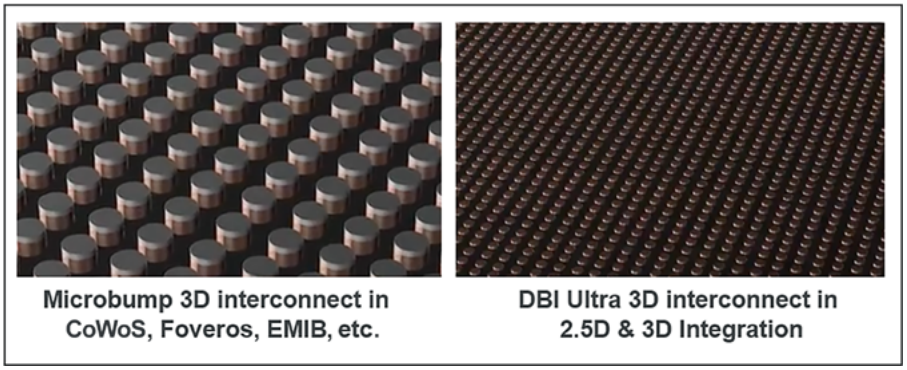

Figure 3: Hybrid bonding supports up to 1000x the interconnect density of microbump schemes.

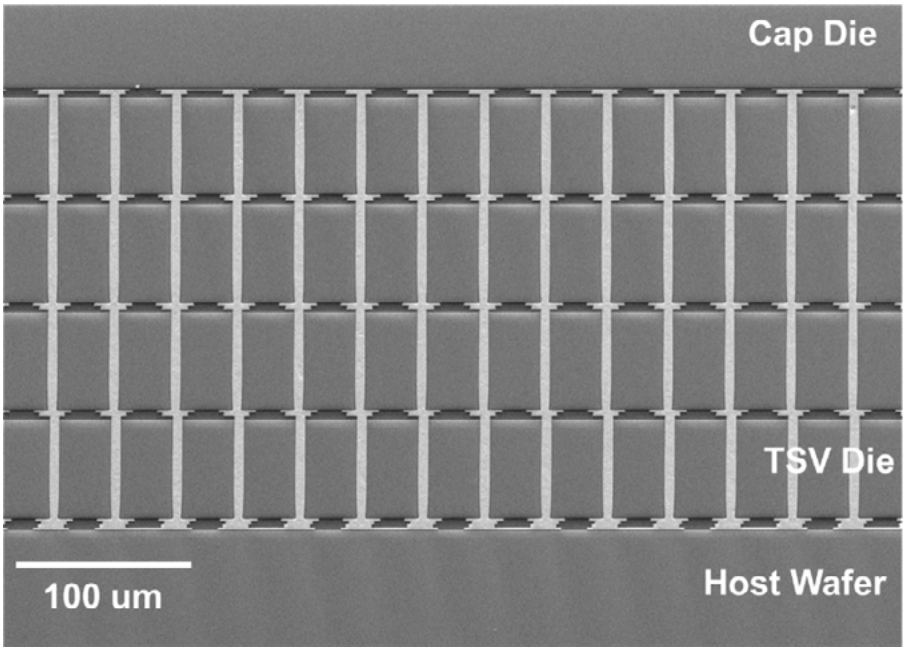

Figure 4: 5-die stack test vehicle with DBI to TSV interconnects.

Single-die face-to-face configurations typical of memory-logic applications have been demonstrated down to a pitch of 4µm in die-to-wafer form [7]. Five-die stacks, fabricated and bonded in a face-to-back configuration with the hybrid bond pad connecting to TSVs similar to HBM applications at about 38µm pitch, showed enhanced reliability performance (**Figure 4**) [8].

Xperi entered into a patent and technology licensing agreement with SK Hynix for 3D high-performance memory applications last year. DBI® Ultra supports stacks of 4, 8, 12, or 16 die and provides enhanced thermal and high-speed performance memory because of the inorganic interface between each die. The total stack thickness is only the sum of the die thicknesses, providing a path to deliver 16-die HBM stacks within the height limitation of 720µm. Although HBM memory chips in products today are approximately 50µm thick, the industry has demonstrated feasibility down to 30µm.

Disaggregating large designs

Other applications benefit from hybrid bonding's ability to integrate die from different technology nodes using diverse wafer sizes and substrate materials. Single-package subsystems can combine glass, sapphire, quartz, or III/V-semiconductor substrates with each other or with silicon, at the wafer-to-wafer, die-to-wafer, or die-to-die level, depending on existing supply chains and the circuit architecture. This flexibility offers many advantages for diverse heterogeneous applications.

Disaggregation allows the designer to combine legacy designs with mature yield with functionality requiring the latest transistor node. The overall product portfolio benefits from chip-set cost reduction and improved time to market. These options allow designers to contemplate new architectural solutions in three-dimensional packaging. For example, large system-on-chip designs approach the 800mm^2 die area limit of the industry's standard reticles. Such large chips are difficult to manufacture efficiently. With a relatively small number of die per wafer, the cost of each is high. Yield tends to decrease as die size increases, i.e., the same number of defects affects a larger fraction of the wafer's total die.

AMD, an early adopter of chiplet architecture with Ryzen, has consistently raised the bar for enhancing performance while driving down the costs of the semiconductor chip set design. Specifically, AMD showed that the disaggregation architecture enables a cost reduction of a factor of 2 compared to a monolithic design with 16 to 48 central processing unit (CPU) cores [9]. Furthermore, the chiplet architecture provides a pathway to a 64 graphics processing unit (GPU) core design, while a monolithic solution does not exist. These trends reinforce the importance of disaggregation in the CPU roadmap. As Intel (Foveros based next-generation CPUs and field-programmable gate arrays [FPGAs]) and Nvidia (next-generation Ampere GPUs and Grace CPUs) move toward chiplet architectures, others will follow.

Hybrid bonding is the packaging technology that provides a pathway to disaggregate such large logic devices into chiplets stacked directly on top of the core processor, with no interposer. High-density interconnects eliminate bottlenecks that might otherwise occur between chips. Instead, designers can treat interfaces between die as comparable to interfaces within die, allowing die to share interconnect layers and a single power supply mesh. With careful attention to vertical placement, such designs cannot just match the monolithic die performance, but improve it by reducing critical path lengths. At the same time, each component chip can use the most cost-effective process for its particular function. There's no need for wafers to carry large area analog features through a high-density logic

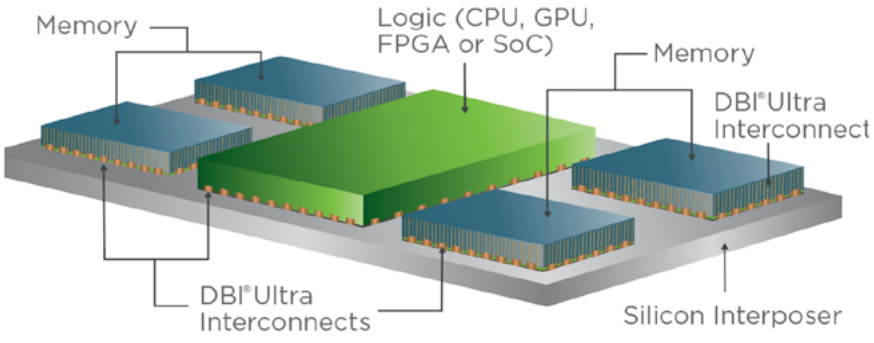

Figure 5: 2.5D structures: logic and memory integration.

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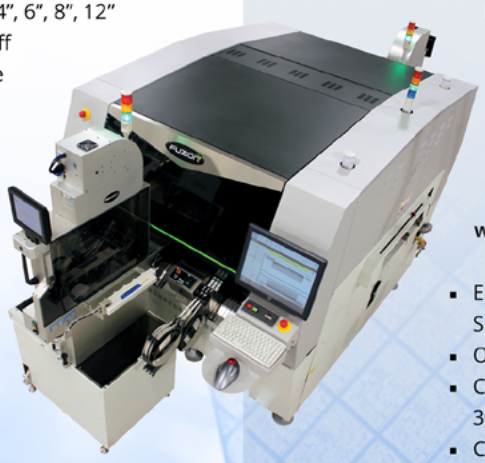

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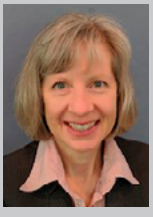
process. Finally, the reduced area of the individual component die improves overall yield.

In simulation results, disaggregation reduced total power by 21% with a logic power improvement of 33.9% all while shortening the wire length by 57%. Additionally, the simulation showed an area reduction of 11%. While a 2D design had better overall thermal performance compared to 3D, the hybrid bonding architecture showed a 33% improved thermal performance over a thermocompression bonding (TCB) interconnect [10]. These studies echo the promise of rearchitecting the 3D package with hybrid bonding for performance and cost improvements (**Figure 5**).

Summary

Xperi invented and pioneered direct and hybrid bonding technologies: DBI® for W2W, and DBI® Ultra for D2W or D2D hybrid bonding technology solutions. Our engineers work closely with customers to unleash the potential of this technology. Under a technology transfer and intellectual property (IP) licensing business model, the technical team builds customer demonstrations and transfers the technology know how to customers' R&D teams. Customers then ramp the technology within their own manufacturing supply chain. Leading semiconductor companies have licensed and are actively integrating the technology with Xperi support at their facilities to enable new in-house capabilities. The hybrid bonding toolkit provides a multi-generational roadmap for products in high-performance computing devices such as CPU, GPU, FPGA, SoC, other logic, memories and chiplet integrations.



Biographies

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3D polylithic integration and thermal implications on BEOL RRAM performance

By Ankit Kaul, Muhannad S. Bakir, Xiaochen Peng, Sreejith Kochupurackal Rajan, Shimeng Yu
[Georgia Institute of Technology]

Conventional feature scaling has been a key enabler in holding the exponential performance trend and democratizing high-performance systems. However, as we approach limitations of traditional scaling and with increasing fabrication costs of advanced nodes, a modular design approach enabled by advanced packaging and 2.5D and 3D heterogeneous integration technologies is being adopted in mainstream products to offset these limitations. Higher logic-memory bandwidth and lower chip-to-chip signal interconnection delay requirements have also led to a technological push towards 3D heterogeneous integration such as through-silicon via (TSV)-based 3D integrated circuits (ICs) [1-3].

3D integration can be broadly classified into the following types: 1) TSV-based 3D integration where solder-capped copper pillars (or μ-bumps) or hybrid bonds and TSVs are utilized to establish vertical interconnections, and 2) Monolithic 3D integration where two or more active device layers and interconnects are sequentially processed using standard lithography tools. While TSV-based 3D die stacking facilitates integration of prefabricated dice of varying technology nodes, it provides limited interconnect density, higher energy per bit (EPB), and higher inter-chip link latency relative to monolithic 3D (Table 1). On the other hand, although monolithic 3D ICs are limited in providing heterogeneity of devices at different technology nodes, they can have higher 3D connectivity (using nanoscale inter-layer vias) leading to better link latency and energy efficiency. Owing to this performance gap, there is a significant interest in monolithic 3D fabrication. Limitations in devices, materials, and temperatures, however, make monolithic 3D integration challenging and limiting.

To bridge the gap in connectivity and heterogeneity, a back-end-of-line (BEOL)-embedded integration scheme is proposed [4] where thinned dice are envisioned to be integrated close to the backend using fine-pitch interconnects. Such an approach can help avoid long wire lengths and large pad sizes and thereby lead to improved EPB and lower chip-to-chip delay. Such a technology can combine the benefits of current heterogeneous ICs (e.g., technology node flexibility, lower costs, higher yield, etc.) with the performance superiority of monolithic 3D ICs.

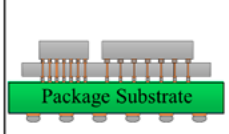
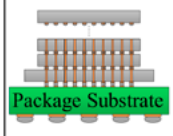
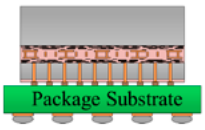
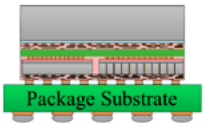
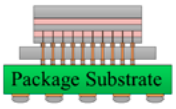
Attribute	Si-Bridge, Si-Interposer	TSV and μ-bump-based 3D	Hybrid bonding-based 3D	Polylithic 3D	Monolithic 3D
Reference(s)	[14], [15]	[14]	[1], [16]	[4]	[8], [17]
Schematic					
Interconnection method	μ-bump, flip-chip (TSVs for Si-interposer)	TSVs and μ-bump	Hybrid bonding D2W, W2W and TSVs	BEOL integration and TSVs	Inter Layer Vias (ILVs) within BEOL
Targeted I/O pitch (μm)	30 – 45	20 – 50	0.9 – 10	Goal: 0.5 – 5	< 1 (with 0.1 μm ILVs possible)
Thermal considerations	• Moderate TC and PD compared to 3D ICs	• Higher TC and PD vs 2.5D ICs	• Higher TC and PD vs 2.5D • Elimination of underfill layer • Higher I/O density vs μ-bumps		• High ILV routing density • Higher inter-tier TC vs other D2D, D2W, W2W 3D due to closer proximity of active tiers
Electrical Attributes	• Limited interconnect density, high EPB and latency vs 3D ICs	• Better EPB, chip-to-chip signal delay vs 2.5D	• Lower EPB, higher BWD, thinner profile vs 2.5D, μ-bump 3D	• Lower EPB, higher BWD, thinner profile vs 2.5D, μ-bump 3D	• Lowest EPB, link latency • Heterogeneous device/material/temperature limited

Table 1: Interconnection and thermal considerations in 3D heterogeneous integration. Notes: TSV=through-silicon via; μ-bump=micro bump; D2W=die to wafer; W2W=wafer to wafer, BEOL=back end of line; TC=thermal coupling; PD=power density (W/cm^2); EPB= energy per bit (pJ/bit); BWD=bandwidth density (GB/sec/mm^2).

With increasing integration complexity and power densities in 3D integrated ICs, heat dissipation, thermo-mechanical reliability, and inter-die bonding yield are becoming challenging. Thermal effects such as inter-die thermal coupling and increased number of hotspots pose a significant challenge in terms of performance and reliability implications. This is because 3D ICs can experience a significant variation in power densities compared to 2D SoCs and thermal performance may not scale linearly. A typical use case for heterogeneous 3D integration is dense memory-logic integration, which is required in state-of-the-art compute in-memory (CIM) hardware accelerators.

While embedded nonvolatile memory (eNVM), such as resistive RAM (RRAM), is a good alternative to static random-access memory (SRAM)/ dynamic random-access memory (DRAM) as a compute in memory (CIM) synaptic device owing to high bit density and low leakage, thermal-induced conductance drift remains a challenge. Lower retention at higher temperatures can be more significant in dense memory-logic 3D integration because of increased volumetric power, which has not been studied in prior work. To this end, the thermal constraints of the proposed polylithic integration architecture, termed 3D seamless off-chip connectivity (3D SoC+), are investigated with aggressive cooling to evaluate thermal limits from transient- and steady-state perspectives. To provide context to these studies in terms of an end application, we quantify the impact of the proposed architecture on bipolar RRAM reliability by estimating thermal-driven long-term image recognition accuracy change for a CIM hardware model. This article is based on our previous work in [4] and [5].

3D integration: background

This section discusses various 3D integration architectures, their associated challenges, and the need for polylithic 3D integration.

Integration architectures and challenges. Several recent 3D integration demonstrations have been explored to enable opportunities in high-performance computing [1-3], imaging [6,7], and gas sensing [8]. In these demonstrations, 3D integration of multiple active device layers is realized primarily through TSV-based 3D stacking [1-3,6] or fabrication of multiple active layers within the same IC (monolithic 3D integration) [7,8].

Compared to single-die system-on-chips, high-density TSV-based 3D aggregation of known good dice (KGD) from different process technologies can enable smaller wire lengths, improved performance, or lower power through efficient partitioning and physical implementation of a 2D design. Additionally, partitioning large 2D system-on-chips into smaller dice and identifying KGD before assembly can improve yield for 3D integration, thereby reducing cost.

Monolithic 3D integration is enabled through fabrication of high-density fine-pitch interlayer vias (ILVs), low-temperature active-layer fabrication processes, and emerging nanotechnology techniques [8]. ILVs can enable higher interlayer connectivity compared to both conventional 2D and TSV-based 3D and can provide higher interconnect density than TSV-based 3D [9,10]. This implies lower EPB and link latency between devices in different active layers in a monolithic 3D IC compared to TSV-based 3D ICs. Based on these studies, there exists a performance gap between TSV-based 3D and monolithic 3D ICs in terms of energy, bandwidth, and interconnect density.

Polylithic 3D integration. A 3D polylithic integration architecture is proposed in [4]. As shown in Figure 1, this scheme represents a densely integrated system divided into multiple device tiers where custom chiplets, such as voltage regulator modules, I/O drivers, and RF frontends and other devices/materials that are not easily fabricated monolithically with complementary metal oxide semiconductors (CMOS), are embedded

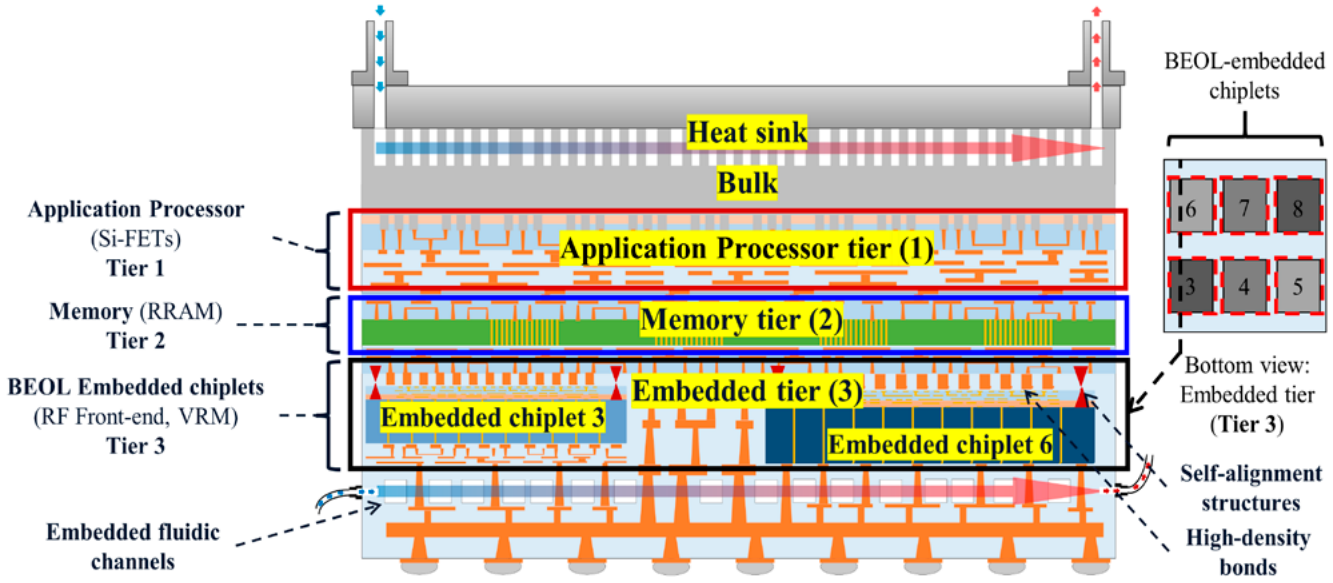


Figure 1: 3D polylithic integration: BEOL-embedded chiplet integration [5].

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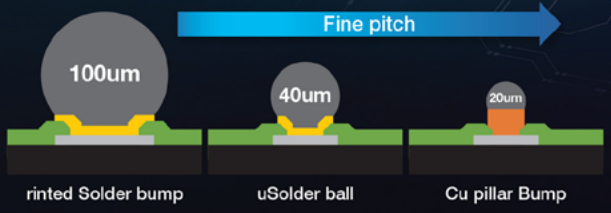

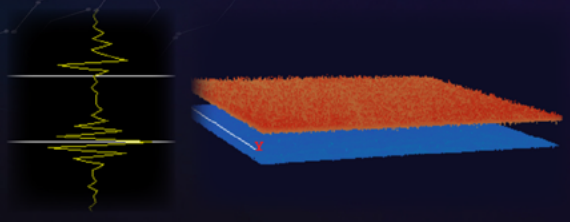

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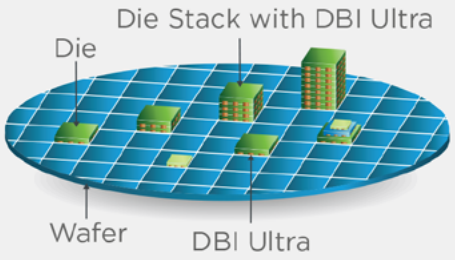

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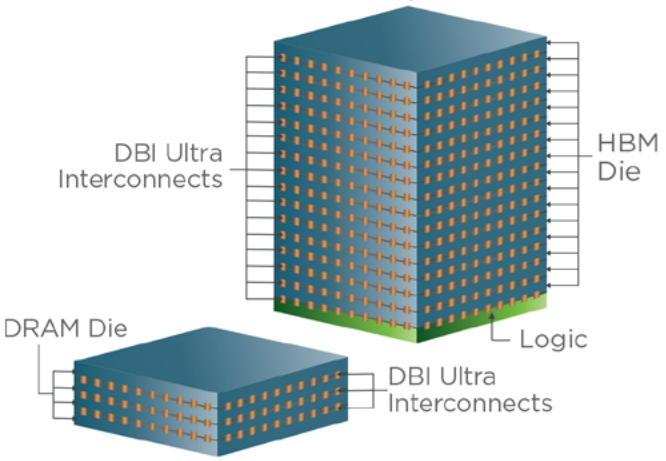

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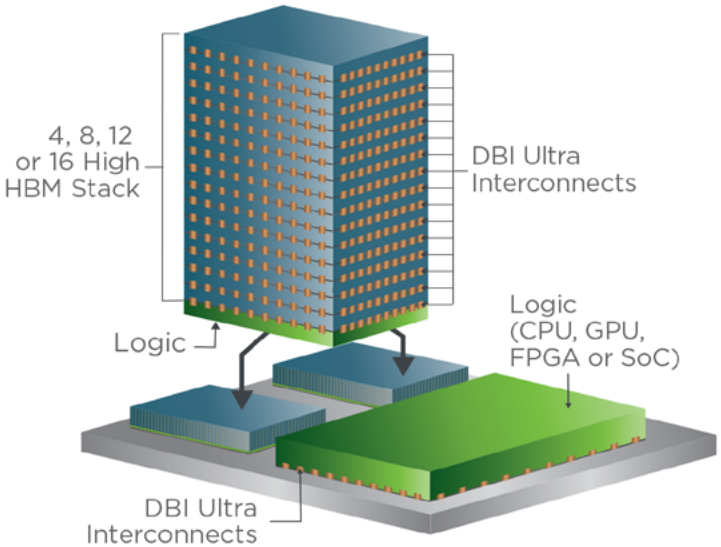

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into the backend of an application processor (AP) tier with a monolithic memory tier, e.g., RRAM. The proposed architecture aims to combine the best of both monolithic and TSV-based 3D ICs, including extreme efficient signaling and large bandwidth density (BWD).

Thermal exploration of 3D polylithic integration

The majority of the heat generated in high-power 2D packages is generally removed through the bulk substrate and faces thermal resistances associated with conduction through the bulk, thermal interface material, and the heat spreader. However, heat is generated within multiple active layers along the stack in high-power 3D packages. Therefore, in a 2-die stack the heat extraction path includes additional thermal resistances from the bulk (lower die), the bonding/underfill layers (between dice), and the BEOL (upper die). Therefore, in this section, we investigate the impact of various design parameters on thermal performance of the proposed scheme.

Figure 1 illustrates the proposed architecture [4], which is envisioned to enable seamless connectivity to BEOL-embedded heterogeneous chiplets. We modeled the proposed structure using a finite volume-based thermal modeling framework described in [11], and the modeling specifications and assumptions are listed in [5]. The simulations were performed for high and moderate power density use cases and with conventional air-cooling and dual-sided liquid cooling (DSC). We compared the maximum junction temperature ($T_{j,max}$) for a steady state simulation to validate our thermal model against ANSYS Mechanical APDL solver (ver. 19.2). The worst-case relative error in maximum and minimum junction temperatures between our model and ANSYS was less than 12.5% [5].

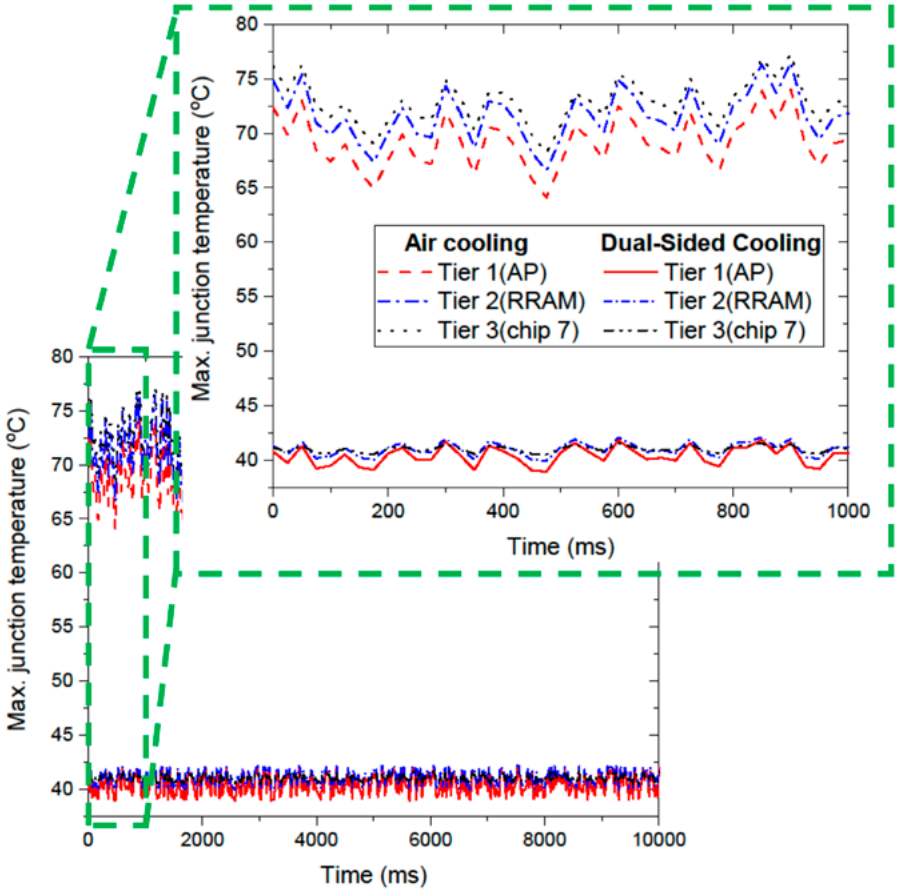

Figure 2: Transient thermal variation for logic (application processor), memory, and embedded tier with air- and dual-sided cooling (DSC) [5].

Transient thermal analysis was performed to quantify the effect of change in power of the logic tier (hypothetical application processor [AP]) on other tiers (Figure 2). The AP tier power map emulates a processor workload, and the AP, memory, and embedded tier power density assumptions are presented in [5]. One way to define transient thermal coupling is the ratio of change in temperatures of the affected tier due to change in temperature of the tier with the transient source [4].

The first key observation was that without inter-tier thermal coupling, the $T_{j,max}$ of the monolithic memory and embedded tiers should be constant, and the coupling defined by equation (1) in [4] will be 0. However, a strong inter-tier coupling was observed (Figure 2). Thermal coupling ratios from AP to an embedded chip were estimated as 0.85 for

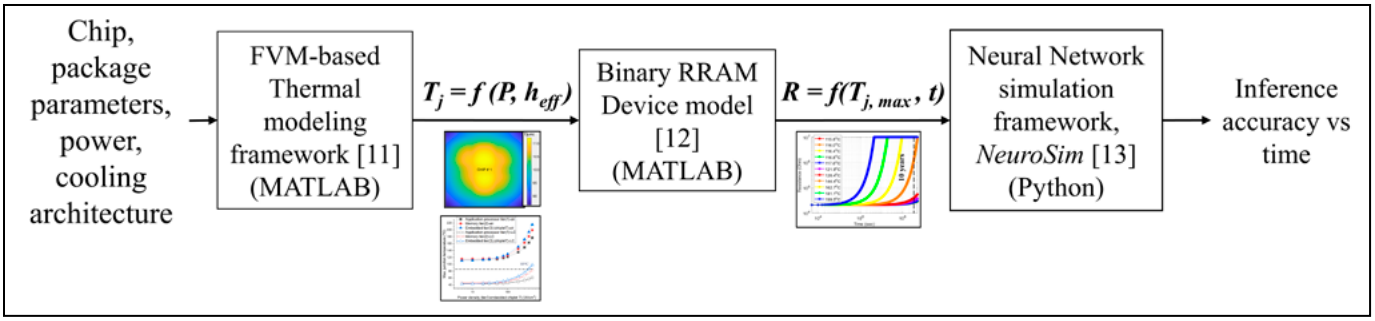

Figure 3: Modeling study flow to evaluate the impact of cooling architectures on binary RRAM devices in a 3D IC form factor by quantifying temporal image recognition accuracy of neural network hardware based on RRAMs. (Notes: $T_{j,max}$=Memory tier maximum junction temperature (°C); P=Total package power (W); h_{eff}:=Effective heat transfer coefficient of heat sink (W/m^2-°C); R=RRAM device resistance (Ω), t=time (sec).

air-cooling and 0.63 for DSC, implying a 20% reduction using an advanced cooling method. Second, the proximity of a heat sink to a tier affects both the tier's thermal coupling from neighboring active tiers and the tier's absolute junction temperature.

RRAM thermal reliability in 3D integration

Heterogeneous 3D integration is a promising approach to stack the large amount of embedded memory required in state-of-the-art CIM AI accelerators.

While benefits such as high-density, low-leakage, and nondestructive read make RRAM a good alternative to SRAM/DRAM as CIM synaptic devices, challenges are posed because of their thermal-induced conductance variations. Dense memory-logic 3D integration can make eNVM devices susceptible to reduced retention at elevated temperatures because of increased volumetric power. This work presents a thermal study to quantify the impact of the proposed integration architecture on bipolar RRAM reliability by estimating change in image recognition accuracy over time for a deep neural network hardware model. An evaluation flow is proposed (Figure 3) that combines thermal analysis, a measurement-calibrated device retention model, and a CIM inference accuracy estimation framework. Using this flow, RRAM reliability is studied as a function of logic tier power density with different cooling architectures to identify thermal limits and challenges in multi-tier 3D integration.

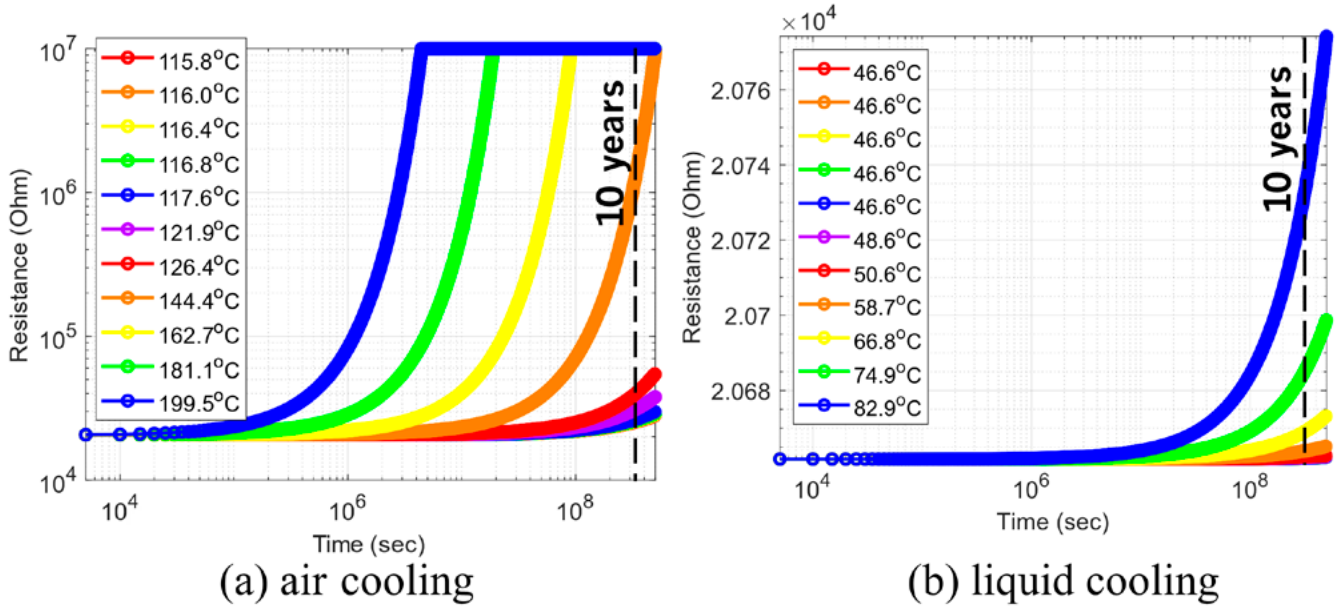

Figure 4: Estimated temporal resistance retention behavior of bipolar RRAM in a polylithic 3D system with: a) air cooling, and b) liquid cooling (LC) [5].

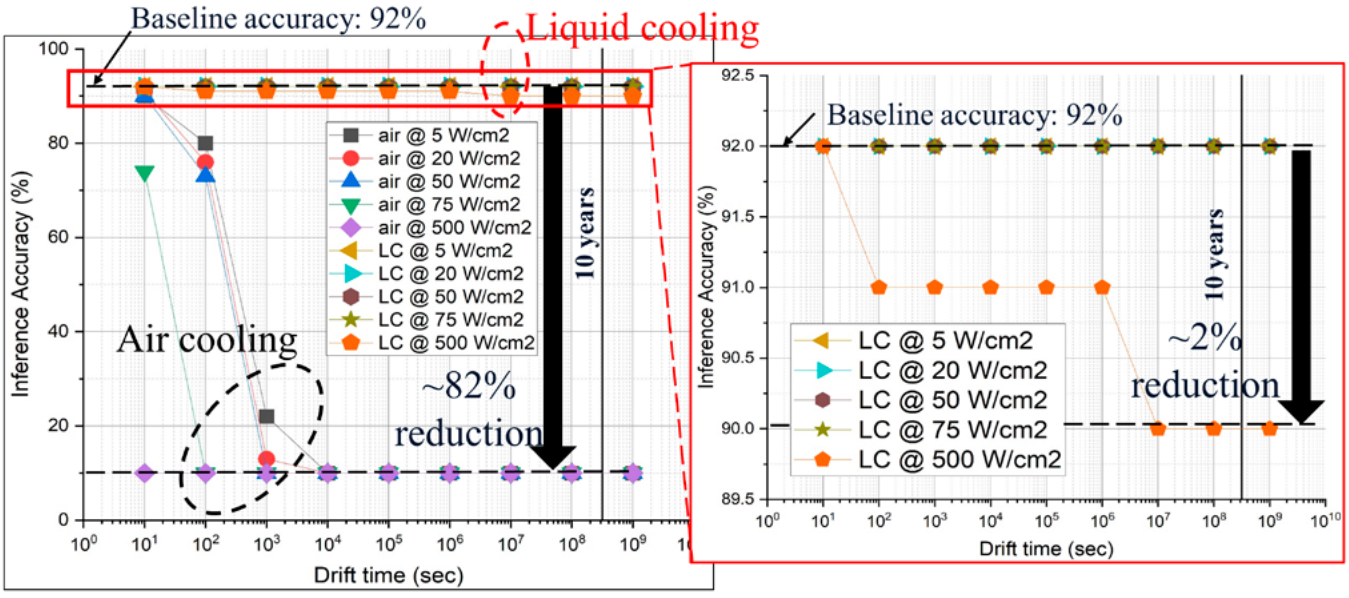

Figure 5: Inference accuracy vs. time of CIM inference engine with binary RRAM device tier in a polylithic 3D system [5].

In the following case study, the power densities of all tiers were fixed except for chiplet 7 in the embedded tier, for which the power density was varied from 5–500W/cm^2 [5]. The figures of merit were evaluated with air and single-sided liquid cooling (LC). The memory device tier's resistance retention behavior over time for a binary RRAM device as a function of embedded chiplet power density is shown in Figure 4 for two types of cooling techniques. The device has lower retention robustness at higher embedded tier power densities, and this can be mitigated with better cooling techniques such as LC. The resistance values were estimated at 10 years (predicted by an HfO_2 RRAM device model [12]), to find the resistance drift ratio with respect to the original resistance. Subsequently, the drift coefficient is adjusted in a retention model to estimate the inference accuracy using NeuroSim (a popular framework to benchmark CIM accelerators [13]). The drift ratio was observed to increase with higher temperature irrespective of the cooling method. However, with air cooling, the increase was more significant compared to LC because the temperature-induced resistance degradation was higher using air cooling than with LC. This finding is expected to impact inference accuracy.

Data retention is one of the key factors for inference accuracy degradation in CIM inference engines. Therefore, the impact of embedded tier chiplet power density was evaluated on inference accuracy of a CIM inference engine for two types of cooling configurations on an accelerator design based on a VGG-8 network for a CIFAR-10 dataset using NeuroSim. The worst-case accuracy drop at 10 years was estimated as 82% for air cooling compared to 2% for LC (Figure 5) because the resistance change over 10 years with LC is minimal.

Summary

A back-end-embedded chiplet integration architecture is proposed that is envisioned to combine the low EPB and high BWD benefits of monolithic 3D ICs with the integration flexibility of TSV-based 3D integration. It was observed from transient thermal analyses that the heat sink proximity to an active tier affects the thermal coupling, with up to 20% reduction observed with advanced microfluidic cooling. The impact of 3D integration and cooling architectures on RRAM reliability has been quantified by estimating image recognition accuracy over time for a deep neural network hardware model. Both studies suggest a need for additional conductive and convective solutions for reliable thermal operation of RRAM-based CIM hardware for 3D integration use cases involving high power densities.

Acknowledgement

This work was supported in part by ASCENT, one of six centers in JUMP, a Semiconductor Research Corporation (SRC) program sponsored by DARPA.

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Biographies

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MSL-1 reliability performance in QFN packages using no-bleed die attach

By Senthil Kanagavel, Dan Hart [MacDermid Alpha Electronic Solutions]

With the advent of autonomous technologies, the semiconductor industry requires a new paradigm of reliability. Certainly, the biggest driver is the goal of autonomous driving, where reliability cannot be sacrificed. To this end, many suppliers are combining businesses to synergize novel approaches to deliver the highest reliability.

Perhaps the principal failure mechanism in chip packages is delamination. The primary causes for delamination arise from issues with thermal expansion and moisture intrusion. Initially, it was believed that controlling thermal expansion coefficients of packaging components was all that was needed. Indeed, for small packages this appears to be true, but as packages become larger and more complicated, it becomes very difficult to control the coefficient of thermal expansion (CTE) of every component.

Attempts to improve reliability by increasing mold compound adhesion have led to maximizing the surface area of the interface between the mold compound and the lead frame. Unfortunately, this led to the unintended consequence of increased resin bleed from die-attach adhesives, which in turn led to failure of the adhesives and delamination under the die. With a plethora of adhesives from multiple suppliers, it becomes difficult to find a "one size fits all" correction for the resin bleed.

By successfully implementing conductive film type die attach, the resin bleed out (RBO) issue becomes nonexistent, eliminating the need for a lead frame surface treatment that can eliminate RBO from all adhesives. More complex packages with multiple dies and high I/O counts are becoming commonplace. Many of these systems in a package (SiP) utilize hybrids of solder die attach and traditional die attach or multiple curing cycles to stack dies. This article reviews some of the critical factors that lead to delamination within a chip-scale package, and methods that alleviate these causes.

Package reliability requirements

As the complexity of various technologies advance, semiconductor package reliability requirements are continually increasing. What once required three or more chip packages, now must be achieved by one so as to pack more I/Os into smaller and smaller volumes. The capabilities of a desktop computer from the 20th century are now housed in a mobile phone that can fit in your pocket. This was made possible by producing chip packages that contain multiple chips, thereby generating more functionality in a single component – a system in a package (SiP). These SiP packages come in a variety of designs: stacked die, side-by-side, or multi-chip fan out, with variations of the same. Each of these designs exhibits its own set of manufacturing issues that can impact reliability. While organizations such as JEDEC, IPC, and AEC define classifications and tests that these parts must pass to qualify for their acceptance, many manufacturers test at even more stringent conditions to ensure the dependability of their production.

In addition to the above consideration, more complex wafers are designed with increased capabilities that require higher lead counts with tighter spacing. In these cases, the chip to die-attach pad area ratio becomes critical. As the area ratio decreases, the chance for delamination at the lead frame-mold compound interface increases. Delamination tests and electrical testing are critical measures of reliability. To achieve higher reliability levels, units are stressed in higher temperature, higher humidity, or extreme thermal cycling tests to verify that production meets pre-determined standards. This article will discuss some of the important issues impacting reliability and solutions that have been developed to overcome them.

Adhesion/delamination

One of the most common problems faced by packaging houses is delamination. Delamination can occur between epoxy mold compound and the lead frame, between the die and lead frame, or between the die and mold compound. To enhance adhesion at the lead frame interface, various roughening techniques have been employed. The two most popular are quite different. One is a subtractive process – etching, and the other is an additive process – electroplating.

The additive process typically uses controlled electroplating conditions to generate a roughened deposit of copper. Because it has been reported that copper and copper oxides can cause decomposition of epoxy resins at elevated temperatures, the reliability of this surface has been questioned unless coated with another material to reduce the impact of copper on the mold compound.

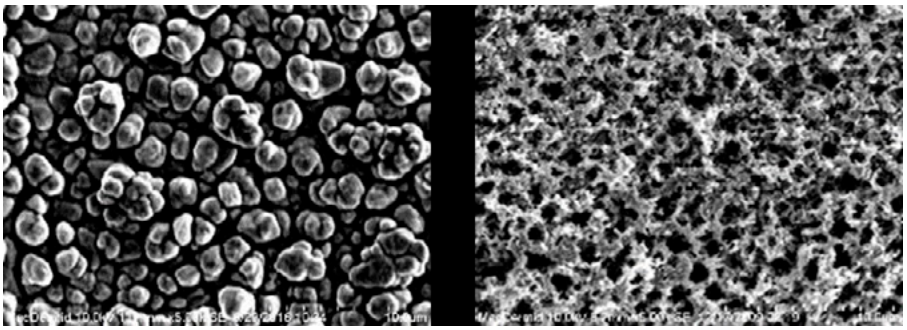

Figure 1: SEM photo of an additive process (left) and a subtractive process (right).

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Frequency : 80GHz(BGA),
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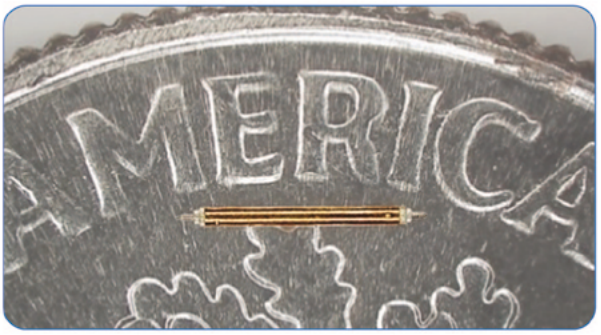
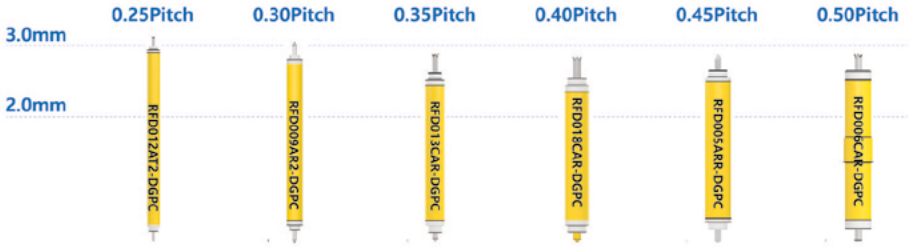
Pitch : 0.25mm ~
Crosstalk : -60dB
Impedance : 50Ω±10%





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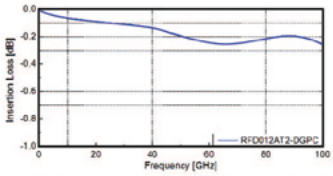
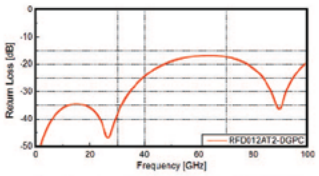
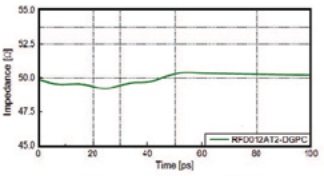


Insertion Loss(-1dB): Up to 100GHz

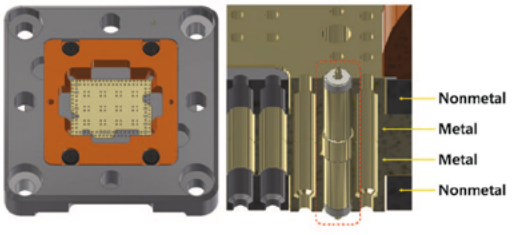


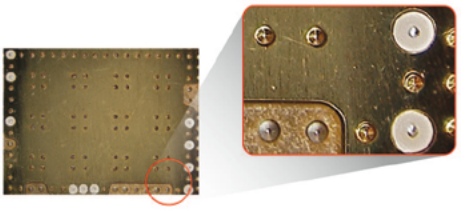
Return Loss(-10dB): Up to 100GHz



Impedance:49.2Ω

Coaxial Probe Socket Structure





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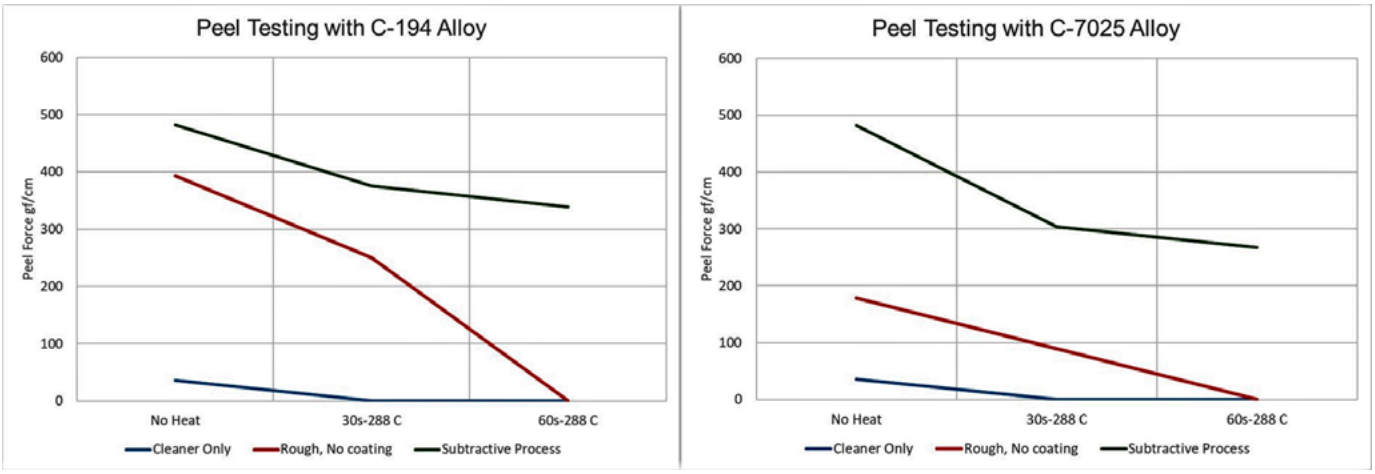

Figure 2: Graphs showing the peel strength of treated and untreated alloy surfaces.

Figure 3: Alloy surface after MSL-1, reflow, and button shear—untreated on the left, treated on the right.

The subtractive process utilizes a special micro-etching composition that concurrently etches a rough morphology and deposits an adhesion-promoting coating. The advantage of this process is that it can be run in the packaging house after die attach. For some SiP configurations, this can be beneficial, whereas plating a conductive copper coating over the entire area will, after die attach, lead to shorts within the package. The subtractive process will not catalyze epoxy decomposition at higher temperatures because the coating that is deposited isolates the copper surface from the molding compound. The differing morphologies of these two processes are shown in **Figure 1**.

Adhesion tests on roughened surfaces with and without the adhesion-promoting coating, compared to no treatment at all, demonstrated the utility of the coating with respect to adhesion after high-temperature treatment. The peeling force to remove a one-centimeter wide strip of lead frame alloy from a cured epoxy surface is illustrated in **Figure 2**. The results demonstrate that the coating is critical for maintaining adhesion at the extreme temperatures tested. No treatment provides very little adhesion improvement compared to the roughened surfaces, but adhesion falls away quickly with temperature exposure unless the adhesion-promoting coating is included.

Button shear testing with epoxy mold compounds (G-600 and G-770 from Sumitomo-Bakelite) after moisture sensitivity level 1 (MSL-1) preconditioning followed by triple reflow at lead-free reflow temperatures demonstrated a similar improvement in adhesion, but also provided some evidence of the mechanism that generates improved resistance to moisture sensitivity. Observation of the alloy surface after the button has been removed (see **Figure 3**) shows a vivid difference. While the untreated surface shows an oxidized appearance, presumably from moisture ingress at the mold compound-lead frame interface, the treated surface remains clean and unchanged. This indicates that the process prevents moisture ingress, which would have led to delamination (popcorning) during reflow.

As discussed in [1,2], a rough surface leads to increased RBO. The most common solution for RBO coats the treated lead frame with a surface modifier to reduce surface energy, thereby inhibiting the flow of the resin. Because not all die-attach adhesives are the same, especially regarding surface wetting, anti-RBO processes must be carefully controlled for each adhesive used. The development of conductive-film die-attach materials that are applied to the wafer, and transfer with the chip to the lead frame, provides a more attractive approach to avoiding RBO.

Conductive film die attach

A conductive film die-attach process starts with the wafer lamination followed by dicing and die bonding. The die bonding is carried out on similar equipment as a standard epoxy die-attach process with slightly different settings to enable the wetting of the film to the roughened surface of

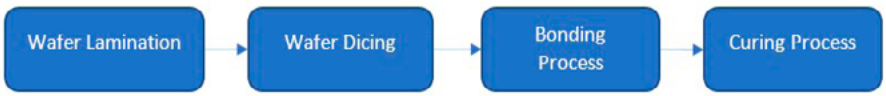

Figure 4: Process flow for conductive film die attach.

the lead frame. The schematic process flow is described in Figure 4.

ATROX® CF200-1D film is evaluated on roughened copper lead frames to determine the delamination resistance of the conductive film die attach after preconditioning. The assembled unit shows minimal to no fillet after bonding, which indicates no resin bleed out and a high rate of adhesion on the lead frame surface. To the contrary, the paste shows RBO on the lead frame surface. Figure 5 illustrates the difference between RBO with liquid die attach compared to the "no-bleed" conductive film die attach.

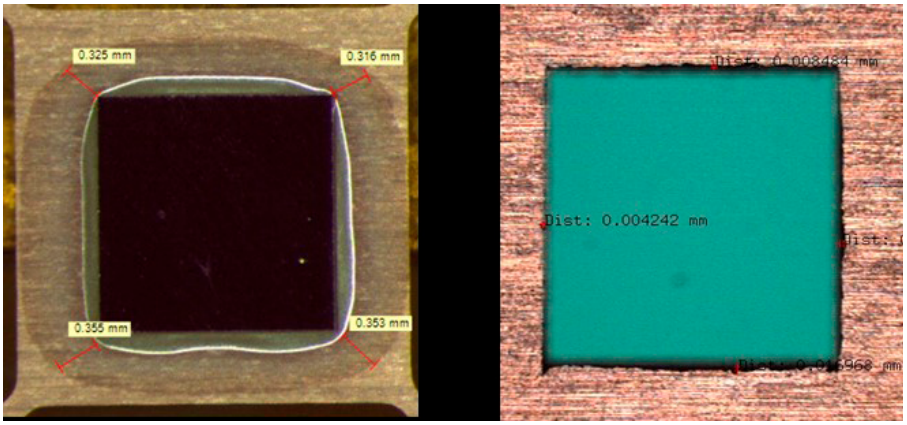

Figure 5: Conductive die attach paste showing RBO vs. conductive film die attach with no resin bleed.

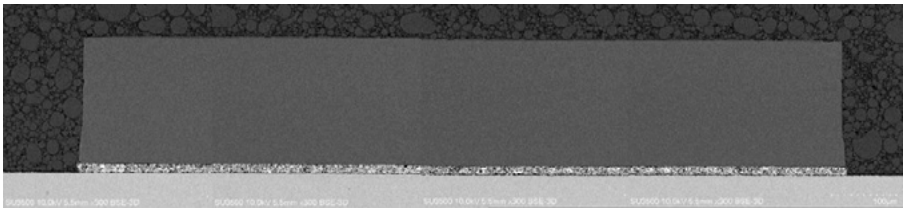

Figure 6: Assembled die on the lead frame using conductive film.

Process/Conditions	Lamination	Dicing	Bonding	Curing
Temp (°C)	75C-85C	<50C	90C-120C	>=175C
Pressure (N/mm2)	>0.3 N/mm2	None	>=1N/mm2	None
Time (min)	< 1 min	Die Size dependent	1 sec Max	120min

Table 1: Assembly settings for conductive film.

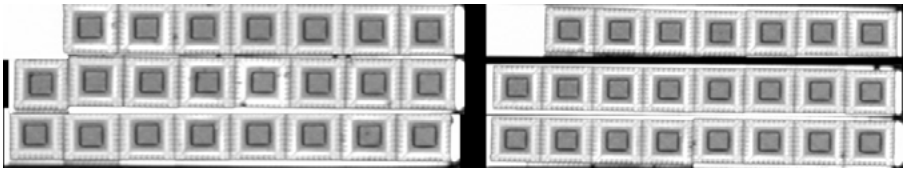

Figure 7: THRU-Scan™ images of conductive die attach film before MSL-1 (left) and after MSL-1 (right).

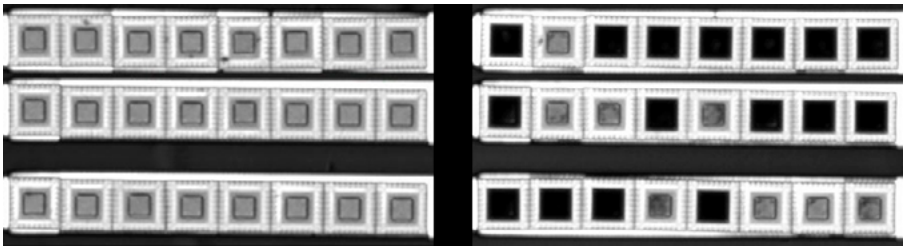

Figure 8: THRU-Scan™ images of die attach paste before MSL-1 (left) and after MSL-1 (right).

Figure 6 shows a cross section image of the film after die bonding and encapsulation. The assembly settings used for the conductive die attach film process are tabulated in Table 1. The conductive film attach parts show very high adhesion results with superior delamination resistance after preconditioning. Figure 7 shows THRU-Scan™ images of a quad flat no-leads (QFN) 5x5 device before and after being subjected to MSL-1 preconditioning followed by 3x reflows at a 260°C peak temperature. In comparison, Figure 8 shows the THRU-Scan™ images of the same parts assembled using a standard paste with RBO; the images show delaminations after MSL-1 indicating that the root cause of failures is attributed to the paste's poor delamination resistance caused by RBO.

For conductive adhesives, the ratio of conductive filler to resin material is critical for maintaining physical properties. The RBO can weaken the composition of the adhesive under the die when the loss of resin increases the filler to resin ratio beyond its optimum range. This can lead to weakening of the adhesive under the die, and ultimately, delamination. Micro-sections of the die attach show that the conductive film has flowed into the roughened surface of the lead frame during the curing process (Figure 9). The ability for both the die attach adhesive and the epoxy mold compound to flow into the surface topography is a critical contributor to delamination improvement.

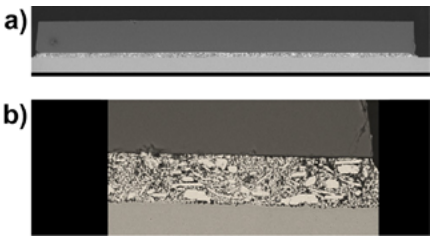

Figure 9: SEM photos of a micro-section of a conductive die attach film after MSL-1 showing: a) (top) a low magnification overview; and b) (bottom) higher magnification detail.

Summary

For many advanced microelectronics devices being used now or in the near future, failure can be catastrophic. Medical devices are now used to measure or control critical bodily functions. Automobiles equipped with autonomous driving capabilities are now asked to react to emergency situations, such as an impending collision. The assembly methods to produce the high reliability required need to be implemented now.

RBO is a constant concern but is extremely difficult to control because of the numerous die-attach adhesives that are commercially available from multiple sources. The resins used in these adhesives arise from various organic compounds. Additives are used to improve adhesion, wettability, filler stability, and RBO. The difficulty with controlling RBO with surface energy modifiers arises from the variety of resin chemistries.

The THRU-Scan™ images illustrate the weakness of poorly controlled RBO. Conductive film die attach is an elegant solution to the issue because it is applied as a solid that creates no RBO but flows into the morphology of the roughened surfaces during cure. The enhanced moisture resistance produced by the roughening mechanism delivers higher MSL reliability without the associated problem of resin bleed.

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Advanced rework technologies: Solder bump repair and rework

By Timo Kubsch [PacTech – Packaging Technologies GmbH]

Even before the current chip shortage, efficiency of the production process (i.e., the yield of devices ultimately created from the same amount of raw material) had grown to become a major factor of concern to anyone involved in the industry. The consumer's ever-growing demand for higher computing power in either the same or smaller form factors has meant that chips and packages have needed smaller and smaller structures. The drawback of smaller structures, however, is that the processes that produce them are prone to error and yield losses. Such errors and losses cost the manufacturer not only money, but also valuable production capacity and ultimately, limit the production output of a given fab. Additionally, concepts like the Internet of Things (IoT) enable chips and packages to be used for an ever-wider range of products and devices. This large field of potential applications increases the market drastically and will continue to do so in the foreseeable future.

A worldwide shortage of semiconductor chips, devices, as well as production capacity increase the demand for high production yields dramatically. Part of the solution is to identify faulty parts in every step of the production process and repair or rework them accordingly so that they may be fed back into production, rather than being discarded. Furthermore, there is a whole industry specializing in sourcing chips from already existing, but faulty, devices—reworking them to use them again in a different device. This eases the load on the production capacity as it fulfills some of the demand of the market with chips that have already been made.

The original manufacturer of such faulty devices, of course, never intended them to be faulty in the first place. To help reduce the amount of warranty claims and dissatisfied customers, it is necessary to understand the failures to avoid them. Here, again, rework capabilities allow for disassembling and inspection of packages, as well as selective repair and reassembling to try out potential fixes. In support of these efforts, PacTech – Packaging Technologies GmbH offers tailored repair and rework solutions for every soldering step in the assembly process. In this first part of a two-part article, we highlight repair and rework capabilities on the level of single solder bumps. In part two (to be published in the next issue), we will illuminate repair processes for chips and stacks of chips.

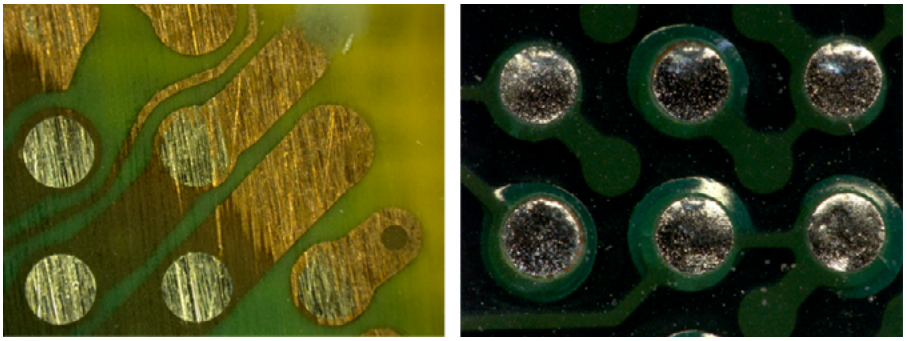

Figure 1: Comparison of samples with a) (left) mechanically removed solder, and b) (right) using PacTech's thermal approach [1].

Bump repair

Some of the conventional abrasive rework processes are either based on a mechanical abrasive procedure like milling, lapping and polishing, or on the use of thermal induction using a hot plate, solder iron, or hot air gun. These process steps pose significant challenges as they damage the under-bump metallization (UBM), as well as contaminating it with material from other parts of the chip or board in question. For example, in Figure 1a, the streaks of the milling device can clearly be made out. These streaks may lead to a significantly reduced bond quality for any solder bump to replace the removed solder. Furthermore, the process is not selective. It may remove the solder on a full ball grid array (BGA), thereby negatively impacting its quality even if only one contact was faulty. Nearby surface-mounted devices such as capacitors, resistors, or even chips or packages, may also be damaged or destroyed in the process. They, too, need to be replaced in order for the complete product to function again.

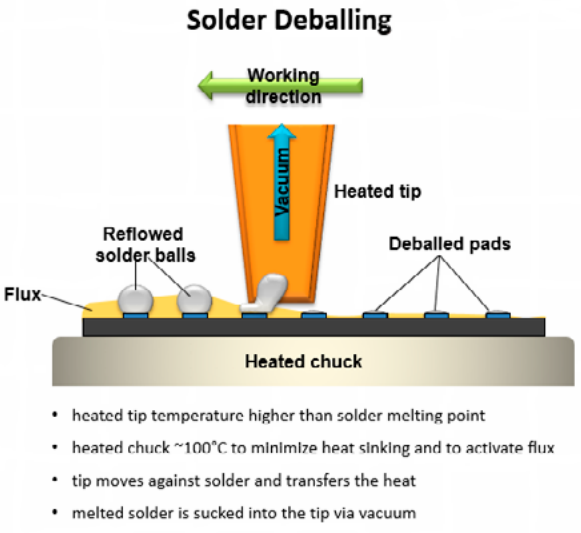

Figure 2: Schematic representation of the solder repair and removal process.

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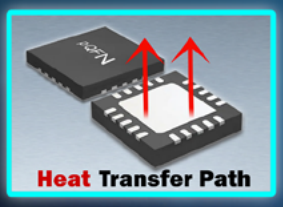

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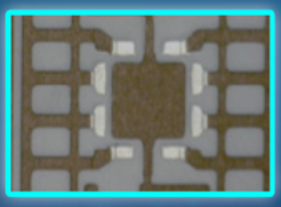

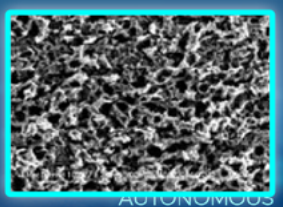

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To combat the above challenges, we perform solder rework by way of a local and selective heating process that uses a ceramic capillary. As a result, the UBM is not at all affected by the process. This process is agnostic to the kind of solder to be processed and is performed according to the following scheme. The capillary is heated to a temperature above the solder's melting point using either resistive heaters or the flow of hot nitrogen. Alternatively, the solder can be heated directly using a laser pulse. Then a vacuum is applied inside the capillary (see **Figure 2**). The solder bumps are usually covered in flux to aid the process and minimize the risk of oxidation.

Using a high-precision 3D axis system, the capillary is lowered to just above the surface and moved into the faulty bump. Depending on the needs of the application in question, the process can be adapted to perform either a vertical or a horizontal motion into the bump. The vertical motion allows for highly selective solder removal—potentially removing the solder on a single pad in a fully-populated BGA without reflowing, or otherwise impacting, adjacent bumps. The horizontal motion is rather tailored towards removing a whole row of neighboring faulty bumps in a minimum amount of time. As the solder liquefies, it is sucked off by the vacuum and deposited into a filter downstream.

A thin layer of solder remains on the pad. This layer contains the intermetallic compound (IMC) formed by it and the pad material and is typically in the range of 5µm. As its upper surface is made of pure solder, it shows excellent wetting properties with the solder that is to be placed on top of it. Furthermore, as the IMC contains a fair amount of the pad metallization, preserving it is important so as to keep the device repairable. Abrasive methods scrape the IMC away, which leaves only a smaller layer of metallization onto which the next solder bump can be placed. This already small layer then shrinks even more as some of it is sacrificed when forming a new IMC with the replacement solder. Should the layer grow too thin, it is entirely possible that it may lose its bond to the underlying substrate. All of these challenges are effectively solved by leaving the IMC untouched and only removing the solder above it.

Bump replacement

In a second step, our SB^2 solder jetting process selectively renews the removed solder bumps, thereby completing the rework process. For this step, spherical solder preforms are singulated within a bond head and dropped into a capillary. There, a quasi-constant wave near-infrared laser melts the solder and jets it out of the capillary using pressurized N_2 (**Figure 3**). The flow of N_2 then stays active until the solder has solidified on the target pad, thereby preventing oxidation. A variety of parameters can influence the bonding process to achieve the desired solder bump geometry. This geometry, within certain limits, can be tailored to the customer's demands and needs. The above process also works with a large variety of solders having melting points in different temperature regimes. Most prominent examples are SAC305 (Sn96.5%, Ag 3.0%, Cu 0.5%), Au80Sn20, Sn10Pb90, Sn63Pb37, and Sn42Bi58.

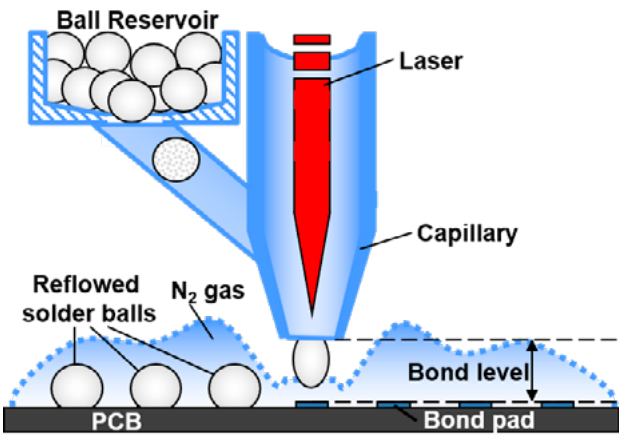

Figure 3: Schematic representation of PacTech's SB^2 jetting process.

The method of performing reflow described above using a millisecond laser pulse rather than placement and oven reflow of the spherical solder preforms has significant advantages for the properties of the resulting solder bump. In a typical oven reflow process, the time the sample stays at the reflow temperature is in the range of tens of seconds. For the laser reflow process, that same episode only takes a few milliseconds, thus reducing the thermal impact by about three to four orders of magnitude. Through extensive testing, it was shown that this has a profound impact on the quality and durability of the bond.

The bond described above is formed by the IMC. This is a layer of material that forms during bonding, as some of the material of the UBM diffuses into the molten solder and some of the solder diffuses into the UBM. Together, they form a new alloy, which effectively is the essence of the physical and electrical bond. While necessary, this IMC more often than not has unfavorable properties when compared to the original UBM and solder. Usually, the IMC is mechanically more brittle and electrically more resistive than either UBM or solder. The ultimate goal is to create an IMC that is large enough to form a stable and reliable bond, yet as thin as possible to minimize its negative impact.

The growth of the IMC is directly related to the thermal cross section the bond experiences not only during formation, but also across its life time [2]. Its electrical resistance in that time leads to a localized conversion of electrical to heat energy right at the IMC layer, thereby further increasing the thermal load. Eventually, the IMC grows so large, that its brittleness makes the bond vulnerable to vibrations that occur naturally during the device's lifetime. As that happens, the bond breaks leaving the device defunct. In separate studies, the formation and lifetime behavior of the IMC have been evaluated. The significant shorter thermal impact during formation leads, as expected, to an overall smaller IMC. In addition, this IMC has a finger-like structure, which is unlike the smooth and layer-like geometry of an IMC formed during an oven reflow process. This finger-like structure is of great importance: even more than the IMC, the interface between it and the solder pose resistance to the electrical current. This resistance decreases, however, when increasing the area of that interface because the current can distribute more widely and the current density decreases.

Further laser reflow steps – which would occur during replacement of the solder above the IMC or repair and

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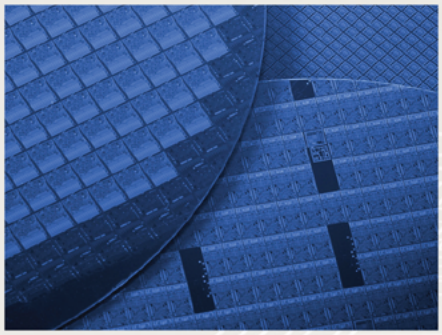

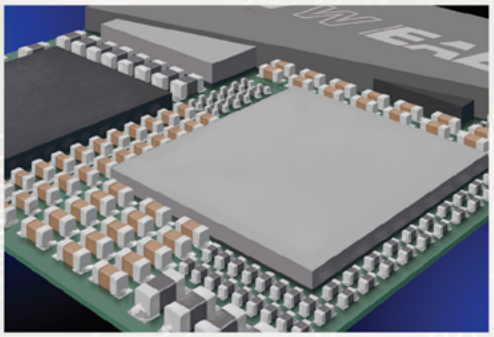

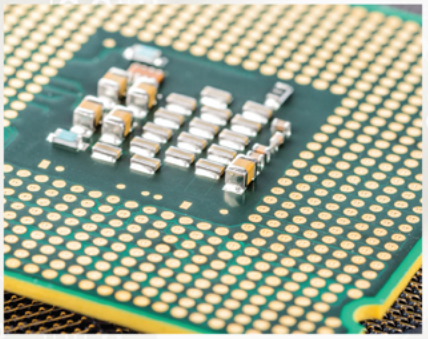

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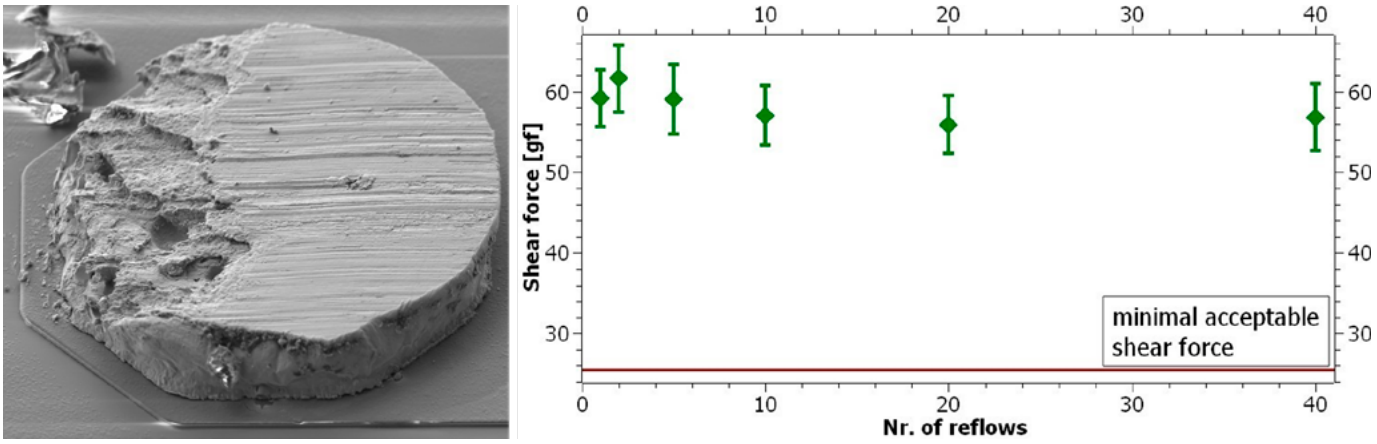

Figure 4: a) (left) SEM image of a sheared solder bump exhibiting the solder shear mode, and b) (right) graph showing the average shear force of sheared solder bumps after a given number of laser reflows.

replacement of a faulty flip chip on such a bump – have no meaningful negative impact on the quality of the bond. In laser reflow trials of solder bumps, the solder was reflowed up to 40 times [3]. The shear force – signifying the mechanical strength of the bond – stayed constant across all performed reflows, and by far exceeded the calculated lower limit for this size of bond (Figure 4b).

The measurement of said shear force was conducted in conformance to the JEDEC standard. The observed shear mode was the so-called solder shear mode (Figure 4a). This mode occurs when the shear tool plows through the solder itself without pulling it off of the pad or the pad from its foundation. This proves that the connection between solder, UBM and underlying material is stronger than the tensile strength of the solder. It can therefore be concluded, that even 40 laser reflows did not introduce any damage to the bonding interface.

The thermal lifetime of the bond described above was simulated using a thermal chamber. Bumps created using the laser reflow and a conventional reflow were exposed to 200 cycles, each lasting 35 minutes and taking the sample to -40°C on the low end, and 125°C on the high end. During this aging process, the IMC in both samples grew, as expected. However, the laser-formed IMC grew by a smaller amount than the reference sample. It is therefore assumed, that the laser reflow process produces bonds that are more resilient to thermal aging and can therefore reach a longer lifetime, even in thermally-challenging environments.

Summary

On the level of individual solder bumps, selective repair and rework are possible in several different configurations. Using our approach, the removal of the solder is not only more gentle on the underlying substrate and promises better wetting for the replacement, it is also selective. This allows the user to repair a given faulty bump within a functioning array of bumps, surface-mounted devices, and connectors. The process is proven to preserve the intermetallic compound and the pad underneath it.

Once the solder is removed, it needs to be replaced. This replacement process needs to be just as selective as the previous removal. PacTech's SB^2 solder jetting process does exactly that while preserving the quality of the bond underneath it. Reflowing the solder by using a millisecond laser pulse makes not only for a reliable IMC, but also one with a favorable geometry, optimal size, and improved thermal aging resilience when compared to results of conventional bonding processes. Both the solder removal and the replacement process are incorporated in a single machine making the complete rework cycle as fast and efficient as possible.

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Biography

Timo Kubsch is a Research & Development Engineer at PacTech – Packaging Technologies GmbH, Nauen, Germany. Since he started working with the company three years ago, he has co-authored 7 scientific papers published by the IEEE. He holds a Master's degree in Physics from the Free U. Berlin. Email Kubsch@pactech.de

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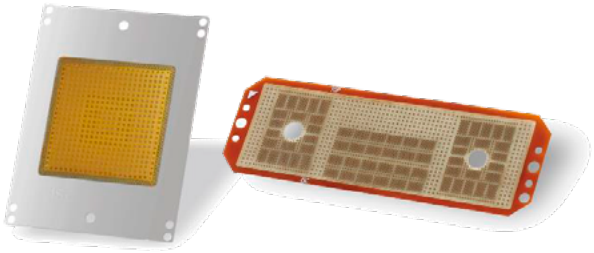

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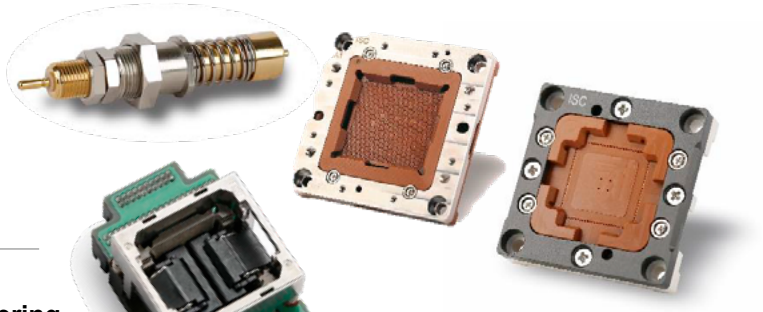

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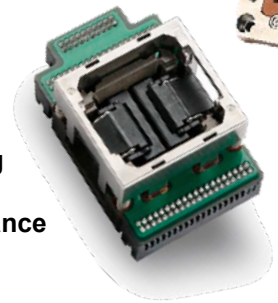

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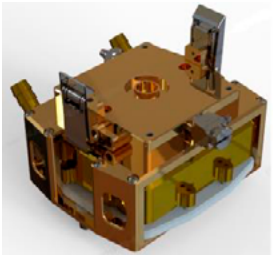

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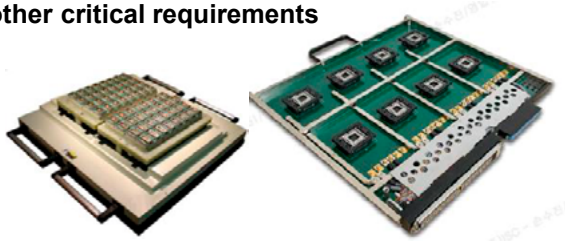

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Enabling low-loss thin glass solutions for 5G/mm-Wave applications

By David H. Levy, Shelby F. Nelson, Aric B. Shorey, Paul Ballentine [Mosaic Microsystems]

Thin glass substrates with fine-pitch through-glass via (TGV) technology provide attractive solutions for radio-frequency (RF) front end/5G, wafer-level packaging, microelectromechanical systems (MEMS) and systems integration [1-5]. High-quality glass can be formed in very thin sheets (<100µm thick) that enables solutions with a small footprint, and eliminates the need for back-grinding operations. Electrical and physical properties of glass have many attractive attributes such as low RF loss, the ability to adjust thermal expansion properties, and low roughness with excellent flatness to achieve fine lines/spaces (L/S). Furthermore, glass can be fabricated in panel format to reduce manufacturing costs.

The biggest challenge to adopting glass as a packaging substrate has been the existence of gaps in the supply chain, caused primarily by the difficulty in handling large, thin glass substrates using standard automation and processing equipment. This paper presents the Viaffirm® temporary bonding technology that allows thin glass substrates to be processed in a semiconductor fab environment without the need to modify existing equipment. We provide an overview of the handling technology along with its advantages, and demonstrate its successful implementation within the supply chain.

Introduction

The advantages include low insertion loss relative to Si-based solutions because when the operating frequency increases above a few GHz, silicon has high electrical losses, and also because of higher integration density compared to laminates and ceramics. Furthermore, research has shown the ability of glass to pass typical reliability testing including thermal shock and drop tests [6-7]. The challenge has been addressing how to make the transition from small-scale demonstration to providing solutions compatible with a high-volume manufacturing (HVM) environment.

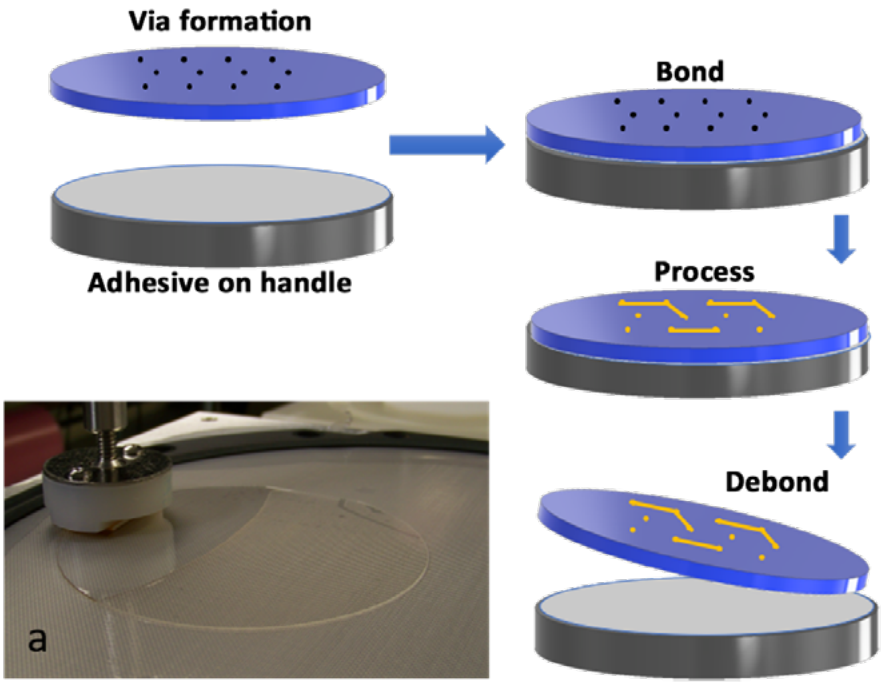

Figure 1: Depiction of temporary bond flow including bonding, process steps and the debond operation. The photo (inset a) shows the image of a debond operation on a bonded pair containing a fused silica device wafer bonded to a fused silica handle.

To address HVM, a thin-glass handling strategy utilizing Viaffirm® temporary bond enables glass processing in the existing manufacturing infrastructure. The approach utilizes a thin inorganic adhesion layer to temporarily bond a thin glass device wafer to a silicon or glass handle wafer (Figure 1). Utilizing a Si handle, in particular, allows the thin glass to be processed with existing equipment and process flows, followed by only a mechanical debond to yield finished substrates.

While the handling solution is compatible with many glass types, two in particular are discussed here. One type is thin aluminoborosilicate glass, which provides an inexpensive large-area substrate with good surface properties. The aluminoborosilicate used in this study is Corning's Willow® glass. The second glass type is high-purity fused silica, obtained by thinning of commercially-available starting wafers. Below, we discuss numerous important aspects of these high-quality glass substrates containing TGVs, and highlight key technology advances including advances in handling. These advances are critical steps enabling the readiness of glass products for high-volume applications.

While glass is generally advantaged for RF packaging, fused silica is particularly well suited to 5G/mm-Wave applications because of properties like its low loss tangent. To demonstrate the usefulness of the thin glass structures possible

with a good handling solution, we finish with recent simulations of low-profile fused-silica-based mm-Wave antennas, compared to analogous structures fabricated with printed circuit board (PCB) technology.

Application to TGV systems

The following sections discuss glass types and via formation, as well as the via fill and processing steps.

Overview of glass types and via formation. In this paper we focus on two different glass types with our temporary bonding system: high-purity fused silica (HPFS) and Willow®. From a standpoint of RF properties, the fused silica has one of the lowest loss tangents in the 10-50GHz range relevant to 5G communications. However, fabrication of substrates thinner than or equal to 200µm requires thinning of the thicker commercially-available fused silica. Additionally, the low CTE of fused silica (~0.6ppm/°C), while generally a desirable property, requires the use of relatively expensive fused silica handles in the temporary bonding framework. However, because the Viaffirm® layer is very thin, it can be leveraged to provide high-precision bond layers for the thinning process. We have developed a methodology to utilize this approach to provide HPFS wafers with straight tapered vias in thicknesses <150µm (see Figure 2 for an example of a tapered via in 150µm-thick HPFS).

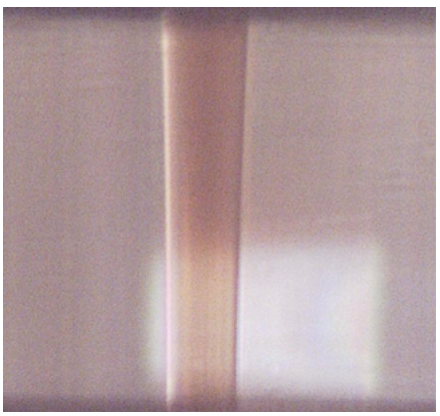

Figure 2: Example of a 30-35µm TGV in 150µm HPFS.

Willow® glass, on the other hand has a moderate loss tangent in the 10-50GHZ range, but provides a practical advantage in that it is manufactured in a large area format, with thicknesses down to 100µm, and with a low surface roughness. This allows you to avoid any grind and polish and provides an opportunity for significant cost savings. Furthermore, it has a CTE of approximately 3.2ppm/°C, which is comparable to silicon allowing the use of silicon handles that are relatively inexpensive and integrate well with existing infrastructure. A few of the properties of both glass types are summarized in Table 1.

Material Property	Glass Type	
	Willow [11]	Fused Silica [12-13]
Modulus (GPa)	74	73
CTE (ppm/°C)	3.2*	0.5**
Dielectric constant	5.3	3.8

*0-300 °C
**-100 – 200 °C

Table 1: Glass properties.

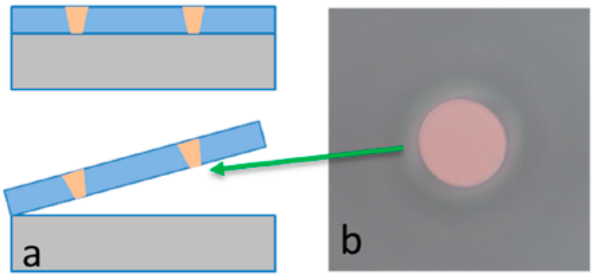

Figure 3: a) Depiction of a debond process showing the region at the base of the via where copper fill detaches from the handle substrate; b) micrograph of the via base region

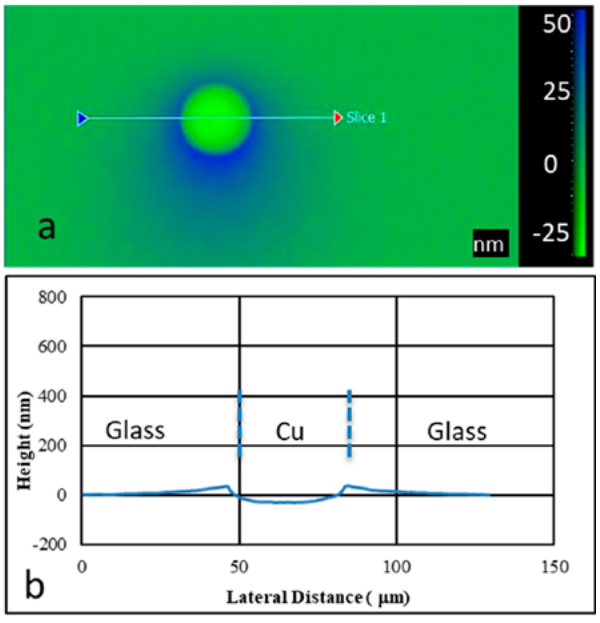

Figure 4: Optical profilometry of a copper fill debond region at the base of the vias. a) Height map of the region showing deviations in height; b) a cross section with heights and delineation of copper and surrounding glass regions, showing that the via-foot is planar to better than 100nm with the glass surface.

Via fill and processing. As illustrated in Figure 1, a via-containing bonded pair can be processed similarly to a silicon wafer. Because the TGVs bonded to a Si handle are essentially blind vias, standard bottom-up plating methodologies can be used to fill the TGVs. Vias have been successfully filled using a physical vapor deposition (PVD) seed process (PVD adhesion layer + PVD copper seed layer) as well as with a metalorganic chemical vapor deposition (MOCVD)-based seed layer process (PVD adhesion layer + MOCVD copper seed). A significant advantage of this approach is that you can achieve void-free vias, which is important for having a reliable product. This is also an important consideration if wafers need to be processed at elevated temperatures because voids in the Cu can cause cracking.

A critical feature of our temporary bond is the ability to debond the device glass from the handle after via fill and retain a suitable morphology of the copper in the via. The sketches in Figure 3a depict the debond operation, illustrating clean separation of the via-filled glass from the handle-wafer. Figure 3b is an optical micrograph of the bottom of a via (via surface facing the handle wafer) after debond, showing a top view of the copper in the via and its apparently smooth surface. In order to assess the topography of the via foot, optical profilometry using the Zygo Zegage ProHR was performed on this base area, shown in Figure 4. Figure 4a shows the topography in top view, with heights as indicated by the associated scale. A slice through the via (Figure 4b) exhibits a

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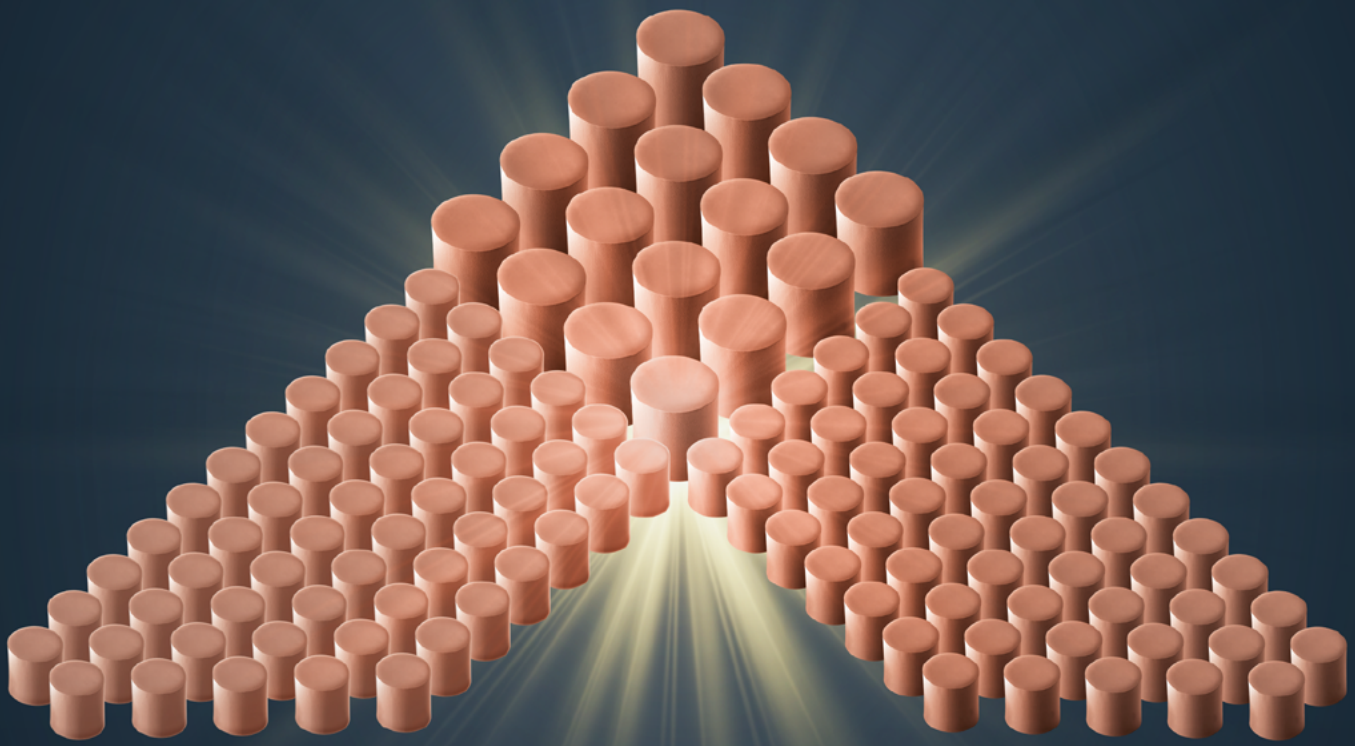

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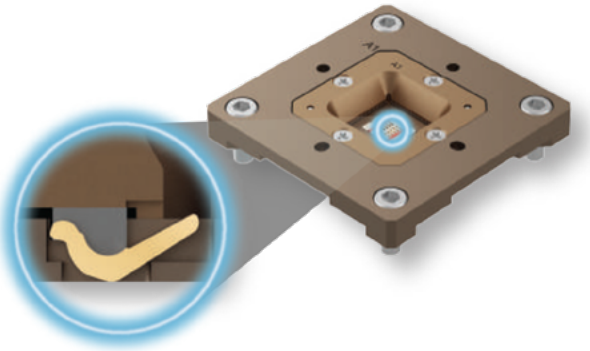
- Thermal capability to support from -40 °C to +125 °C
- Polyimide base for superior mechanical durability



Joule 20 test socket is Smiths Interconnect's advanced solution to address the rapidly growing demand for QFN package testing.

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very low disturbance from planarity (note the difference in lateral and vertical scales): the entire vertical scale of Figure 4b is 1µm. Root mean square (RMS) roughness of the copper surface was assessed by using a 5µm spatial filter to remove curvature of the surface, and yields roughness values of less than 0.5nm. Therefore, a smooth surface with planar (better than 100nm) filled-via areas is obtained after debond with no further processing.

Via hermeticity is an important aspect for many glass packaging structures, particularly for MEMS applications. We have done preliminary hermeticity assessment on device wafers that have been filled, and had the overburden removed by chemical mechanical polishing (CMP), while using our temporary bonding approach. We characterized two representative wafers. We first characterized the wafer for gross leak through dye penetrant testing. Regions that passed the dye penetrant test were then tested for fine leaks using He leak testing. In this test, the die is exposed to vacuum on one side and helium gas on the other. Leak rates are determined by a calibrated helium leak detector. Three typical die that were tested exhibited leak rates of 1.1e-9atm-cc/s, 3.0e-10atm-cc/s, and 2.2e-10atm-cc/s, respectively. Each of the areas contained a 12 x 11.5mm die with 600 vias.

Simulations for 5G/mm-wafer applications

We have shown that the glass handling approach described above allows for void-free, hermetic vias in thin glass, while the robust temporary bond allows for further processing including CMP, surface metallization, and a clean debond. In order to demonstrate the advantages of glass-based devices in mm-Wave communications, we have worked with Fraunhofer IZM to simulate antenna structures possible with glass using the above processes, as well as simulation of relevant comparison structures possible with PCB materials.

Among the benefits of glass are excellent insulating properties at the mm-Wave frequencies of 5G communications, and a very smooth surface compared with PCB and ceramic substrates, enabling lower RF loss. Additionally, glass is very robust to humidity and temperature fluctuations, and is a highly uniform, homogeneous material with properties consistent across the substrate. Finally, glass manufacturing for the display industry has made large, thin, form factors available, providing significant opportunities for cost-effective and large-area solutions. While we anticipate utilizing both fused silica and Willow® in future applications, the initial simulation work discussed in this paper focuses on fused silica because of its advantaged loss tangent.

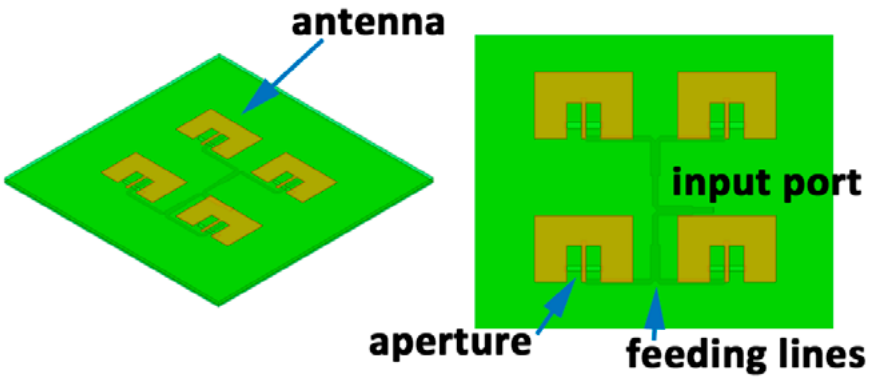

Figure 5: A 28GHz antenna test structure.

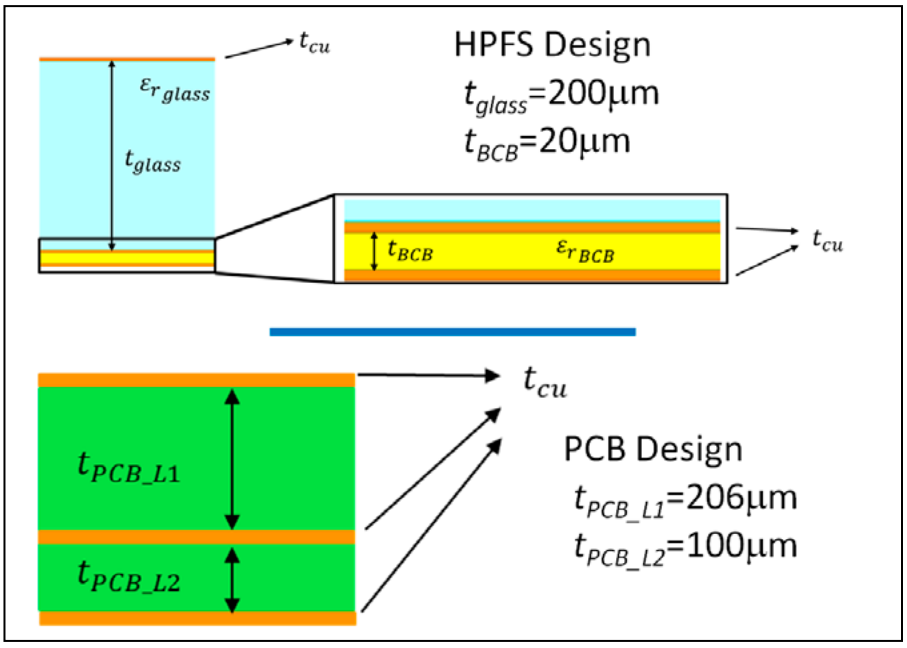

Figure 6: Cross section views of an antenna test structure showing thickness and materials used.

Simulation methodology

The test vehicle used for these simulations is a 2x2 aperture-coupled patch antenna array designed to operate in mm-Wave 5G applications at 20-30GHz. The design is relevant to cellular femtocells, highly distributed base stations intended to operate over 10m-20m distances. Figure 5 shows the basic test structure in perspective and top-down views. The structure contains three copper layers each separated by an insulator: the top layer contains the antennas as listed in the figure, while the bottom layer has the input port and feeding lines, shown shaded in the figure. Between these two metal layers is a ground layer that has an aperture (light green) beneath each antenna that allows coupling of the input signal in the feeding line to the antenna structure. The entire antenna structure is 15.4x15.4mm, while the individual antenna elements are approximately 2.5x3.7mm.

The architectures in cross section are shown in Figure 6, and highlight the different constructions used to achieve the glass- and PCB-based structures. A driving force for the simulation was to maintain thin structures, convenient for a glass-based structure made with our handling solution and useful for general miniaturization. Materials were chosen to achieve this goal as closely as possible within the constraint of having a reasonable path to fabrication.

Another reason to maintain similar thickness structures, and with similar values of dielectric constant ε_r, is that the antenna operating frequency and bandwidth depend on these combined with the planar antenna geometry.

The glass-based antenna simulation uses fused silica glass between the top and middle copper with a thickness of 200µm, while the comparison PCB version uses Panasonic Megtron 6 laminate and Prepreg with a total thickness of 206µm. Both materials have comparable dielectric constants (ε(fused silica)=3.8, ε(PCB)=3.71) while the fused silica does have a lower loss tangent of 0.0002 compared to the PCB at 0.004.

For the insulator between the mid copper layer and the bottom feeding lines, the glass structure uses patterned benzocyclobutene (BCB) at a thickness of 20µm, envisioning a solution-applied insulator consistent with the glass handling-based processes. The PCB structure, on the other hand, leverages the commercially-available Megtron 6 for this part of the stack at 100µm. This thickness disparity is a significant difference in the design parameters, but an offshoot of the desire to keep both structures consistent with available materials and fabrication processes. Finally, a possible advantage of the glass structure is the very smooth surface compared to the PCB, which promotes lower loss conduction at high frequencies [11]. This effect was not included in the simulations and would be more pronounced on the feed network than the patch array because of the long conductor lines.

Simulation results

After both antenna structures were modeled, the bandwidth was assessed by examining the reflection S-parameter, a measure of impedance matching, over the range from 24 to 32GHz as shown in Figure 7. The bandwidth, assessed as the region with reflection less than -10db, is similar for both structures, with the glass device exhibiting a bandwidth of 1630MHz while the PCB comparison device exhibits 1670MHz. Bandwidth dictates the ability to maximize the number of communication channels, and the fact that both structures exhibit similar values validates the fact that the materials and dimensions chosen create a suitable comparison.

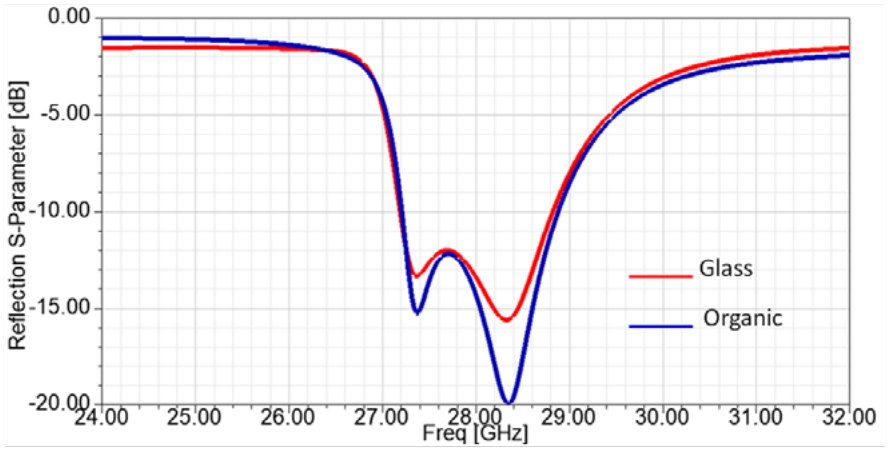

Figure 7: Impedance matching of simulated fused silica (glass) and PCB (organic) structures showing a similar bandwidth for both structures.

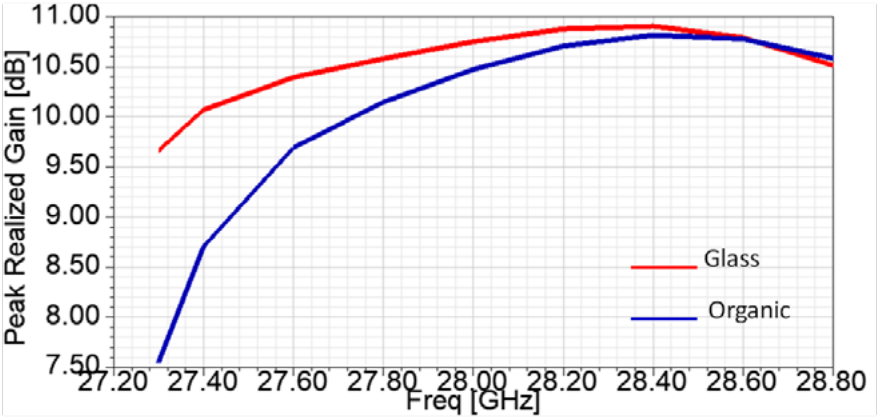

Figure 8: Peak realized gain for simulated fused silica (glass) and PCB (organic) structures, showing a higher and broader gain for fused silica.

Simulation results for the peak realized gain are shown in Figure 8, with the frequency axis adjusted to cover only the impedance matching region. For this parameter, it can be seen that the glass antenna not only shows a higher peak gain (10.9dbi vs. 10.5dbi for the PCB structure), but that gain has a broader maximum over the matched frequency band. The increased gain leads to a radiation efficiency of 80% for the glass structure, as opposed to 76% for the PCB version. Based upon these promising results, construction of this antenna structure in both glass and PCB is underway in order to validate the simulation results. While not discussed here, additional simulations show further benefits by using glass in the antenna feed networks because of the low roughness and reduction of losses due to the skin effect. Fabrication of these devices is in process as well.

Summary

We have described a temporary bonding approach that enables processing of thin glass – notably aluminoborosilicate glasses – as well as fused silica. The process allows for a tunable and stable bond energy between substrate and handle, and this bond has been shown suitable for TGV fill as well as for aggressive downstream processes such as CMP.

When a Si handle is used, the bonded stacks mimic Si wafers with blind TGVs. The combined effect makes existing supply chains viable for volume fabrication of thin glass substrates. This has been demonstrated in a number of use cases that includes demonstrating reliable TGV structures that are hermetic and have many advantages for RF/5G, advanced packaging, MEMS and other applications. In particular, the usefulness of such glass substrates to applications in 5G/mm-Wave communications was explored by simulations comparing a fused silica structure to one made with conventional PCB approaches. Promising simulation results validate the value of such glass structures in high-frequency RF communications applications.

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Low-temperature polyimide processing for next-gen backend applications

By Zia Karim [Yield Engineering Systems, Inc. (YES)]

The thermal, mechanical and dielectric properties of polyimide materials are critical to meeting the demands of fan-out or wafer-level processing for 3D stacking applications. The team at YES worked together with colleagues at Hitachi Dupont (Melvin Zussman and Ron Legario) as well as colleagues at Fuji to study those properties for various low-temperature polyimides as a function of different process parameters under atmospheric and vacuum process conditions. This article will briefly explain the experimental process used and will present results for HD-7110 (a low-temperature polyimide from Hitachi Dupont), in comparison with HD-4100, Fuji's LTC-9320 (E07 version), and Asahi's BL-301. Some data on Hitachi Dupont's polybenzoxazole (PBO) HD-8820 will also be shared. The characterizations of these low-temperature polyimides under different process conditions will be followed by conclusions and a discussion of the benefits for future packaging solutions.

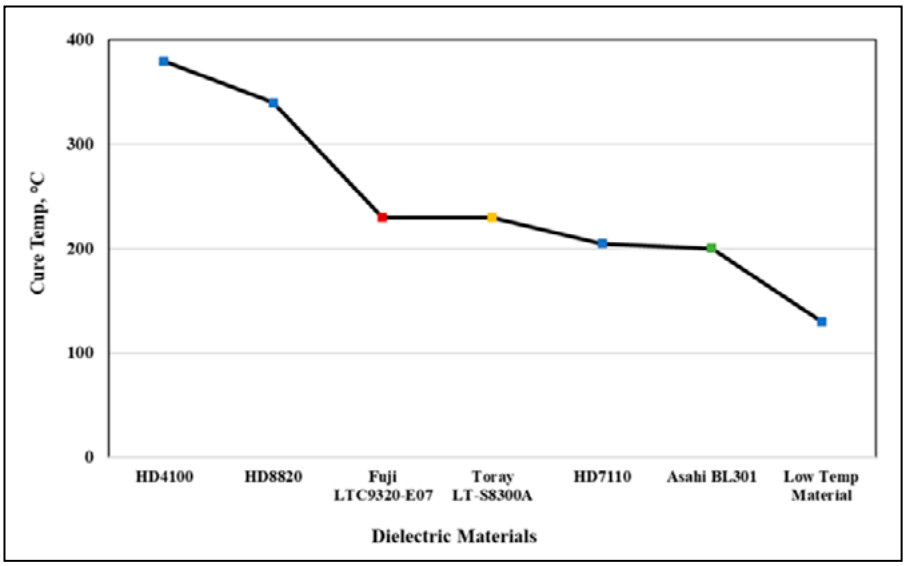

Figure 1: Lower temperature polyimide (PI) trend requires vacuum cure.

Reducing thermal budget while maintaining performance

Figure 1 lists the low-temperature polyimides known to the YES team from partners and chemical suppliers. The decreasing trend in cure temperatures is evident. Many engineers are familiar with HD-4100 (cured at 375ºC) and and HD-8820 (a PBO that is cured at 320ºC). However, more polyimides are now emerging that are cured between 200–230ºC, to satisfy the ever-lower thermal budgets of 3D stacking and heterogeneous integration applications. Hitachi Dupont offers its HD-7110 with a recommended cure temperature of 205ºC, Asahi offers its BL-301, Fuji offers its LTC-9320, and Toray offers a film that cures between 200 and 230ºC. These polyimides are used for redistribution (RDL) interconnect dielectrics. Even lower temperature dielectrics are being proposed; one from Fuji can be cured between 160 and 180ºC.

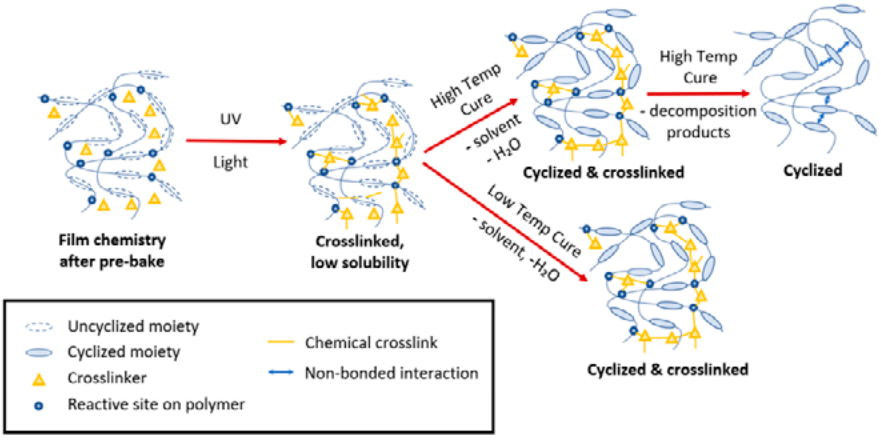

Figure 2: Cure chemistry of photosensitive low-temp PI.

Curing polyimide at low temperatures is good for stress and the RDL, but only if the properties of the cured films are also good. So the team tested not only the physical characterizations of outgassing, shrinkage, stress and scanning electron microscope (SEM) profile, but also mechanical, thermal and electrical properties of the cured films to determine how well these cured films would work in the multilevel RDL process.

How it works

As illustrated in Figure 2, photosensitive polyimides designed for high-temperature cure undergo two main types of reactions: cyclization of the backbone to form imide groups, and decomposition and volatilization of the cross-linked compounds, leaving behind only the cyclized polyimide. Low-temperature polyimide curing uses a

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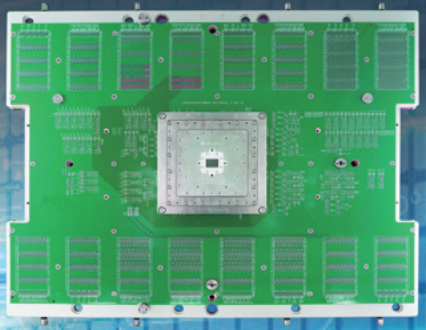

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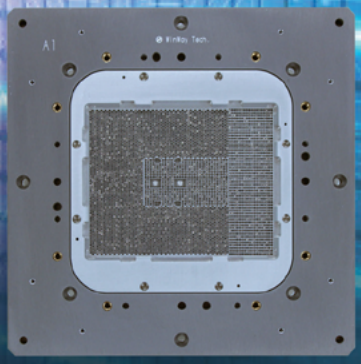

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similar mechanism. The difference for low-temperature cure is that the cross-linked compounds are not decomposed but remain in the cured polyimide.

Low-temperature curing materials are targeted between 200 and 250ºC. This temperature range is sufficient to allow the imidization reaction to proceed, but removing the casting solvent becomes more and more challenging the lower the cure temperature goes. As an example, the boiling point of N-Methylpyrrolidone (NMP), the most common solvent, is 202 degrees at atmosphere. However, if the process pressure is 200Torr, the boiling point goes down to 150°C. So when pressure is lower, it becomes easier to take the solvent and water out of the film, enabling good imidization. The team's studies revealed how this impacted the properties of the cured polyimides.

Goals and methods

As mentioned above, this article will first compare results for HD-4100 and HD-7110, and will also discuss results for HD-8820, as well as polyimides from Fuji and Asahi. Four of these are negative-tone polyimides and one is positive-tone. The goal was to cure these films at as low a temperature as possible while maintaining desired properties. For RDL and other backend applications, when a low-temperature polyimide is proposed, the polyimide must exhibit no outgassing, good thermal stability (ability to withstand the thermal cycling process), chemical resistance, good mechanical properties – especially high elongation – and good dielectric properties. The cure process of a dielectric material should perform complete imidization, removing casting solvents and creating highly cured film with good, complete cross-linking.

An additional goal was to reduce cure time in order to reduce thermal budget. The atmospheric cure process usually involves three steps: oxygen removal, solvent removal, and cross-linking. It typically requires 6-8 hours, compared to 3.5 to 4.5 hours for low-pressure cure.

YES systems use a low-pressure vacuum cure process, which maintains excellent temperature uniformity, laminar gas flows and active heating and cooling for effectively curing polyimide and PBO materials. **Figure 3** illustrates the low-pressure polyimide cure process that was used in the experiments. An initial three-cycle pump-and-purge process took the oxygen to less than 10ppm. The vacuum process consisted of only one step: ramping up to the recommended cure temperature and coming down. In this study, we examined the effects of various cure pressures on the physical, mechanical, thermal, and electrical properties of the cured film.

Both HD-4100 and HD-7110 were coated, baked and developed using automated track systems. In some cases, for determining mechanical and thermal properties when the film needed to be released from the wafer after cure, a coating of polyimide 2611 was used as the substrate. The control samples were cured at atmosphere using a commercially-available atmospheric cure oven. For all the studies, cure pressures were varied between 50 and 760Torr.

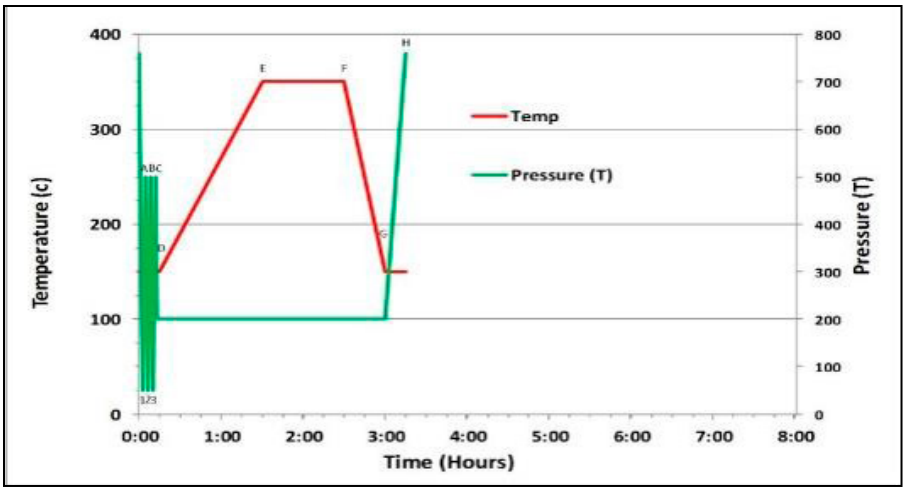

Figure 3: YES vacuum cure process.

Results

The next sections describe our results for various polyimide materials.

HD-4100 and HD-7110. The Fourier transform infrared spectroscopy (FTIR) spectra of cured polyimides under vacuum and atmospheric conditions were analyzed to compare the extent of imidization. These FTIR analyses exhibited almost identical profiles, confirming that even though the vacuum cure process requires much less cure time, complete imidization was, nonetheless, obtained for both films.

The FTIR characterizations showed better imidization in the low-pressure curing process for low-temperature polyimide, in comparison to the atmospheric cure process. Seeing better imidization with FTIR, it can be assumed that this process will result in better molecular packing, and will also show an improvement in thermal, mechanical and electrical properties. Gas chromatography mass spectrometry (GCMS) was used to identify volatiles from HD-4100 cured at 200Torr and at atmospheric pressure. The outgassed volatiles were much higher for the atmospheric cured film compared to the vacuum-cured film. Most of the peaks are related to solvent NMP or water, in the case of atmospheric-cured films. No outgassing was observed for vacuum-cured films up to about 300ºC for most of the cured films. Similar GCMS analysis was carried out for HD-7110 cured at the recommended cure temperature of 205ºC, at three different pressures: 200Torr, 400Torr and 760Torr (atmospheric). The volatiles of NMP, the major solvent in HD-7110, were much lower in the vacuum-cured films. For total NMP volatiles, the parts-per-billion (ppb) values were calculated and plotted against the various pressures. They indicated a decrease in NMP content of 35% with a decrease in cure pressure from 760Torr to 200Torr. If we extrapolate this trend to 100Torr, the NMP content decreases by about 50%. The efficient removal of solvent and other volatiles is critical to achieve better molecular packing and better cross-linking, to help improve thermal stability, and also to improve dielectric strength. These properties are, therefore, expected to be better for vacuum-cured films.

Next, the mechanical, electrical, and thermal properties of these films were examined. The tensile strength and the modulus of a film are important indicators of the ability of a film to absorb and withstand the mechanical stresses that occur at the interface between the film and metals. This is especially important for multilayer films that experience inter-layer stress. From the studies of tensile strength at different cure pressures, no variation of the mechanical properties was found as a function of the cure pressures, for either HD-7110 or 4100. So even though HD-7110 is a low-temperature polyimide that may still contain the cross-linker, there was not much change in its tensile strength when it was cured under vacuum. However, we observed that while elongation is 60% for HD-4100, it was only 36% for HD-7110. Similarly, HD-7110's other mechanical properties like modulus, strength, and residual stress were worse compared to the cured HD-4100 film. These results suggest that HD-7110 may have less ability to withstand interconnect stress exerted during material processing.

Figure 4 shows thermal properties of HD-4100 and HD-7110. These were measured by changes in weight, as determined by thermogravimetric analysis (TGA). The changes in weight are due to the loss of materials in the film that are volatile at higher temperature. The source of these volatiles is not only water, but also other chemical components at elevated temperature, including cross-linkers. This was especially critical for the low-temperature polyimide, HD-7110. For HD-4100, when the Td 1% and the Td 5% were measured (Td 1% is 1% weight loss at temperature and Td 5% is 5% weight loss at temperature), as the cure

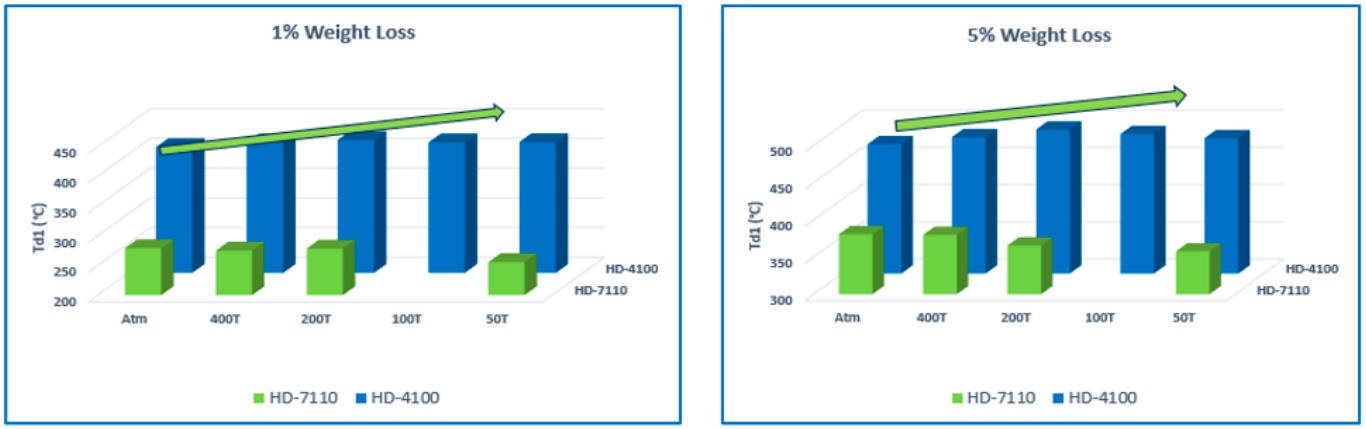

Figure 4: Thermal properties of HD-4100 and HD-7110 (Td 1% and 5%).

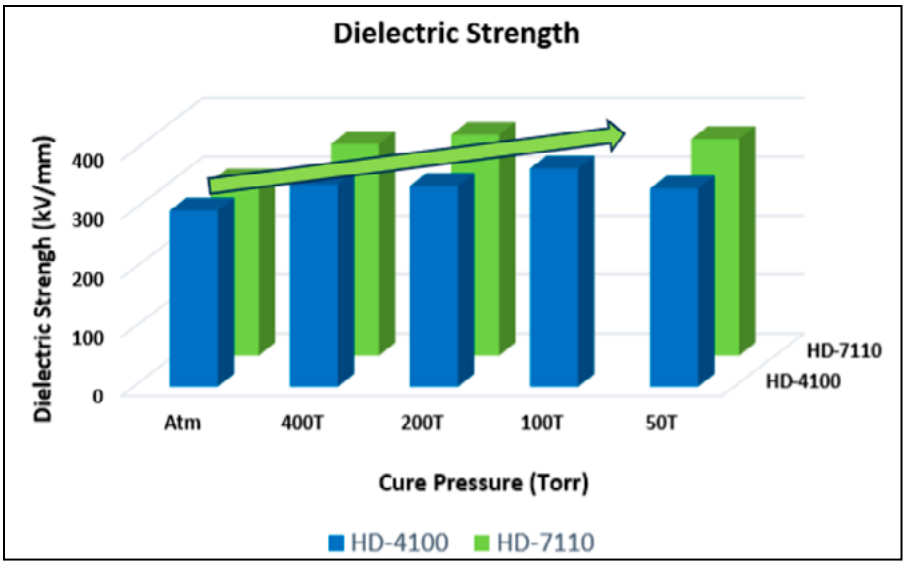

Figure 5: Dielectric strength of HD-4100 and HD-7100 at varying pressures.

pressure decreased, there was an increase in Td 1% of 31%. This means the film shows much better thermal stability under vacuum cure. Also, the glass transition temperature of HD-4100 was 15 to 20 degrees higher with vacuum compared to the atmospheric cure process. However, no such effect was found for the low-temperature polyimide HD-7110 with the pressure changes, either for 1% weight loss, or 5% weight loss. This means that there is minimal dependence on cure pressures for HD-7110, showing lower thermal stability compared to the more popular HD-4100, probably due to the decomposition of the cross-linker at elevated temperature.

Next, electrical properties were examined. Dielectric properties (dielectric strength, dielectric constant, and dissipation factor) were the main parameters measured. These properties are solely dependent on the degree of imidization, impurity content, and the packing density of the polyimide. Lower dielectric constant (DK) supports higher transmission speed, and lower dissipation factor (DF) improves signal integrity.

We measured values of DK for HD-4100 and HD-7110. DK was around 3.3, which is consistent with expected values. Dissipation factor for the low-temperature polyimide was higher. While HD-4100 was around 0.009, DF was 0.016 for the low-temperature polyimide. This higher DF was probably due to the existence of the cross-linker, which is assumed to remain during the curing process in the case of low-temperature polyimide. However, very good results were observed for the dielectric strength, showing the biggest improvement at low pressure compared to atmospheric cure. As shown in

Figure 5, 20-25% higher dielectric strength was consistently achieved with vacuum for both low-temperature polyimide (HD-7110) and high-temperature polyimide (HD-4100) compared to atmospheric cure. This is certainly related to better packing density as well as better dielectric properties of vacuum-cured polyimide films.

PBO HD-8820. Though most of our customers are now moving from PBO to polyimide and low-temperature polyimide, some data is included here on PBO HD-8820. The team's study of PBO HD-8820 for physical, thermal, mechanical and electrical properties showed little variation of these properties with cure pressure. Figure 6 plots glass transition temperature (Tg), Td 1%, and Td 5% weight loss for HD-8820. Most of these values showed minimal variation among atmospheric, 400Torr, 200Torr and 50Torr cure pressures; the same was true of the dissipation factor. One notable observation was that for HD-8820 the dissipation factor was .006, which is even lower than that of HD-4100, so HD-8820 will likely provide a much better signal-to-noise ratio. Most of the properties measured – elongation, modulus, tensile strength, and stress – were very good and were consistent with the literature values. For the most part, HD-8820 PBO showed stable performance overall, and at higher pressure (greater than 400Torr), the results showed better stability of the films.

Fuji LTC-9320 E07. A low-temperature polyimide from Fuji (LTC-9320, which has a cure temperature of 230 degrees) was also studied. The recommended atmospheric cure is a two-step process, which was conducted at 230ºC and which took 6.5h. The one-step YES best-known method (BKM) process was then used, which took about 4.5h. Dwell time was further reduced, by 50%, which resulted in a cure time of 3.5h.

As with the Hitachi Dupont films, the team achieved similar characteristics (or better characteristics, for dielectric strength). But we were also able to reduce the cure time by about 35% and thereby improve throughput. Additionally, the objective here was to see if cure time could be reduced while obtaining similar or better film properties. For this film, even when cure time was cut from 8 hours to around 3.5 hours, its physical properties, like shrinkage and stress, remained the same. The intrinsic properties of the film did not change, which probably indicates that the film was already fully cured. This was consistent in the FTIR analysis of LTC-9320 at the above conditions – identical FTIR spectra indicated the same imidization. Even with reduced cure time, fully-cured cross-linked films were obtained, showing that shrinkage, stress and imidization remained the same.

Figure 7 shows thermal and mechanical properties for the fully-cured LTC-9320 E07 films. The cure temperature was 230ºC, and most of the film properties were very consistent with those from the atmospheric process. However, the team was able to reduce the cure time from 6.5 or 7h to about 3.5h. One interesting thing: the dissipation factor was approximately 15% lower when the films were cured at 200Torr compared to the atmospheric process – a very exciting result for this Fuji polyimide, which will provide better signal-to-noise performance for high-frequency film. To conclude, the

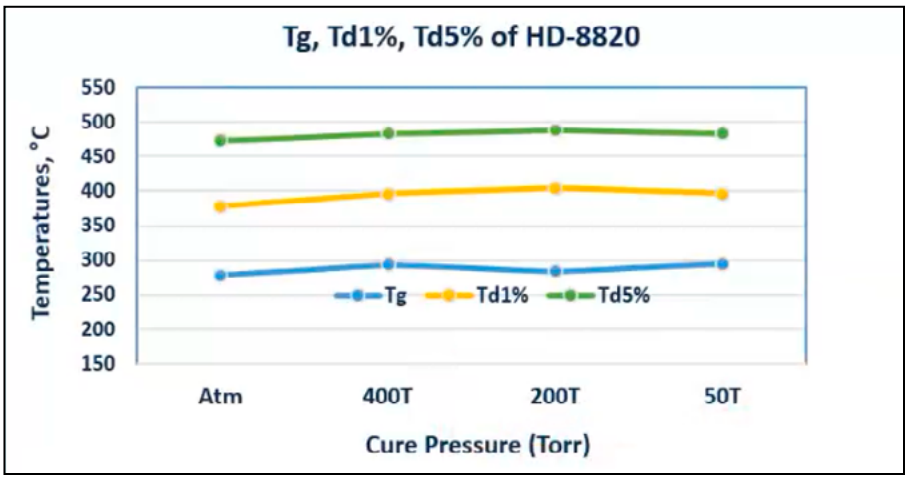

Figure 6: Glass transition temperature (Tg), Td 1%, and Td 5% weight loss for HD-8820.

thermal, mechanical and reliability tests on this film showed that most of the properties were consistent despite a cure time reduction of about 35%, and tests showed a good dissipation factor reduction for a high-frequency application.

Asahi BL-301. Finally, we consider results for another low-temperature polyimide: Asahi's BL-301. Once again, the low-pressure process was compared to the atmospheric cure process recommended by Asahi, for which the temperature is 230ºC. In this case, the dwell time was again reduced by 50%, and cure time was reduced by 38% using low-pressure cure compared to the recommended recipe. As shown in **Figure 8**, total time was reduced from 6.5h to 4h; however, most of the results reported here (e.g., Td 5%, glass transition temperature, CTE, elongation, strength and Young's modulus) are similar. The cured film showed an improvement of approximately 5% in elongation, which gives better mechanical properties, with the vacuum cure process. When, in addition to the reduced cure time, the cure temperature was reduced to 200ºC, the resulting film showed characteristics that would likely be acceptable for this process.

FILM PROPERTY TESTED	RESULTS
Cure condition	YES 230°C
2% weight loss	321°C
5% weight loss	335°C
Tg	206°C
CTE	55.7ppm
Elongation	76.9%
Tensile strength	183.1 MPa
Young's modulus	2.6
Imidization index	100%

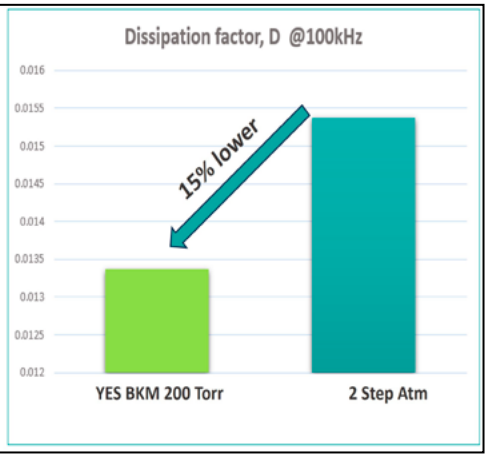

Figure 7: Film properties of Fuji LTC-9320 E07.

Process	Dwell Temp (°C)	Dwell Time (min)	Total Time (hr)	Td 5%	Tg	CTE	Elongation	Strength	Young's Modulus
Asahi Rec. Recipe	250	120	6.5	370	235	55	55	125	3.3
YES BKM	250	60	4	370	235	55	60	125	3.3
YES BKM	200	60	4	340	215	60	50	130	3.4

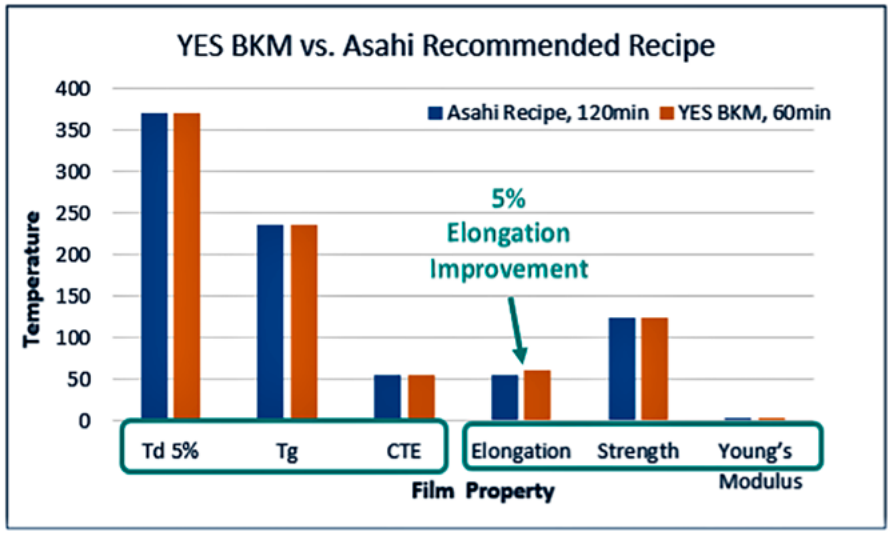

Figure 8: Film properties of Asahi BL-301.

Summary

The 3D packaging roadmap involves enhancing the capabilities of high-density backend processing by increasing the number of RDLs, shrinking line width and spacing, and reducing pad size and pitch. The trend of the polyimides and the PBO used in these interlevel RDLs is increasingly toward low cure temperatures, where the vacuum curing process offers significant benefits.

For both polyimide and PBO film, using vacuum reduced the thermal budget by reducing both the cure time and cure temperature. Vacuum cure also resulted in better film properties. Further integration studies are needed to qualify these films, and we are working with some partners, including imec, to do that. Overall, a reduction in cure time of approximately 35% was achieved using the vacuum cure process. Reduction in thermal budget, which reduces film stress, is required for 3D stacking and heterogeneous integration. Hopefully, this article will help to position these low-temperature polyimides – with less outgassing, better imidization, and better dielectric strength – as suitable for 3D packaging and the stacking of chiplets, as well as for other heterogeneous integration applications.

Biography

Zia Karim is CTO of Yield Engineering Systems, Inc. (YES), Fremont, California. Before joining YES, Dr. Karim spent 15 years as VP of Business Development and Technology at Eugenus/AIXTRON/Genus. He also held senior management positions at Applied Materials and Novellus. He received his PhD in Electrical Engineering from Dublin City U. in Ireland, and the Certificate of Business Excellence from the Haas School at UC Berkeley. He holds 16 patents; email: zkarim@yieldengineering.com.

Highlights of the 71st ECTC Conference

By Nancy Stoffel
2021 ECTC General Chair

The IEEE Electronic Components and Technology Conference (ECTC) went virtual this year to deliver the latest in packaging R&D, and industry insights. The 71st ECTC, which started on June 1 and was extended by popular request to July 16, 2021, was a success in connecting technologists globally in these challenging times. There were 1,380 attendees from 23 countries. The conference included 346 papers in 46 oral sessions and 14 special sessions and panels. The Heterogeneous Integration Roadmap workshop was integrated into the ECTC platform and professional development courses on 14 topics were delivered by industry experts.

The virtual platform removed the constraints of parallel sessions and room size limitations, allowing attendees to watch the most relevant content on their own schedule. The hottest topics at ECTC 2021 reflected the interests in 2.5 and 3D heterogeneous integration, chiplet-enabled advanced packaging approaches and wafer/panel fanout technologies. We were honored to have Sam Naffziger, AMD Senior Vice President, give a keynote presentation to open the conference. His presentation focused on the impact of chiplet-based system-on-chip (SoC) architectures and manufacturing from a packaging perspective for computing applications. Over 550 attendees have watched Sam's presentation to date. The most watched session of the conference with more than 650 views, was Session 1: 2D and 3D Chiplet Interconnects in FOWLP/PLP organized by the Packaging Technologies technical committee. Attendees were eager to hear the latest research from Intel, ASE, Samsung, TSMC, Fraunhofer IZM, and Tohoku University and TU Dresden.

This year the conference included a record 14 special sessions and panel sessions that combined deep dive discussions of technology developments, trends, and challenges. Following up on Sam Naffziger's keynote presentation, Kanad Ghose/Binghamton University, and Dale Becker/IBM, invited a panel of experts to discuss the opportunities and challenges of chiplet designs and applications. The panel discussed both technical and business challenges (deployment, sourcing, security, trade-offs between thermal, warpage and electrical performance). The Plenary session, organized by Jan Vardaman, Kim Yess and Mark Poliks, brought together a panel of 7 experts on the transformation of the electronics industry in a post-COVID world. The assembled experts discussed the growth the electronics industry has experienced resulting from the global pandemic. Existing trends were accelerated including growth in data centers, increased use of artificial intelligence (AI), and the growth of telemedicine. Demand increased

for a variety of products including game consoles, laptops, monitors and tablets for education and business use. This panel presented their perspectives on the continued transformation of the industry and expectations that will drive packaging developments in the future.

A strong, effective, and vibrant workforce is critical to our industry's continued development. ECTC hosted three events to support diversity, women in engineering and young professionals. A Diversity Panel was organized by Allyson Hartzell from Philips and Kitty Pearsall from Boss Precision, Inc. The panel focused on how trends in gender equality, and ethnic and cultural diversity can boost business performance.

Industrial partners continued their strong support of the ECTC mission again this year. Their participation allowed ECTC to create a rich global online destination for academics and industrial researchers to exchange information and ideas on electronic packaging and integration technologies. The conference had a record 43 sponsors and 61 Technology Corner Exhibitors.

Looking forward, the 72nd ECTC will be held in San Diego, California, May 31- June 3, 2022. The Call for Papers can be found at www.ectc.net. Abstract submission will close October 4, 2021. Plan now to attend for in-person sessions, and network with your colleagues!

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